

EV28163-Q-00A

High Efficiency Single Inductor Buck-Boost DC-DC Converter **Evaluation Board**

DESCRIPTION

The EV28163-Q-00A Evaluation Board is designed to demonstrate the capabilities of MPS' MP28163.

The MP28163 is a highly efficient, low quiescent current Buck-Boost converter, which operates from input voltage above, below and equal to the output voltage. The device provides power solution for products powered by a one-cell Lithium-Ion or multi-cell alkaline battery applications where the output voltage is within battery voltage rang.

The MP28163 operates with input voltage from 2V to 5.5V to provide adjustable output voltage (1.5V to 5V), and is available in QFN10-3x3mm package.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Supply Voltage	V _{IN}	2 – 5.5	V
Output Voltage	V _{OUT}	3.3	V
Output Current	I _{OUT}	0 – OCP	А

FEATURES

- High efficiency up to 95%.
- Load disconnect during shutdown •
- Input voltage range: 2V to 5.5V •
- adjustable output voltage from 1.5V to 5V •
- 1MHz switching frequency
- Pulse skipping mode at light load
- Typical 80uA quiescent current •
- Internal loop compensation for fast response
- Internal soft start •
- OTP, hiccup SCP
- Available in small QFN10-3x3 package

APPLICATIONS

- Battery-powered products
- Portable instruments
- **Tablet PCs**
- POS systems

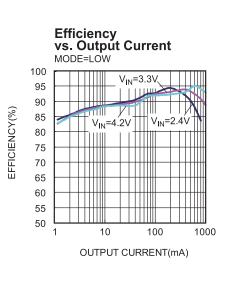
All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page. "MPS" and "The Future of Analog IC Technology", are Registered Trademarks of Monolithic Power Systems, Inc.

EV28163-Q-00A EVALUATION BOARD



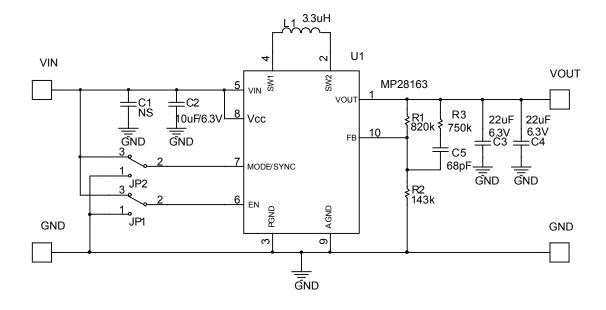
(L × W × H) 5.08cm × 5.08cm × 1.3cm

Board Number	MPS IC Number	
EV28163-Q-00A	MP28163GQ	



www.MonolithicPower.com MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2014 MPS. All Rights Reserved.

EVALUATION BOARD SCHEMATIC

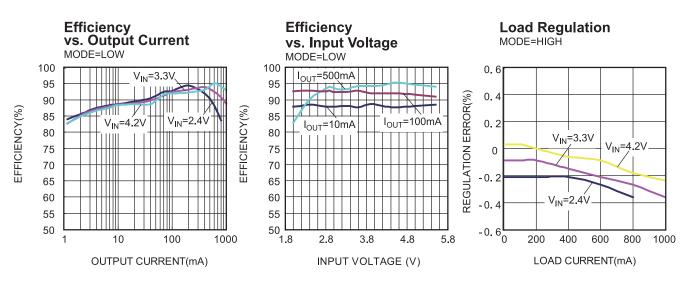


EV28163-Q-00A BILL OF MATERIALS

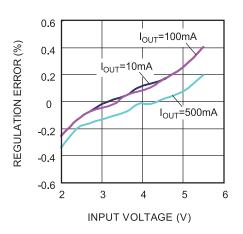
Qty	RefDes	Value	Description	Manufacturer	Manufacturer P/N	Package
1	C1	NS				0805
1	C2	10uF	6.3V X7R ceramic capacitor	muRata	GRM21BR60J106KE19D	0805
2	C3, C4	22uF	6.3V X5R ceramic capacitor	muRata	GRM21BR60J226ME39L	0805
1	C5	68pF	50V, X7R ceramic Capacitor	muRata	GRM188R71H680KL	0603
2	JP1, JP2		3 pins header			DI
1	L1	3.3uH	9mOhm, 8A inductor	Wurth	744314330	SMD
1	R1	820k	Film resistor, 1%	YAGEO	RC0603FR-07820KL	0603
1	R2	143k	Film resistor, 1%	YAGEO	RC0603FR-07143KL	0603
1	R3	750k	Film resistor, 5%	YAGEO	RC0603JR-07750KL	0603
1	U1	MP28163	2~5.5V, 2.6A buck- boost converter	MPS	MP28163GQ	QFN10-3*3

EVB TEST RESULTS

Performance waveforms are tested on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 3.3V$, $L = 3.3\mu$ H, $C_{OUT}=2x22u$ F, $T_A = 25^{\circ}$ C, unless otherwise noted.

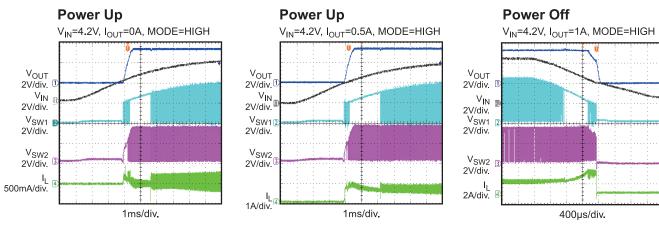


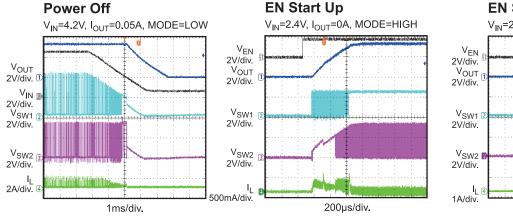
Line Regulation MODE=HIGH

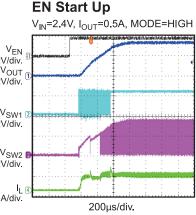


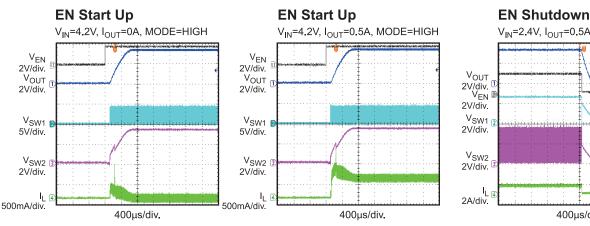
EVB TEST RESULTS (continued)

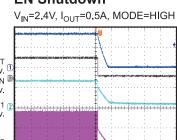
Performance waveforms are tested on the evaluation board. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} =2x22uF, T_A = 25°C, unless otherwise noted.





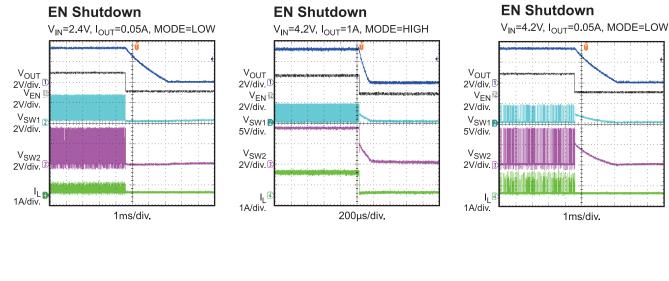


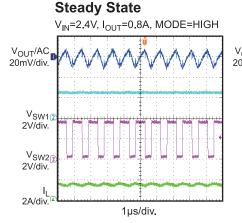


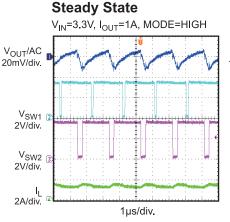


EVB TEST RESULTS (continued)

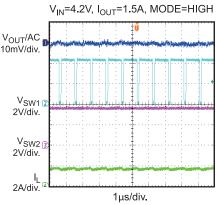
Performance waveforms are tested on the evaluation board. $V_{IN} = 3.3V$, $V_{OUT} = 3.3V$, $L = 3.3\mu$ H, $C_{OUT}=2x22\mu$ F, $T_A = 25^{\circ}$ C, unless otherwise noted.

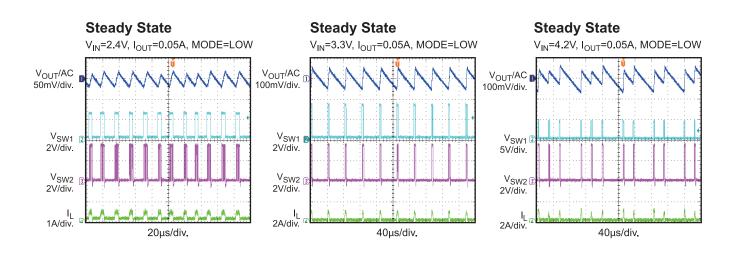








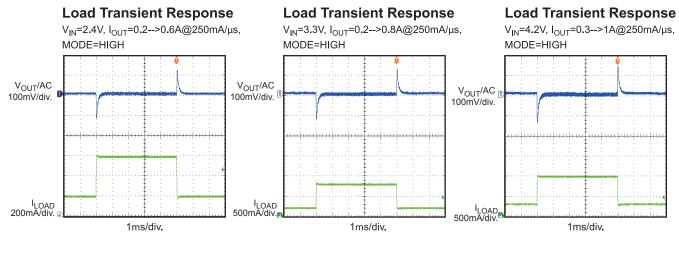




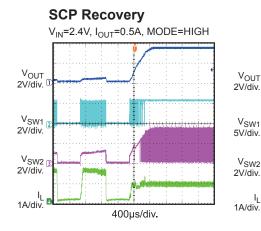
7.1.0 www.MonolithicPower.com MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2014 MPS. All Rights Reserved.

EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board. V_{IN} = 3.3V, V_{OUT} = 3.3V, L = 3.3µH, C_{OUT} =2x22uF, T_A = 25°C, unless otherwise noted.



SCP Entry V_{IN}=2.4V, I_{OUT}=0.5A, MODE=HIGH V_{OUT} 2V/div. V_{SW1} 2V/div V_{SW2} 2V/div. ا 1A/div. 1ms/div.

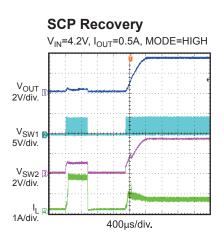


V_{IN}=4.2V, I_{OUT}=0.5A, MODE=HIGH V_{SW2}

SCP Entry

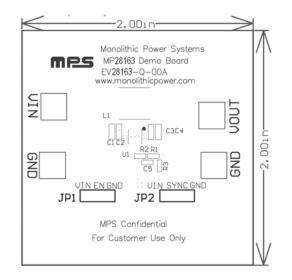


ΙL



EV28163-Q-00A Rev.1.0 www.MonolithicPower.com 1/26/2014 MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited. © 2014 MPS. All Rights Reserved.

PRINTED CIRCUIT BOARD LAYOUT



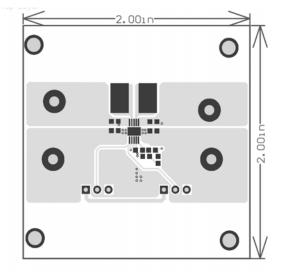


Figure 1: Top Silkscreen Layer

Figure 2: Top Layer

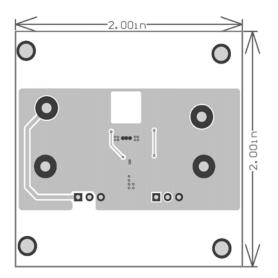


Figure 3: Bottom Silkscreen Layer