

### DESCRIPTION

The MP3426 is a current-mode step-up converter with a 6A, 90mΩ internal switch that provides a highly efficient regulator with a fast response. The MP3426 features a programmable frequency of up to 2MHz that allows for easy filtering and reduces noise. An external compensation pin gives the user flexibility in setting loop dynamics, and uses small, low-ESR, ceramic output capacitors. Soft-start results in a small inrush current and can be programmed with an external capacitor. The MP3426 operates from an input voltage as low as 3.2V and can generate up to a 35V output.

The MP3426's features include under-voltage lockout, current limiting, and thermal overload protection. The MP3426 is available in a low profile 14-pin 3mm×4mm QFN package with an exposed pad.

### FEATURES

- 6A, 90mΩ, 45V Power MOSFET
- Uses Very Small Capacitors and Inductors
- Wide Input Range: 3.2V to 22V
- Output Voltage as High as 35V
- Programmable  $f_{sw}$ : 300kHz to 2MHz
- Programmable UVLO, Soft-Start, UVLO Hysteresis
- Micropower Shutdown <1μA
- Thermal Shutdown 160°C
- Available in 14-Pin 3mm×4mm QFN Package

### APPLICATIONS

- Telecom—Power Supplies
- Audio—Microphone and Tuner Bias
- Automotive

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### ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	$V_{IN}$	6-9	V
Output Voltage	$V_{OUT}$	12	V
Output Current	$I_{OUT}$	2	A

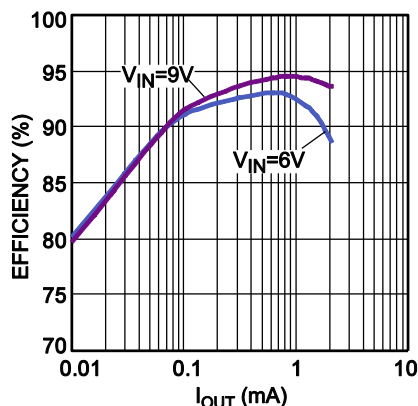
### EV3426-L-00A EVALUATION BOARD



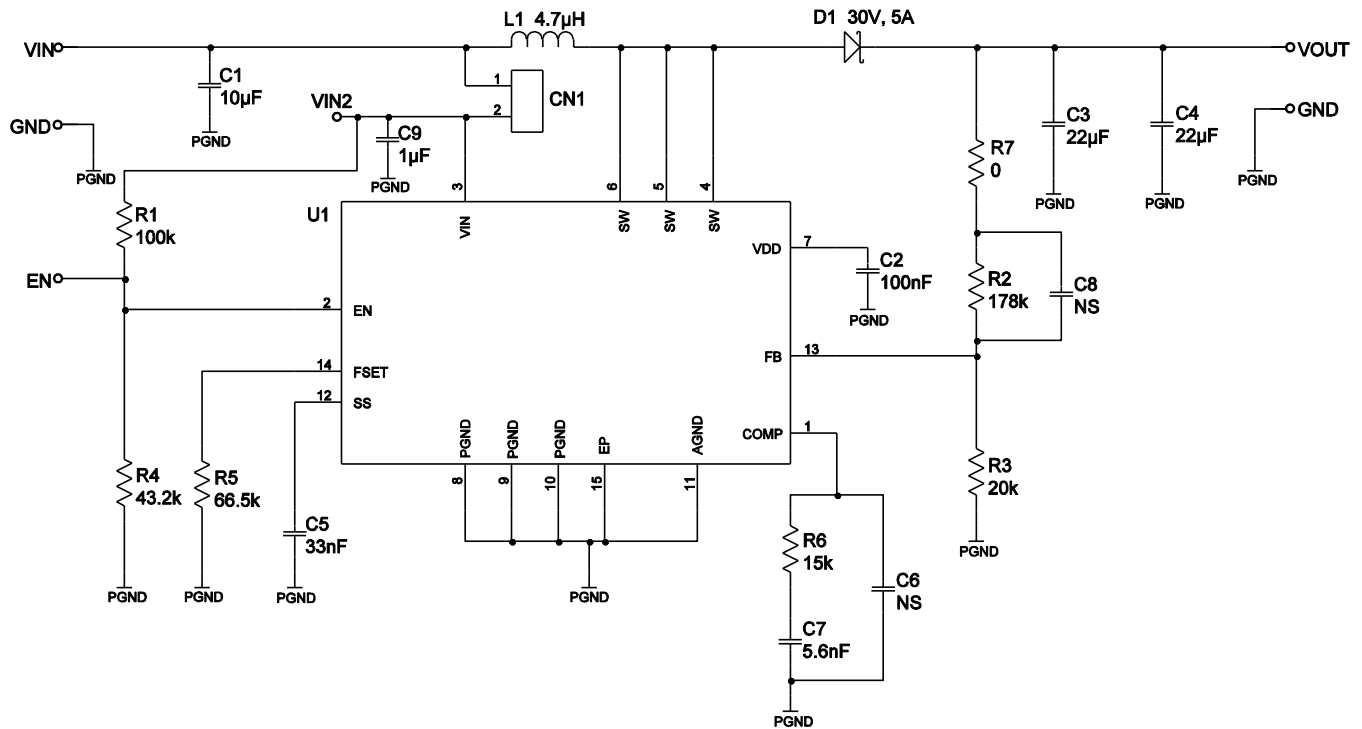
(L x W x H) 2.5" x 2.5" x 0.4"  
(6.35cm x 6.35cm x 1.0cm)

Board Number	IC Number
EV3426-L-00A	MP3426DL

### Efficiency



## EVALUATION BOARD SCHEMATIC



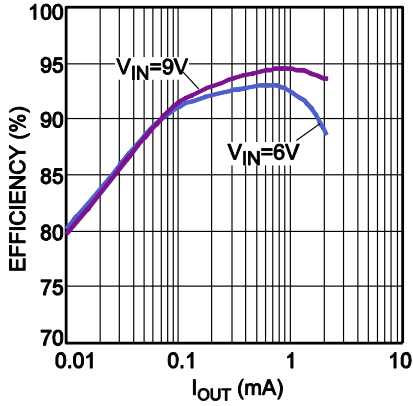
## EV3426-L-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
1	R1	100k	Film Res,5%	0603	ROYAL	RL0603FR-07100KL
1	R2	178k	Film Res,1%	0603	ROYAL	RL0603FR-07178KL
1	R3	20k	Film Res,1%	0603	ROYAL	RL0603FR-0720KL
1	R4	43.2k	Film Res,5%	0603	ROYAL	RC0603FR-0743K2L
1	R5	66.5k	Film Res,1%	0603	ROYAL	RC0603FR-0766K5L
1	R6	15k	Film Res,5%	0603	ROYAL	RL0603FR-0715KL
1	R7	0	Film Res,5%	0603	ROYAL	RC0603FR-070RL
1	C1	10µF	Ceramic Cap,25V,X7R	1210	muRata	GRM32DR71E106KA12L
1	C2	0.1µF	Ceramic Cap,16V,X7R	0805	muRata	GRM219R71C104KA01D
2	C3,C4	22µF	Ceramic Cap,25V,X7R	1210	muRata	GRM32ER71E226KE15L
1	C5	33nF	Ceramic Cap,50V,X7R	0603	TDK	C1608X7R1H333K
1	C6,C8	NC				
1	C7	5.6nF	Ceramic Cap,50V,X7R	0603	muRata	GRM188R71H562KA01D
1	C9	1.0µF	Ceramic Cap,25V,X5R	0805	muRata	GRM216R61E105KA12D
1	L1	4.7µH	IR=15.5A, Isat=17A, Rdc=6.35mOhm		Würth	744 332 047 0
1	D1	SS5P3	Schottky diode 30V 5A	TO-277A	Vishay	SS5P3
1	U1	MP3426	Boost converter	QFN	MPS	MP3426

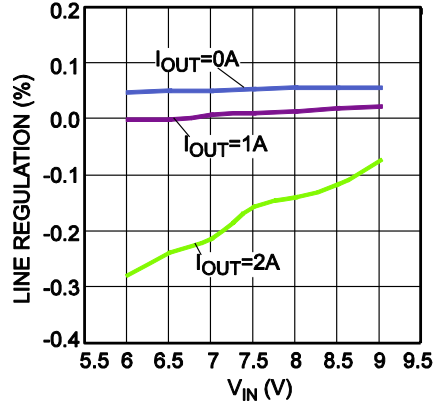
## EVB TEST RESULTS

Performance waveforms are tested on the evaluation board.

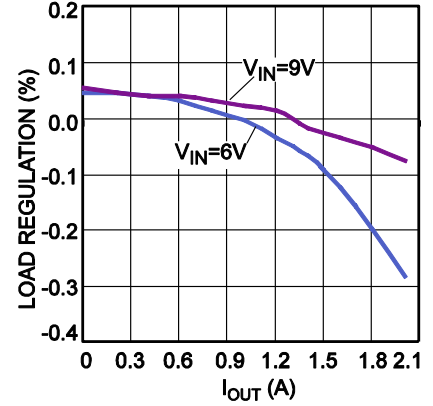
### Efficiency



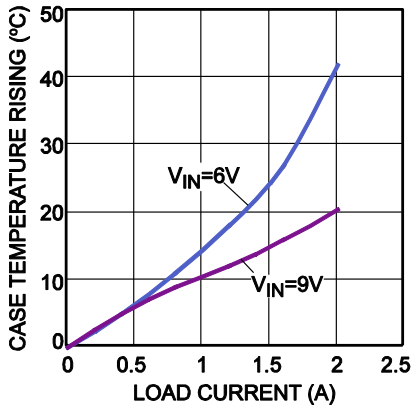
### Line Regulation



### Load Regulation



### Case Temperature Rising vs. Load Current

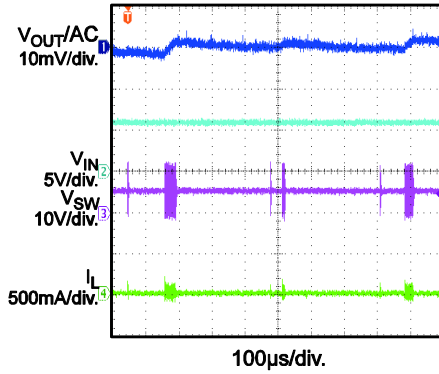


## EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board.

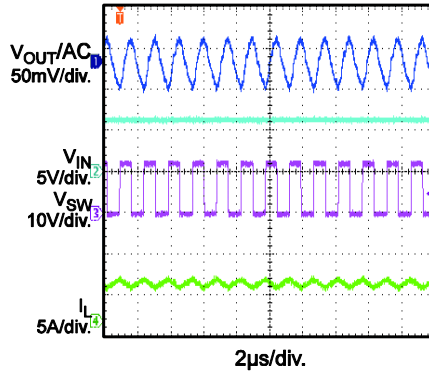
### Steady State

$V_{IN} = 6V, V_{OUT} = 12V/0A$



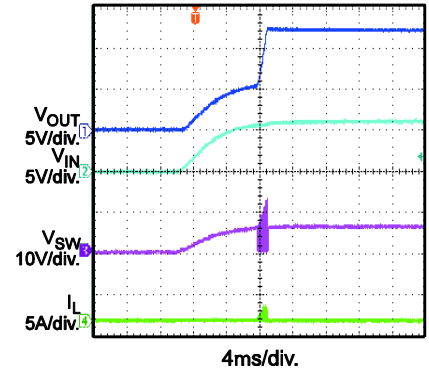
### Steady State

$V_{IN} = 6V, V_{OUT} = 12V/2A$



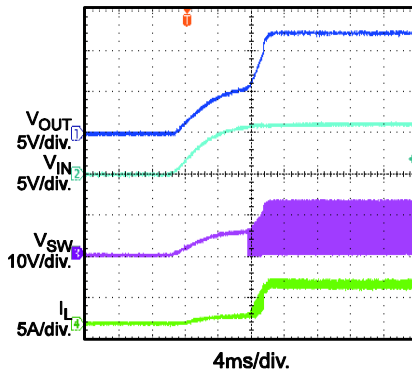
### VIN Start Up

$V_{IN} = 6V, V_{OUT} = 12V/0A$



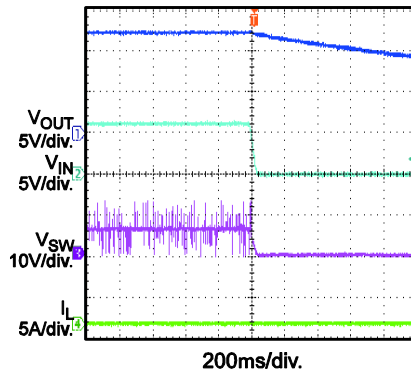
### VIN Start Up

$V_{IN} = 6V, V_{OUT} = 12V/2A$



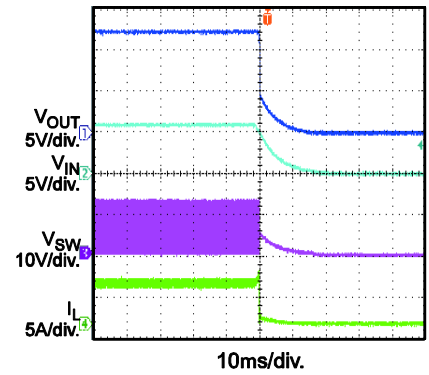
### VIN Shutdown

$V_{IN} = 6V, V_{OUT} = 12V/0A$



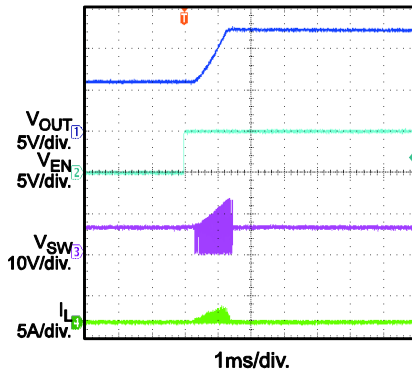
### VIN Shutdown

$V_{IN} = 6V, V_{OUT} = 12V/2A$



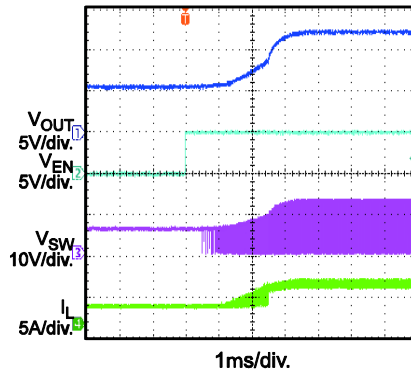
### EN Startup

$V_{IN} = 6V, V_{OUT} = 12V/0A$



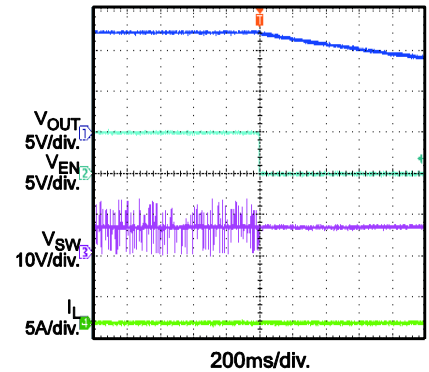
### EN Startup

$V_{IN} = 6V, V_{OUT} = 12V/2A$



### EN Shutdown

$V_{IN} = 6V, V_{OUT} = 12V/0A$

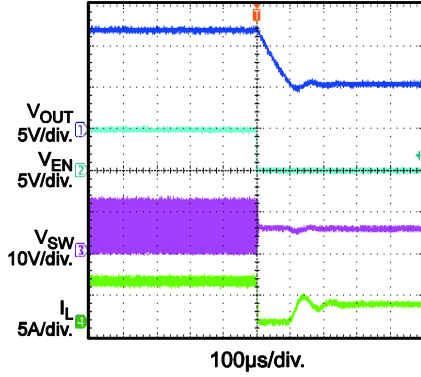


## EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.

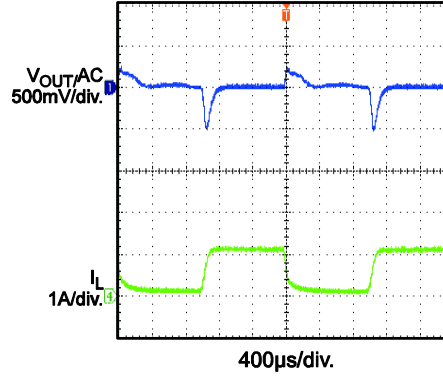
### EN Shutdown

$V_{IN} = 6V$ ,  $V_{OUT} = 12V/2A$



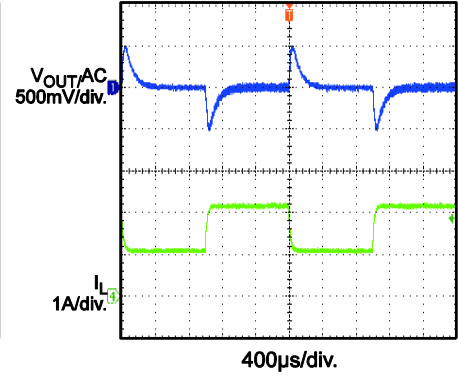
### Load Transient

$V_{IN} = 6V$ ,  $V_{OUT} = 12V$ ,  
 $I_{OUT} = 0$  to 1A,  $I_{RAMP} = 10mA/\mu s$



### Load Transient

$V_{IN} = 6V$ ,  $V_{OUT} = 12V$ ,  
 $I_{OUT} = 1$  to 2A,  $I_{RAMP} = 10mA/\mu s$



## PRINTED CIRCUIT BOARD LAYOUT

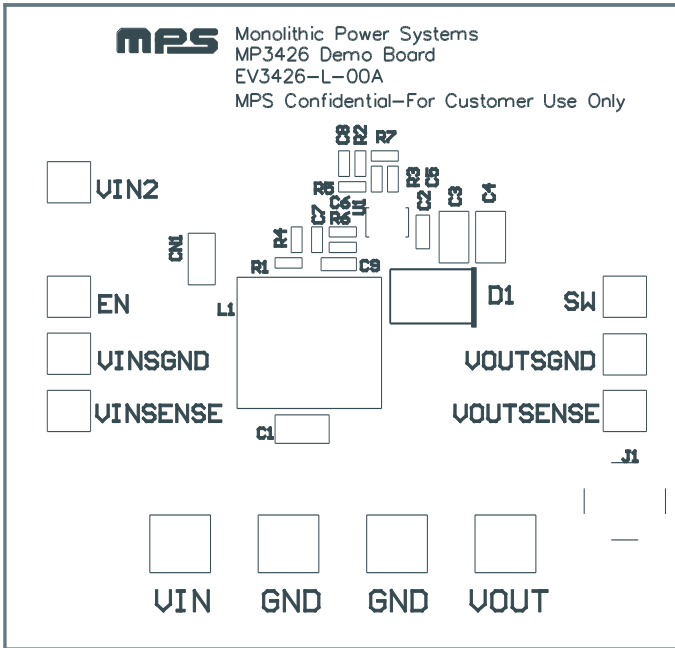


Figure 1—Top Silk Layer

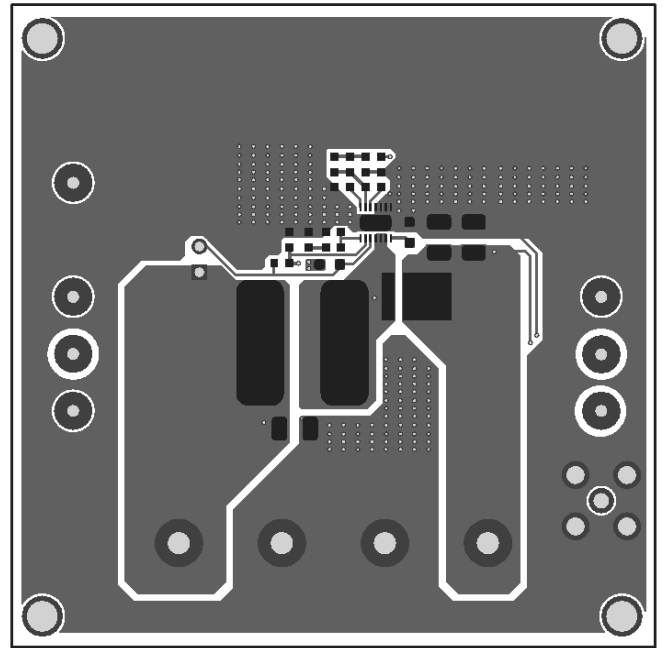


Figure 2—Bottom Layer

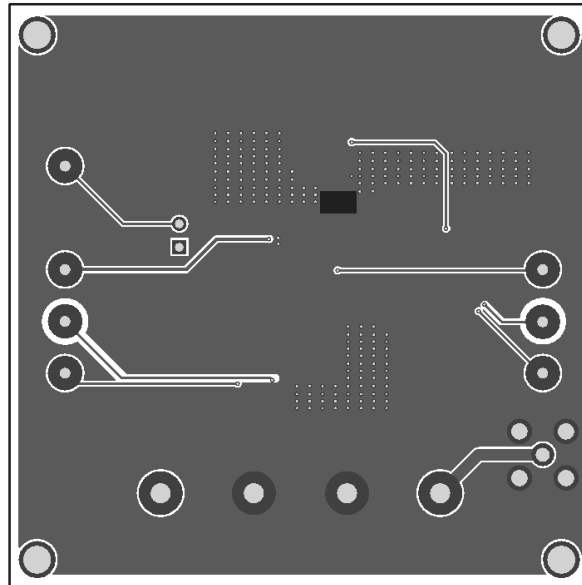


Figure 3—Bottom Layer