EV5512-V-00A

Peak Power Assist for Smart/AI-Enabled Speakers and Power Back-up for SSDs Evaluation Board

The Future of Analog IC Technology

DESCRIPTION

EV5512-V-00A Evaluation Board is designed to demonstrate the capabilities of MP5512. MP5512 is a peak power assist device intelligently designed for use in solid state drives and smart speakers.

MP5512 supports input hot-swap, input reverse current protection, input power failure indication and high efficient power backup. The built-in boost mode converter charges storage bulk capacitors to a programmed voltage while the system is powered up. For smart speakers, during peak power consumption, MP5512 supplies additional energy to the system to prevent browning out and system reset. For SSDs, in the case of input power failure, MP5512 transfers energy to support system data backup.

MP5512 is available in QFN28-4x5mm package.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	12	V
Storage Voltage	V_{STRG}	35	V
Input Pfail Threshold	V_{PFI}	6.1	V
Bus Backup Voltage	V_{RLS}	7.8	V
Bus Backup Max Load	$I_{RELEASE}$	3	A

FEATURES

- Wide 4V to 18V Operating Input Range
- Programmable up to 40V Storage Voltage
- Up to 4.5A Input Current Limit
- Input Reverse Current Protection
- Adjustable Slew Rate for VB Start-up Rising
- 14mΩ MOSFET for Input Hot-swap
- High Efficiency Power Backup with Internal 140mΩ and 110mΩ Power Switches
- Input Failure Indicator and Input Early Warning for V_{IN}
- Programmable Input Current Limit and Current Monitor
- Stable Work with 0.1μF Input Capacitor for Hot-swap
- Thermal Protection
- Available in a QFN28 (4mm×5mm) Package

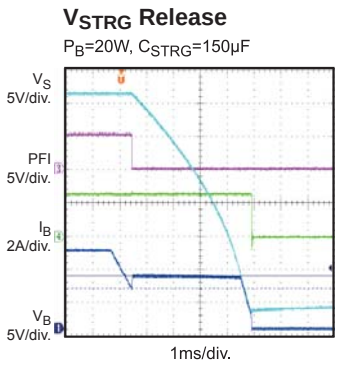
APPLICATIONS

- Peak Power Smoother for Smart Speakers
- Artificial Intelligence (AI)-Enabled Speakers
- Solid-State Drives
- Hard-Disk Drives
- Power Back-up Systems

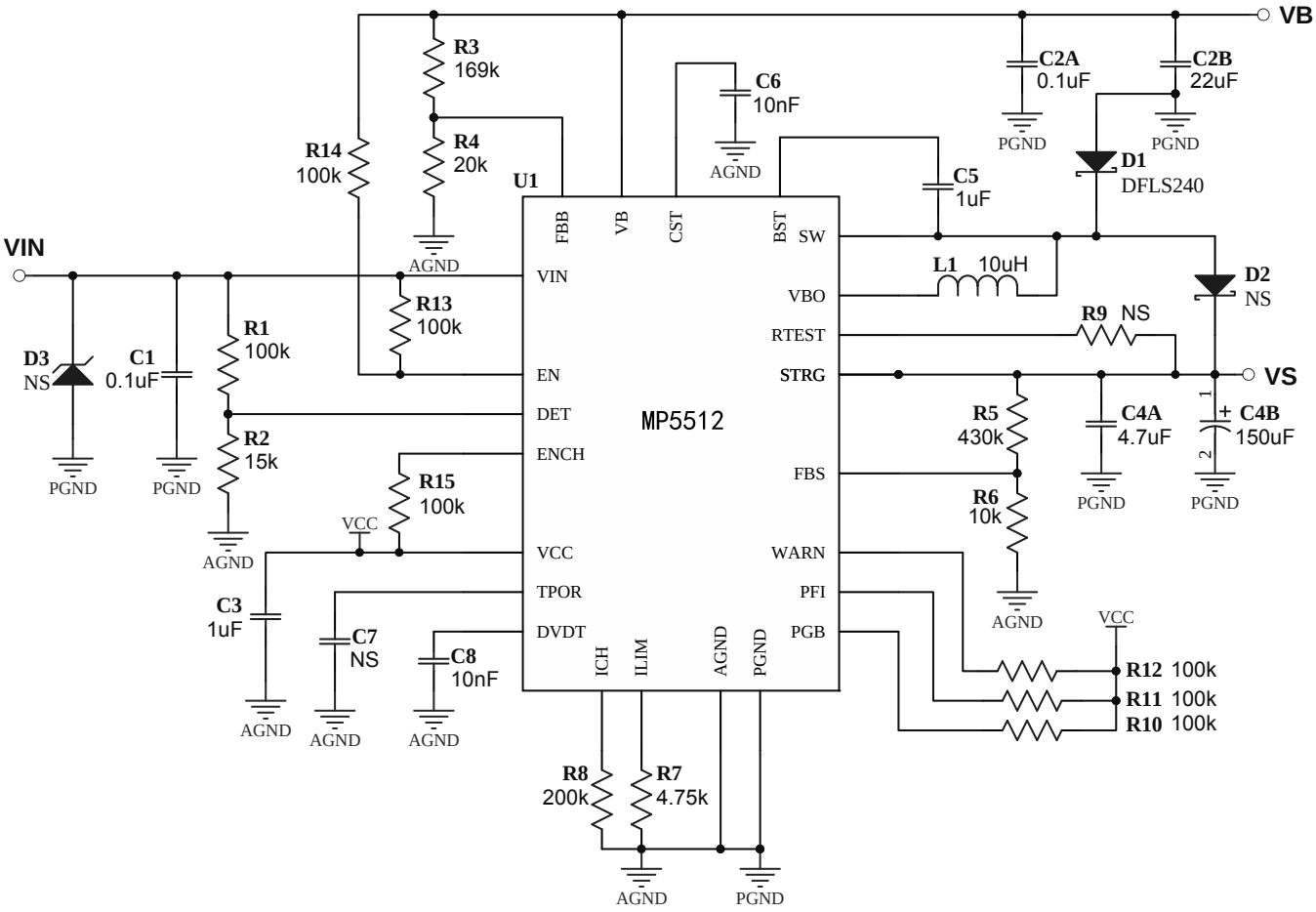
EV5512-V-00A EVALUATION BOARD

(L x W x H) 6.35cm x 6.35cm x 1.4cm

Board Number	MPS IC Number
EV5512-V-00A	MP5512GV



EVALUATION BOARD SCHEMATIC



Note:
1) Schottky diode D1 is required in all applications.

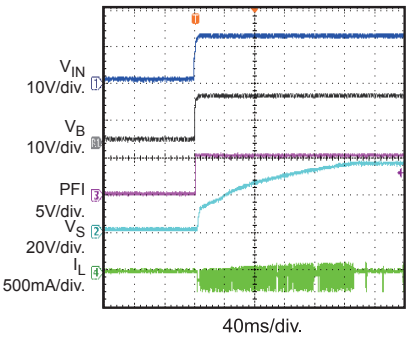
EV5512-V-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Part Number
2	C1, C2A	0.1μF	Ceramic Cap., 25V, X7R	0603	Murata	GRM188R71E104KA01D
1	C2B	22μF	Ceramic Cap., 25V, X7R	1206	Murata	GRM31ER71E226KE15L
2	C3, C5	1μF	Ceramic Cap., 10V, X5R	0402	Murata	GRM155R61A105KE15D
1	C4A	4.7μF	Ceramic Cap., 50V, X7R	1206	Murata	GRM31CR71H475KA12L
1	C4B	150μF	Electrolytic Cap., 50V	DIP	JiangHai	CD284
2	C6, C8	10nF	Ceramic Cap., 50V, X7R	0402	Murata	GRM155R71H103KA88D
0	C7	NS				
1	D1	DFLS240L	Schottky Diode, 40V, 2A	PowerDI123	Diodes	DFLS240L-7
0	D2, D3	NS				
1	L1	10μH	Inductor, I_{SAT}=4.9A, 41mΩ	SMD	Coilcraft	XAL5050-103ME
7	R1, R10, R11, R12, R13, R14, R15	100kΩ	Film Res., 1%	0402	Yageo	RC0402FR07100KL
1	R2	15kΩ	Film Res., 1%	0402	Yageo	RC0402FR0715KL
1	R3	169kΩ	Film Res., 1%	0402	Yageo	RC0402FR07169KL
1	R4	20kΩ	Film Res., 1%	0402	Yageo	RC0402FR0720KL
1	R5	430kΩ	Film Res., 1%	0402	Yageo	RC0402FR07430KL
1	R6	10kΩ	Film Res., 1%	0402	Yageo	RC0402FR0710KL
1	R7	4.75kΩ	Film Res., 1%	0402	Yageo	RC0402FR074K75L
1	R8	200kΩ	Film Res., 1%	0402	Yageo	RC0402FR07200KL
0	R9	NS				
1	U1	MP5512	Energy Storage and Management Unit	QFN28 4x5	MPS	MP5512GV

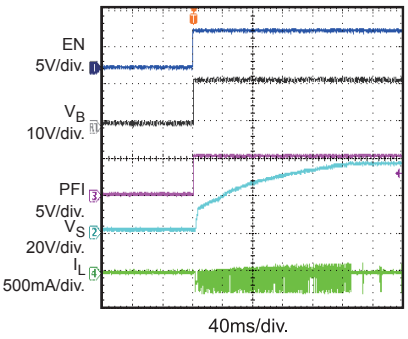
EVB TEST RESULTS

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{STRG} = 35V, V_{PFI} = 6.1V, V_{RLS} = 7.8V(2), L = 10µH, T_A = 25ºC, P_{OUT} = 20W, unless otherwise noted.

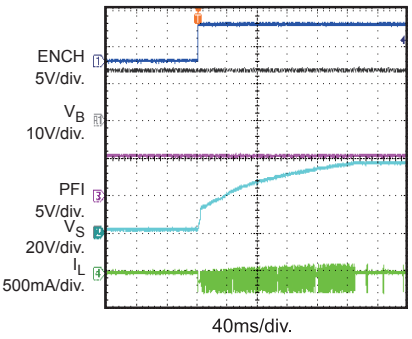
V_{IN} Power On



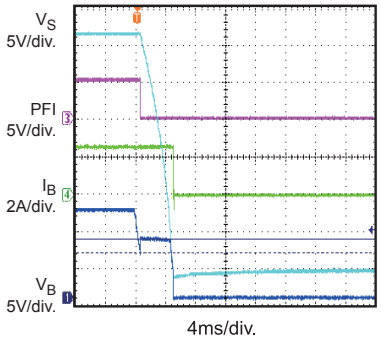
EN Power On



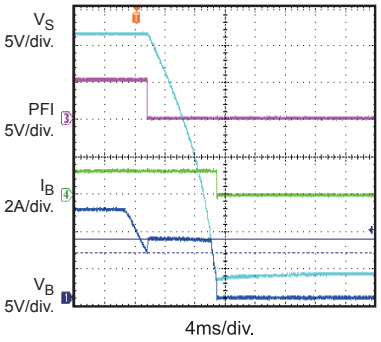
ENCH Power On



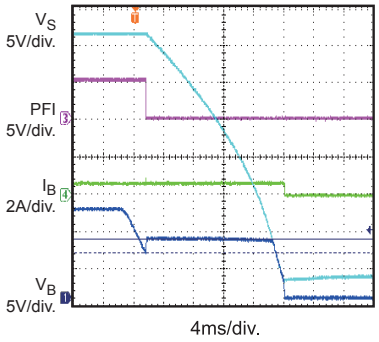
V_{STRG} Release
P_B=20W, C_{STRG}=150µF



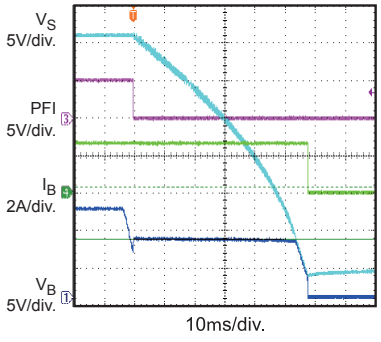
V_{STRG} Release
P_B=10W, C_{STRG}=150µF



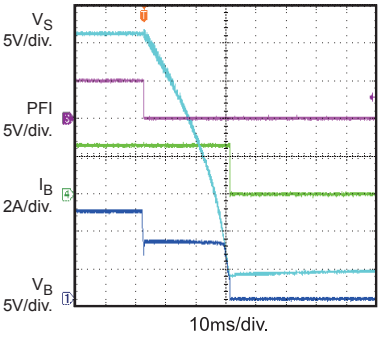
V_{STRG} Release
P_B=5W, C_{STRG}=150µF



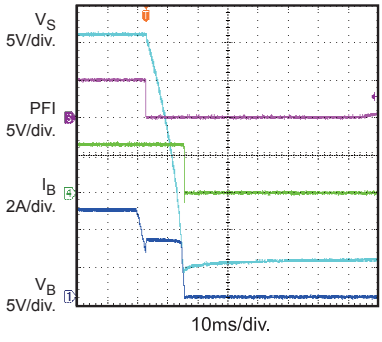
V_{STRG} Release
P_B=20W, C_{STRG}=2200µF



V_{STRG} Release
P_B=20W, C_{STRG}=1000µF



V_{STRG} Release
P_B=20W, C_{STRG}=440µF



Note:
2) V_{RLS} voltage varies a little with different V_{STRG} voltage because the internal RAMP voltage on FBB changes with duty cycle. 7.8V voltage is estimated based on 30V V_{STRG} condition.

PRINTED CIRCUIT BOARD LAYOUT

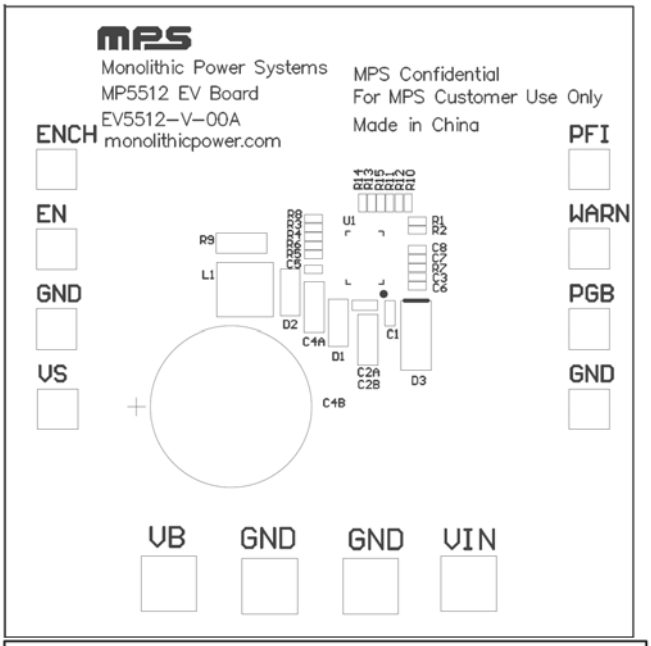


Figure 1—Top Silk Layer

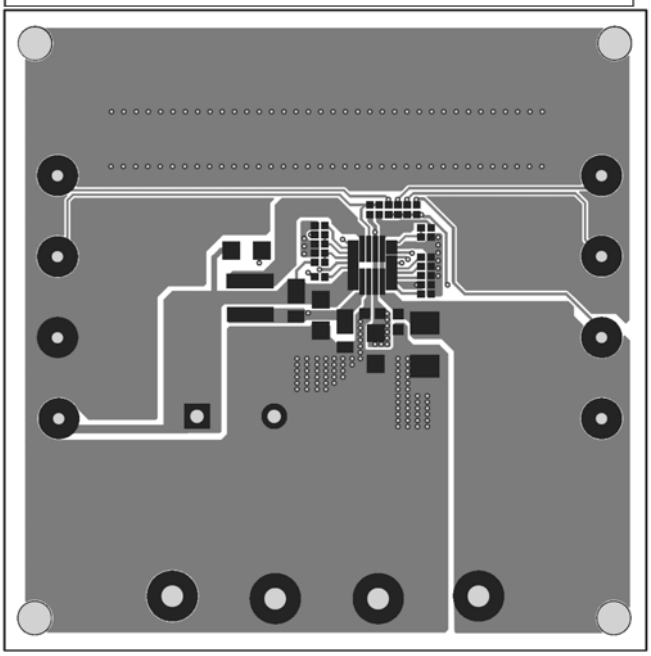


Figure 2—Top Layer

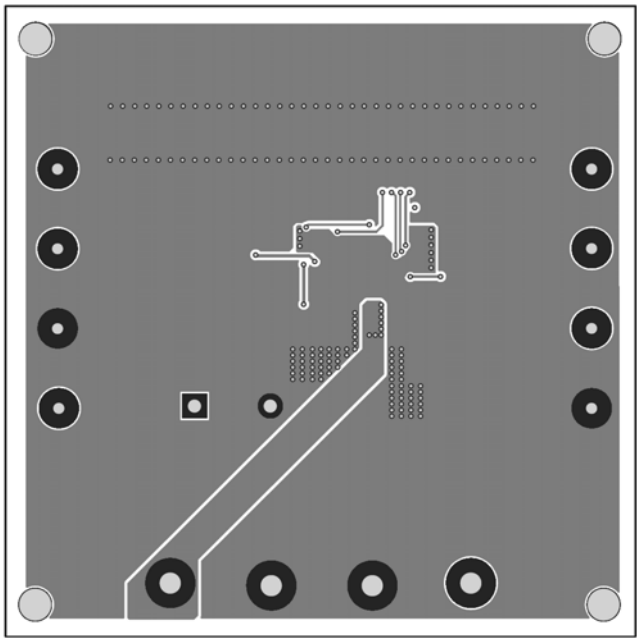


Figure 3—Bottom Layer