

DESCRIPTION

The EV5610-QG-00A is an evaluation board for the MP5610. The MP5610 is a dual-output converter for small size LCD panel bias supply.

With the 2.7V-5V input voltage, the EV5610-QG-00A can provide +/-5.4V output voltage with 40mA current capability for LCD. The voltage tracking between positive and negative output is good under variable load condition.

The variety protections are including in EV5610-QG-00A. Output OVP, Output UVP, Input DC Current Limit, Cycle-by-Cycle Current Limit and OTP.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage	V _{IN}	2.7-5	V
Positive Output Voltage	V ₊	5.4	V
Negative Output Voltage	V ₋	-5.4	V
Output Current	I _o	0-40	mA

FEATURES

- 2.7V-to-5.5V Input Voltage
- Max. 50mA Output Current for Each Output
- Up to Programmable 5.8V Output Voltage
- 0.5% Line Regulation for Step-up Converter
- 0.5% Load Regulation for Step-up Converter
- 1% Voltage Tracking Between Dual-ch
- 600mV Feedback Voltage with ±1% Accuracy
- 270us Soft Start Time
- Input DC Current Limit Protection
- Output Over Voltage Protection
- Output Under Voltage Protection
- Input UVLO Protection
- Over Temperature Protection
- Available in a QFN-10 (1.4mm×1.8mm) Package

APPLICATIONS

- Feature Phones and Smart Phones
- Small Size LCD Displays

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology", are Registered Trademarks of Monolithic Power Systems, Inc.

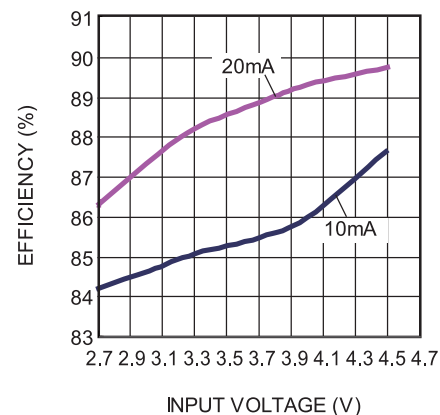
EV5610-QG-00A EVALUATION BOARD



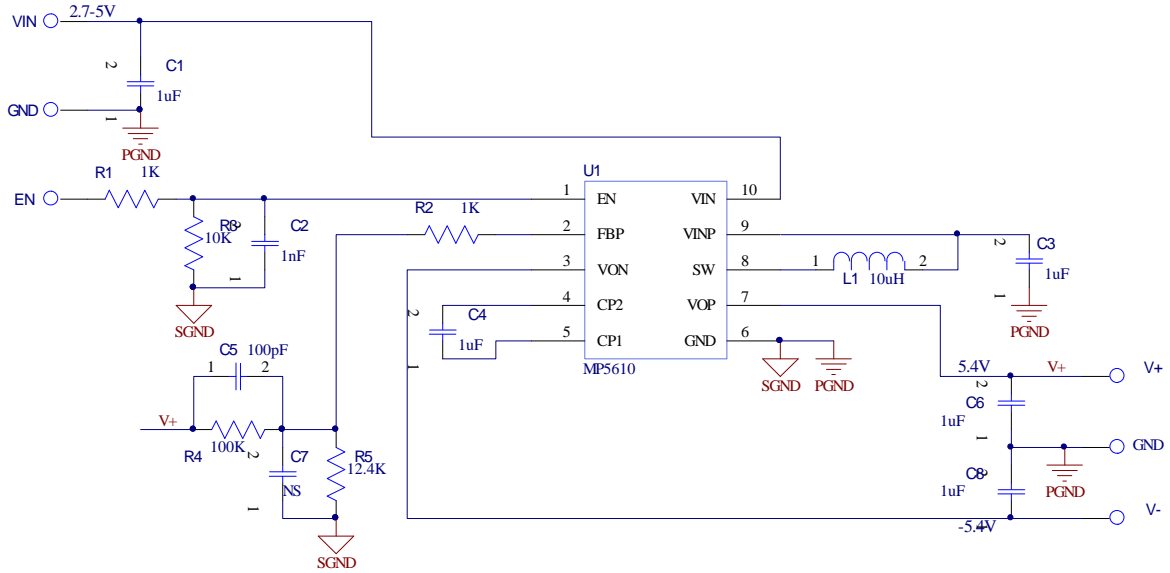
(L x W x H) 5cm x 4.6cm x 3mm

Board Number	MPS IC Number
EV5610-QG-00A	MP5610GQG

Efficiency vs. V_{IN}



EVALUATION BOARD SCHEMATIC



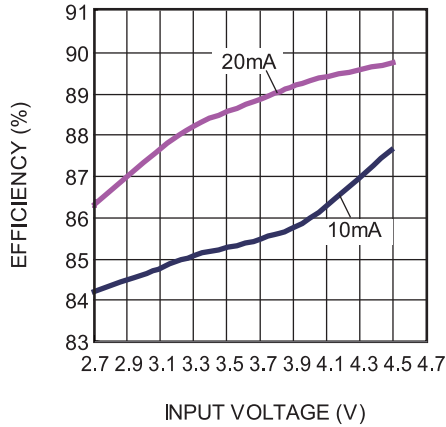
BILL OF MATERIALS

Qty	Designator	Value	Description	Package	Manufacture	Manufacture_PN
2	C1, C3	1uF/6.3V	Ceramic Capacitor;6.3V;X7R;0603;	0603	Murata	GRM188R70J105KA01D
1	C2	1nF	Ceramic Capacitor;50V;X7R;0603;	0603	TDK	C1608X7R1H102K
3	C4, C6, C8	1uF/10V	Ceramic Capacitor;10V;X7R;0603	0603	Murata	GRM188R71A105KA61D
1	C5	100pF	Ceramic Capacitor;50V;COG;0603;	0603	TDK	C1608COG1H101J
1	C7	NS				
1	L1	10uH	Inductor;10uH;420m;300mA	3225	TOKO	DFE322512C 1277AS-H-100M
2	R1, R2	1K	Film Resistor;1%	0603	Yageo	RC0603FR-071KL
1	R3	10K	Film Resistor;1%;	0603	Yageo	RC0603FR-0710KL
1	R4	100K	Film Resistor;1%;	0603	Yageo	RC0603FR-07100KL
1	R5	12.4K	Film Resistor;1%;	0603	Yageo	RC0603FR-0712K4L
1	U1	MP5610	Dual-ch LCD Bias	QFN-10	MPS	MP5610GQG

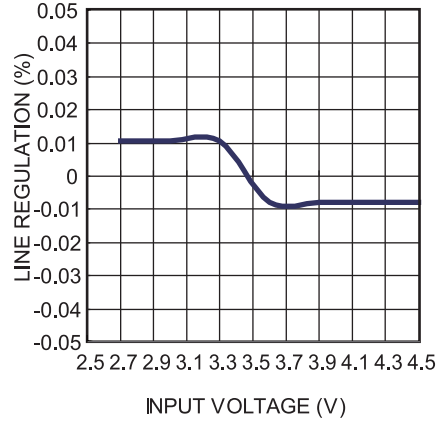
EVB TEST RESULTS

$V_{IN} = 3.7V$, $V_{+} = 5.4V$, $V_{-} = -5.4V$, $T_A = 25^{\circ}C$, unless otherwise noted.

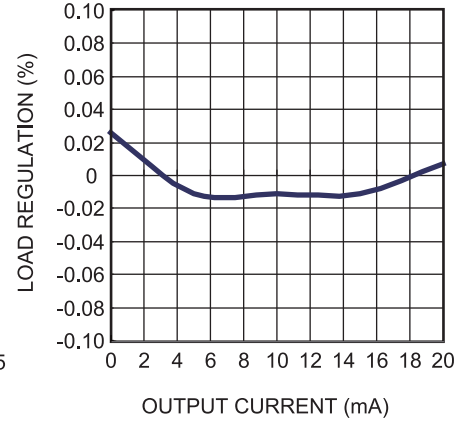
Efficiency vs. V_{IN}



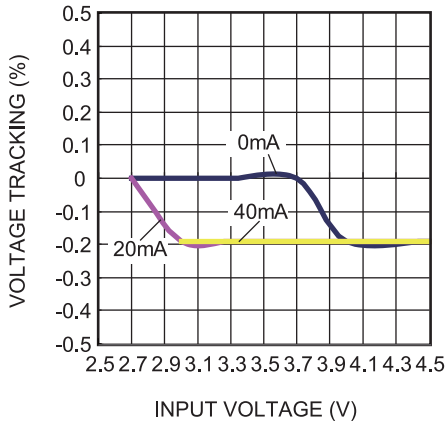
Line Regulation



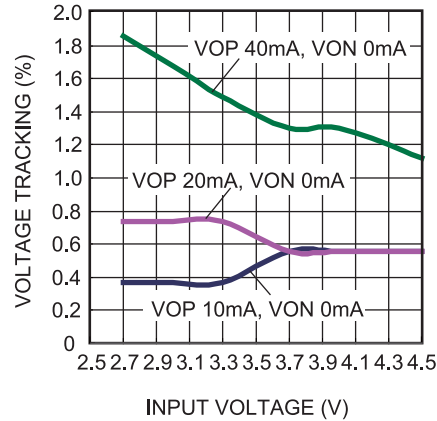
Load Regulation



Voltage Tracking @ Symmetric Load



Voltage Tracking @ Asymmetric Load

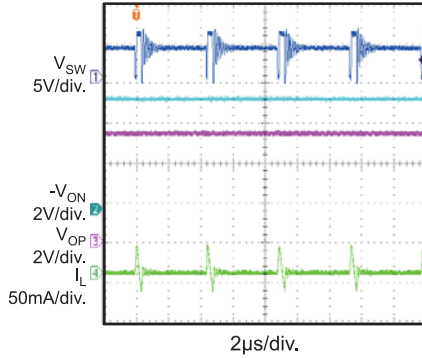
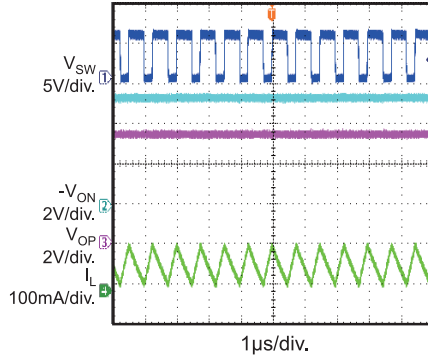
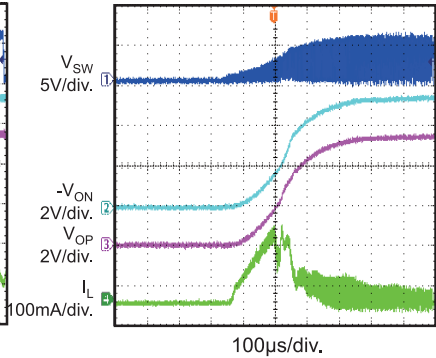
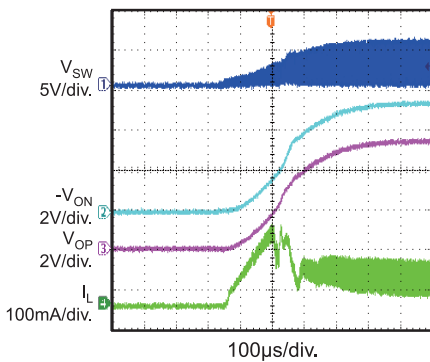
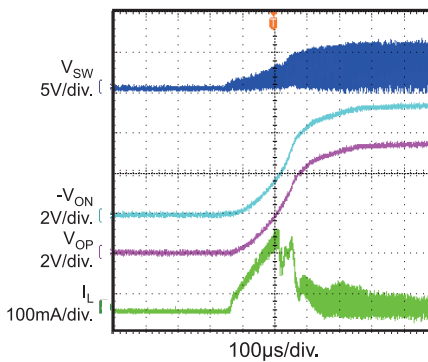
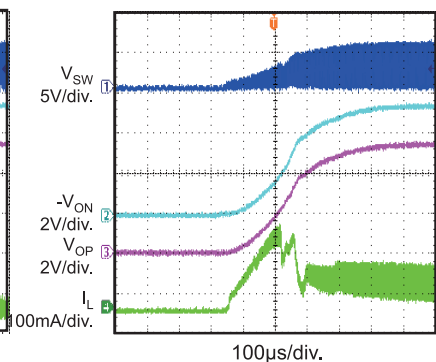
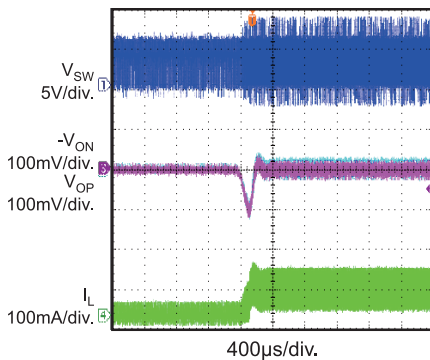
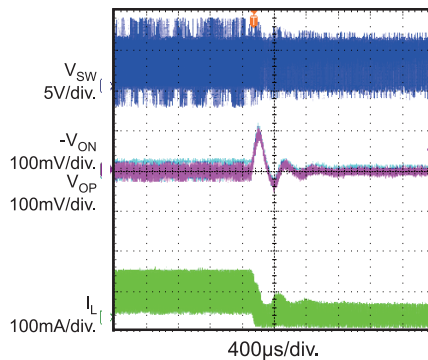
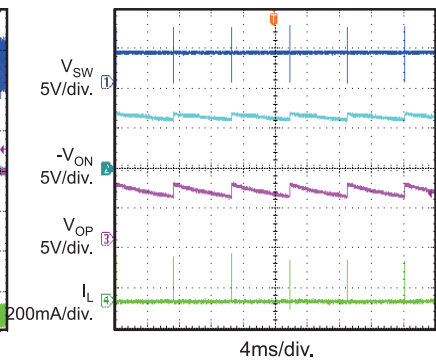


Notes:

(a) Line/Load Regulation: $(V_{OP} - V_{OP,AVG}) / V_{OP,AVG} * 100\%$.

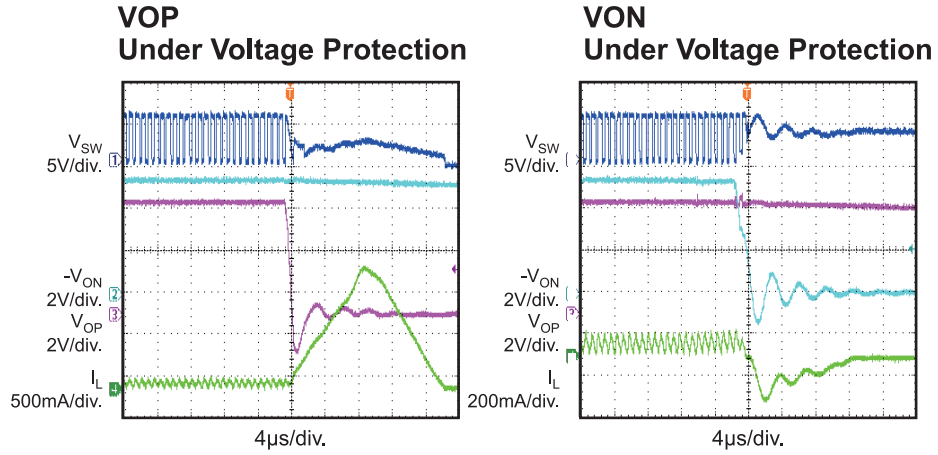
(b) Voltage Tracking: $(|V_{ON}| - V_{OP}) / V_{OP} * 100\%$.

EVB TEST RESULTS (continued)
 $V_{IN} = 3.7V$, $V_{+} = 5.4V$, $V_{-} = -5.4V$, $T_A = 25^{\circ}C$, unless otherwise noted.

**Steady State
@ No Load**

**Steady State
@ 20mA Symmetric Load**

**V_{IN} Startup
@ No Load**

**V_{IN} Startup
@ 20mA Symmetric Load**

**EN Startup
@ No Load**

**EN Startup
@ 20mA Symmetric Load**

**Load Transient
0->20mA**

**Load Transient
20mA->0mA**

Over Voltage Protection


EVB TEST RESULTS (continued)

$V_{IN} = 3.7V$, $V_{+} = 5.4V$, $V_{-} = -5.4V$, $T_A = 25^{\circ}C$, unless otherwise noted.



PRINTED CIRCUIT BOARD LAYOUT

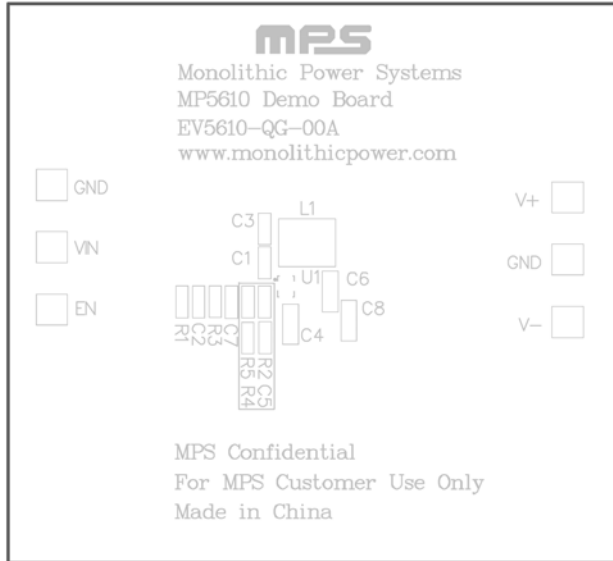


Figure 1—Top Silk Layer

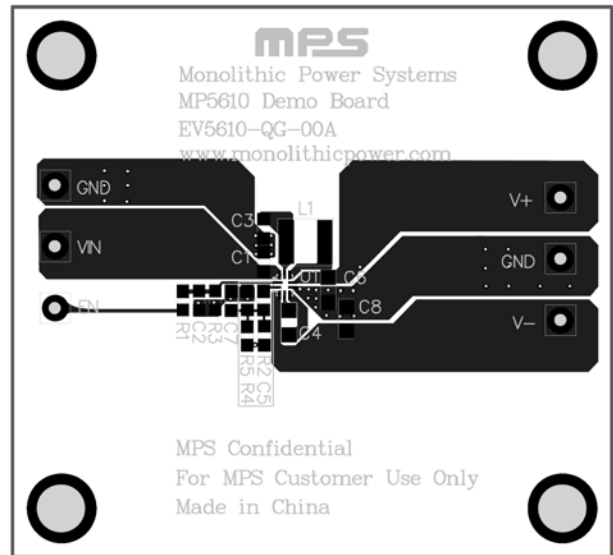


Figure 2—Top Layer

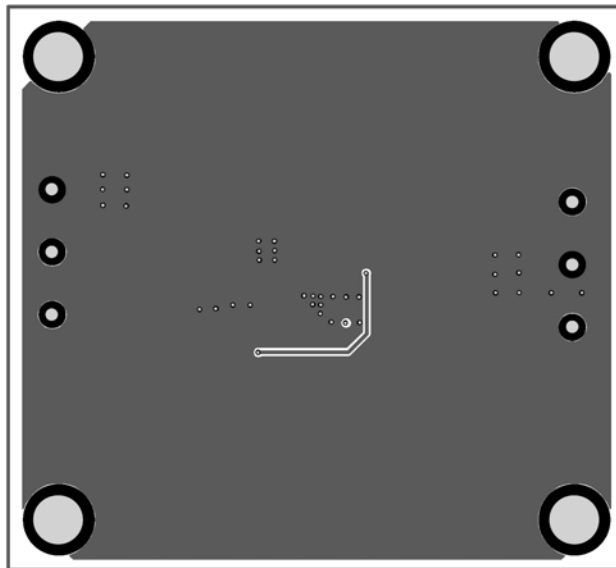


Figure 3—Bottom Layer