

DESCRIPTION

The EV8110DS-00A is an evaluation board for the MP8110, a low-cost, precision, high-side current-sense amplifier. The input voltage ranges from 2.5V to 40V. The output voltages are proportional to the load current with a 1V output corresponding to 5A of load current.

The MP8110 operates from a single 2.5V to 40V supply and typically consumes 17µA. It is ideal for today's notebook computers, cell phones and other systems where battery/DC current monitoring is critical.

High-side current monitoring is especially useful in battery-powered systems since it does not interfere with the ground path of the battery charger. The input common-mode range of 1.4V to 40V is independent of the supply voltage and ensures that the current-sense feedback remains viable even when connected to a 2-cell battery pack in deep discharge.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	$V_{IN}=V_{CC}$	2.5 – 40	V
Load Current	I_{LOAD}	0 – 5	A
Output Voltage 1	V_{OUT1}	0 – 1	V
Output Voltage 2	V_{OUT2}	0 – 1	V

FEATURES

- 2.5V to 40V Operating Supply Voltage
- 1.4V to 40V Input Common Mode Range
- Fully Assembled and Tested

APPLICATIONS

- Portable PCs
- PDA's
- Smart Battery Packs
- Cell Phones
- Portable Test/Measurement Systems
- Battery-Operated Systems
- Energy Management Systems

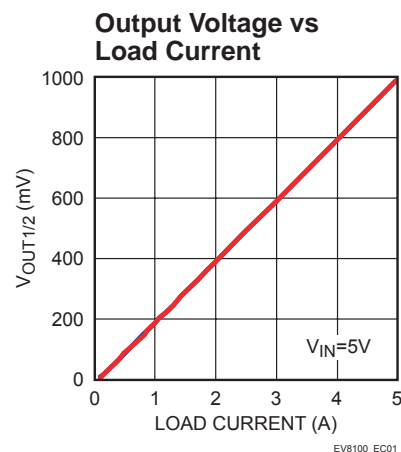
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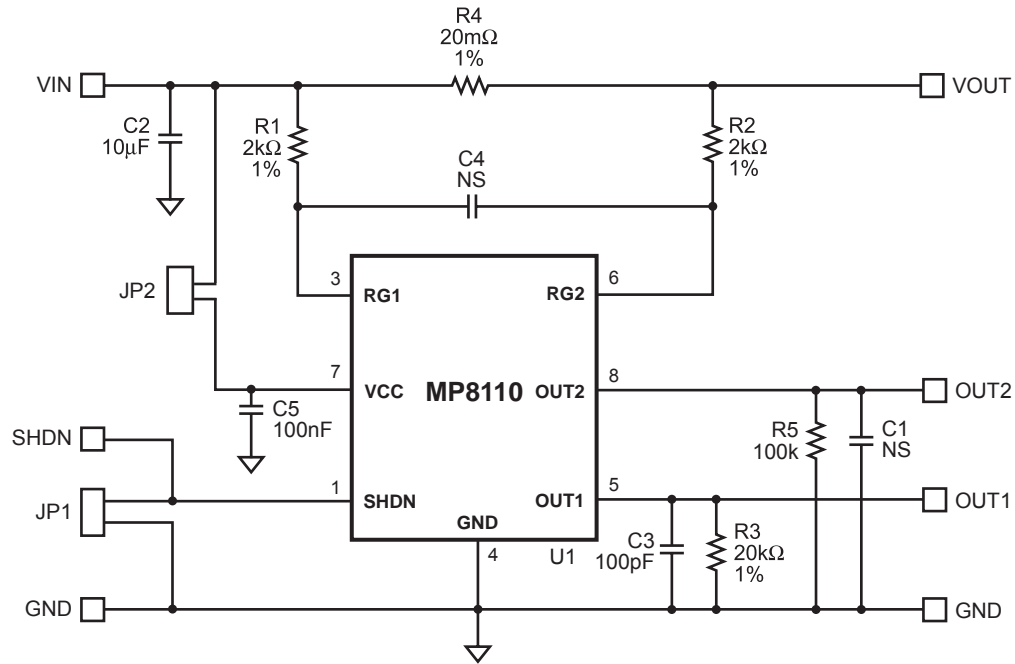
EV8110DS-00A EVALUATION BOARD



(L x W x H) 1.7" x 1.6" x 0.6"
(4.4cm x 4.2cm x 1.4cm)

Board Number	MPS IC Number
EV8110DS-00A	MP8110DS



EVALUATION BOARD SCHEMATIC

EV8110DS-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer P/N
1	C3	100pF	Ceramic Cap., 50V, NPO	805	TDK
1	C5	100nF	Ceramic Cap., 50V, X7R	805	TDK
1	C2	NS	Electrolytic Cap, 50V	F60	United Chemi-con
1	C4	NS	Do Not Stuff	805	
1	C1	NS	Do Not Stuff	805	
2	R1, R2	2k Ohm	Film Res., 1%	805	Panasonic
1	R3	20k Ohm	Film Res., 1%	805	Panasonic
1	R4	0.02 Ohm	Film Res., 1%	2512	Panasonic
1	R5	100k Ohm	Film Res., 5%	805	Panasonic

PRINTED CIRCUIT BOARD LAYOUT

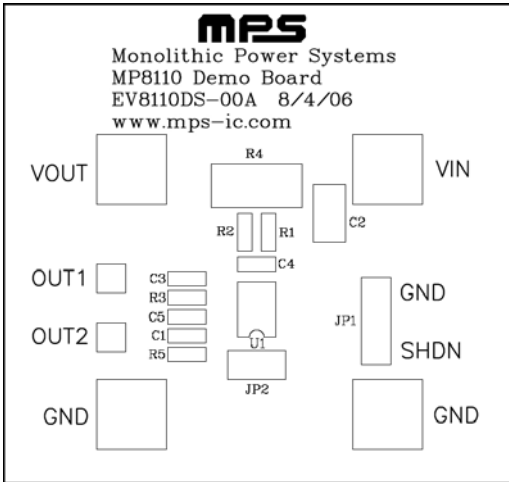


Figure 1—Top Silk Layer

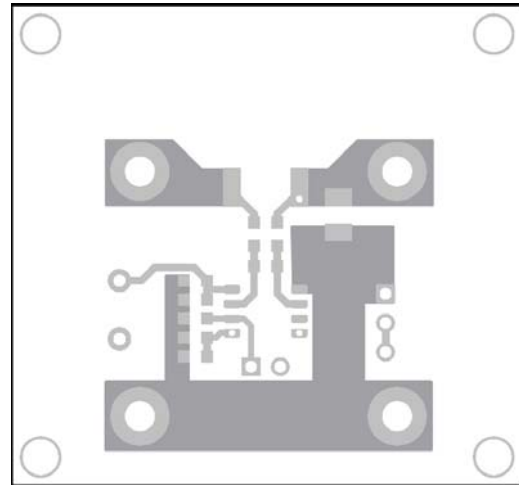


Figure 2—Top Layer

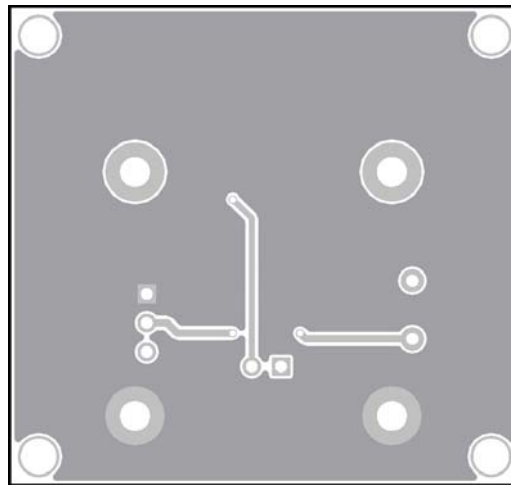


Figure 3—Bottom Layer