

### DESCRIPTION

The EV9486A-N-00A Evaluation Board is designed to demonstrate the performances of MPS' MP9486A which is a 4.5V-to-100V-input step-down converter.

The MP9486A employs hysteresis voltage control method to provide fast response to line or load transient. It integrates a high-side high voltage power MOSFET with a current limit of typical 3.5A. MPS's proprietary feedback control scheme minimizes the number of external components.

This board is configured for 5V step-down application. It can support 1A continuous load or 2A pulse load. The circuit requires only a minimal number of readily-available, standard, external components.

### ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Supply Voltage	$V_{IN}$	8 – 95	V
Output Voltage	$V_{OUT}$	5	V
Output Current	$I_{OUT}$	0-1	A

### FEATURES

- 8V-to-95V Wide Input Range<sup>(1)</sup>
- Hysteretic Control: Simple Compensation
- Up to 1MHz Switching Frequency
- Hiccup mode Short Circuit Protection
- Thermal Shut Down
- 170 $\mu$ A Quiescent Current
- Available in SOIC8 with Exposed Pad Package

**Note:** 1) MP9486A can support 4.5V-to-95V DC input, 8V minimum voltage is needed when  $V_{OUT}$  sets to 5V. MP9486A can support up to 100V input spike voltage.

### APPLICATIONS

- Scooter, E-bike Control Power Supply
- Solar Energy System
- Automotive System Power
- Industrial Power Supply

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

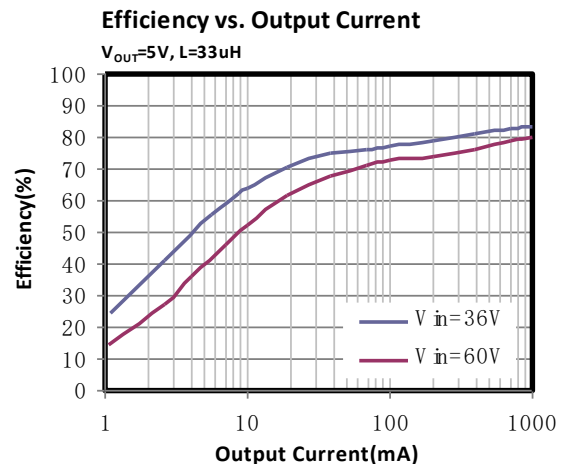
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### EV9486A-N-00A EVALUATION BOARD

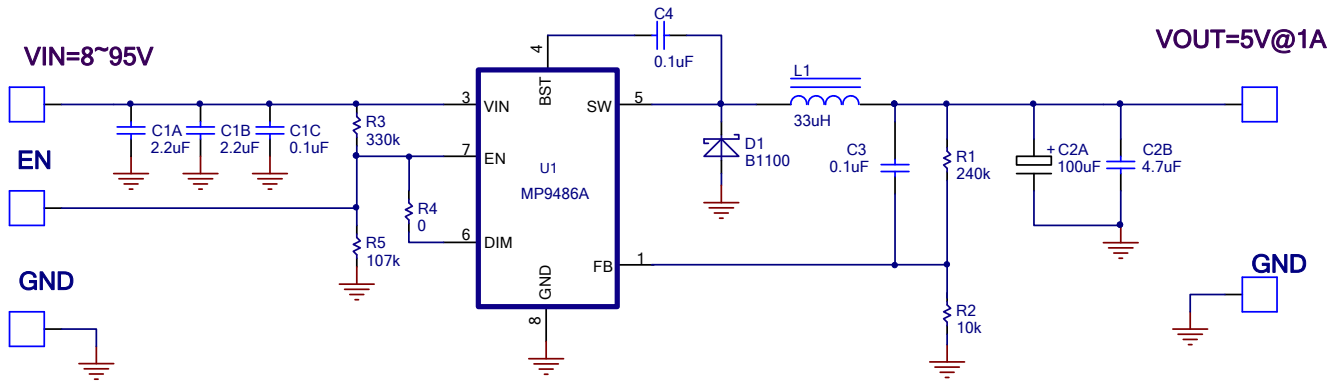


(L x W x H) 6.3cm x 6.3cm x 1.3cm

Board Number	MPS IC Number
EV9486A-N-00A	MP9486AGN



## EVALUATION BOARD SCHEMATIC



**EV9486A-N-00A BILL OF MATERIALS**

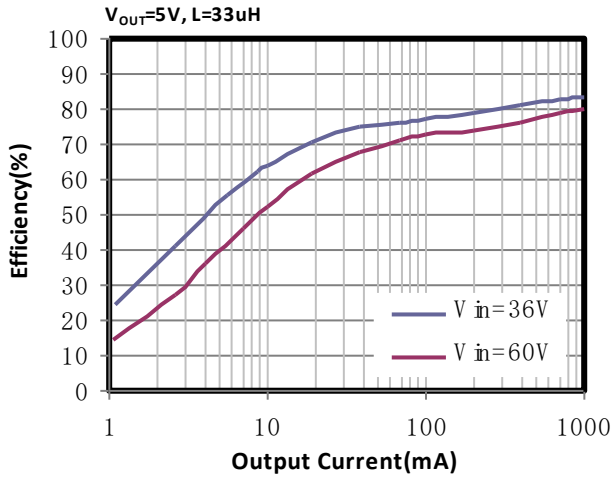
Qty	Ref	Value	Description	Package	Manufacturer	Part Number
2	C1A, C1B	2.2 $\mu$ F	Ceramic Cap., 100V, X7R	1210	muRata	GRM32ER72A225K
1	C1C	0.1 $\mu$ F	Ceramic Cap., 100V, X7R	0805	muRata	GCM21BR72A104K
1	C2A	100 $\mu$ F	10V, 0.74A solid tantalum capacitor, ESR=200m $\Omega$	SMD (3.2x6.0)	VISHAY	TR3C107M010C0200
1	C2B	4.7 $\mu$ F	25V X7R Ceramic Capacitor	0805	muRata	GRM21AR71E475KL
2	C3,C4	0.1 $\mu$ F	25V Ceramic Capacitor	0603	muRata	GRM188R71E104KL
1	D1	B1100	100V,1A,schottky diode	SMA	DIODES	B1100-LS
1	L1	33 $\mu$ H	66 m $\Omega$ , Isat=2.9A inductor	SMD (10X10)		744771433
1	R1	240k	Film resistor, 1%	0603	YAGEO	RC0603FR-07240KL
1	R2	10k	Film resistor, 1%	0603	YAGEO	RC0603FR-0710KL
1	R3	330k	Film resistor, 1%	0603	YAGEO	RC0603FR-07330KL
1	R4	0	Film resistor, 5%	0603	YAGEO	RC0603JR-070RL
1	R5	107k	Film resistor, 1%	0603	YAGEO	RC0603FR-07107KL
1	U1	MP9486A	100V INPUT, 3.5A STEP-DOWN CONVERTER	SOIC8	MPS	MP9486AGN

## EVB TEST RESULTS

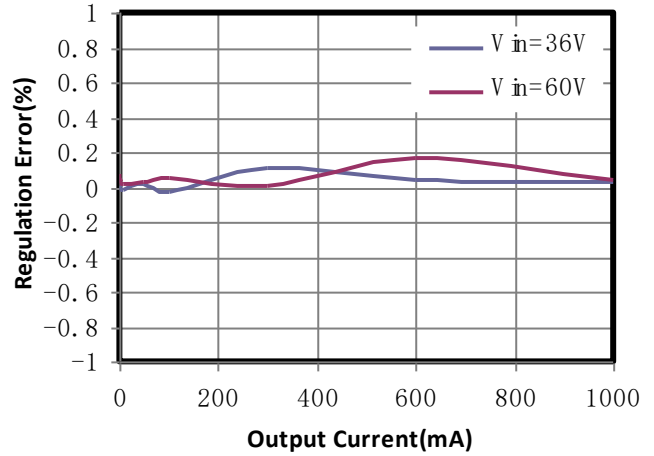
Performance waveforms are tested on the evaluation board.

$V_{IN} = 60V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ ,  $L=33\mu H$ ,  $C_{OUT} = 100\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

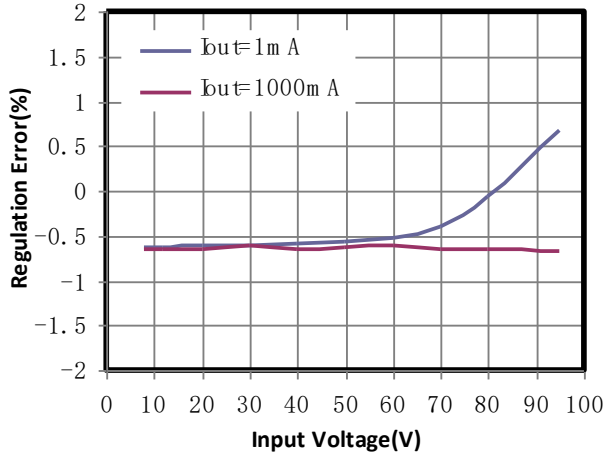
**Efficiency vs. Output Current**



**Load Regulation**



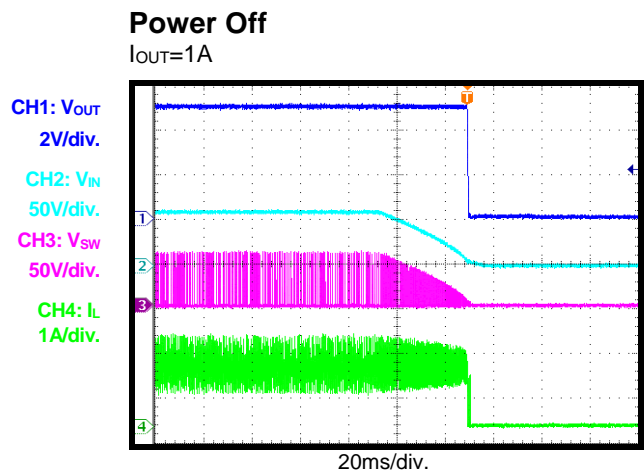
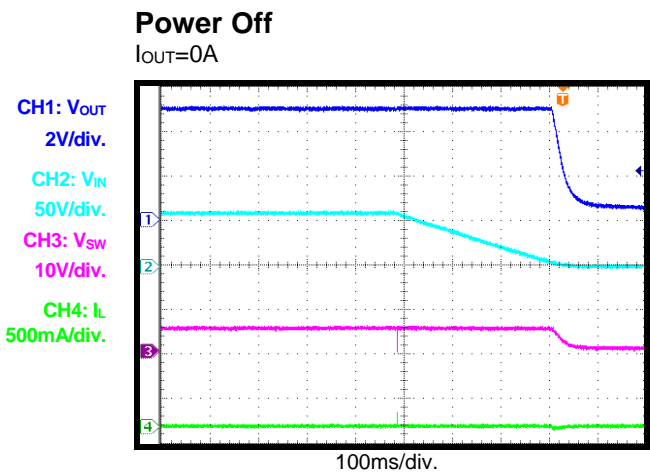
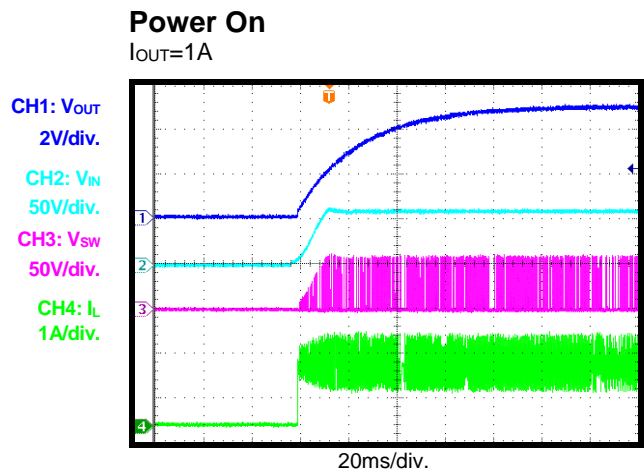
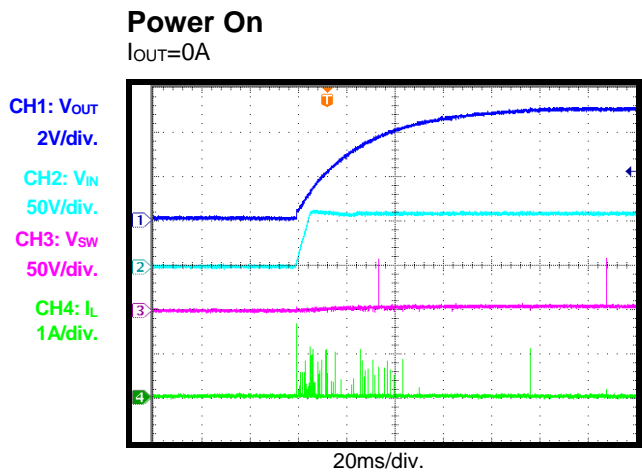
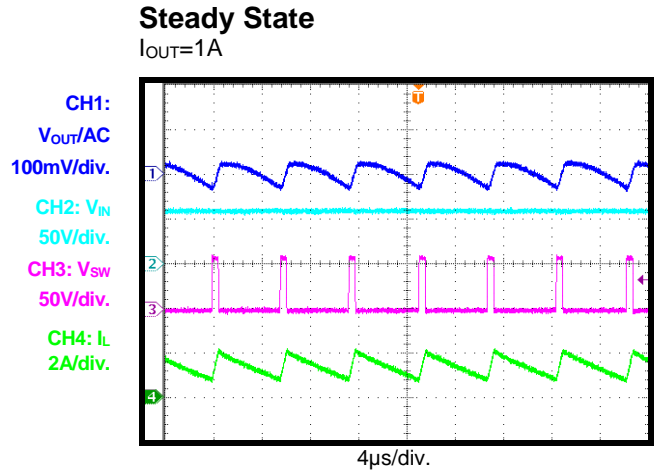
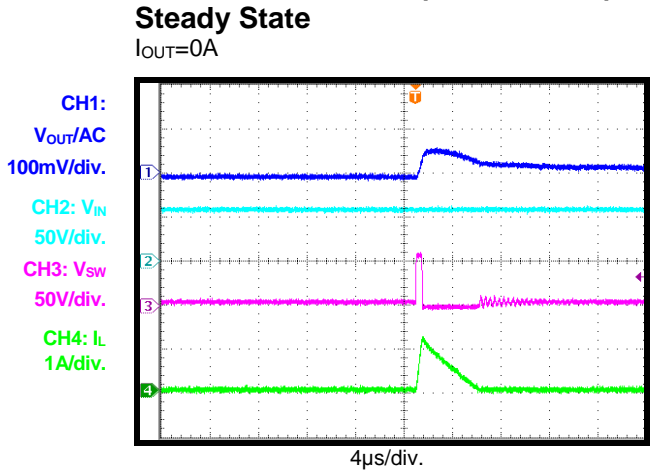
**Line Regulation**



## EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.

$V_{IN} = 60V$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 1A$ ,  $L=33\mu H$ ,  $C_{OUT} = 100\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



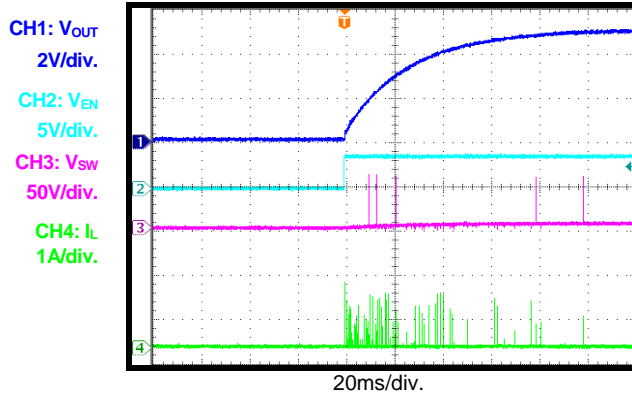
## EVB TEST RESULTS (continued)

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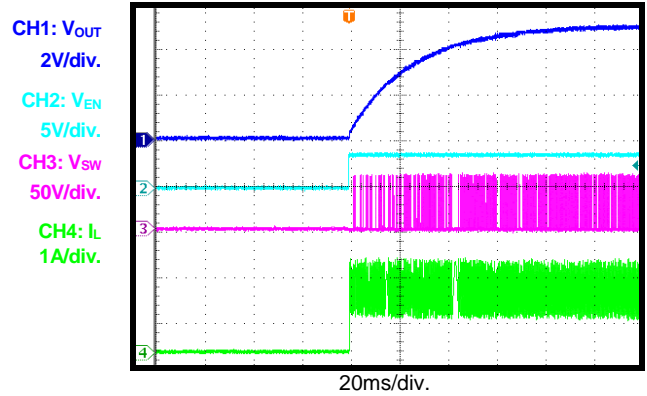
### EN Start-Up

$I_{OUT}=0A$



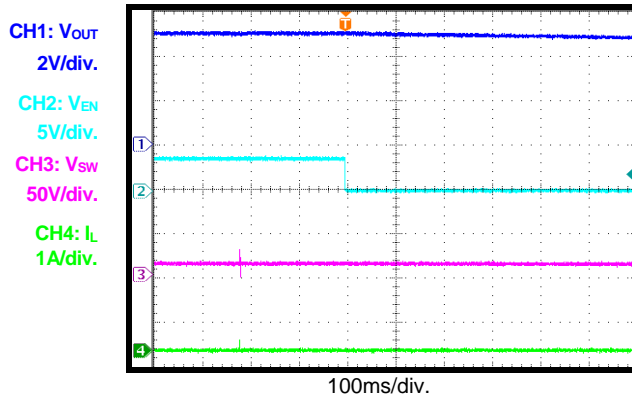
### EN Start-Up

$I_{OUT}=1A$



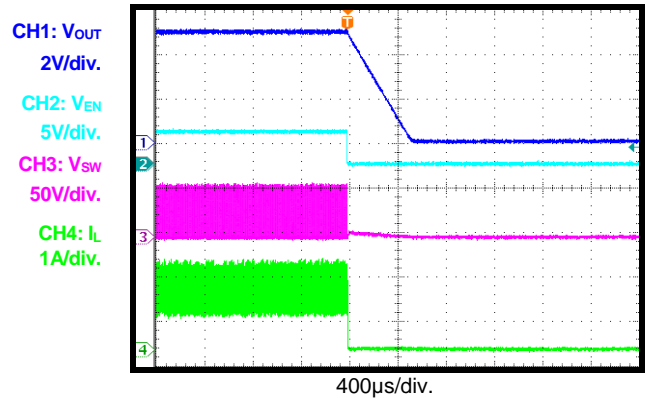
### EN Shutdown

$I_{OUT}=0A$



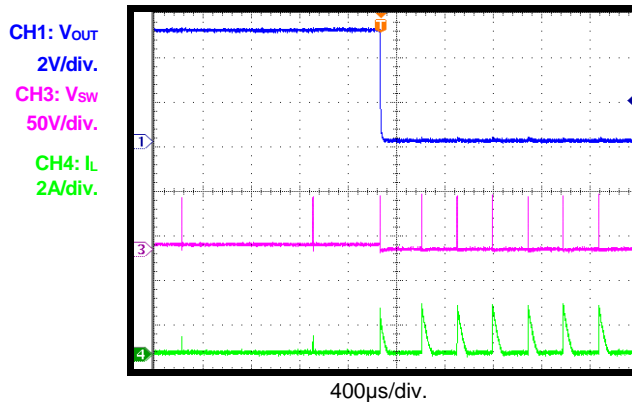
### EN Shutdown

$I_{OUT}=1A$



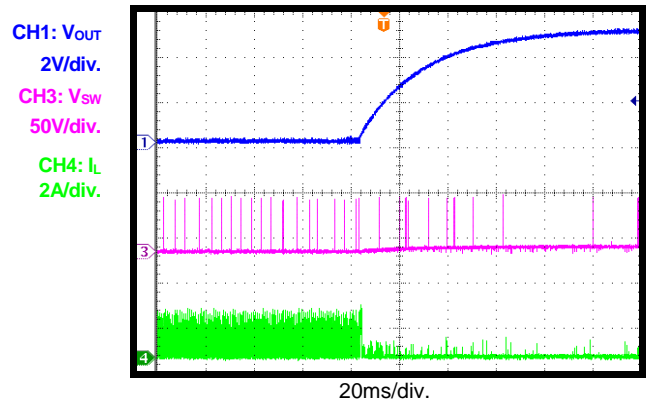
### SCP Entry

$I_{OUT}=0A$



### SCP Recovery

$I_{OUT}=0A$



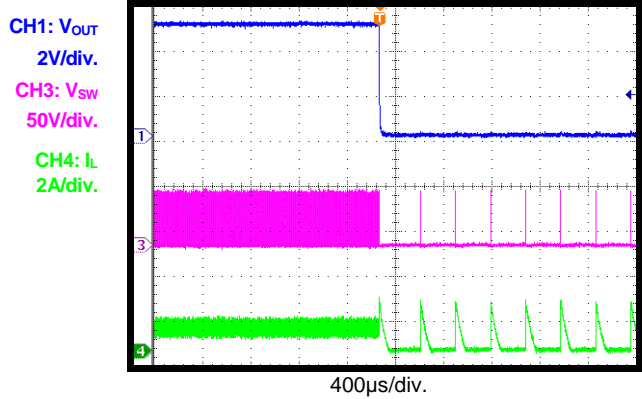
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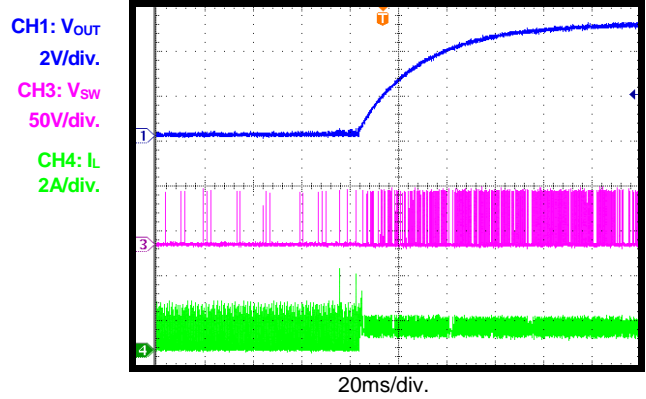
### SCP Entry

$I_{OUT}=1A$



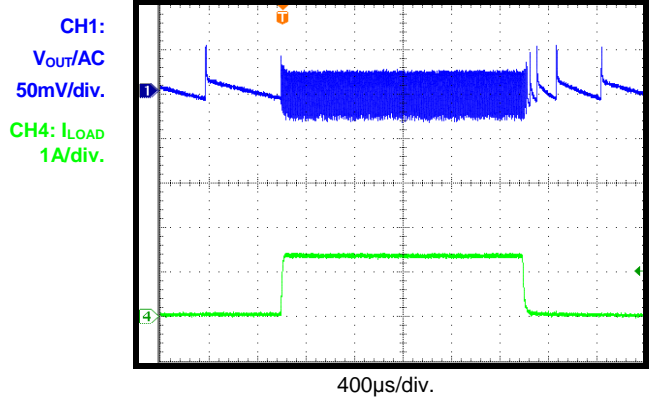
### SCP Recovery

$I_{OUT}=1A$ , E-load turn-on Threshold=0.32V



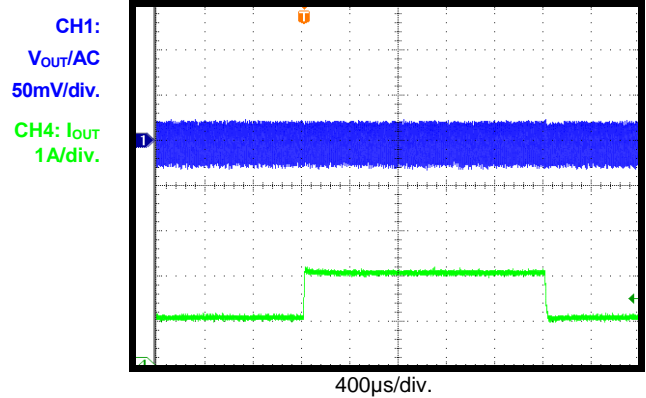
### Load Transient

$I_{OUT}=0A \rightarrow 1A @ 70mA/\mu s$



### Load Transient

$I_{OUT}=1A \rightarrow 2A @ 70mA/\mu s$



## PRINTED CIRCUIT BOARD LAYOUT

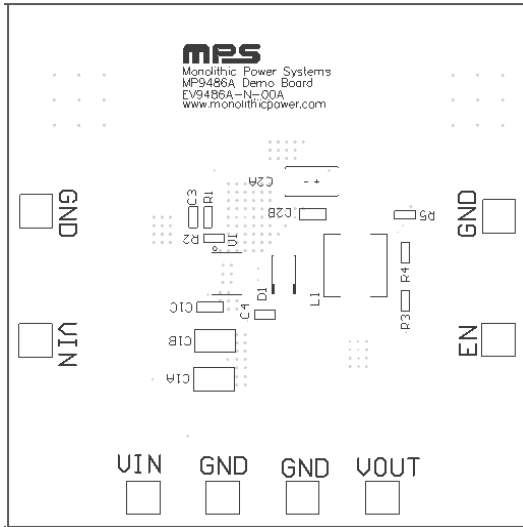


Figure 1: Top Silkscreen Layer

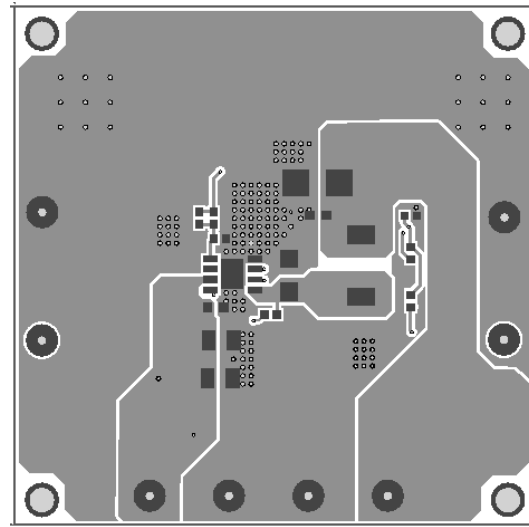


Figure 2: Top Layer

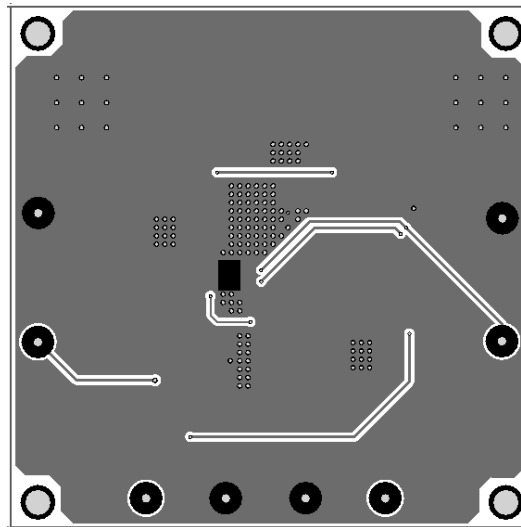


Figure 3: Bottom Layer