EVAL-5CH6CHSOICEBZ User Guide
UG-936

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Using the EVAL-5CH6CHSOICEBZ *i*Coupler Standard Data Isolator Evaluation Board

FEATURES

- Access to all data channels
- Multiple connection options
- Support for active probes
- Provisions for cable terminations
- Support for printed circuit board (PCB) edge mounted coaxial connectors
- Easy configuration

SUPPORTED *i*Coupler DEVICES

Sample *i*Coupler digital isolators must be ordered separately; supported *i*Coupler devices are as follows:

ADuM150N/ADuM151N/ADuM152N
ADuM160N/ADuM161N/ADuM162N/ADuM163N
ADuM250N/ADuM251N/ADuM252N
ADuM260N/ADuM261N/ADuM262N/ADuM263N

PHOTOGRAPH OF THE EVALUATION BOARD

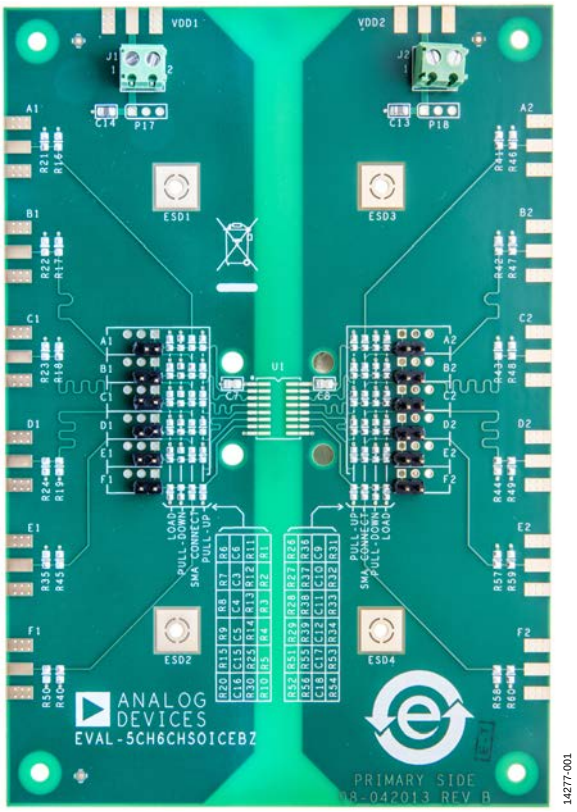

Figure 1.

GENERAL DESCRIPTION

The EVAL-5CH6CHSOICEBZ supports 5-channel and 6-channel *i*Coupler® standard data isolators in a 16-lead SOIC package. The evaluation board provides a JEDEC standard, 16-lead SOIC_N and SOIC_W pad layout. This layout supports signal distribution, loopback, and loads referenced to the VDDx or GNDx planes, as well as optimal bypass capacitance. Signal sources can be conducted to the evaluation board through header pins or through edge mounted SMA connectors (SMA connectors must be ordered separately). Screw terminal blocks on the evaluation board provide power connections.

The evaluation board includes 0.2 inch header positions for compatibility with active probes (probe header pins must be ordered separately).

The evaluation board follows best PCB design practices for 4-layer boards, including a full power plane and ground plane on each side of the isolation barrier. No other electromagnetic interference (EMI) or noise mitigation design features are included on the evaluation board. In cases of high speed operation, or when ultralow emissions are required, refer to the AN-1109 Application Note for additional evaluation board layout techniques.

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REVISION HISTORY

10/2016—Rev. 0 to Rev. A

Added ADuM250N/ADuM251N/ADuM252N and ADuM260N/ADuM261N/ADuM262N/ADuM263N ..... Throughout
Change to General Description 1

9/2016—Rev. 0 to Rev. A

Changes to Features Section, Supported *i*Coupler Devices Section, and General Description Section 1
Changes to PCB Evaluation Goals Section 3

5/2016—Revision 0: Initial Version

EVALUATION BOARD CIRCUITRY

PCB EVALUATION GOALS

The EVAL-5CH6CHSOICEBZ achieves the following goals:

- Evaluates the full range of *i*Coupler data transfer functions.
- Independently powers each side of an *i*Coupler isolator.
- Allows high differential voltage to be applied between the two sides of an *i*Coupler isolator. The evaluation board is intended for evaluation of the components, but is not safety certified for high voltage operation. If applying differential voltages above 60 V, external safety measures appropriate for the voltage must be in place.
- Allows easy connection to power supplies, data channels, and instrumentation.

The evaluation board comes installed with power terminals, bypass capacitors, and header pins. The EVAL-ADuM163N0EBZ is available with the ADuM163N0 device, which is installed on the EVAL-5CH6CHSOICEBZ evaluation board. All other compatible *i*Coupler digital isolators must be ordered and installed separately on the EVAL-5CH6CHSOICEBZ evaluation board.

The board is compatible with 5-channel and 6-channel devices, such as the ADuM150N/ADuM151N/ADuM152N, the ADuM160N/ADuM161N/ADuM162N/ADuM163N, the ADuM250N/ADuM251N/ADuM252N, and the ADuM260N/ADuM261N/ADuM262N/ADuM263N.

CONNECTORS

The PCB provides support for three types of interconnections.

- SMA edge mounted connectors
- Through-hole signal ground pairs
- Terminal blocks for power connections

With these three options, temporary and permanent connections to the evaluation board can be made.

When coaxial connections are required, SMA connector positions are available for digital input/output signals and the VDD1/VDD2 power supplies. The SMA connector positions are unpopulated as shipped and must be ordered from a distributor separately. Figure 2 shows examples of installed SMA connectors; these connectors are not only low profile and provide excellent mechanical connections to the PCB, but also support 50 Ω coaxial cabling.

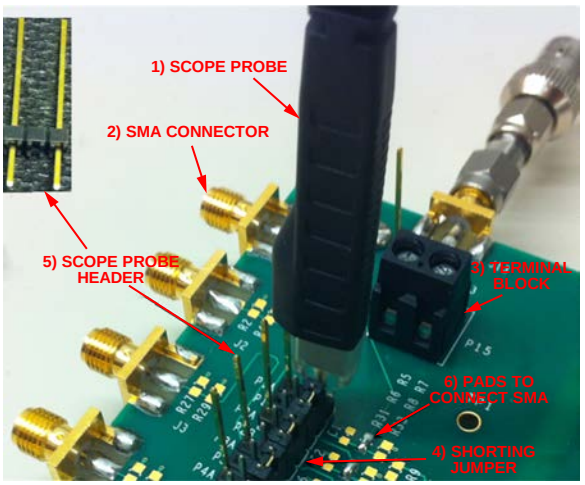

Figure 2. Optional Components

Power can be connected through the J1 and J2 screw terminals or through the optional VDD1 and VDD2 SMA connectors. Signals can be routed in or out with the provided header pins or the optional SMA connectors. The pin spacing of each through-hole connector is 0.1 inch between the centers. There are additional signal test points with 0.2 inch spacing provided for active scope probes. These header pins must be added separately. The installed probe points are shown in Figure 2.

INPUT POWER

Each side of an *i*Coupler standard data isolator requires an off-board power source. On the silkscreen, the J1 and J2 screw terminals are marked 1 for VDDx and 2 for GNDx.

Divided power and ground planes are present on Layer 2 and Layer 3 of the PCB on each side of the isolation barrier. This configuration is shown in Figure 6 and Figure 7, respectively.

DATA INPUT/OUTPUT (I/O) STRUCTURES

Each data channel has a variety of structures to help configure, load, and monitor both the input and output. Figure 3 shows an example of the routing from an external connection to the pin of the device under test (DUT). Each data channel has similar connections.

Starting at the external connection, the signal path is constructed in the following order (see Figure 3 for the locations of these components):

1. A pad layout for a PCB board edge mounted SMA connector.
2. Two 0805 pads are provided where 100 Ω resistors to ground can be installed. The combined resistance is 50 Ω to provide a termination for a standard coaxial cable.
3. A standard 0805 pad layout that allows the coaxial and termination structures to be connected to the rest of the signal path.
4. A 0603 pad layout between the signal path and VDDx for a pull-up resistor, if required.

5. A populated 2-pin header to provide a signal ground pair for use with clip leads or for temporarily shorting a channel to ground.
6. Groupings of three open through holes consisting of a signal and two ground connections. These holes can hardwire signal wires into the PCB, install a header to accept an active probe, or install a 2-pin header to allow adjacent channels to temporarily be shorted together.
7. A 0805 pad layout between the signal and GNDx where a load capacitor or pull-down resistor can be installed.

Figure 2 shows many of the optional components installed, as well as how the jumpers can temporarily connect channels. Figure 2 also shows a signal connected to the first channel SMA, which is then fanned out to the top three channels and monitored by an active scope probe.

BYPASS CAPACITANCE ON THE PCB

Several positions and structures are provided to allow optimal bypass capacitance for the DUT on the evaluation board. Provisions are made for optional surface-mount bulk capacitors to be installed near the power connectors to compensate for long cables to the power supply. Bypass capacitors are installed near the *i*Coupler data isolator and consist of a 0.1 µF capacitor for each DUT VDDx pin on the top side of the evaluation board.

The PCB also implements a distributed capacitive bypass. This bypass consists of power and ground planes closely spaced on the inner layers of the PCB, which reduces noise and the transmission of EMI without using complex design features.

HIGH VOLTAGE CAPABILITY

This PCB is designed in adherence with 2500 V basic insulation practices. High voltage testing beyond 2500 V is not recommended. Do not rely on the evaluation board for safety functions.

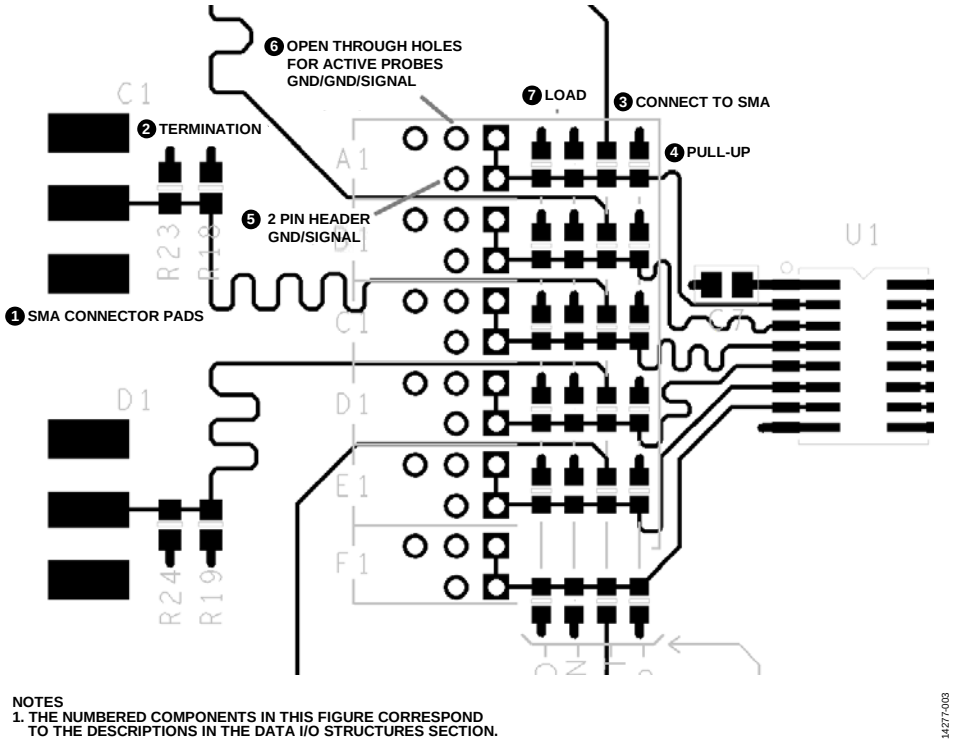

Figure 3. Configuration and Monitoring Structures

EVALUATION BOARD SCHEMATICS AND ARTWORK

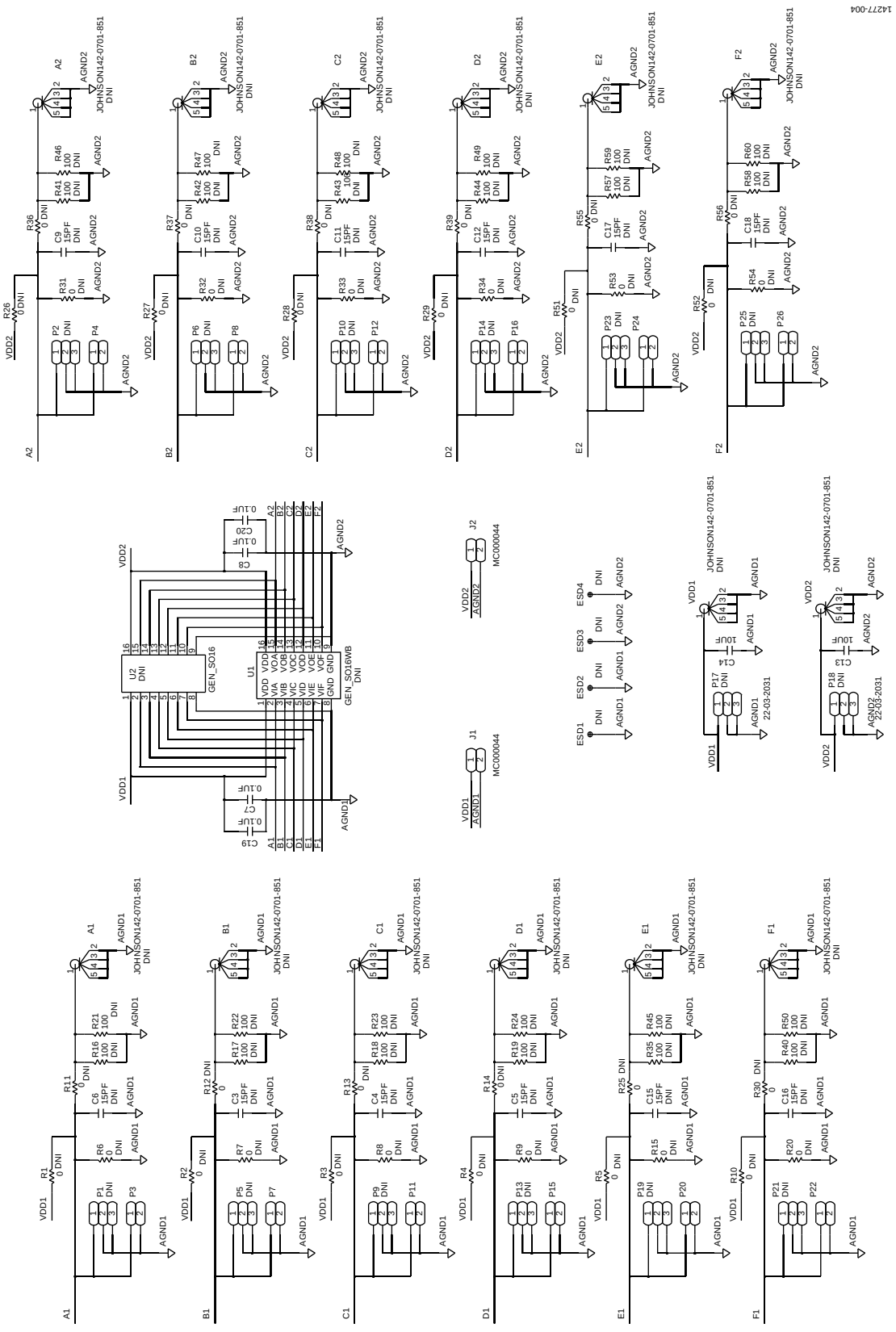

Figure 4. EVAL-5CH6CHSOICEBZ Schematic

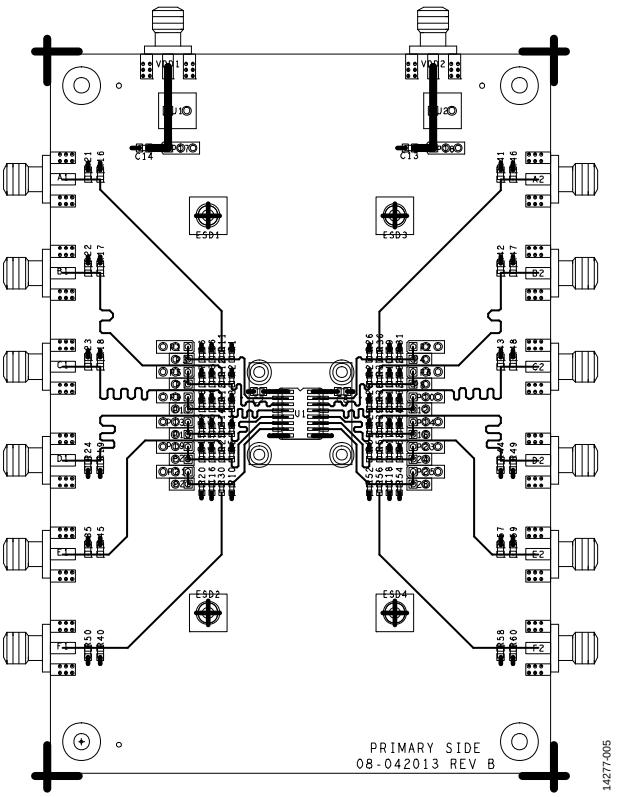

Figure 5. Top Level Signal Routing and Assembly (Layer 1)

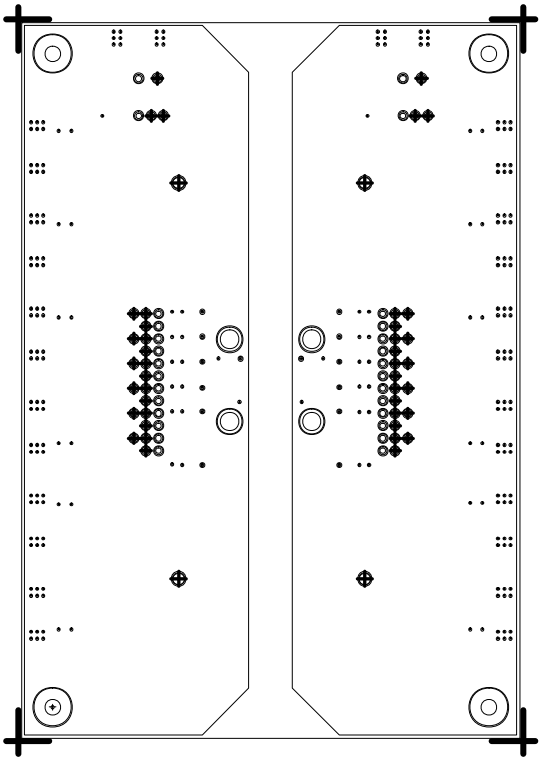

Figure 6. GND1 and GND2 Planes (Layer 2)

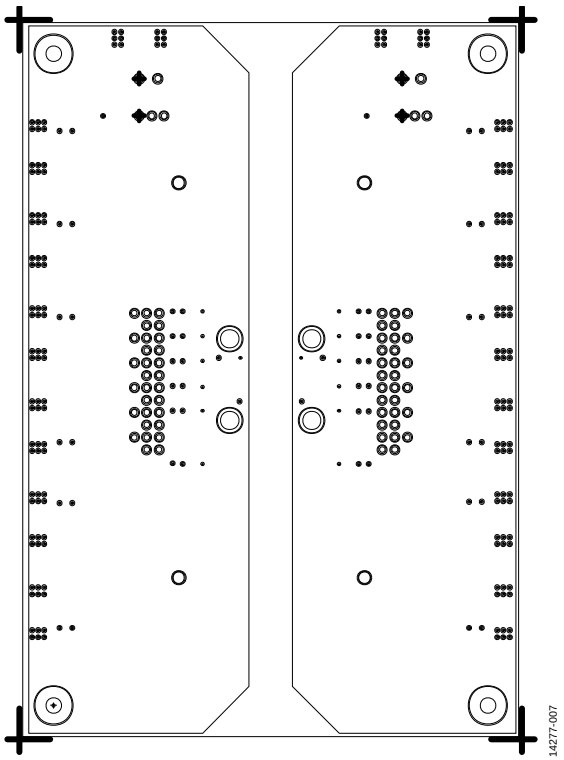

Figure 7. VDD1 and VDD2 Power Plane (Layer 3)

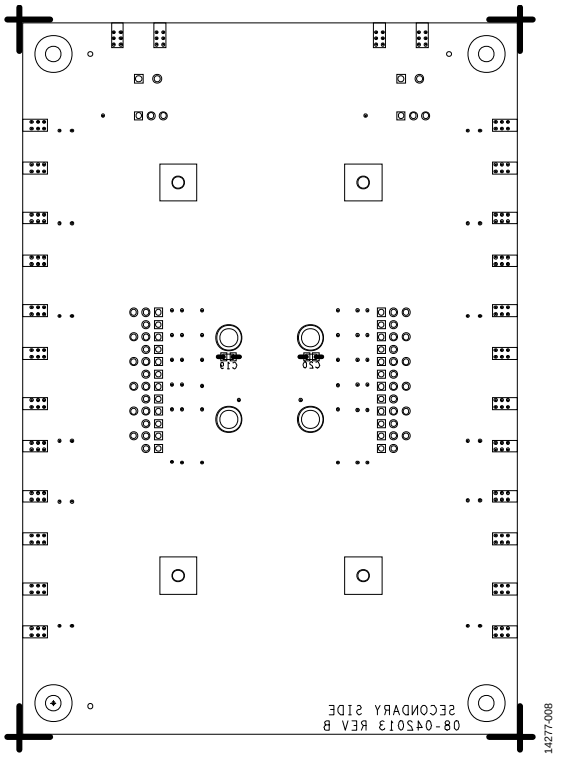

Figure 8. Bottom Layer Assembly and Routing (Layer4)