10-Bit *nano*DAC with SPI/I²C Interface and 2 ppm/°C On-Chip Reference

Data Sheet

AD5310R/AD5311R

FEATURES

- High relative accuracy (INL): ±0.5 LSB maximum
- Low drift 2.5 V reference: 2 ppm/°C typical
- Selectable span output: 2.5 V or 5 V
- Total unadjusted error (TUE): 0.06% of FSR maximum
  - Offset error: ±1.5 mV maximum
  - Gain error: ±0.05% of FSR maximum
- Low glitch: 0.1 nV-sec
- High drive capability: 20 mA
- Low power: 1.2 mW at 3.3 V
- Independent logic supply: 1.8 V logic compatible
- Wide operating temperature range: −40°C to +105°C
- Robust 4 kV HBM ESD protection

APPLICATIONS

- Process controls
- Data acquisition systems
- Digital gain and offset adjustment
- Programmable voltage sources
- Optical modules

GENERAL DESCRIPTION

The AD5310R/AD5311R, members of the *nano*DAC® family, are low power, single-channel, 10-bit buffered voltage output DACs. The devices include an enabled by default internal 2.5 V reference, and provides 2 ppm/°C. The output span can be programmed to be 0 V to V_{REF} or 0 V to 2 × V_{REF}. All devices operate from a single 2.7 V to 5.5 V supply and are guaranteed monotonic by design. The devices are available in 10-lead MSOP packages.

The internal power-on reset circuit of the AD5310R/AD5311R ensures that the DAC register is written to zero scale at powerup when the internal output buffer is configured in normal mode. The devices contain a power-down mode that reduces the current consumption of the device to 2 µA at 5 V.

The AD5310R/AD5311R use a versatile SPI or I²C interface, including an asynchronous $\overline{\text{RESET}}$ pin and a V_{LOGIC} pin that provides 1.8 V compatibility.

FUNCTIONAL BLOCK DIAGRAMS

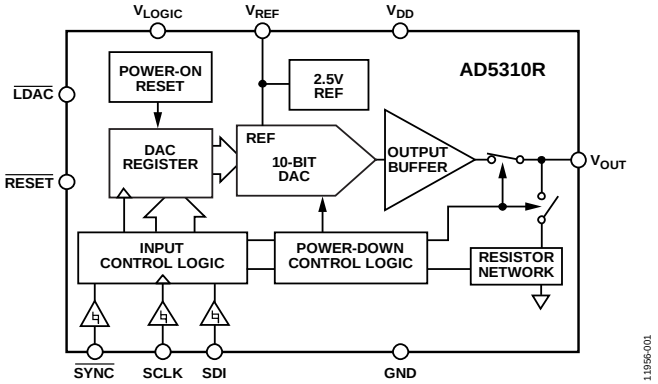

Figure 1. AD5310R

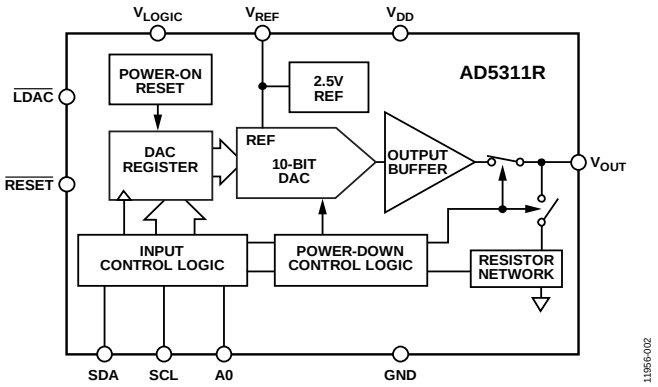

Figure 2. AD5311R

Table 1. Related Devices

Interface	Reference	12-Bit	10-Bit
SPI	External	AD5681R	AD5310[1]
I²C	External		AD5311[1]

[1] The AD5310R and AD5311R are not pin-to-pin or software compatible with the AD5310 and AD5311, respectively.

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL): ±0.5 LSB maximum.
2. Low Drift 2.5 V On-Chip Reference: 5 ppm/°C maximum temperature coefficient.

Rev. B

Document Feedback

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1/2014—Rev. 0 to Rev. A

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Removed Solder Heat Reflow Section and Figure 44; Renumbered Sequentially ... 23

1/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REF} ≤ V_{DD}, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[1]					
Resolution	10			Bits	
Relative Accuracy, INL			±0.5	LSB	
Differential Nonlinearity, DNL			±0.5	LSB	
Zero-Code Error			1.25	mV	All 0s loaded to DAC register
Offset Error			±1.5	mV	
Full-Scale Error			±0.075	% of FSR	All 1s loaded to DAC register
Gain Error			±0.05	% of FSR	
Total Unadjusted Error, TUE			±0.16	% of FSR	Internal reference, gain = 1
			±0.14	% of FSR	Internal reference, gain = 2
			±0.075	% of FSR	External reference, gain = 1
			±0.06	% of FSR	External reference, gain = 2
Zero-Code Error Drift		±1		µV/°C	
Offset Error Drift		±1		µV/°C	
Gain Temperature Coefficient		±1		ppm/°C	
DC Power Supply Rejection Ratio, PSRR		0.2		mV/V	DAC code = midscale, V_{DD} = 5 V ± 10%
OUTPUT CHARACTERISTICS					
Output Voltage Range	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	V	Gain = 2
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 2 kΩ
Resistive Load	1			kΩ	C_L = 0 µF
Load Regulation		10		µV/mA	V_{DD} = 5 V, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ 30 mA
		10		µV/mA	V_{DD} = 3 V, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ 20 mA
Short-Circuit Current	20		50	mA	
Load Impedance at Rails[2]		20		Ω	
REFERENCE OUTPUT					
Output Voltage	2.4975		2.5025	V	At ambient temperature
Voltage Reference TC[3]		2	5	ppm/°C	See the Terminology section
Output Impedance		0.05		Ω	
Output Voltage Noise		16.5		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	At ambient temperature; f = 10 kHz, C_L = 10 nF
Capacitive Load Stability		5		µF	R_L = 2 kΩ
Load Regulation, Sourcing		50		µV/mA	At ambient temperature; V_{DD} ≥ 3 V
Load Regulation, Sinking		30		µV/mA	At ambient temperature
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
Line Regulation		80		µV/V	At ambient temperature
Thermal Hysteresis		125		ppm	First cycle
		25		ppm	Additional cycles

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input Current, I_{IN}			±1	µA	Per pin
			±4	µA	SDA and SCL pins (AD5311R)
Input Low Voltage, V_{INL}			0.3 × V_{LOGIC}	V	
Input High Voltage, V_{INH}	0.7 × V_{LOGIC}			V	
Pin Capacitance, C_{IN}		2		pF	
LOGIC OUTPUT (SDA)					AD5311R
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{LOGIC} − 0.4			V	I_{SOURCE} = 200 µA
Pin Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.62		5.5	V	
I_{LOGIC}		0.25	3	µA	V_{IH} = V_{LOGIC} or V_{IL} = GND
V_{DD}	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}					V_{IH} = V_{DD}, V_{IL} = GND
Normal Mode[4]		350	500	µA	Internal reference enabled
		110	180	µA	Internal reference disabled
Power-Down Modes[5]			2	µA	

[1] Linearity is calculated using a reduced code range: Code 8 to Code 1024, output unloaded.
[2] When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 20 Ω typical channel resistance of the output devices; for example, when sinking 1 mA, the minimum output voltage with 20 Ω, 1 mA generates 20 mV. See Figure 29.
[3] Reference temperature coefficient calculated as per the box method. See the Terminology section for more information.
[4] Interface inactive. DAC active. Code = zero-scale, DAC output unloaded.
[5] DAC powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 2.5 V ≤ V_{REF} ≤ V_{DD}, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.[1]

Table 3.

Parameter[2]	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time	5	7	µs	Gain = 1, ¼ to ¾ scale settling to ±0.25 LSB
Slew Rate	0.7		V/µs	
Digital-to-Analog Glitch Impulse	0.1		nV-sec	±1 LSB change around major carry, gain = 1
Digital Feedthrough	0.1		nV-sec	
Total Harmonic Distortion (THD)	−83		dB	V_{REF} = 2 V ± 0.1 V p-p, f = 10 kHz
Output Noise Spectral Density	200		nV/√Hz	DAC code = midscale, f = 10 kHz
Output Noise	6		µV p-p	0.1 Hz to 10 Hz; internal reference
Signal-to-Noise Ratio (SNR)	90		dB	At ambient temperature, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Spurious-Free Dynamic Range (SFDR)	88		dB	At ambient temperature, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Signal-to-Noise-and Distortion (SINAD) Ratio	82		dB	At ambient temperature, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] Temperature range = −40°C to +105°C, typical at 25°C.
[2] See the Terminology section.

TIMING CHARACTERISTICS

AD5310R

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 4.

Parameter [1]	Symbol	1.8 V ≤ V_{LOGIC} ≤ 2.7 V			2.7 V ≤ V_{LOGIC} [2] ≤ 5.5 V			Unit
		Min	Typ	Max	Min	Typ	Max	
SCLK Cycle Time	t_1	33			20			ns
SCLK High Time	t_2	16			10			ns
SCLK Low Time	t_3	16			10			ns
$\overline{SYNC}$ to SCLK Falling Edge Setup Time	t_4	15			10			ns
Data Setup Time	t_5	5			5			ns
Data Hold Time	t_6	5			5			ns
SCLK Falling Edge to $\overline{SYNC}$ Rising Edge	t_7	15			10			ns
Minimum $\overline{SYNC}$ High Time	t_8	20			20			ns
$\overline{SYNC}$ Falling Edge to SCLK Fall Ignore	t_9	16			10			ns
$\overline{SYNC}$ Rising Edge to SCLK Falling Edge	t_{10}							ns
$\overline{SYNC}$ Rising Edge to $\overline{LDAC}$ Falling Edge	t_{11}	25			25			ns
$\overline{LDAC}$ Pulse Width Low	t_{12}	20			15			ns
$\overline{RESET}$ Minimum Pulse Width Low	t_{13}	75			75			ns
$\overline{RESET}$ Pulse Activation Time	t_{14}	150			150			ns
$\overline{SYNC}$ Rising Edge to $\overline{SYNC}$ Rising Edge (DAC Updates)	t_{15}	1.9			1.7			µs
$\overline{LDAC}$ Falling Edge to $\overline{SYNC}$ Rising Edge	t_{16}	1.8			1.65			µs
Reference Power-Up[3]	$t_{REF\_POWER\_UP}$[4]		600			600		µs
Exit Shutdown[3]	$t_{SHUTDOWN}$[5]			6			6	µs

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Substitute V_{DD} for V_{LOGIC} on devices that do not include a V_{LOGIC} pin.
[3] Not shown in Figure 3.
[4] Same timing must be expected when powering up the device after V_{DD} = 2.7 V.
[5] Time required to exit power-down to normal mode of AD5310R/AD5311R operation; $\overline{SYNC}$ rising edge to 90% of DAC midscale value, with output unloaded.

Timing and Circuit Diagrams

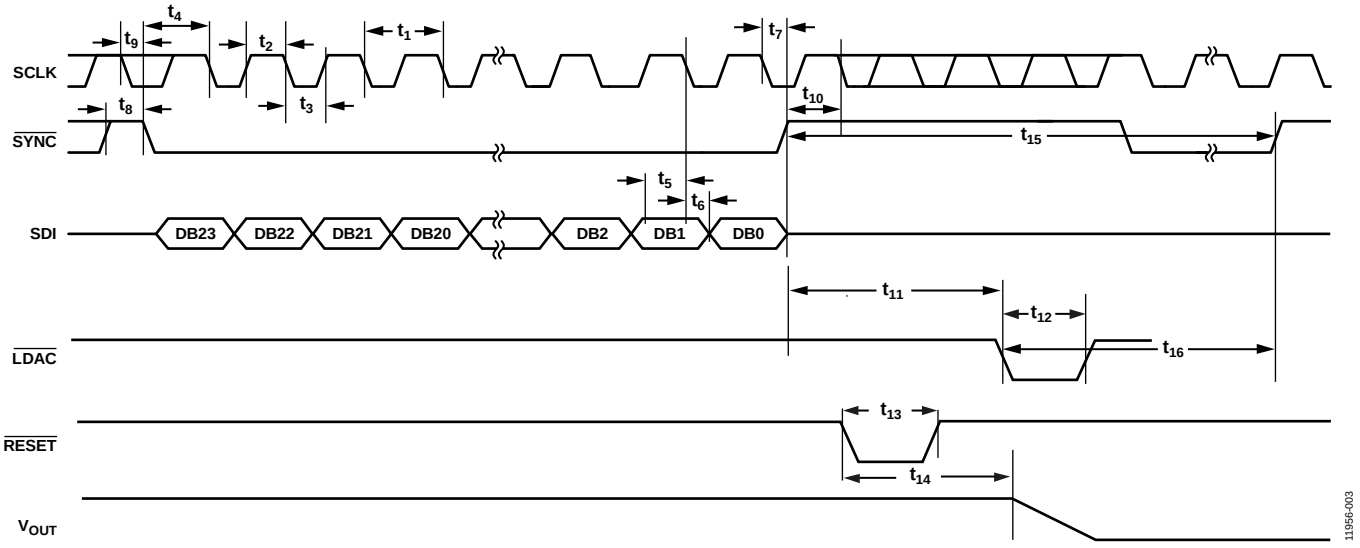

Figure 3. SPI Timing Diagram, Compatible with Mode 1 and Mode 2 (See the AN-1248 Application Note)

AD5311R

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, −40°C < T_A < +105°C, unless otherwise noted.

Table 5.

Parameter[1]	Symbol	Min	Typ	Max	Unit
Serial Clock Frequency (Not Shown in Figure 4 or Figure 5)	f_{SCL}[2]			400	kHz
SCL High Time, t_{HIGH}	t_1	0.6			µs
SCL Low Time, t_{LOW}	t_2	1.3			µs
Data Setup Time, $t_{SU;DAT}$	t_3	100			ns
Data Hold Time, $t_{HD;DAT}$	t_4	0		0.9	µs
Setup Time for a Repeated Start Condition, $t_{SU;STA}$	t_5	0.6			µs
Hold Time (Repeated) Start Condition, $t_{HD;STA}$	t_6	0.6			µs
Bus Free Time Between a Stop and a Start Condition, t_{BUF}	t_7	1.3			µs
Setup Time for a Stop Condition, $t_{SU;STO}$	t_8	0.6			µs
Rise Time of SDA Signal, t_R	t_9	20		300	ns
Fall Time of SDA Signal, t_F	t_{10}	20 × (V_{DD}/5.5 V)		300	ns
Rise Time of SCL Signal, t_R	t_{11}	20		300	ns
Fall Time of SCL Signal, t_F	t_{12}	20 × (V_{DD}/5.5 V)		300	ns
Pulse Width of Suppressed Spike (Not Shown in Figure 4 Figure 5)	t_{SP}	0		50	ns
$\overline{\text{LDAC}}$ Falling Edge to SCL Falling Edge	t_{13}	400			ns
$\overline{\text{LDAC}}$ Pulse Width (Synchronous Mode)	t_{14}	400			ns
$\overline{\text{LDAC}}$ Pulse Width (Asynchronous Mode)	t_{15}	20			ns
$\overline{\text{RESET}}$ Pulse Width	t_{16}	75			ns
Reference Power-Up (Not Shown in Figure 4 or Figure 5)	$t_{REF\_POWER\_UP}$[3]		600		µs
Exit Shutdown (Not Shown in Figure 4 or Figure 5)	$t_{SHUTDOWN}$[4]			6	µs

[1] Maximum bus capacitance is limited to 400 pF. All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate; however, it has a negative effect on the EMC behavior of the device.
[3] Same timing should be expected when powering the device after V_{DD} = 2.7 V.
[4] Time to exit power-down to normal mode of operation.

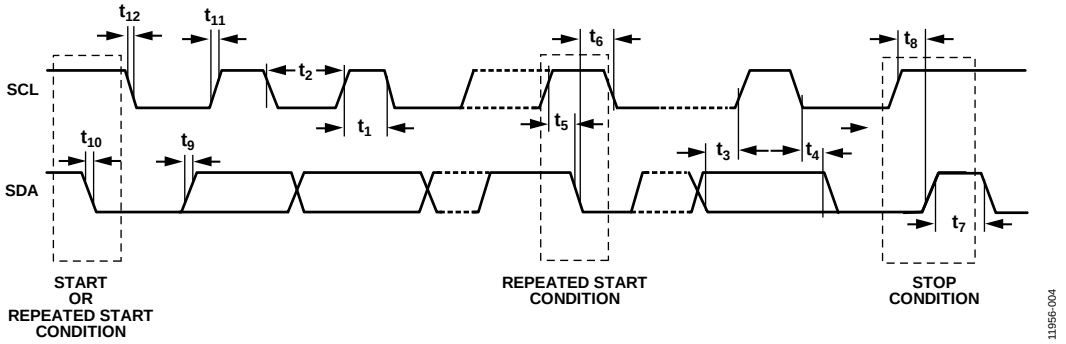

Figure 4. I²C Serial Interface Timing Diagram

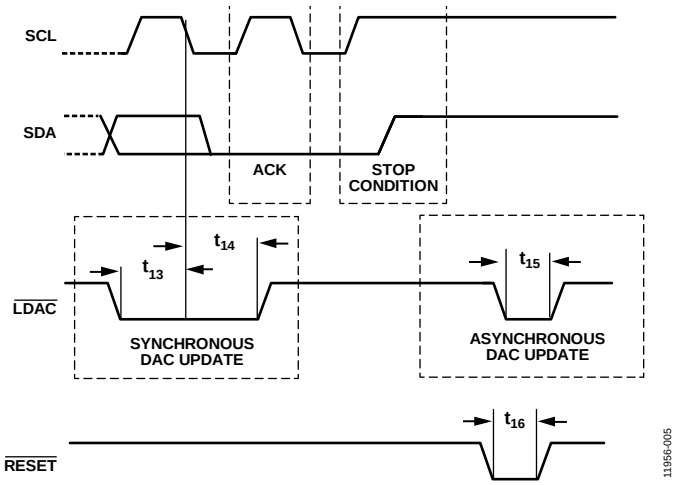

Figure 5. I²C, LDAC, and RESET Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V or +7 V (whichever is less)
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	135°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
ESD[1]	4 kV
FICDM[2]	1.25 kV

[1] Human body model (HBM) classification.
[2] Field-induced charged-device model classification.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is defined by the JEDEC JESD51 standard, and the value is dependent on the test board and test environment.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
10-Lead MSOP	135[1]	N/A[2]	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec airflow).
[2] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

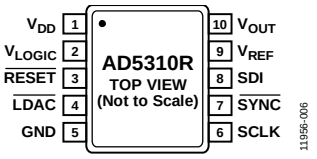

Figure 6. Pin Configuration, AD5310R

Table 8. AD5310R Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. This device can be operated from 2.7 V to 5.5 V. Decouple the supply to GND.
2	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V. Decouple the supply to GND.
3	$\overline{RESET}$	Hardware Reset Pin. The $\overline{RESET}$ input is low level sensitive. When $\overline{RESET}$ is low, the device is reset and external pins are ignored. The input and DAC registers are loaded with zero-scale values, and the control register is loaded with default values. This pin can be tied to V_{LOGIC} if not used.
4	$\overline{LDAC}$	Load DAC. $\overline{LDAC}$ can be operated in asynchronous mode (see Figure 3). Pulsing this pin low allows the DAC register to be updated if the input register has new data. This pin can be tied permanently low; in this case, the DAC register is automatically updated when new data is written to the input register.
5	GND	Ground Reference.
6	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data is transferred at rates up to 50 MHz.
7	$\overline{SYNC}$	Synchronization Data Input. When $\overline{SYNC}$ goes low, it enables the SCLK and SDI buffers and the input shift register.
8	SDI	Serial Data Input. Data is sampled on the falling edge of the SCLK.
9	V_{REF}	Reference Input/Output. By default, this pin is a reference output. It is recommended that this pin be decoupled with a 10 nF capacitor to GND.
10	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.

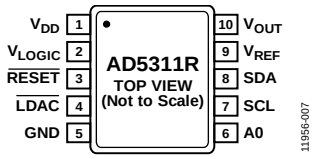

Figure 7. Pin Configuration, AD5311R

Table 9. AD5311R Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. These devices can be operated from 2.7 V to 5.5 V. Decouple the supply to GND.
2	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V. Decouple the supply to GND.
3	$\overline{RESET}$	Hardware Reset Pin. The $\overline{RESET}$ input is low level sensitive. When $\overline{RESET}$ is low, the device is reset and external pins are ignored. The input and DAC registers are loaded with zero-scale value, and the control register is loaded with default values. This pin can be tied to V_{LOGIC} if not used.
4	$\overline{LDAC}$	Load DAC. Transfers the contents of the input register to the DAC register. It can be operated in two modes, asynchronously and synchronously, as shown in Figure 5. This pin can be tied permanently low; the DAC updates when new data is written to the input register.
5	GND	Ground Reference.
6	A0	Programmable Address (ADDR1) for Multiple Package Decoding. The address pin can be updated on-the-fly.
7	SCL	Serial Clock Line.
8	SDA	Serial Data Input/Output.
9	V_{REF}	Reference Input/Output. The default for this pin is as a reference output. It is recommended to decouple this pin with a 10 nF capacitor to GND.
10	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.

TYPICAL PERFORMANCE CHARACTERISTICS

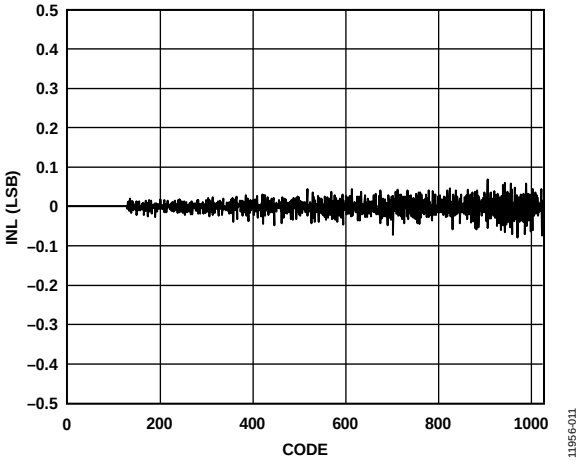

Figure 8. INL

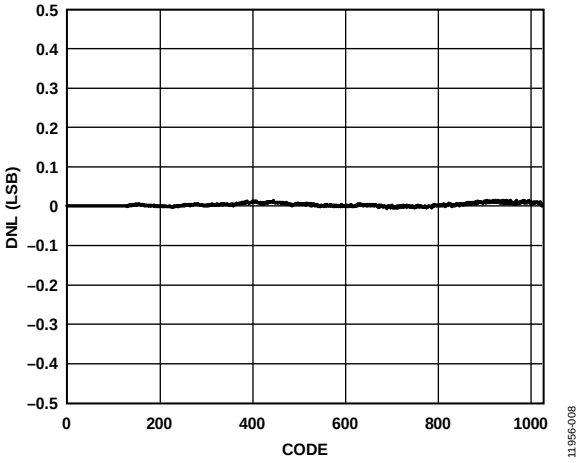

Figure 11. DNL

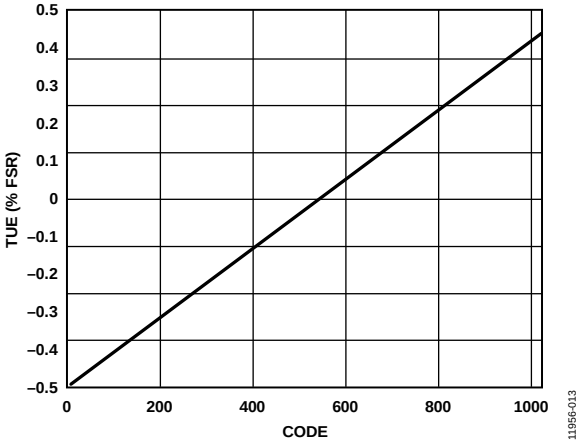

Figure 9. TUE vs. Code

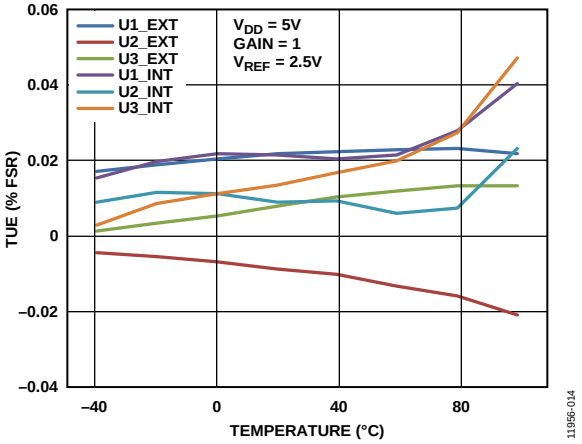

Figure 12. TUE vs. Temperature

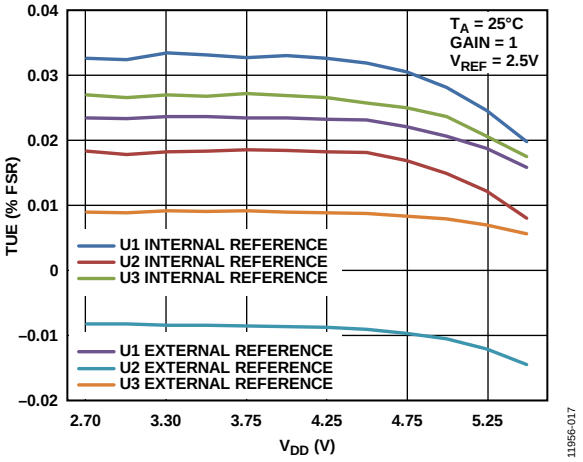

Figure 10. TUE vs. Supply, Gain = 1

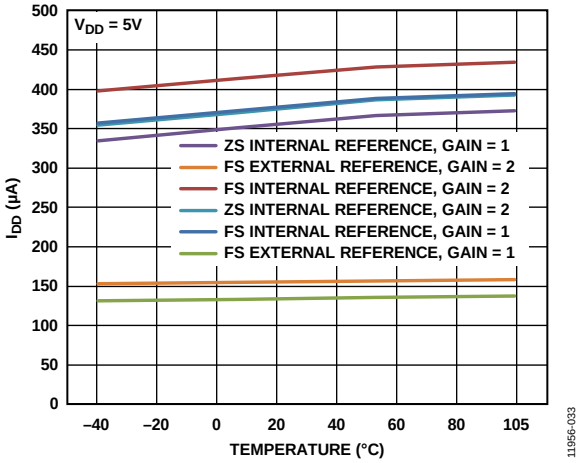

Figure 13. Supply Current vs. Temperature

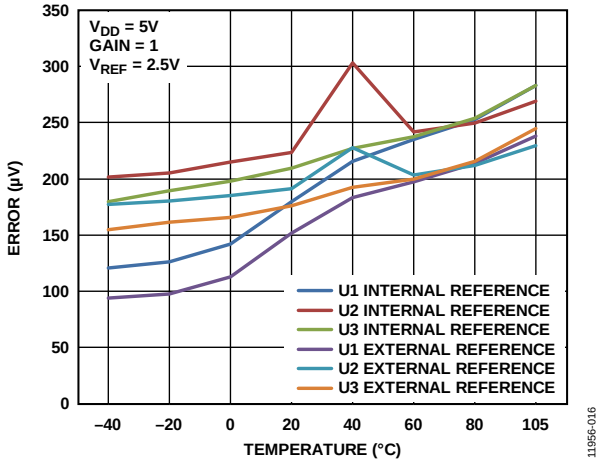

Figure 14. Zero-Code Error and Offset Error vs. Temperature

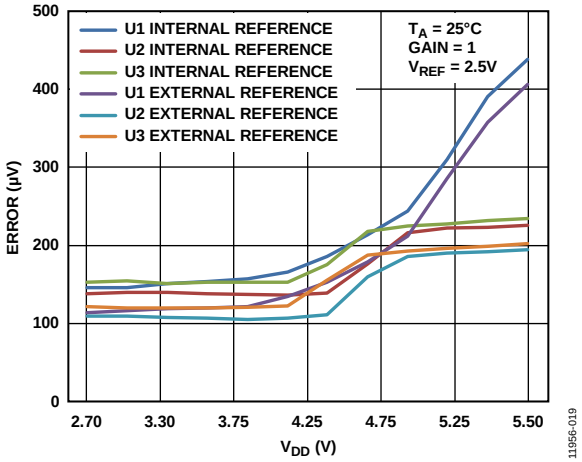

Figure 17. Zero-Code Error and Offset Error vs. Supply

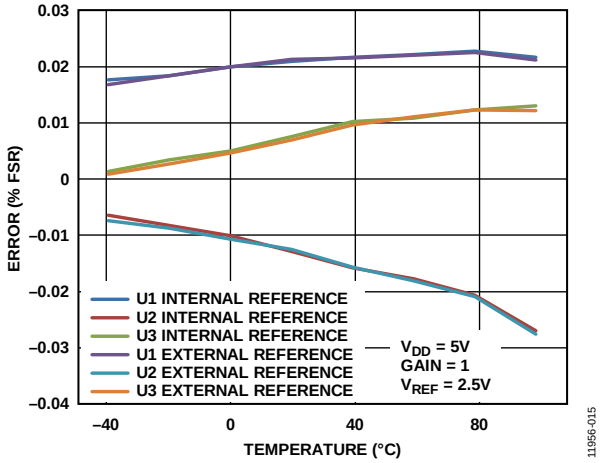

Figure 15. Gain Error and Full-Scale Error vs. Temperature

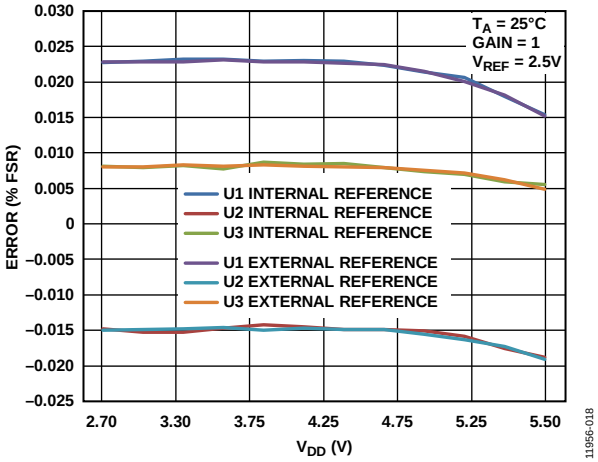

Figure 18. Gain Error and Full-Scale Error vs. Supply

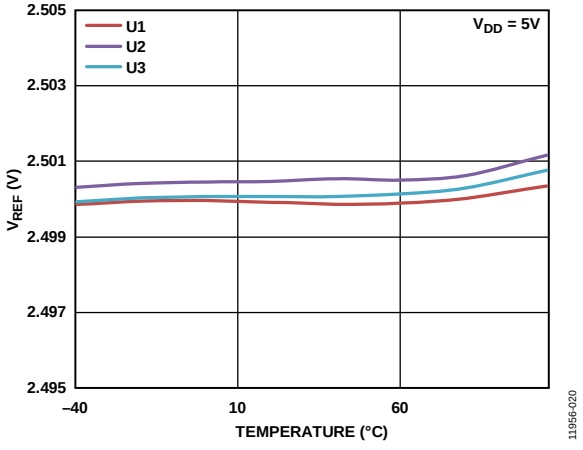

Figure 16. Internal Reference Voltage vs. Temperature

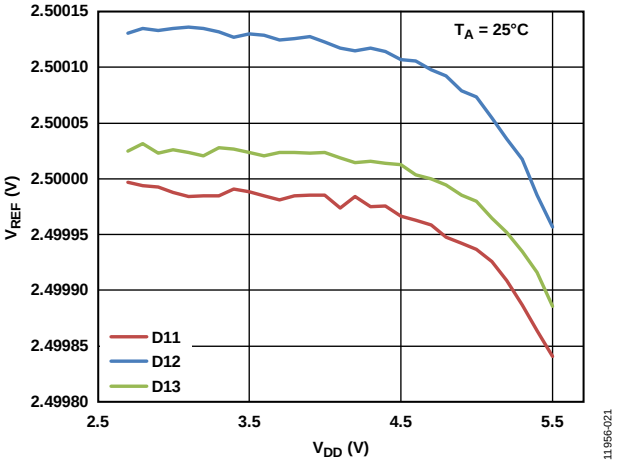

Figure 19. Internal Reference Voltage vs. Supply Voltage

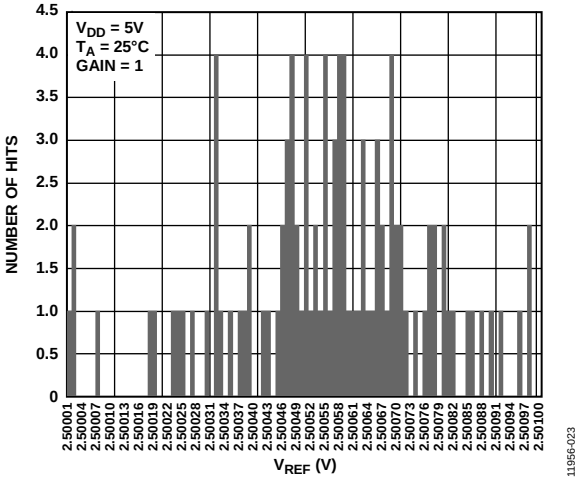

Figure 20. Reference Output Spread

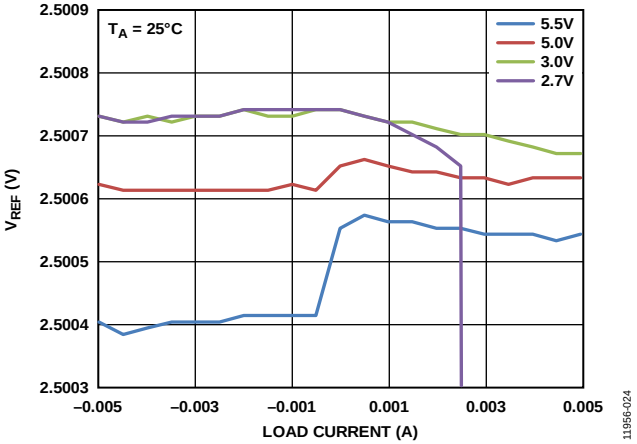

Figure 23. Internal Reference Voltage vs. Load Current

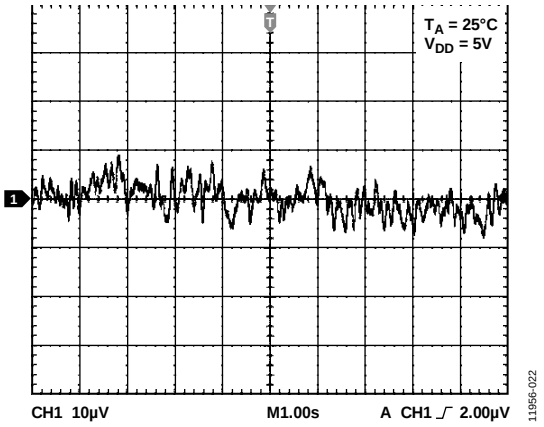

Figure 21. Internal Reference Noise, 0.1 Hz to 10 Hz

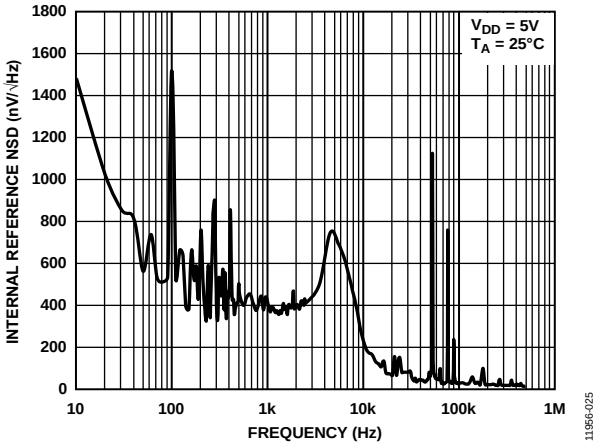

Figure 24. Internal Reference Noise Spectral Density vs. Frequency

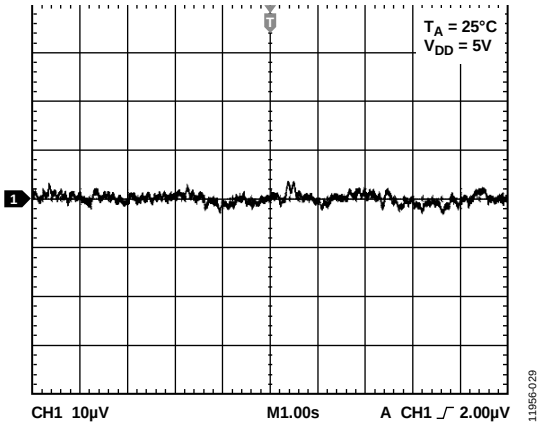

Figure 22. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

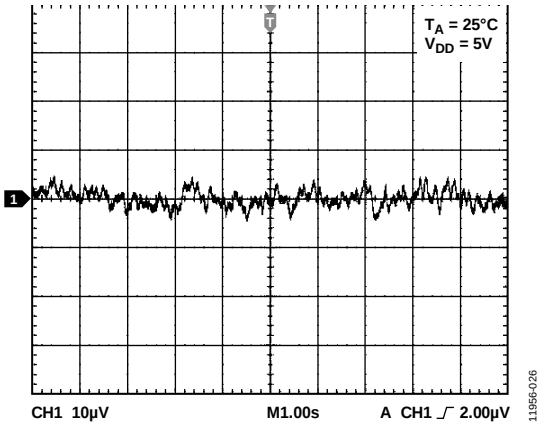

Figure 25. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

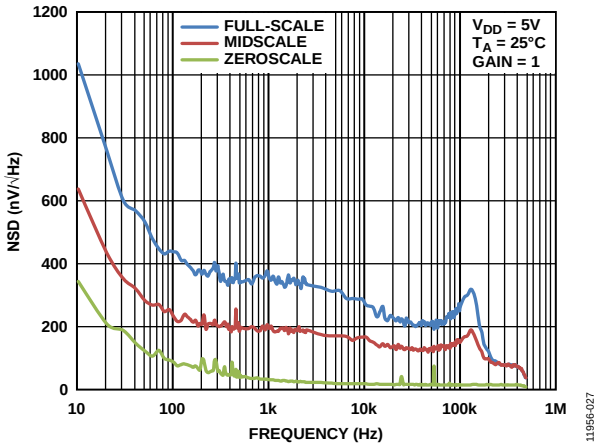

Figure 26. Noise Spectral Density, Gain = 1

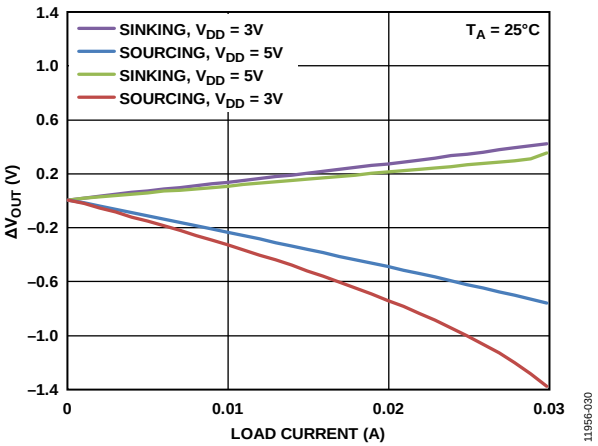

Figure 29. Headroom/Footroom vs. Load Current

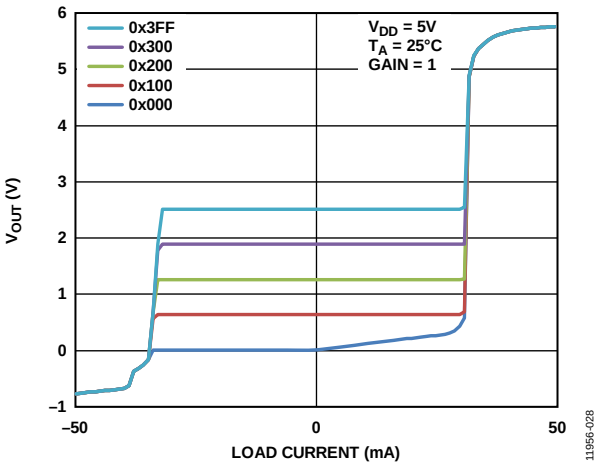

Figure 27. Source and Sink Capability, Gain = 1

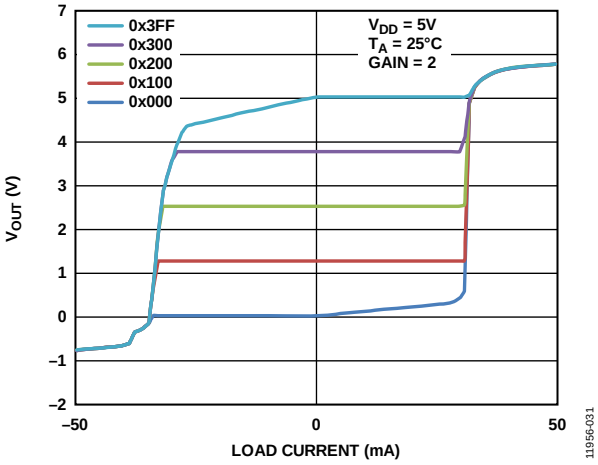

Figure 30. Source and Sink Capability, Gain = 2

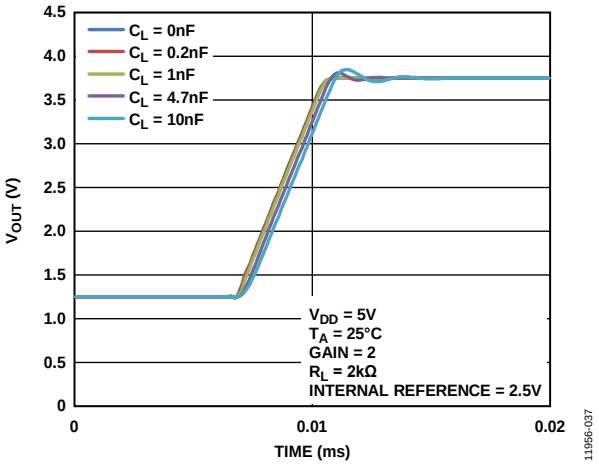

Figure 28. Settling Time vs. Capacitive Load, Gain = 2

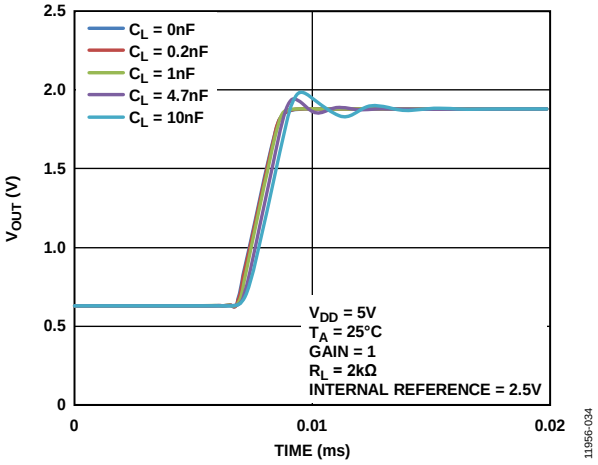

Figure 31. Settling Time vs. Capacitive Load, Gain = 1

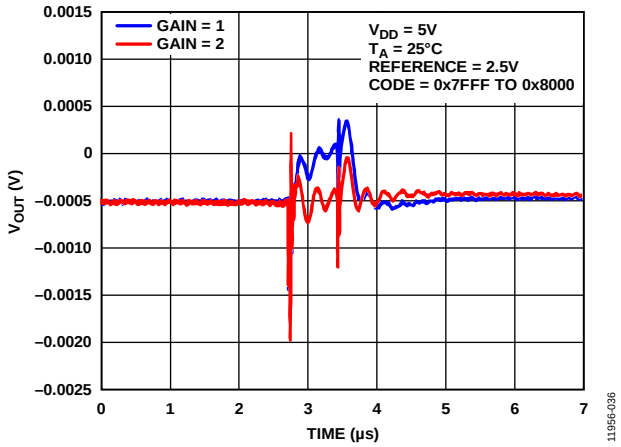

Figure 32. Digital-to-Analog Glitch Impulse

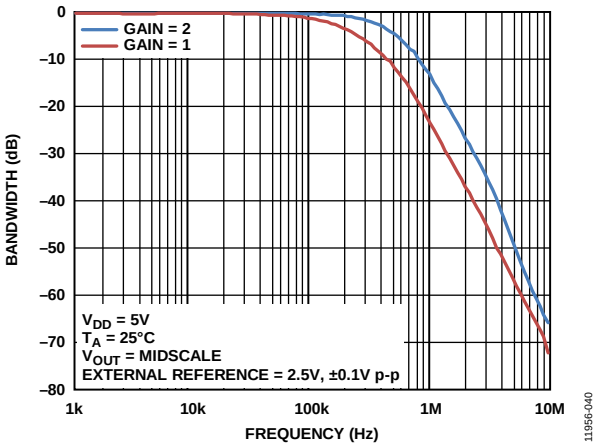

Figure 35. Multiplying Bandwidth, External Reference 2.5 V ± 0.1 V p-p, 10 kHz to 10 MHz

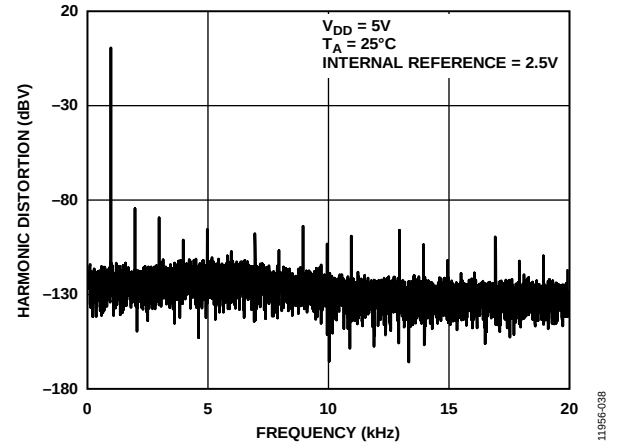

Figure 33. Total Harmonic Distortion at 1 kHz

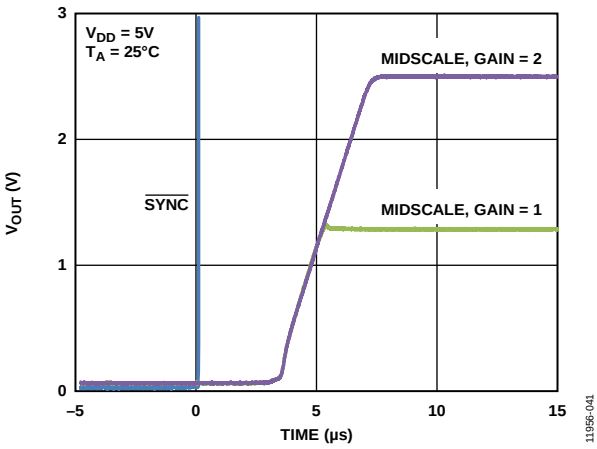

Figure 36. Exiting Power-Down to Midscale

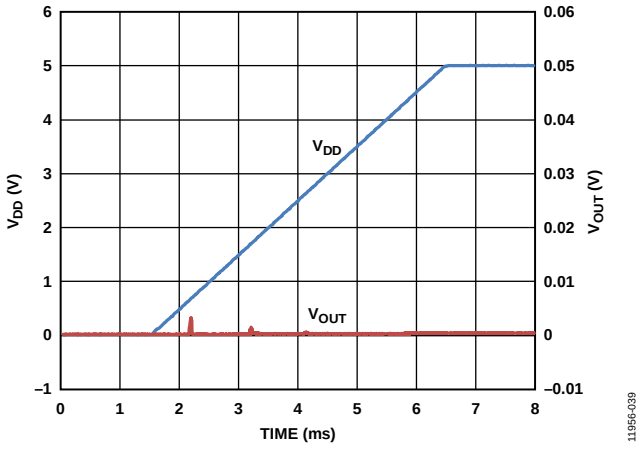

Figure 34. Power-On, Reset to 0 V

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy (or integral nonlinearity) is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. See Figure 8 for a typical INL vs. code plot.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. See Figure 11 for a typical DNL vs. code plot.

Zero Code Error
Zero code error is a measurement of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero code error of the input is always positive; the output of the DAC cannot fall below 0 V due to a combination of the offset errors in the DAC and in the output amplifier. Zero code error is expressed in mV. See Figure 14 and Figure 17 for plots of zero code error.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0x3FF) is loaded to the DAC register. The recommended output is V_{REF} – 1 LSB or $|2 \times V_{REF}|$ – 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR). See Figure 15 and Figure 18 for plots of full-scale error.

Gain Error
Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as % of FSR.

Zero-Code Error Drift
Zero-code error drift is a measurement of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured with Code 4 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V, and V_{DD} varies by ±10%.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at a major carry transition (0x1FF to 0x200).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. Digital feedthrough is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Output Noise Spectral Density
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. See Figure 22, Figure 25, and Figure 26 for plots of noise spectral density. See Figure 21 and Figure 24 for plots of the noise spectral density for the internal reference.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)
Voltage reference TC is a measurement of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:
V_{REFmax} is the maximum reference output measured over the total temperature range.
V_{REFmin} is the minimum reference output measured over the total temperature range.
V_{REFnom} is the nominal reference output voltage, 2.5 V.
TempRange is the specified temperature range, −40°C to +105°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5310R/AD5311R are single-channel, 10-bit, serial input, voltage output DACs with a 2.5 V internal reference. The devices operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5310R/AD5311R in a 24-bit word format via an I²C serial interface or SPI interface.

The AD5310R/AD5311R incorporate a power-on reset circuit that ensures that the DAC output powers up to a zero scale. The devices also have a software power-down mode that reduces the typical current consumption to 2 µA maximum in specs.

TRANSFER FUNCTION

The internal reference is on by default. The input coding to the DAC is straight binary, and the ideal output voltage is given by the following equations:

For the AD5310R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[\frac{D}{1024}\right]$$

For the AD5311R,

$$V_{OUT}(D) = Gain \times V_{REF} \times \left[\frac{D}{1024}\right]$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register.
Gain is the gain of the output amplifier and is set to ×1 by default. The gain can also be set to 1 or 2 using the gain select bit in the control register.

DAC ARCHITECTURE

The DAC architecture implements a segmented string DAC with an internal output buffer. Figure 37 shows the internal block diagram.

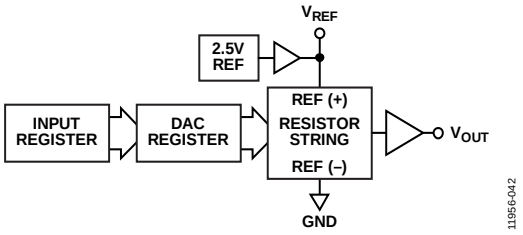

Figure 37. DAC Channel Architecture Block Diagram

The simplified segmented resistor string DAC structure is shown in Figure 38. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

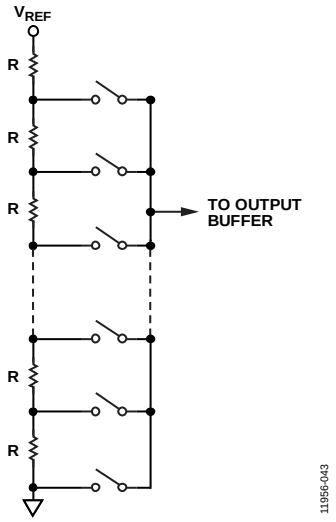

Figure 38. Simplified Resistor String Structure

Internal Reference

The AD5310R/AD5311R has a 2.5 V, 2 ppm/°C reference that provides a full-scale output of 2.5 V or 5 V, depending on the state of the gain bit, see Table 15.

The AD5310R/AD5311R on-chip reference is on at power-up but can be disabled via a write to the control register.

The internal reference is available at the V_{REF} pin. It is internally buffered and capable of driving external loads of up to 50 mA.

External Reference

The V_{REF} pin can be configured as an input pin, allowing the use of an external reference if the application requires it. The default condition of the on-chip reference is on at power-up.

Before connecting an external buffer to the pin, a write to the control register is required to disable the internal reference, see the REF Bit section.

Output Buffer

The output buffer is designed as an input/output rail-to-rail buffer, which gives a maximum output voltage range of up to 0 V to V_{DD}. The gain bit sets the segmented string DAC gain to ×1 or ×2 as shown in Table 15. The output buffer voltage is determined by V_{REF}, the gain bit, and the offset and gain errors.

The output buffer can drive 10nF capacitance with a 2 kΩ resistor in parallel, as shown in Figure 34. If a higher capacitance load is required, a shunt resistor must be connected between the output amplifier and the load. The slew rate is 0.7 V/µs with a ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

AD5310R SPI SERIAL DATA INTERFACE

The AD5310R has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDI) that is compatible with serial peripheral interface (SPI), Mode 1 and Mode 2, and with completely synchronous interfaces such as SPORT. See Figure 3 for a timing diagram of a typical write sequence. See the AN-1248 Application Note for more information about the SPI interface.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the SDI line is sampled into the input shift register on the falling edge of SCLK. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word (16 bits) is loaded from the SDI pin, as shown in Figure 3. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the instructions in Table 10.

$\overline{\text{SYNC}}$ must be brought high for a minimum of 20 ns before the next write sequence such that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

If $\overline{\text{SYNC}}$ is brought high after 16 falling clock edges occur, it is interpreted as a valid write and the first 16 bits are loaded to the input shift register.

If $\overline{\text{SYNC}}$ is brought high before 16 falling clock edges, the serial write is ignored and the write sequence is considered invalid.

To minimize power consumption, it is recommended that all serial interface pins be operated close to the supply rails.

DAISY-CHAIN MODE COMPATIBILITY

The AD5310R can be operated in a daisy-chain configuration, but cannot forward data because there is no SDO pin. To connect the AD5310R in daisy-chain mode, it is possible to connect only one device per chain, and the AD5310R should be connected the last device.

Daisy-chaining minimizes the number of pins required from the controlling IC. As shown in Figure 39, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased because of the propagation delay of the line between subsequent devices. By default, the daisy-chain configuration mode is disabled. To enable it, the DCEN bit must be set in the control register, as shown in Table 11.

When the DCEN bit is enabled in the control register, the AD5310R accepts as a valid frame any data-word longer than 24 bits, and decodes the last 24 bits received, with the last 10 LSB as do not care bits.

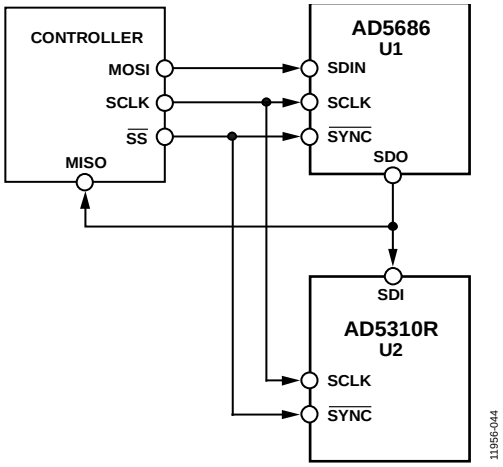

Figure 39. Daisy-Chain Connection

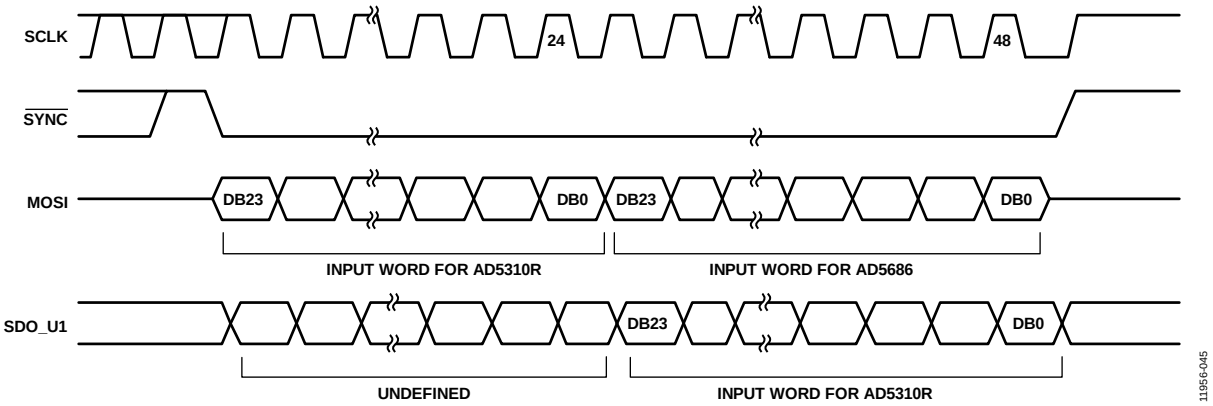

Figure 40. Daisy-Chain Timing Diagram

Table 10. SPI Command Operation

Command Bits[DB15:DB12]				Data Bits [DB11:DB0][1]											Operation
C3	C2	C1	C0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	[DB1:DB0]	
0	0	0	0	X	X	X	X	X	X	X	X	X	X	XX	NOP. Do nothing.
0	0	0	1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	XX	Write input register.
0	0	1	0	X	X	X	X	X	X	X	X	X	X	XX	Update DAC register ($\overline{\text{LDAC}}$ software).
0	0	1	1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	XX	Write DAC and input register.
0	1	0	0	DB9	DB8	DB7	DB6	DB5	DB4	0	0	0	0	00	Write control register.

[1] X = don't care.

Table 11. Control Register Bits

DB11	DB10	DB9	DB8	DB7	DB6
RESET	PD1	PDO	REF	GAIN	DCEN

AD5311R I²C SERIAL DATA INTERFACE

The AD5311R has a 2-wire, I²C-compatible serial interface. These devices can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 4 for a timing diagram of a typical write sequence.

The AD5311R supports standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The 2-wire serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all the data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then high during the tenth clock pulse to establish a stop condition.

I²C Address

The AD5311R has a 7-bit slave address. The five MSBs are 10011. The second to the last bit, set by the state of the A0 address pin and the LSB, is 0. The ability to make hardwired changes to A0 lets the user have two of these devices on one bus, as outlined in Table 12. Additionally, the pin can be updated before starting the transmission, allowing multiples devices in the same bus by connecting the pin to a GPIO or a multiplexer.

Table 12. Device Address Selection

A0 Pin Connection	A0 Bit	I²C Address
GND	0	1001100
V_{LOGIC}	1	1001110

I²C Write Operation

When writing to the AD5311R, the user must begin with a start condition followed by an address byte (R/$\overline{\text{W}}$= 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low, as shown in Figure 41. The AD5311R requires a command byte that controls various DAC functions (see Table 13) and two bytes of data for the DAC. All these data bytes are acknowledged by the AD5311R. A stop condition follows. The write sequence is shown in Figure 41.

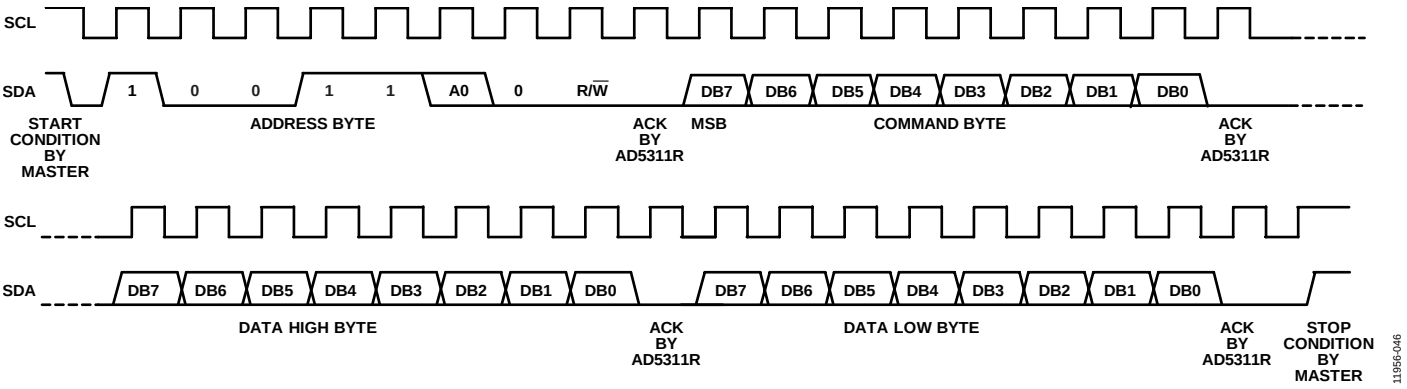

Figure 41. I²C Write Operation

Table 13. I²C Command Table[1]

Command Byte					Data High Byte		Data Low Byte		
DB7	**DB6**	**DB5**	**DB4**	**[DB3:DB0]**	**[DB7:DB3]**	**[DB2:DB0]**	**[DB7:DB6]**	**[DB5:DB0]**	**Operation**
0	0	0	0	XXXX	XXXXX	XXX	XX	XXXXX	NOP: do nothing.
0	0	0	1	XXXX	DB9:DB5	DB:DB2	DB1:DB0	XXXXX	Write input register.
0	0	1	0	XXXX	XXXXX	XXX	XX	XXXXX	Update DAC register ($\overline{\text{LDAC}}$ software).
0	0	1	1	XXXX	DB9:DB5	DB4:DB2	DB1:DB0	XXXXX	Write DAC and input registers.
0	1	0	0	XXXX	DB9:DB5	000	00	00000	Write control register.

[1] X = don't care.

Table 14. Control Register Bits

DB9	DB8	DB7	DB6	DB5
RESET	PD1	PDO	REF	GAIN

COMMANDS

Write Input Register

The input register allows the preloading of a new value for the DAC register. The transfer from the input register to the DAC register can be triggered by hardware, by the $\overline{\text{LDAC}}$ pin, or by software using Command 2.

If new data is loaded into the DAC register, the DAC register automatically overwrites the input register.

Update DAC Register

This command transfers the contents of the input register to the DAC register and, consequently, the V_{OUT} pin is updated. The data contained in the serial write is ignored.

This operation is equivalent to a software $\overline{\text{LDAC}}$.

Write DAC Register

This command updates the DAC register on completion of the write operation. The input register is refreshed automatically with the DAC register value.

Write Control Register

The write control register command is used to set the power-down and gain functions. It is also used to enable/disable the internal reference and perform a software reset. See Table 14 for the control register bits.

Gain Bit

The gain bit selects the gain of the output amplifier. Table 15 shows how the output voltage range corresponds to the state of the gain bit.

Table 15. Gain Bit

Gain	Output Voltage Range
0	0 V to V_{REF} (default)
1	0 V to 2 × V_{REF}

REF Bit

The on-chip reference is on at power-up by default. This reference can be turned on or off by setting a software programmable bit, DB6, in the control register. Table 16 shows how the state of the bit corresponds to the mode of operation.

To reduce power consumption, it is recommended that the internal reference be disabled if the device is placed in power-down mode.

Table 16. REF Bit

REF	Reference Function
0	Reference enabled (default)
1	Reference disabled

PD0 and PD1 Bits

The AD5310R/AD5311R provide two separate modes of operation that are accessed by writing to the write control register.

In normal mode, the output buffer is directly connected to the V_{OUT} pin.

In power-down mode, the output buffer is internally disabled and the V_{OUT} pin output impedance can be selected to a well-known value, as shown in Table 17.

Table 17. Operation Modes

Operating Mode	PD1	PD0
Normal Mode	0	0
Power-Down Modes		
1 kΩ Output Impedance	0	1
100 kΩ Output Impedance	1	0
Three-State Output Impedance	1	1

In power-down mode, the part disables the output buffer, but does not disable the internal reference. To achieve maximum power saving, it is recommend that the REF bit be disabled.

Disabling both the internal reference and the output buffer results in the supply current falling to 2 µA at 5 V.

The output stage is illustrated in Figure 42.

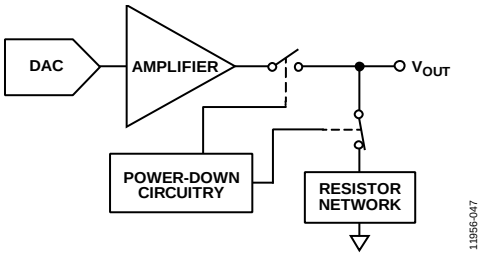

Figure 42. Output Stage During Power-Down

The output amplifier is shut down when the power-down mode is activated. However, unless the internal reference is powered down, the bias generator, reference, and resistor string remain on. The supply current falls to 2 µA at 5 V. The contents of the DAC register are unaffected in power-down mode, and the DAC register can be updated while the device is in power-down mode. The time that is required to exit power-down is typically 4 µs for V_{DD} = 5 V, or 600 µs if the reference is disabled.

Reset Bit

The write control register of the AD5310R/AD5311R contains a software reset bits that resets the DAC registers to zero scale and resets the input, the DAC, and the control registers to their default values. A software reset is initiated by setting the reset bit in the control register to 1. When the software reset is completed, the reset bit is cleared to 0 automatically.

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5310R/AD5311R have a double buffered interface consisting of an input register and a DAC register. The $\overline{\text{LDAC}}$ pin transfers data from the input register to the DAC register, and the output is updated.

Synchronous DAC Update (AD5311R Only)

If the $\overline{\text{LDAC}}$ pin is held low while the input register is written, the DAC register, input register, and output are updated on the last SCL falling edge before the ACK bit, as shown in Figure 5.

Asynchronous DAC Update

$\overline{\text{LDAC}}$ is held high while data is transmitted to the device. The DAC output is updated by taking $\overline{\text{LDAC}}$ low after the stop condition is generated. The output DAC is updated on the falling edge of the $\overline{\text{LDAC}}$ pin.

If $\overline{\text{LDAC}}$ is pulsed while the device is accessed, the pulse is ignored.

HARDWARE $\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is an active low signal that resets the DAC output to zero scale and sets the input, DAC, and control registers to their default values. It is necessary to keep $\overline{\text{RESET}}$ low for 75 ns to complete the operation. When the $\overline{\text{RESET}}$ signal returns high, the output remains at zero scale until a new value is programmed. While the $\overline{\text{RESET}}$ pin is low, the AD5310R/AD5311R ignore any new command.

If $\overline{\text{RESET}}$ is held low at power-up, the internal reference is not initialized correctly until the $\overline{\text{RESET}}$ pin is released.

AD5311R, I²C READ OPERATION

When reading the input register back from the AD5311R DAC, the user begins with an address byte (R/$\overline{\text{W}}$ = 1), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. Two bytes of data containing the contents of the input register are then read from the DAC, as shown in Figure 43. A NACK condition from the master followed by a stop condition completes the read sequence.

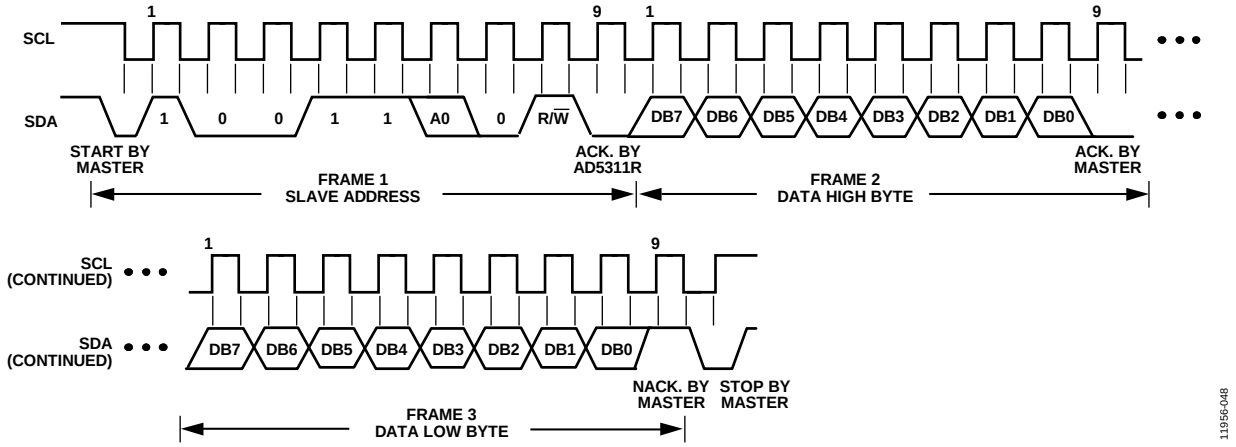

Figure 43. I²C Read Operation

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot, and then back to ambient.

The thermal hysteresis data is shown in Figure 44. It is measured by sweeping the temperature from ambient +25°C to −40°C, then to +105°C, and finally returning to ambient +25°C. The V_{REF} delta is next measured between the two ambient measurements and shown in the solid lines in Figure 44. The same temperature sweep and measurements are immediately repeated and the results are shown in the dashed lines in Figure 44.

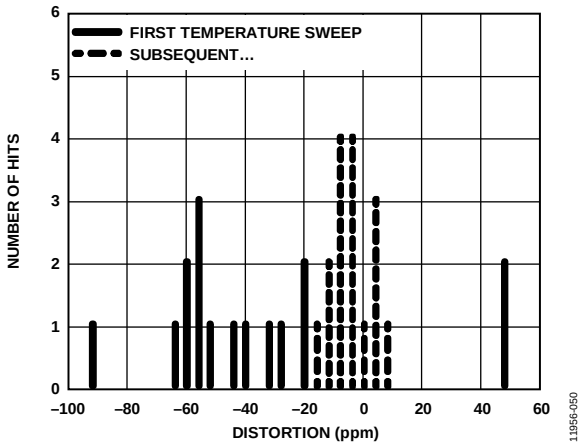

Figure 44. Thermal Hysteresis

POWER-UP SEQUENCE

Because diodes limit the voltage compliance at the digital and analog pins, it is important to power GND first before applying any voltage to V_{DD}, V_{OUT}, and V_{LOGIC}. Otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally. The ideal power-up sequence is GND, V_{DD}, V_{LOGIC}, V_{REF}, followed by the digital inputs.

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5310R/AD5311R are mounted should be designed such that the AD5310R/AD5311Rare placed on the analog plane.

Ensure that the AD5310R/AD5311R have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. Use a 0.1 µF capacitor with low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.