Quad, 10-Bit *nano*DAC with 2 ppm/°C Reference, I²C Interface

Data Sheet **AD5316R**

FEATURES

Low drift 2.5 V on-chip reference: 2 ppm/°C typical
Tiny package: 3 mm × 3 mm, 16-lead LFCSP
TUE: ±0.1% of FSR maximum
Offset error: ±1.5 mV maximum
Gain error: ±0.1% of FSR maximum
High drive capability: 20 mA, 0.5 V from supply rails
User-selectable gain of 1 or 2 (GAIN pin)
Reset to zero scale or midscale (RSTSEL pin)
1.8 V logic compatibility
400 kHz I²C-compatible serial interface
4 I²C addresses available
Low glitch: 0.5 nV-sec
Low power: 3.3 mW at 3 V
2.7 V to 5.5 V power supply
−40°C to +105°C temperature range

APPLICATIONS

Digital gain and offset adjustment
Programmable attenuators
Industrial automation
Data acquisition systems

FUNCTIONAL BLOCK DIAGRAM

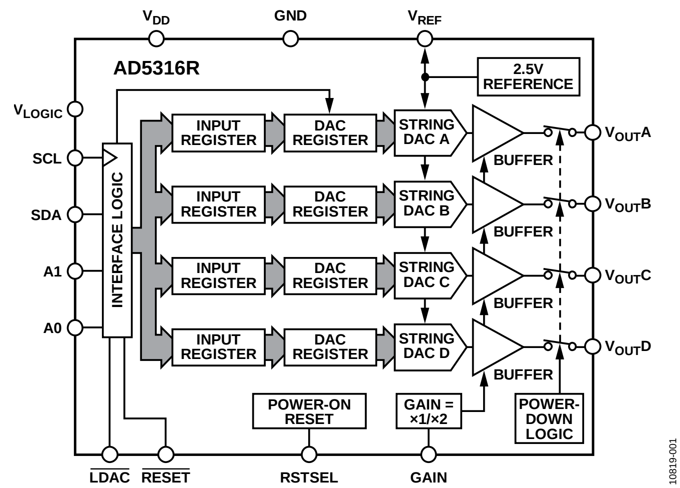

Figure 1.

GENERAL DESCRIPTION

The AD5316R, a member of the *nano*DAC® family, is a low power, quad, 10-bit buffered voltage output DAC. The device includes a 2.5 V, 2 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7 V to 5.5 V supply, is guaranteed monotonic by design, and exhibits less than 0.1% FSR gain error and 1.5 mV offset error performance. The device is available in a 3 mm × 3 mm lead lead frame chip scale package (LFCSP) and in a thin shrink small outline package (TSSOP).

The AD5316R also incorporates a power-on reset circuit and a RSTSEL pin. The RSTSEL pin ensures that the DAC outputs power up to zero scale or midscale and remain at that level until a valid write takes place. The device contains a per channel power-down feature that reduces the current consumption of the device in power-down mode to 4 µA at 3 V.

The AD5316R uses a versatile 2-wire serial interface that operates at clock rates up to 400 kHz and includes a V_{LOGIC} pin intended for 1.8 V/3 V/5 V logic.

Table 1. Related Devices

Interface	Reference	12-Bit	10-Bit
SPI	Internal	AD5684R	AD5317R
	External	AD5684	AD5317
I²C	Internal	AD5694R	
	External	AD5694	AD5316[1]

[1] The AD5316R and the AD5316 are not pin-to-pin or software compatible.

PRODUCT HIGHLIGHTS

1. Precision DC Performance.
   Total unadjusted error (TUE): ±0.1% of FSR maximum
   Offset error: ±1.5 mV maximum
   Gain error: ±0.1% of FSR maximum
2. Low Drift 2.5 V On-Chip Reference.
   2 ppm/°C typical temperature coefficient
   5 ppm/°C maximum temperature coefficient
3. Two Package Options.
   3 mm × 3 mm, 16-lead LFCSP
   16-lead TSSOP

Rev. D **Document Feedback**

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7/2012—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, R_L = 2 kΩ, C_L = 200 pF, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1, 2]
STATIC PERFORMANCE[3]					
Resolution	10			Bits	
Relative Accuracy		±0.12	±0.5	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic by design
Zero-Code Error		0.4	1.5	mV	All 0s loaded to DAC register
Offset Error		+0.1	±1.5	mV	
Full-Scale Error		+0.01	±0.1	% of FSR	All 1s loaded to DAC register
Gain Error		±0.02	±0.1	% of FSR	
TUE		±0.01	±0.1	% of FSR	External reference, gain = 2, TSSOP
			±0.2	% of FSR	Internal reference, gain = 1, TSSOP
Offset Error Drift[4]		±1		µV/°C	
Gain Temperature Coefficient[4]		±1		ppm	Of FSR/°C
DC Power Supply Rejection Ratio[4]		0.15		mV/V	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk[4]		±2		µV	Due to single channel, full-scale output change
		±3		µV/mA	Due to load current change
		±2		µV	Due to power-down (per channel)
OUTPUT CHARACTERISTICS[4]					
Output Voltage Range	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	V	Gain = 2 (see Figure 25)
Capacitive Load Stability		2		nF	R_L = ∞
		10		nF	R_L = 1 kΩ
Resistive Load[5]	1			kΩ	
Load Regulation					DAC code = midscale
		80		µV/mA	5 V ± 10%; −30 mA ≤ I_{OUT} ≤ +30 mA
		80		µV/mA	3 V ± 10%; −20 mA ≤ I_{OUT} ≤ +20 mA
Short-Circuit Current[6]		40		mA	
Load Impedance at Rails[7]		25		Ω	See Figure 25
Power-Up Time		2.5		µs	Coming out of power-down mode; V_{DD} = 5 V
REFERENCE OUTPUT					
Output Voltage[8]	2.4975		2.5025	V	At T_A
Reference TC[9]		2	5	ppm/°C	See the Terminology section
Output Impedance[4]		0.04		Ω	
Output Voltage Noise[4]		12		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density[4]		240		nV/√Hz	At T_A, f = 10 kHz, C_L = 10 nF
Load Regulation, Sourcing[4]		20		µV/mA	At T_A
Load Regulation, Sinking[4]		40		µV/mA	At T_A
Output Current Load Capability[4]		±5		mA	V_{DD} ≥ 3 V
Line Regulation[4]		100		µV/V	At T_A
Thermal Hysteresis[4]		125		ppm	First cycle
		25		ppm	Additional cycles
LOGIC INPUTS[4]					
Input Current			±2	µA	Per pin
Input Low Voltage, V_{INL}			0.3 × V_{LOGIC}	V	
Input High Voltage, V_{INH}	0.7 × V_{LOGIC}			V	
Pin Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1, 2]
LOGIC OUTPUTS (SDA)[4]					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
Floating State Output Capacitance		4		pF	
POWER REQUIREMENTS					
V_{LOGIC}	1.8		5.5	V	
I_{LOGIC}			3	µA	
V_{DD}	2.7		5.5	V	Gain = 1
	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}					$V_{IH} = V_{DD}$, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[10]		0.59	0.7	mA	Internal reference off
		1.1	1.3	mA	Internal reference on, at full scale
All Power-Down Modes[11]		1	4	µA	−40°C to +85°C
			6	µA	−40°C to +105°C

[1] Temperature range is −40°C to +105°C.
[2] The AD5316R and the AD5316 are not pin-to-pin or software compatible.
[3] DC specifications are tested with the outputs unloaded, unless otherwise noted. Upper dead band (10 mV) exists only when $V_{REF} = V_{DD}$ with gain = 1 or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 4 to 1020.
[4] Guaranteed by design and characterization; not production tested.
[5] Channel A and Channel B can have a combined output current of up to 30 mA. Similarly, Channel C and Channel D can have a combined output current of up to 30 mA up to a junction temperature of 110°C.
[6] V_{DD} = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
[7] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 25).
[8] Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the Solder Heat Reflow section.
[9] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +105°C. Reference temperature coefficient is calculated as per the box method. See the Terminology section for more information.
[10] Interface inactive. All DACs active. DAC outputs unloaded.
[11] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; V_{REF} = 2.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; R_L = 2 kΩ; C_L = 200 pF; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
Output Voltage Settling Time		5	7	µs	¼ to ¾ scale settling to ±1 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse		0.5		nV-sec	1 LSB change around major carry transition
Digital Feedthrough		0.13		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		0.2		nV-sec	
DAC-to-DAC Crosstalk		0.3		nV-sec	
Total Harmonic Distortion (THD)[4]		−80		dB	At T_A, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density		300		nV/√Hz	DAC code = midscale, 10 kHz, gain = 2, internal reference enabled
Output Noise		6		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C; typical at 25°C.
[4] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, 1.62 V ≤ V_{LOGIC} ≤ 5.5 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2]	Min	Max	Unit	Description
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD,STA}$, start/repeated start hold time
t_5	100		ns	$t_{SU,DAT}$, data setup time
t_6[3]	0	0.9	µs	$t_{HD,DAT}$, data hold time
t_7	0.6		µs	$t_{SU,STA}$, repeated start setup time
t_8	0.6		µs	$t_{SU,STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}[4]	0	300	ns	t_R, rise time of SCL and SDA when receiving
t_{11}[4, 5]	20 + 0.1C_B	300	ns	t_F, fall time of SCL and SDA when transmitting/receiving
t_{12}	20		ns	$\overline{LDAC}$ pulse width
t_{13}	400		ns	SCL rising edge to $\overline{LDAC}$ rising edge
t_{SP}[6]	0	50	ns	Pulse width of suppressed spike
C_B[5]		400	pF	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization; not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the SCL falling edge.
[4] t_R and t_F are measured from 0.3 × V_{DD} to 0.7 × V_{DD}.
[5] C_B is the total capacitance of one bus line in pF.
[6] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

Timing Diagram

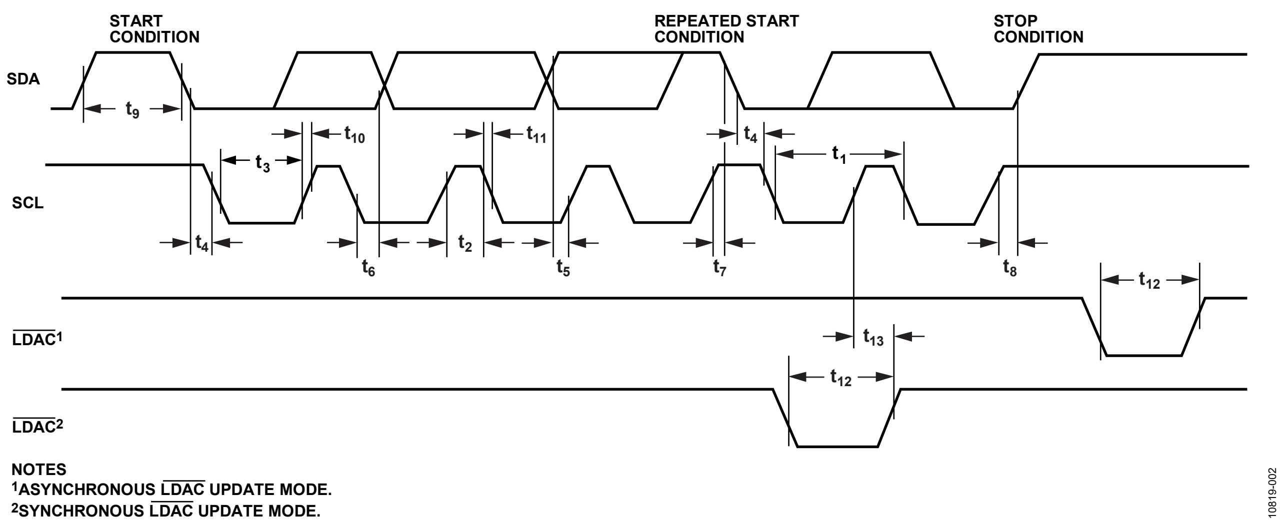


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND[1]	−0.3 V to V_{LOGIC} + 0.3 V
SDA and SCL to GND	−0.3 V to +7 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C

[1] Excluding SDA and SCL.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

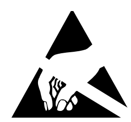
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This value was measured using a JEDEC standard 4-layer board with zero airflow. For the LFCSP package, the exposed pad must be tied to GND.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	70	°C/W
16-Lead TSSOP	112.6	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

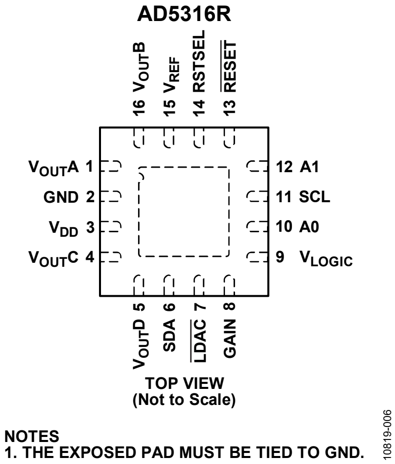


Figure 3. 16-Lead LFCSP Pin Configuration

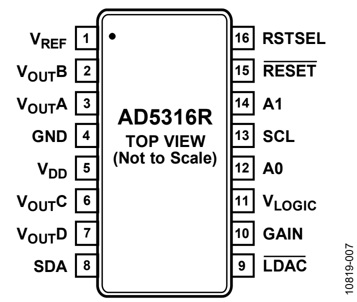


Figure 4. 16-Lead TSSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
LFCSP	**TSSOP**	**Mnemonic**	**Description**
1	3	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	4	GND	Ground Reference Point for All Circuitry on the Device.
	5	V_{DD}	Power Supply Input. The device can be operated from 2.7 V to 5.5 V. The supply must be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	6	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	7	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
6	8	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
7	9	LDAC	LDAC can be operated in two modes, asynchronous update mode and synchronous update mode. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data; all DAC outputs are simultaneously updated. This pin can also be tied permanently low.
8	10	GAIN	Gain Select Pin. When this pin is tied to GND, all four DAC outputs have a span of 0 V to V_{REF}. When this pin is tied to V_{LOGIC}, all four DAC outputs have a span of 0 V to 2 × V_{REF}.
9	11	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V.
10	12	A0	Address Input. Sets the first LSB of the 7-bit slave address.
11	13	SCL	Serial Clock Line. This pin is used in conjunction with the SDA line to clock data into or out of the 24-bit input shift register.
12	14	A1	Address Input. Sets the second LSB of the 7-bit slave address.
13	15	RESET	Asynchronous Reset Input. The RESET input is falling edge sensitive. When RESET is activated (low), the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. When RESET is low, all LDAC pulses are ignored. If the pin is not used, tie it permanently to V_{LOGIC}. If the pin is forced low at power-up, the POR circuit does not initialize correctly until the pin is released.
14	16	RSTSEL	Power-On Reset Pin. When this pin is tied to GND, all four DACs are powered up to zero scale. When this pin is tied to V_{LOGIC}, all four DACs are powered up to midscale.
15	1	V_{REF}	Reference Voltage. The AD5316R has an internal reference. When the internal reference is used, V_{REF} is the reference output pin. When an external reference is used, V_{REF} is the reference input pin. By default, the internal reference is used, and this pin is a reference output.
16	2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
17	N/A	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

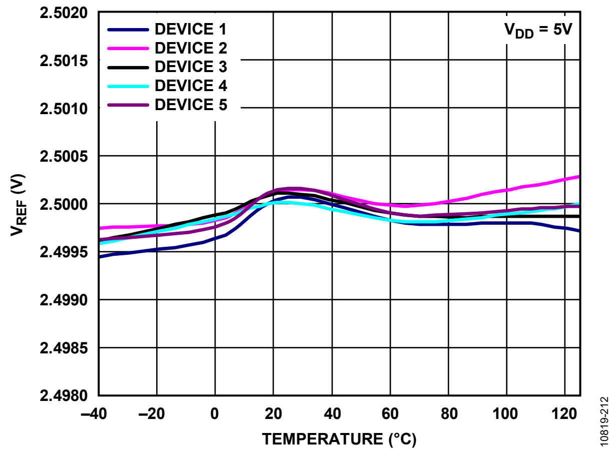


Figure 5. Internal Reference Voltage (V_{REF}) vs. Temperature

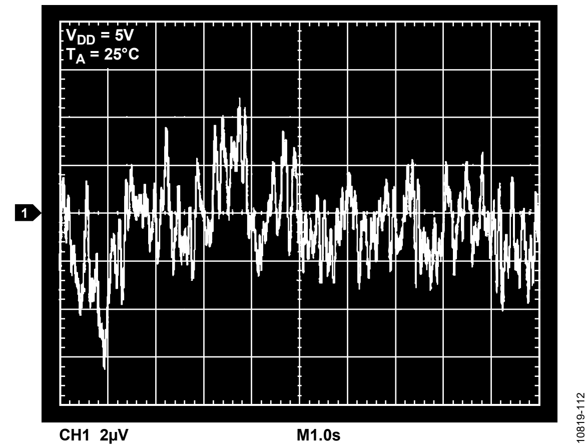


Figure 8. Internal Reference Noise, 0.1 Hz to 10 Hz

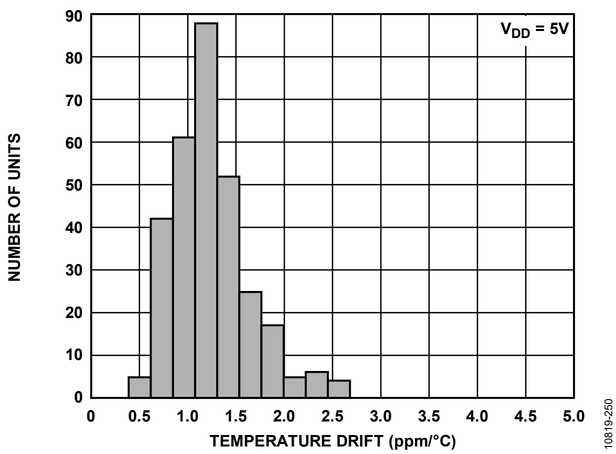


Figure 6. Reference Output Temperature Drift Histogram

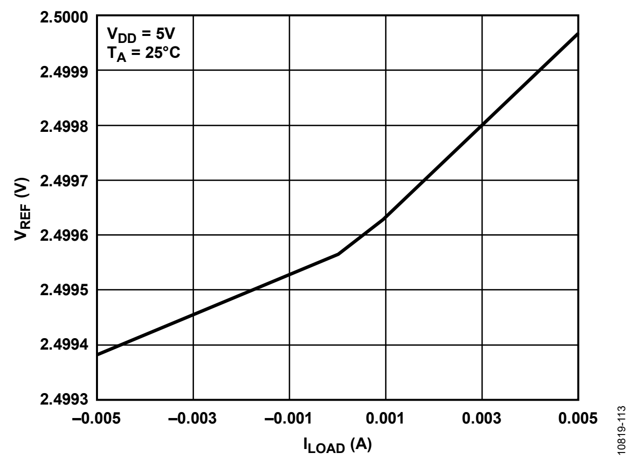


Figure 9. V_{REF} vs. Load Current (I_{LOAD})

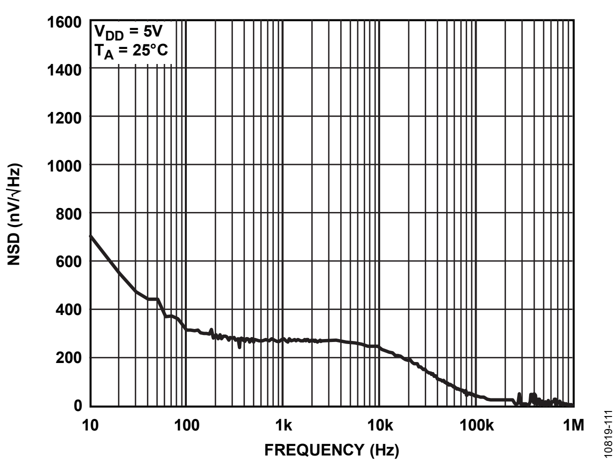


Figure 7. Internal Reference Noise Spectral Density (NSD) vs. Frequency

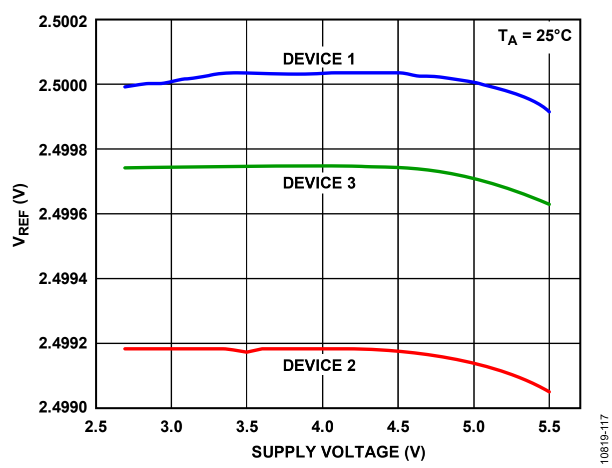


Figure 10. V_{REF} vs. Supply Voltage

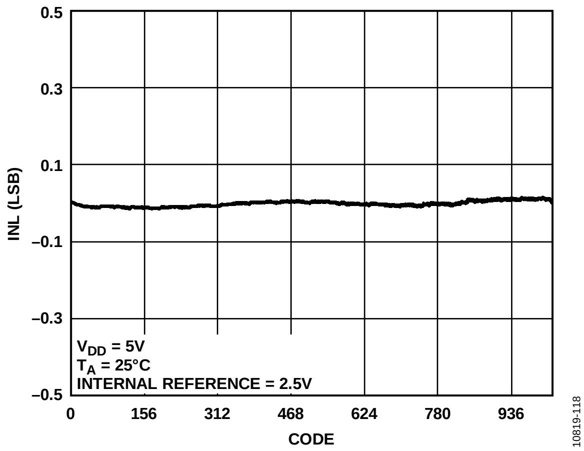


Figure 11. INL vs. Code

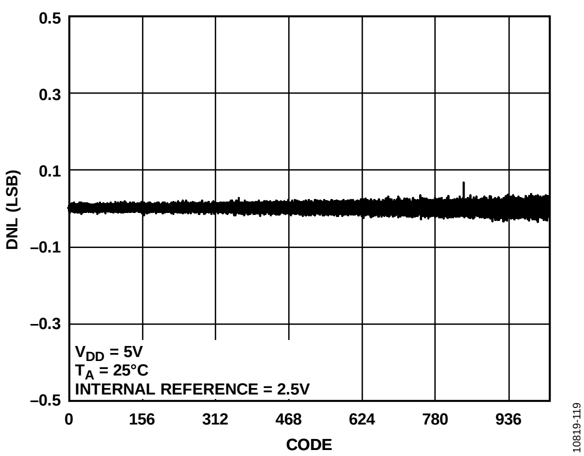


Figure 12. DNL vs. Code

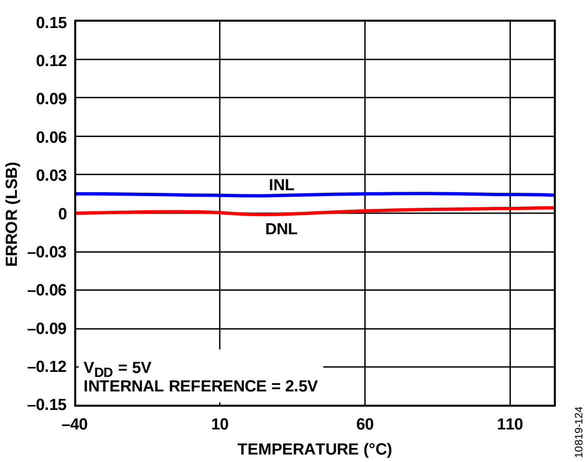


Figure 13. INL Error and DNL Error vs. Temperature

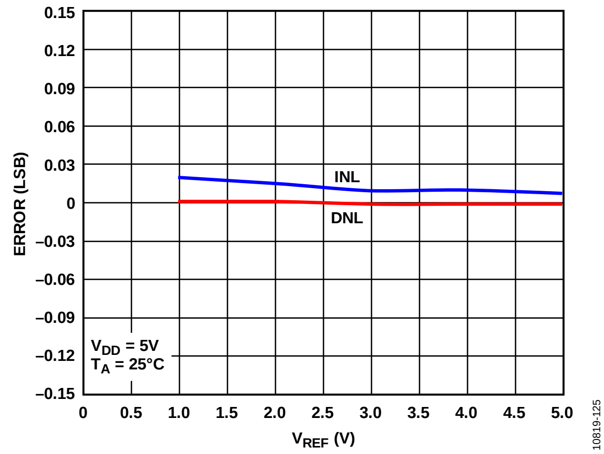


Figure 14. INL Error and DNL Error vs. V_{REF}

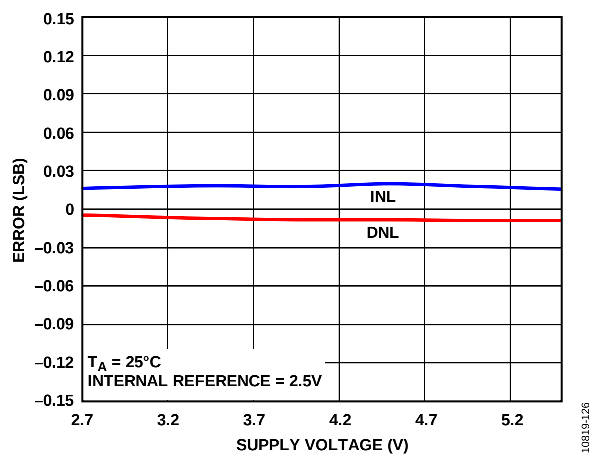


Figure 15. INL Error and DNL Error vs. Supply Voltage

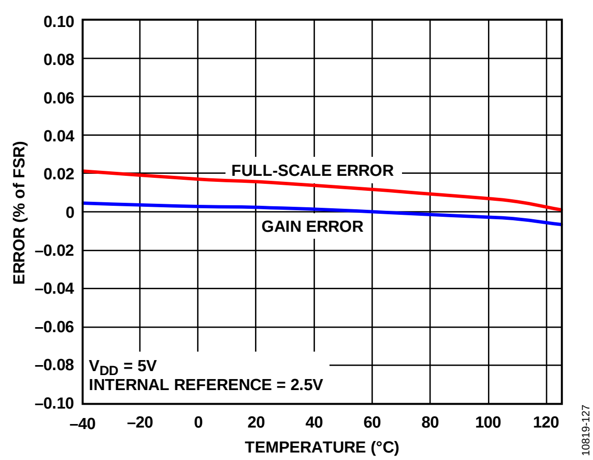


Figure 16. Gain Error and Full-Scale Error vs. Temperature

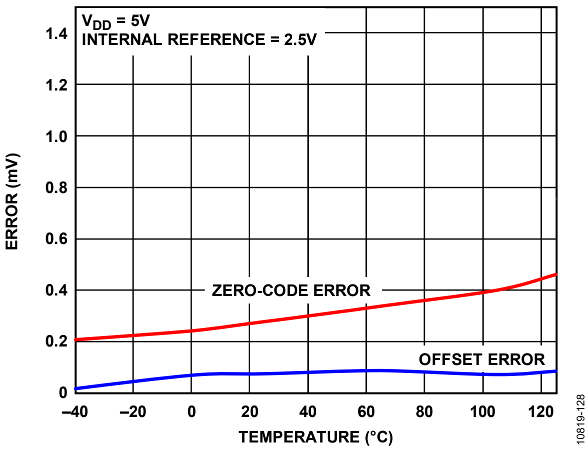


Figure 17. Zero-Code Error and Offset Error vs. Temperature

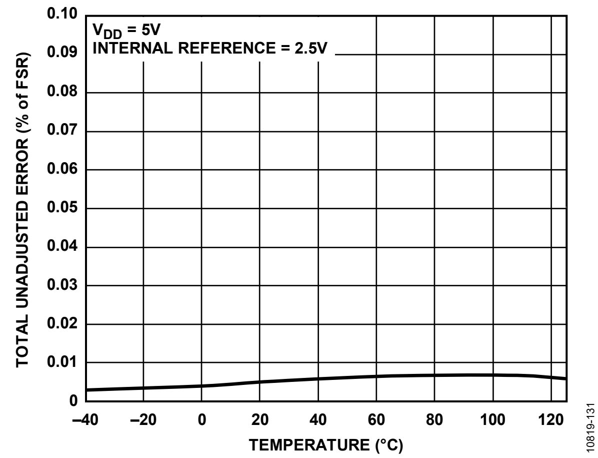


Figure 20. TUE vs. Temperature

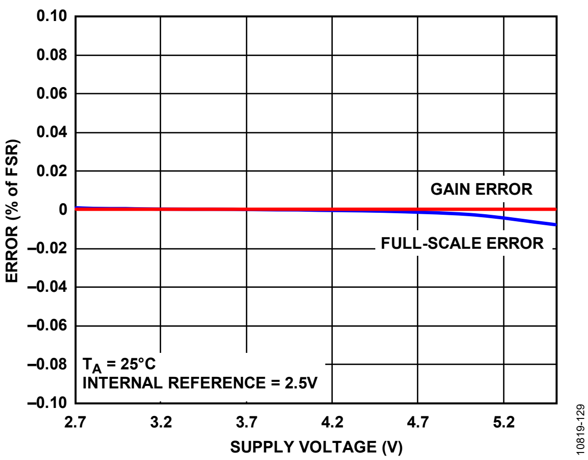


Figure 18. Gain Error and Full-Scale Error vs. Supply Voltage

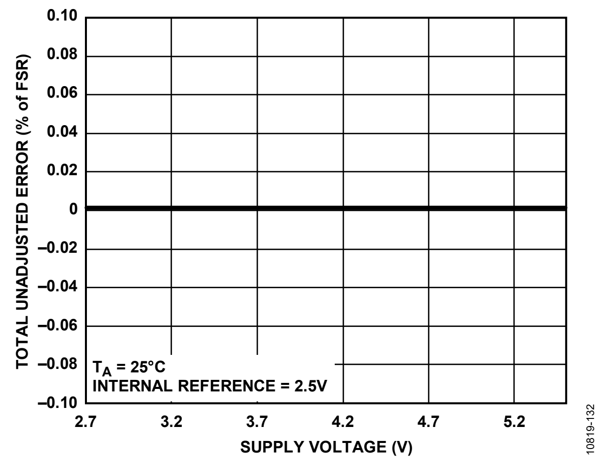


Figure 21. TUE vs. Supply Voltage, Gain = 1

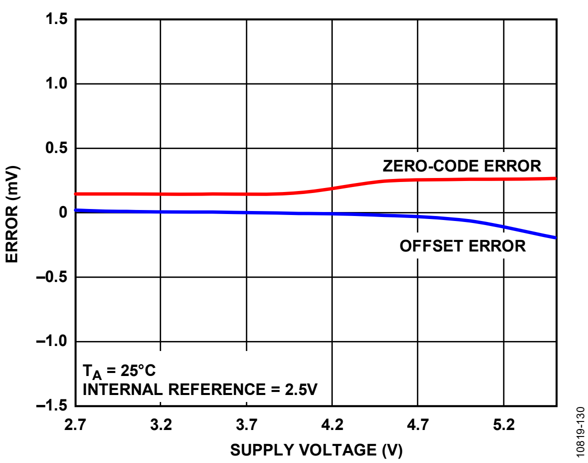


Figure 19. Zero-Code Error and Offset Error vs. Supply Voltage

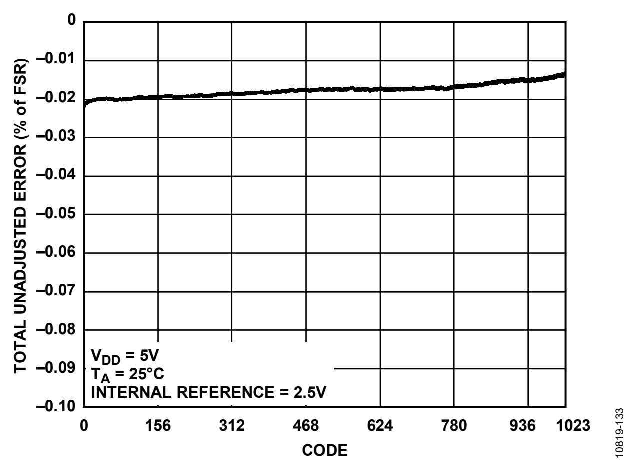


Figure 22. TUE vs. Code

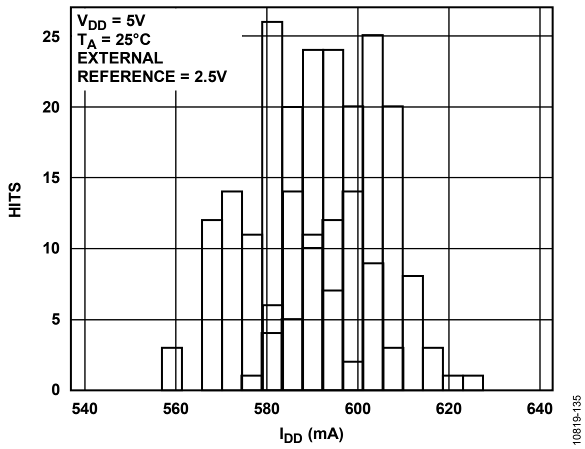


Figure 23. I_{DD} Histogram with External Reference, 5 V

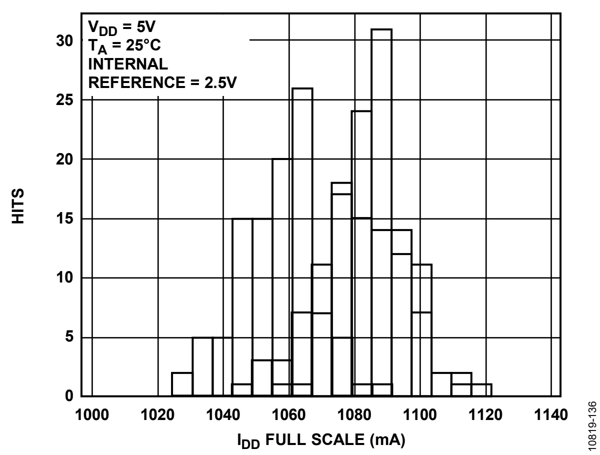


Figure 24. I_{DD} Histogram with Internal Reference, V_{REF} = 2.5 V, Gain = 2

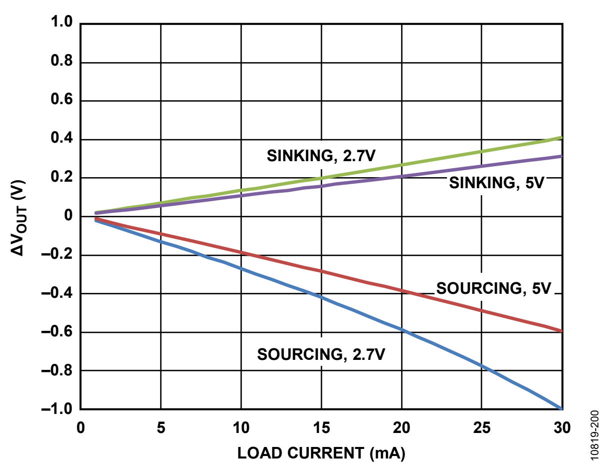


Figure 25. Headroom/Footroom vs. Load Current

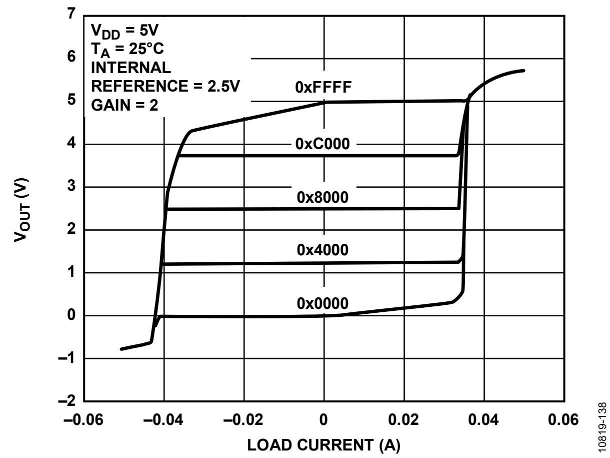


Figure 26. Source and Sink Capability at 5 V

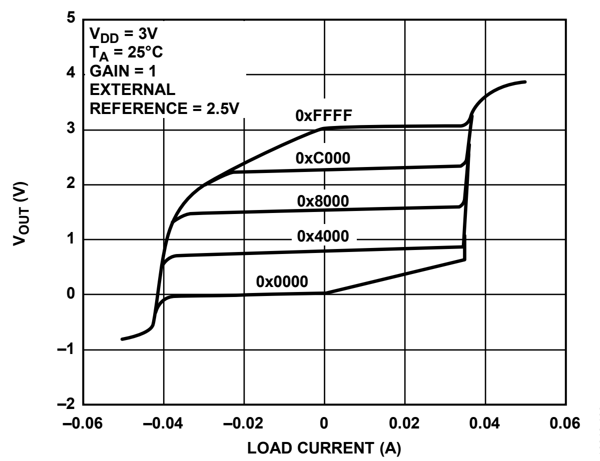


Figure 27. Source and Sink Capability at 3 V

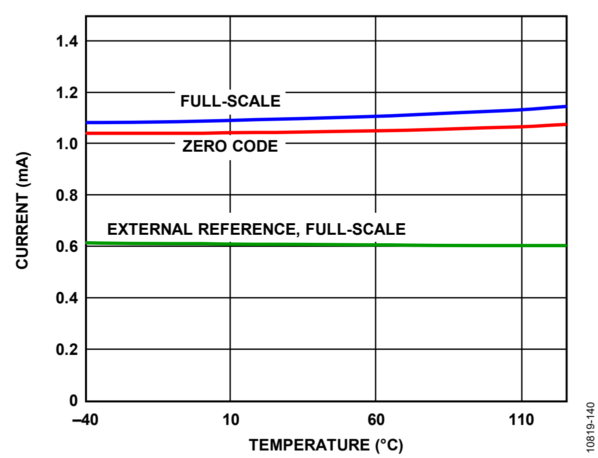


Figure 28. Supply Current vs. Temperature

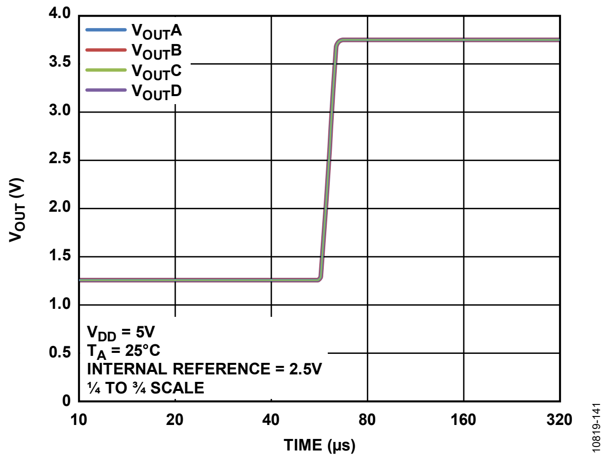


Figure 29. Settling Time

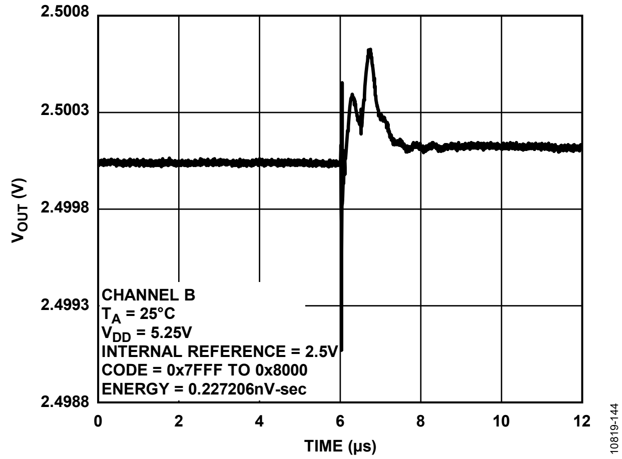


Figure 32. Digital-to-Analog Glitch Impulse

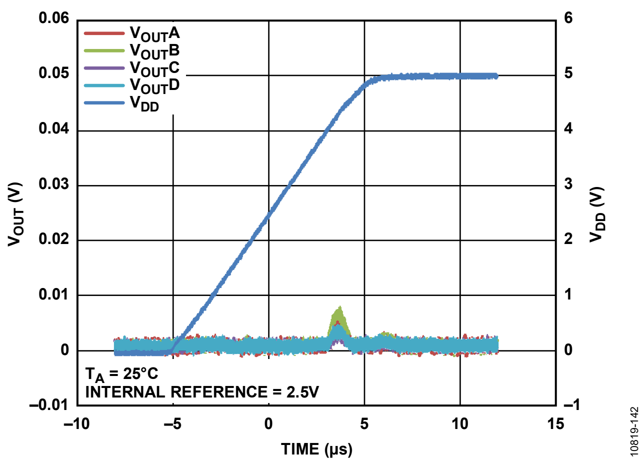


Figure 30. Power-On Reset to 0 V

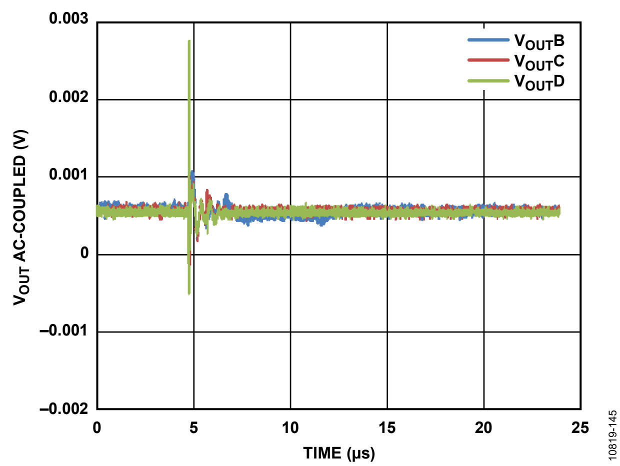


Figure 33. Analog Crosstalk, $V_{OUT}A$

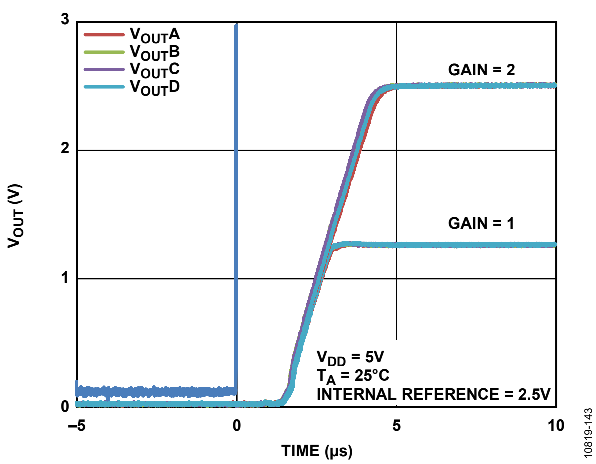


Figure 31. Exiting Power-Down to Midscale

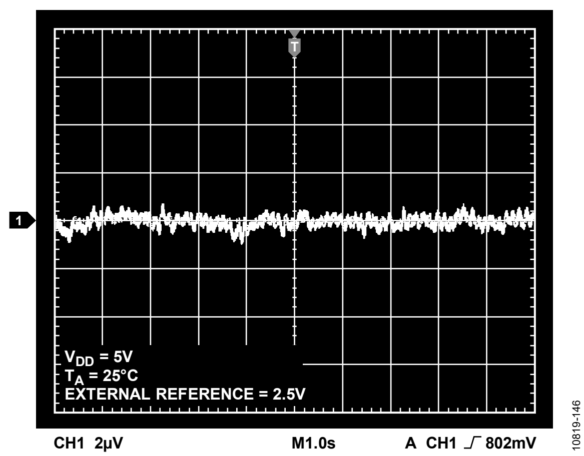


Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V External Reference

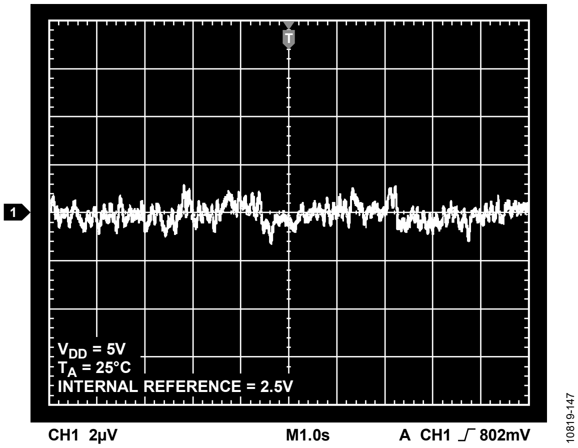


Figure 35. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

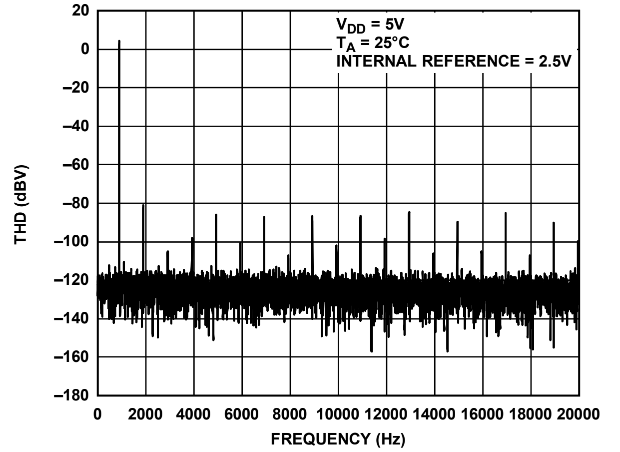


Figure 37. THD at 1 kHz

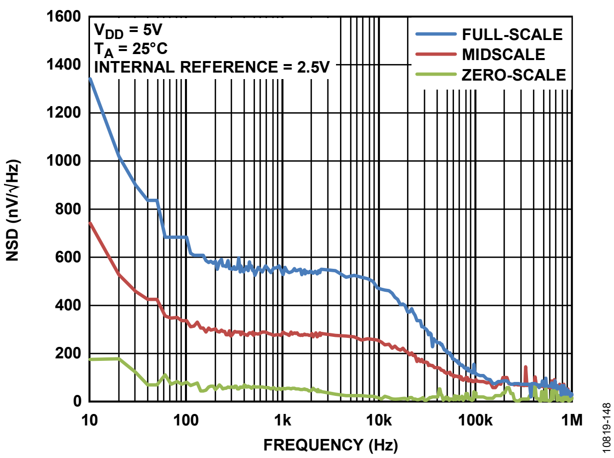


Figure 36. NSD

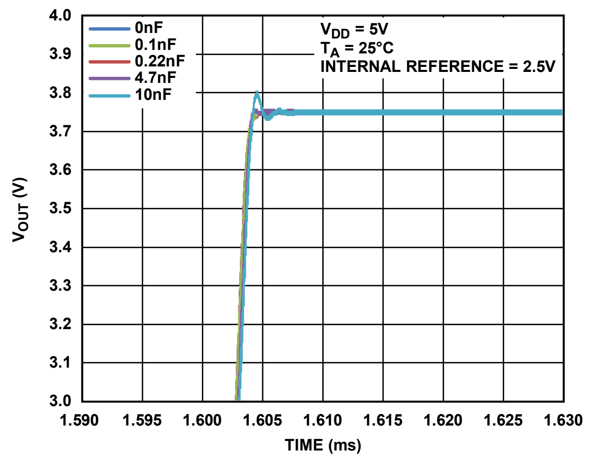


Figure 38. Settling Time at Various Capacitive Loads

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
Relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Figure 11 shows a typical INL vs. code plot.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. The AD5316R is guaranteed monotonic by design. Figure 12 shows a typical DNL vs. code plot.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5316R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. Figure 17 shows a plot of zero-code error vs. temperature.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range (% of FSR). Figure 16 shows a plot of full-scale error vs. temperature.

Gain Error
Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % of FSR.

Gain Temperature Coefficient
Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. It can be negative or positive.

Offset Error Drift
Offset error drift is a measurement of the change in offset error with changes in temperature. It is expressed in µV/°C.

DC Power Supply Rejection Ratio (PSRR)
DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for midscale output of the DAC. It is measured in mV/V. V_{REF} is held at 2.5 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 32).

Digital Feedthrough
Digital feedthrough is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Noise Spectral Density (NSD)
Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz) and is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. Figure 36 shows a plot of noise spectral density.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measurement of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV-sec.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC in response to a change in the output of another DAC. To measure analog crosstalk, load one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), and then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC in response to a digital code change and subsequent analog output change of another DAC. It is measured by loading one channel with a full-scale code change (all 0s to all 1s and vice versa) using the write to and update commands while monitoring the output of another channel that is at mid-scale. The energy of the glitch is expressed in nV-sec.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC; THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measurement of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:

V_{REFmax} is the maximum reference output measured over the total temperature range.

V_{REFmin} is the minimum reference output measured over the total temperature range.

V_{REFnom} is the nominal reference output voltage, 2.5 V.

TempRange is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD5316R is a quad, 10-bit, serial input, voltage output DAC with an internal reference. The device operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5316R in a 24-bit word format via a 2-wire serial interface. The AD5316R incorporates a power-on reset circuit to ensure that the DAC output powers up to a known output state. The device also has a software power-down mode that reduces the typical current consumption to 1 µA.

TRANSFER FUNCTION

The internal reference is on by default. Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REF} \times Gain\left[\frac{D}{2^N}\right]$$

where:
V_{REF} is the value of the external reference.
Gain is the gain of the output amplifier and is set to 1 by default. The gain can be set to 1 or 2 using the gain select pin. When the GAIN pin is tied to GND, all four DAC outputs have a span of 0 V to V_{REF}. When this pin is tied to V_{DD}, all four DAC outputs have a span of 0 V to 2 × V_{REF}.
D is the decimal equivalent of the binary code that is loaded to the DAC register (0 to 1023).
N is the DAC resolution (10 bits).

DAC ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 39 shows a block diagram of the DAC architecture.

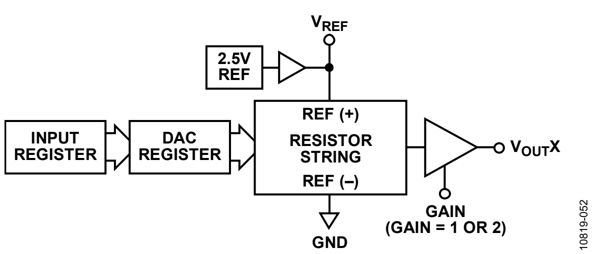


Figure 39. Single DAC Channel Architecture Block Diagram

The resistor string structure is shown in Figure 40. Each resistor in the string has a value R. The code loaded to the DAC register determines the node on the string from which the voltage is tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches that connect the string to the amplifier. Because the AD5316R is a string of resistors, it is guaranteed monotonic.

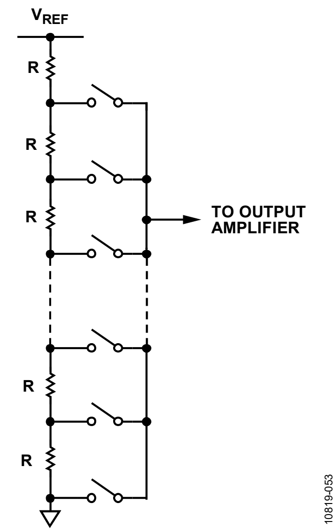


Figure 40. Resistor String Structure

Internal Reference

The AD5316R on-chip reference is on at power-up but can be disabled via a write to a control register. For more information, see the Internal Reference Setup section.

The 2.5 V, 2 ppm/°C internal reference provides a full-scale output of 2.5 V or 5 V, depending on the state of the GAIN pin. The internal reference is available at the V_{REF} pin. This buffered reference is capable of driving external loads of up to 10 mA.

Output Amplifiers

The output buffer amplifier can generate rail-to-rail voltages on its output for an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the GAIN pin, the offset error, and the gain error. The GAIN pin selects the gain of the output.

- When this pin is tied to GND, all four outputs have a gain of 1, and the output range is from 0 V to V_{REF}.
- When this pin is tied to V_{DD}, all four outputs have a gain of 2, and the output range is from 0 V to 2 × V_{REF}.

The output amplifiers are capable of driving a load of 1 kΩ in parallel with 2 nF to GND. The slew rate is 0.8 V/µs with a ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

The AD5316R has a 2-wire, I²C-compatible serial interface (see the *I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductors now NXP Semiconductors). See Figure 2 for a timing diagram of a typical write sequence. The AD5316R can be connected to an I²C bus as a slave device, under the control of a master device. The AD5316R supports standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing or general call addressing.

Input Shift Register

The input shift register of the AD5316R is 24 bits wide. Data is loaded into the device, MSB first, as a 24-bit word under the control of the serial clock input, SCL. The input shift register consists of an 8-bit command byte and a 16-bit data-word (see Figure 41). The first eight MSBs make up the command byte.

- The first four bits of the command byte are the command bits (C3, C2, C1, and C0), which control the mode of operation of the device (see Table 8).
- The last four bits of the command byte are the address bits (DAC D, DAC C, DAC B, and DAC A), which select the DAC that is operated on by the command (see Table 9).

Table 8. Command Definitions

Command Bits				
C3	C2	C1	C0	Command
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference setup register
1	X[1]	X[1]	X[1]	Reserved

[1] X = don't care.

Table 9. Address Bits and Selected DACs

Address Bits				
DAC D	DAC C	DAC B	DAC A	Selected DAC Channels[1]
0	0	0	1	DAC A
0	0	1	0	DAC B
0	0	1	1	DAC A and DAC B
0	1	0	0	DAC C
0	1	0	1	DAC A and DAC C
0	1	1	0	DAC B and DAC C
0	1	1	1	DAC A, DAC B, and DAC C
1	0	0	0	DAC D
1	0	0	1	DAC A and DAC D
…	…	…	…	…
1	1	1	1	All DACs

[1] Any combination of DAC channels can be selected using the address bits.

The 8-bit command byte is followed by two data bytes, which contain the data-word. The data-word comprises the 10-bit input code, followed by six don't care bits (see Figure 41). The data bits are transferred to the input register on the 24 falling edges of SCL.

Commands can be executed on one DAC channel, any two or three DAC channels, or on all four DAC channels, depending on the address bits selected (see Table 9).

WRITE AND UPDATE COMMANDS

For more information about the $\overline{\text{LDAC}}$ function, see the Load DAC (Hardware $\overline{\text{LDAC}}$ Pin) section.

Write to Input Register n (Dependent on $\overline{\text{LDAC}}$)

Command 0001 allows the user to write to each DAC's dedicated input register individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent (if not controlled by the $\overline{\text{LDAC}}$ mask register).

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers/outputs with the contents of the input registers selected by the address bits (see Table 9) and updates the DAC outputs directly.

Write to and Update DAC Channel n (Independent of $\overline{\text{LDAC}}$)

Command 0011 allows the user to write to the DAC registers and update the DAC outputs directly, independent of the state of the $\overline{\text{LDAC}}$ pin.

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
C3	C2	C1	C0	DAC D	DAC C	DAC B	DAC A	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X
COMMAND				DAC ADDRESS				DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

10819-300

Figure 41. Input Shift Register Contents

I²C SLAVE ADDRESS

The AD5316R has a 7-bit I²C slave address. The five MSBs are 00011 and the two LSBs (A1 and A0) are set by the state of the A1 and A0 address pins. The ability to make hardwired changes to A1 and A0 allows the user to incorporate up to four AD5316R devices on one bus (see Table 10).

Table 10. Device Address Selection

A1 Pin Connection	A0 Pin Connection	A1 Bit	A0 Bit
GND	GND	0	0
GND	V_{LOGIC}	0	1
V_{LOGIC}	GND	1	0
V_{LOGIC}	V_{LOGIC}	1	1

SERIAL OPERATION

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address.
2. The slave device with the transmitted address responds by pulling SDA low during the 9th clock pulse (this is called the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, the input shift register.
3. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). Transitions on the SDA line must occur during the low period of SCL; SDA must remain stable during the high period of SCL.
4. After all data bits are read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and then high again during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5316R, the user must begin with a start command followed by an address byte ($R/\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5316R requires two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC with the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 42. All these data bytes are acknowledged by the AD5316R. A stop condition follows.

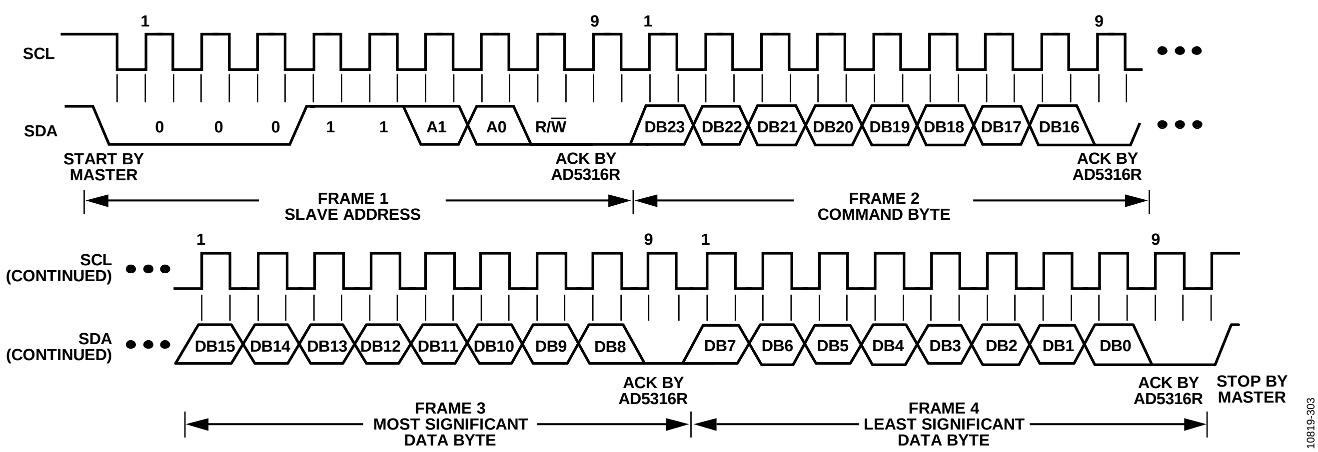


Figure 42. I²C Write Operation

READ OPERATION

When reading data back from the AD5316R, the user must begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which determines both the read command that is to follow and the pointer address to read from; the command byte is also acknowledged by the DAC. The user configures the channel to read back the contents of one or more DAC registers and sets the readback command to active using the command byte.

Following this, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 43. A NACK condition from the master, followed by a stop condition, completes the read sequence. If more than one DAC is selected, Channel A is read back by default.

MULTIPLE DAC READBACK SEQUENCE

When reading data back from multiple AD5316R DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte must be followed by the command byte, which is also acknowledged by the DAC. The user selects the first channel to read back using the command byte.

Following this, the master establishes a repeated start condition, and the address is resent with R/$\overline{W}$ = 1. This byte is acknowledged by the DAC, indicating that it is prepared to transmit data. The first two bytes of data are then read from DAC Input Register n (selected using the command byte), most significant byte first, as shown in Figure 43. The next two bytes read back are the contents of DAC Input Register n + 1, and the next bytes read back are the contents of DAC Input Register n + 2. Data is read from the DAC input registers in this autoincremented fashion until a NACK followed by a stop condition follows. If the contents of DAC Input Register D are read out, the next two bytes of data that are read are the contents of DAC Input Register A.

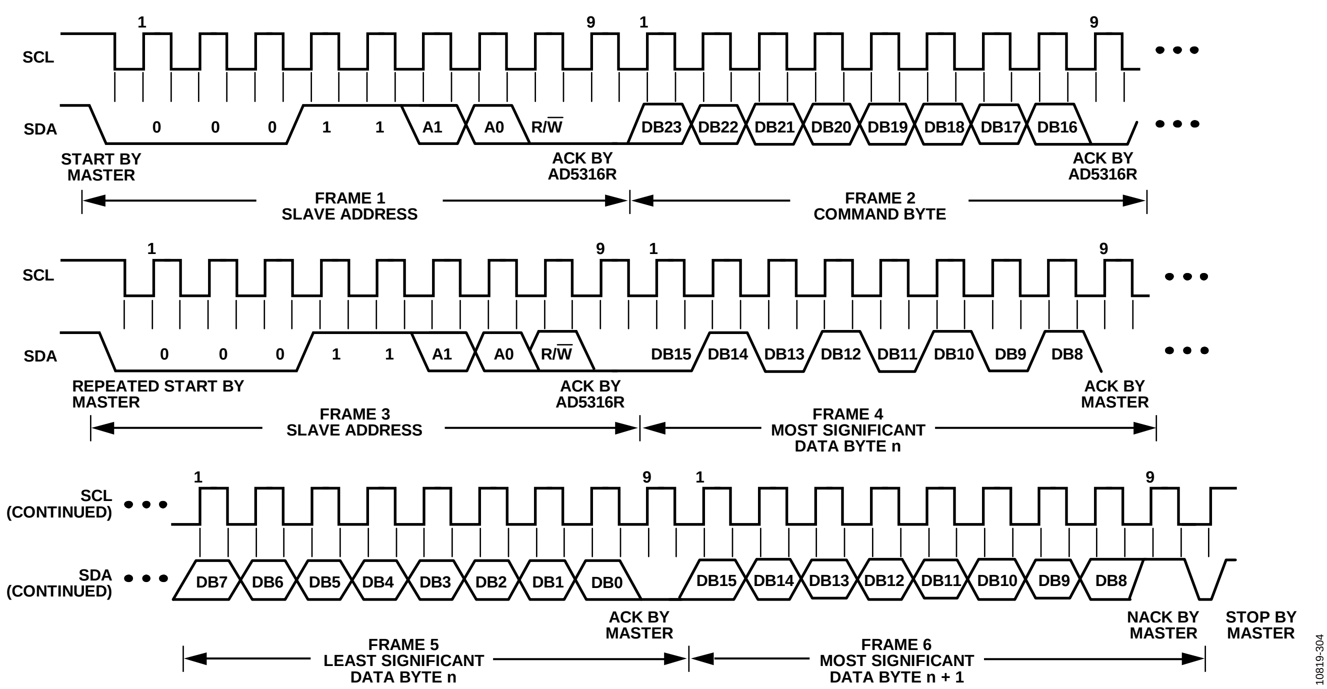


Figure 43. I²C Read Operation

POWER-DOWN OPERATION

Command 0100 is designated for the power-down function. The AD5316R provides three separate power-down modes (see Table 11). These power-down modes are software programmable by setting Bit DB7 to Bit DB0 in the input shift register (see Table 12). Two bits are associated with each DAC channel. Table 11 shows how the state of these two bits corresponds to the mode of operation of the device.

Table 11. Modes of Operation

Operating Mode	PDx1	PDx0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
100 kΩ to GND	1	0
Three-State	1	1

Any or all DACs (DAC A to DAC D) can be powered down to the selected mode by setting the corresponding bits in the input shift register. See Table 12 for the contents of the input shift register during the power-down/power-up operation.

When both Bit PDx1 and Bit PDx0 (where x is the DAC selected) in the input shift register are set to 0, the part works normally with its normal power consumption of 1.1 mA at 5 V. When Bit PDx1, Bit PDx0, or both Bit PDx1 and Bit PDx0 are set to 1, the part is in power-down mode. In power-down mode, the supply current falls to 4 µA at 5 V.

In power-down mode, the output stage is internally switched from the output of the amplifier to a resistor network of known values. In this way, the output impedance of the part is known when the part is in power-down mode.

Table 11 lists the three power-down options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 44.

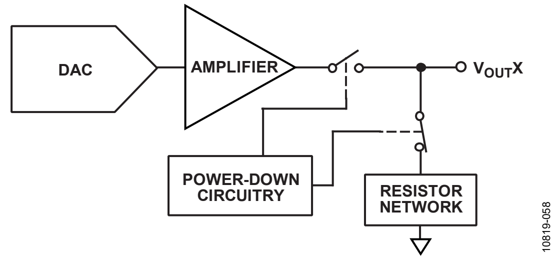


Figure 44. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the DAC registers are unaffected in power-down mode, and the DAC registers can be updated while the device is in power-down mode. The time required to exit power-down is typically 2.5 µs for V_{DD} = 5 V.

To reduce the current consumption further, the on-chip reference can be powered off (see the Internal Reference Setup section).

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5316R DAC has double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers (see Table 9). Updates to the DAC registers are controlled by the $\overline{\text{LDAC}}$ pin.

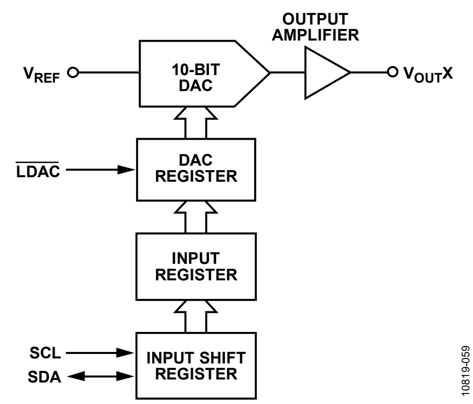


Figure 45. Simplified Diagram of Input Loading Circuitry for a Single DAC

Table 12. 24-Bit Input Shift Register Contents for Power-Down/Power-Up Operation[1]

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB16	DB15 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
0	1	0	0	X	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0
Command bits (C3 to C0)				Address bits (don't care)	Don't care	Power-down select, DAC D		Power-down select, DAC C		Power-down select, DAC B		Power-down select, DAC A	

[1] X = don't care.

Instantaneous DAC Updating (LDAC Held Low)

For instantaneous updating of the DACs, LDAC is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the 24th clock, and the output begins to change (see Table 14).

Deferred DAC Updating (LDAC Pulsed Low)

For deferred updating of the DACs, LDAC is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by pulling LDAC low after the 24th clock. The update occurs on the falling edge of LDAC.

LDAC MASK REGISTER

Command 0101 is reserved for the software LDAC function. When this command is executed, the address bits are ignored. When writing to the DAC using Command 0101, the 4-bit LDAC mask register (DB3 to DB0) is loaded. Bit DB3 of the LDAC mask register corresponds to DAC D; Bit DB2 corresponds to DAC C; Bit DB1 corresponds to DAC B; and Bit DB0 corresponds to DAC A.

The default value of these bits is 0; that is, the LDAC pin works normally. Setting any of these bits to 1 forces the selected DAC channel to ignore transitions on the LDAC pin, regardless of the state of the hardware LDAC pin. This flexibility is useful in applications where the user wishes to select which channels respond to the LDAC pin.

The LDAC mask register allows the user extra flexibility and control over the hardware LDAC pin (see Table 13). Setting the LDAC bit (DB3 to DB0) to 0 for a DAC channel allows the hardware LDAC pin to control the updating of that channel.

Table 13. LDAC Overwrite Definition

Load LDAC Register		
LDAC Bit (DB3 to DB0)	**LDAC Pin**	**LDAC Operation**
0	1 or 0	Determined by the LDAC pin.
1	X[1]	DAC channels are updated. (DAC channels see LDAC pin as 1.)

[1] X = don't care.

HARDWARE RESET PIN (RESET)

RESET is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the reset select pin (RSTSEL). It is necessary to keep RESET low for a minimum of 30 ns to complete the operation.

When the RESET signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the RESET pin is low.

There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function (see Table 8). Any events on LDAC during a power-on reset are ignored. If the RESET pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5316R contains a power-on reset circuit that controls the output voltage during power-up. When the RSTSEL pin is tied to GND, the outputs power up to zero scale (note that this is outside the linear region of the DAC). When the RSTSEL pin is tied to V_{DD}, the outputs power up to midscale. The outputs remain powered up at the level set by the RSTSEL pin until a valid write sequence is made to the DAC.

Table 14. Write Commands and LDAC Pin Truth Table[1]

Command	Description	Hardware LDAC Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on LDAC)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low transition on the hardware LDAC pin always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the LDAC mask register.
[2] When the LDAC pin is permanently tied low, the LDAC mask bits are ignored.

INTERNAL REFERENCE SETUP

By default, the internal reference is on at power-up. To reduce the supply current, the on-chip reference can be turned off. Command 0111 is reserved for setting up the internal reference. To turn off the internal reference, set the software programmable bit, DB0, in the input shift register using Command 0111, as shown in Table 16. Table 15 shows how the state of the DB0 bit corresponds to the mode of operation.

Table 15. Internal Reference Setup Register

Internal Reference Setup Register (Bit DB0)	Action
0	Reference on (default)
1	Reference off

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc., performs a reliability test called precondition to mimic the effect of soldering a device to a board. The output voltage specification in Table 2 includes the effect of this reliability test.

Figure 46 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

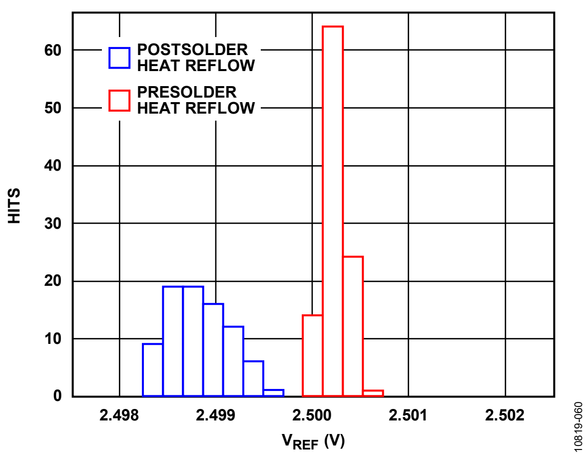


Figure 46. SHR Reference Voltage Shift

LONG-TERM TEMPERATURE DRIFT

Figure 47 shows the change in the V_{REF} (ppm) value after 1000 hours at 25°C ambient temperature.

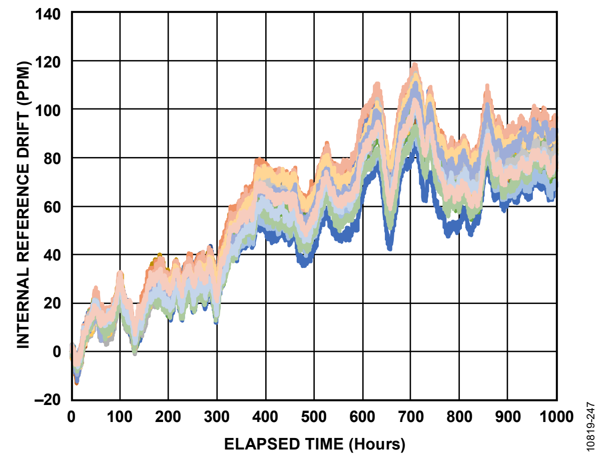


Figure 47. Reference Drift Through to 1000 Hours

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, then to hot, and then back to ambient.

Thermal hysteresis data is shown in Figure 48. It is measured by sweeping the temperature from ambient to −40°C, then to +105°C, and then back to ambient. The V_{REF} delta is then measured between the two ambient measurements (shown in blue in Figure 48). The same temperature sweep and measurements were immediately repeated, and the results are shown in red in Figure 48.

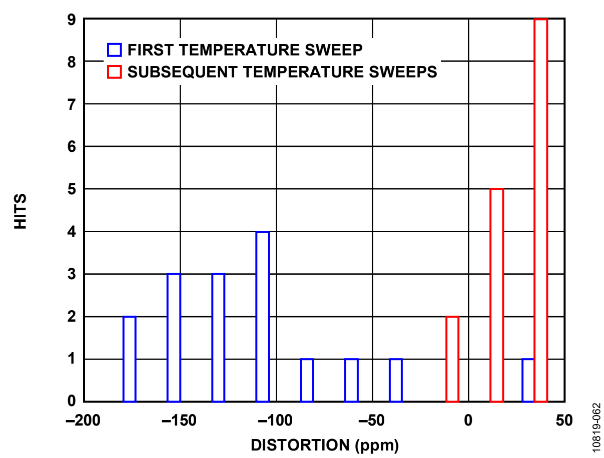


Figure 48. Thermal Hysteresis

Table 16. 24-Bit Input Shift Register Contents for Internal Reference Setup Command[1]

DB23 (MSB)	DB22	DB21	DB20	DB19 to DB16	DB15 to DB1	DB0 (LSB)
0	1	1	1	X	X	1 or 0
Command bits (C3 to C0)				Address bits (don't care)	Don't care	Reference setup register

[1] X = don't care.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5316R is via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

AD5316R TO ADSP-BF531 INTERFACE

The I²C interface of the AD5316R is designed for easy connection to industry-standard DSPs and microcontrollers. Figure 49 shows the AD5316R connected to the Analog Devices Blackfin® processor. The Blackfin processor has an integrated I²C port that can be connected directly to the I²C pins of the AD5316R.

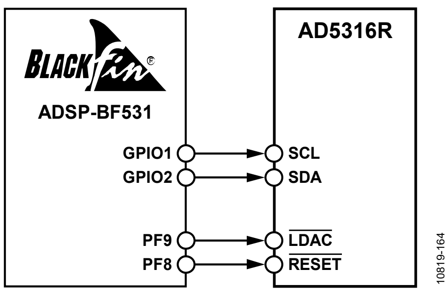


Figure 49. AD5316R to ADSP-BF531 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5316R is mounted should be designed so that the AD5316R lies on the analog plane.

The AD5316R has ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitor is the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types; these capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where many devices are on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The AD5316R LFCSP models have an exposed pad beneath the device. Connect this pad to the GND supply for the part. For optimum performance, use special considerations to design the motherboard and to mount the package.

For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the LFCSP package to the corresponding thermal land paddle on the PCB. Design thermal vias into the PCB land paddle area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 50) to provide a natural heat sinking effect.

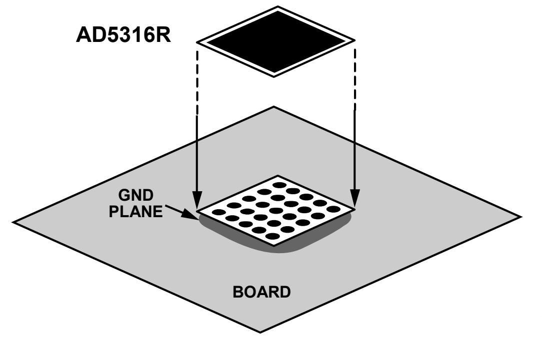


Figure 50. Paddle Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur.

The Analog Devices *i*Coupler® products provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5316R makes the device ideal for isolated interfaces as the number of interface lines is kept to a minimum. Figure 51 shows a 4-channel isolated interface to the AD5316R using the ADuM1400. For more information, visit http://www.analog.com/icouplers.

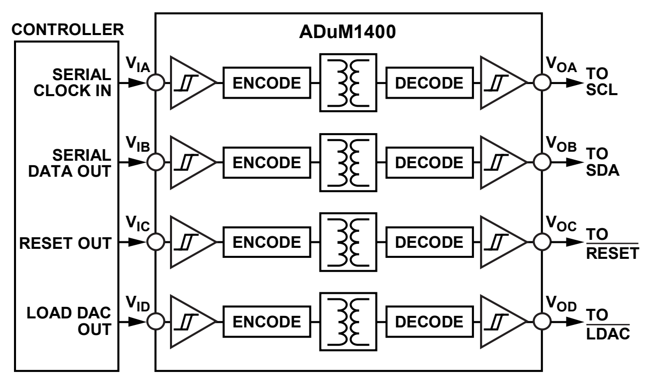


Figure 51. Isolated Interface