2.5 V to 5.5 V, 400 µA, 2-Wire Interface, Quad Voltage Output, 8-/10-/12-Bit DACs

AD5306/AD5316/AD5326

FEATURES

AD5306: 4 buffered, 8-bit DACs in 16-lead TSSOP
A version: ±1 LSB INL; B version: ±0.625 LSB INL
AD5316: 4 buffered, 10-bit DACs in 16-lead TSSOP
A version: ±4 LSB INL; B version: ±2.5 LSB INL
AD5326: 4 buffered, 12-bit DACs in 16-lead TSSOP
A version: ±16 LSB INL; B version: ±10 LSB INL
Low power operation: 400 µA @ 3 V, 500 µA @ 5 V
2-wire (I^2C®-compatible) serial interface
2.5 V to 5.5 V power supply
Guaranteed monotonic by design over all codes
Power-down to 90 nA @ 3 V, 300 nA @ 5 V ($\overline{PD}$ pin or bit)
Double-buffered input logic
Buffered/unbuffered reference input options
Output range: 0 V to V_{REF} or 0 V to 2 V_{REF}
Power-on reset to 0 V
Simultaneous update of outputs ($\overline{LDAC}$ pin)
Software clear facility
Data readback facility
On-chip rail-to-rail output buffer amplifiers
Temperature range −40°C to +105°C

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators
Industrial process control

FUNCTIONAL BLOCK DIAGRAM

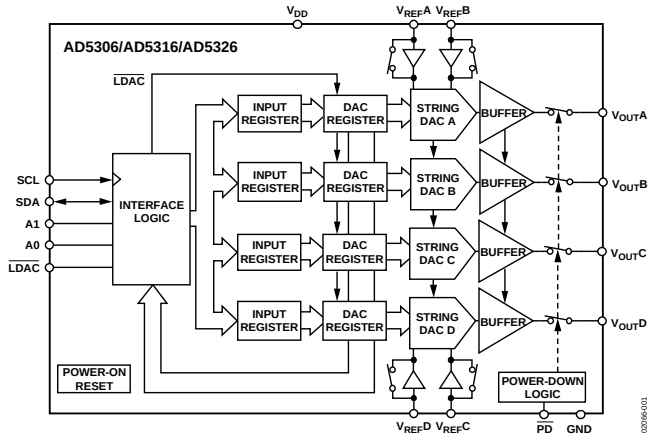

Figure 1.

GENERAL DESCRIPTION

The AD5306/AD5316/AD5326[1] are quad 8-/10-/12-bit buffered voltage output DACs in 16-lead TSSOP packages that operate from a single 2.5 V to 5.5 V supply, consuming 500 µA at 3 V. Their on-chip output amplifiers allow rail-to-rail output swing with a slew rate of 0.7 V/µs. A 2-wire serial interface, which operates at clock rates up to 400 kHz, is used. This interface is SMBus-compatible at V_{DD} < 3.6 V. Multiple devices can be placed on the same bus.

Each DAC has a separate reference input that can be configured as buffered or unbuffered. The outputs of all DACs can be updated simultaneously using the asynchronous $\overline{LDAC}$ input. The parts incorporate a power-on reset circuit that ensures the DAC outputs power up to 0 V and remain there until a valid write to the device takes place. The software clear function clears all DACs to 0 V. The parts contain a power-down feature that reduces the current consumption of the device to 300 nA @ 5 V (90 nA @ 3 V).

All three parts have the same pinout, which allows users to select the amount of resolution appropriate for their application without redesigning their circuit board.

[1] Protected by U.S. Patent Numbers 5,969,657 and 5,684,481.

Rev. F

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6/00—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Version[1]			B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[3, 4]								
AD5306								
Resolution		8			8		Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.625	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes.
AD5316								
Resolution		10			10		Bits	
Relative Accuracy		±0.5	±4		±0.5	±2.5	LSB	
Differential Nonlinearity		±0.05	±0.5		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes.
AD5326								
Resolution		12			12		Bits	
Relative Accuracy		±2	±16		±2	±10	LSB	
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	Guaranteed monotonic by design over all codes.
Offset Error		±5	±60		±5	±60	mV	V_{DD} = 4.5 V, gain = 2; see Figure 4 and Figure 5.
Gain Error		±0.3	±1.25		±0.3	±1.25	% of FSR	V_{DD} = 4.5 V, gain = 2; see Figure 4 and Figure 5.
Lower Deadband[5]		10	60		10	60	mV	See Figure 4; lower deadband exists only if offset error is negative.
Upper Deadband[5]		10	60		10	60	mV	See Figure 5; upper deadband exists only if $V_{REF} = V_{DD}$ and offset plus gain error is positive.
Offset Error Drift[6]		−12			−12		ppm of FSR/°C	
Gain Error Drift[6]		−5			−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		−60			−60		dB	ΔV_{DD} = ±10%.
DC Crosstalk[6]		200			200		µV	R_L = 2 kΩ to GND or V_{DD}.
DAC REFERENCE INPUTS[6]								
V_{REF} Input Range	1		V_{DD}	1		V_{DD}	V	Buffered reference mode.
	0.25		V_{DD}	0.25		V_{DD}	V	Unbuffered reference mode.
V_{REF} Input Impedance		>10			>10		MΩ	Buffered reference mode and power-down mode.
	148	180		148	180		kΩ	Unbuffered reference mode; 0 V to V_{REF} output range.
	74	90		74	90		kΩ	Unbuffered reference mode; 0 V to 2 V_{REF} output range.
Reference Feedthrough		−90			−90		dB	Frequency = 10 kHz.
Channel-to-Channel Isolation		−75			−75		dB	Frequency = 10 kHz.
OUTPUT CHARACTERISTICS[6]								
Minimum Output Voltage[7]		0.001			0.001		V	This is a measure of the minimum and maximum drive capability of the output amplifier.
Maximum Output Voltage[7]		V_{DD} − 0.001			V_{DD} − 0.001		V	
DC Output Impedance		0.5			0.5		Ω	

Parameter[2]	A Version[1] Min	A Version[1] Typ	A Version[1] Max	B Version[1] Min	B Version[1] Typ	B Version[1] Max	Unit	Conditions/Comments
Short-Circuit Current		25			25		mA	V_{DD} = 5 V.
		16			16		mA	V_{DD} = 3 V.
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode; V_{DD} = 5 V.
		5			5		µs	Coming out of power-down mode; V_{DD} = 3 V.
LOGIC INPUTS (Excluding SCL, SDA)[6]								
Input Current			±1			±1	µA	
V_{IL}, Input Low Voltage			0.8			0.8	V	V_{DD} = 5 V ± 10%.
			0.6			0.6	V	V_{DD} = 3 V ± 10%.
			0.5			0.5	V	V_{DD} = 2.5 V.
V_{IH}, Input High Voltage	1.7			1.7			V	V_{DD} = 2.5 V to 5.5 V; TTL and 1.8 V CMOS compatible.
Pin Capacitance		3			3		pF	
LOGIC INPUTS (SCL, SDA)[6]								
V_{IH}, Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	0.7 V_{DD}		V_{DD} + 0.3	V	SMBus compatible at V_{DD} < 3.6 V.
V_{IL}, Input Low Voltage	−0.3		+0.3 V_{DD}	−0.3		+0.3 V_{DD}	V	SMBus compatible at V_{DD} < 3.6 V.
I_{IN}, Input Leakage Current			±1			±1	µA	
V_{HYST}, Input Hysteresis	0.05 V_{DD}			0.05 V_{DD}			V	See Figure 20.
C_{IN}, Input Capacitance		8			8		pF	
Glitch Rejection			50			50	ns	Input filtering suppresses noise spikes of less than 50 ns.
LOGIC OUTPUT (SDA)[6]								
V_{OL}, Output Low Voltage			0.4			0.4	V	I_{SINK} = 3 mA.
			0.6			0.6	V	I_{SINK} = 6 mA.
Three-State Leakage Current			±1			±1	µA	
Three-State Output Capacitance		8			8		pF	
POWER REQUIREMENTS								
V_{DD}	2.5		5.5	2.5		5.5	V	
I_{DD} (Normal Mode)[8]								V_{IH} = V_{DD} and V_{IL} = GND; interface inactive.
V_{DD} = 4.5 V to 5.5 V		500	900		500	900	µA	All DACs in unbuffered mode. Buffered mode, extra current is typically x mA per DAC, where x = 5 µA + V_{REF}/R_{DAC}.
V_{DD} = 2.5 V to 3.6 V		400	750		400	750	µA	
I_{DD} (Power-Down Mode)								V_{IH} = V_{DD} and V_{IL} = GND; interface inactive.
V_{DD} = 4.5 V to 5.5 V		0.3	1		0.3	1	µA	I_{DD} = 3 µA (max) during readback on SDA.
V_{DD} = 2.5 V to 3.6 V		0.09	1		0.09	1	µA	I_{DD} = 1.5 µA (max) during readback on SDA.

[1] Temperature range (A, B versions): −40°C to +105°C; typical at +25°C.
[2] See the Terminology section.
[3] DC specifications tested with the outputs unloaded.
[4] Linearity is tested using a reduced code range: AD5306 (Code 8 to 255); AD5316 (Code 28 to 1023); AD5326 (Code 115 to 4095).
[5] This corresponds to x codes. x = deadband voltage/LSB size.
[6] Guaranteed by design and characterization; not production tested.
[7] For the amplifier output to reach its minimum voltage, the offset error must be negative; for the amplifier output to reach its maximum voltage, V_{REF} = V_{DD}, the offset plus gain error must be positive.
[8] Interface inactive; all DACs active. DAC outputs unloaded.

AC CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A, B Versions[1, 2]				
Parameter[3]	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
AD5306		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0)
AD5316		7	9	µs	1/4 scale to 3/4 scale change (0x100 to 0x300)
AD5326		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p, unbuffered mode
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] Temperature range (A, B versions): −40°C to +105°C; typical at +25°C.
[3] See the Terminology section.

TIMING CHARACTERISTICS[1]

V_{DD} = 2.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[2]	A, B Versions Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	
t_7	0.6	µs min	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	250	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1C_B[4]	ns min	t_F, fall time of SCL and SDA when transmitting
t_{12}	20	ns min	$\overline{\text{LDAC}}$ pulse width
t_{13}	400	ns min	SCL rising edge to $\overline{\text{LDAC}}$ rising edge
C_B[4]	400	pF max	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization; not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of SCL's falling edge.
[4] C_B is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.

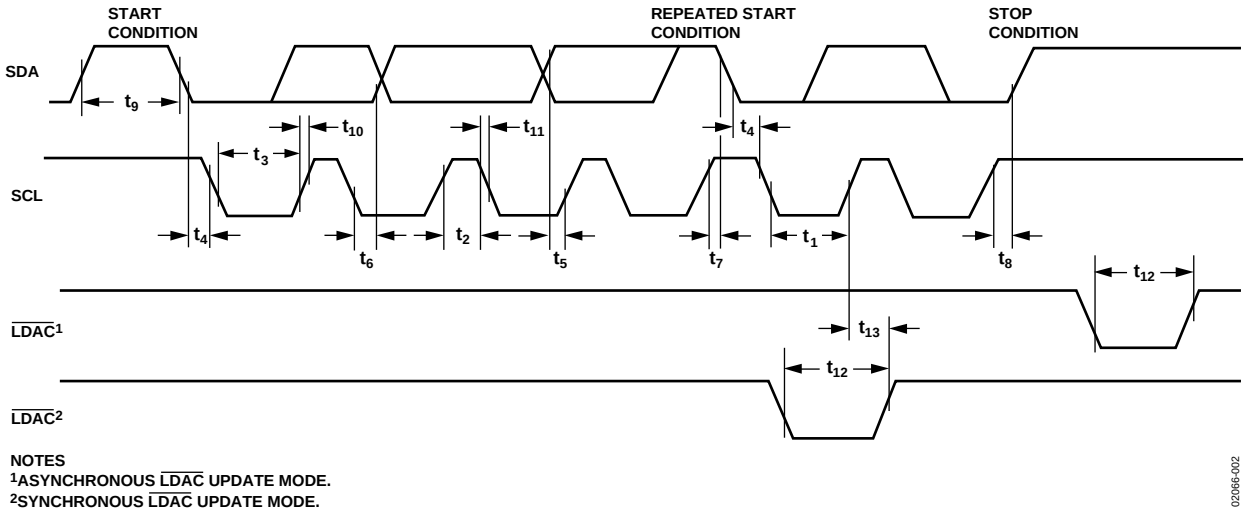

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter[1]	Value
V_{DD} to GND	−0.3 V to +7 V
SCL, SDA to GND	−0.3 V to V_{DD} + 0.3 V
A0, A1, $\overline{LDAC}$, $\overline{PD}$ to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT}A to V_{OUT}D to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A, B Versions)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
16-Lead TSSOP	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering	
Peak Temperature	220°C
Time at Peak Temperature	10 sec to 40 sec

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

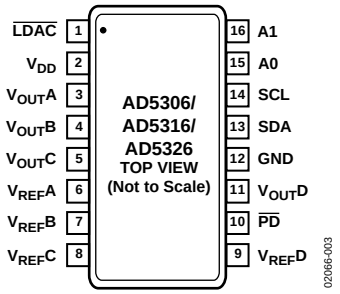

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Active Low Control Input. Transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows simultaneous update of all DAC outputs. Alternatively, this pin can be tied permanently low.
2	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V and the supply should be decoupled with a10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
3	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
4	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
6	$V_{REF}A$	Reference Input Pin for DAC A. This pin can be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC A. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
7	$V_{REF}B$	Reference Input Pin for DAC B. This pin can be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC B. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
8	$V_{REF}C$	Reference Input Pin for DAC C. This pin can be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC C. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
9	$V_{REF}D$	Reference Input Pin for DAC D. This pin can be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC D. It has an input range from 0.25 V to V_{DD} in unbuffered mode and from 1 V to V_{DD} in buffered mode.
10	$\overline{\text{PD}}$	Active Low Control Input. Acts as a hardware power-down option. All DACs go into power-down mode when this pin is tied low. The DAC outputs go into a high impedance state. The current consumption of the part drops to 300 nA @ 5 V (90 nA @ 3 V).
11	$V_{OUT}D$	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
12	GND	Ground Reference Point for All Circuitry on the Part.
13	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 16-bit input shift register. It is a bidirectional open-drain data line that should be pulled to the supply with an external pull-up resistor.
14	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400 kbps can be accommodated in the I^2C-compatible interface.
15	A0	Address Input. Sets the LSB of the 7-bit slave address.
16	A1	Address Input. Sets the second LSB of the 7-bit slave address.

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, it is a measure, in LSB, of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Typical INL vs. code plots are shown in Figure 6, Figure 7, and Figure 8.

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. code plots are shown in Figure 9, Figure 10, and Figure 11.

Offset Error
A measure of the offset error of the DAC and the output amplifier. It can be positive or negative. See Figure 4 and Figure 5. Offset error is expressed in mV.

Gain Error
A measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift
A measure of the change in offset error with changes in temperature. Offset error drift is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
A measure of the change in gain error with changes in temperature. Gain error drift is expressed in (ppm of full-scale range)/°C.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. PSRR is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied 10%.

DC Crosstalk
The dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s, and vice versa) and output change of another DAC. DC crosstalk is expressed in μV.

Reference Feedthrough
The ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated, that is, when $\overline{\text{LDAC}}$ is high. Reference feedthrough is expressed in dB.

Channel-to-Channel Isolation
The ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. Channel-to-channel isolation is measured in dB.

Major-Code Transition Glitch Energy
The energy of the impulse injected into the analog output when the code in the DAC register changes state. This energy is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

Digital Feedthrough
A measure of the impulse injected into the analog output of a DAC from the digital input pins of the device when the DAC output is not being updated. Digital feedthrough is specified in nV-s and is measured with a worst-case change on the digital input pins (that is, from all 0s to all 1s, and vice versa).

Digital Crosstalk
The glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s, and vice versa) in the input register of another DAC. The energy of the glitch is expressed in nV-s.

Analog Crosstalk
The glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. Analog crosstalk is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s, and vice versa) while keeping $\overline{\text{LDAC}}$ high and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The energy of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
The glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. Crosstalk is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s, and vice versa) with $\overline{\text{LDAC}}$ low and then monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
The difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. THD is measured in dB.

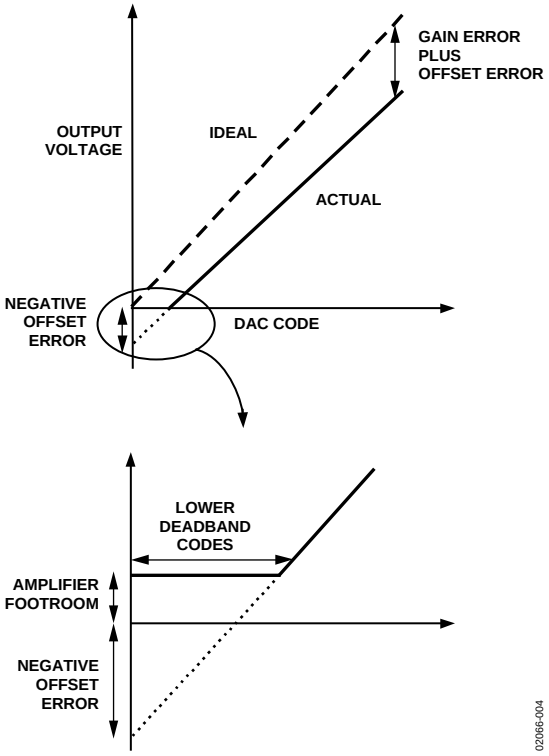

Figure 4. Transfer Function with Negative Offset

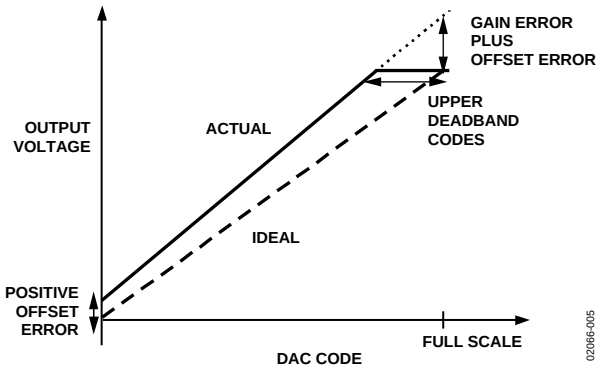

Figure 5. Transfer Function with Positive Offset ($V_{REF} = V_{DD}$)

TYPICAL PERFORMANCE CHARACTERISTICS

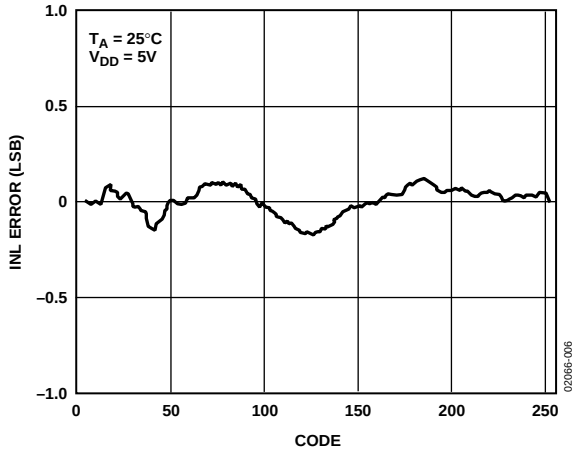

Figure 6. AD5306 INL

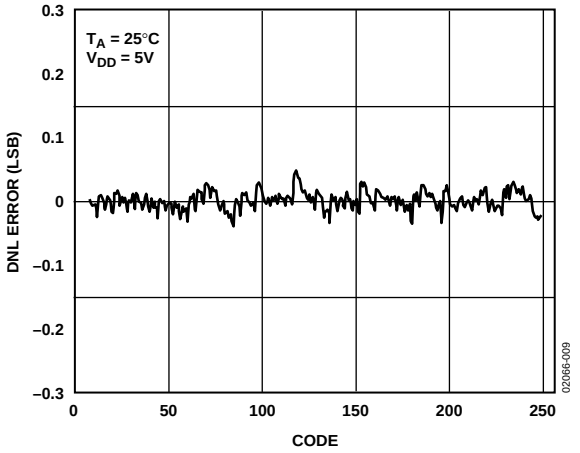

Figure 9. AD5306 DNL

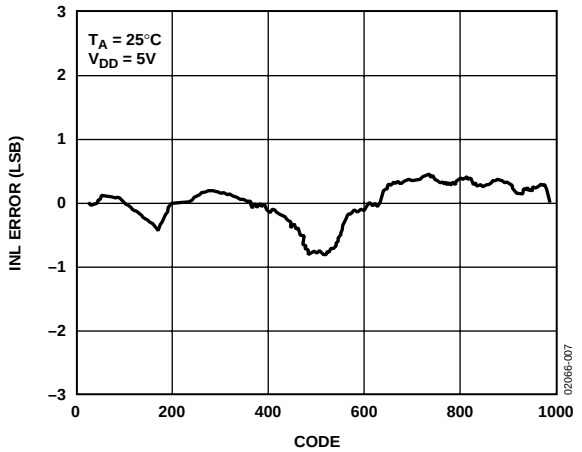

Figure 7. AD5316 INL

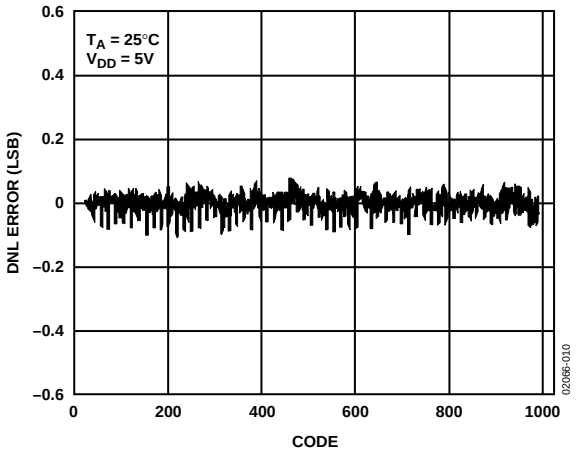

Figure 10. AD5316 DNL

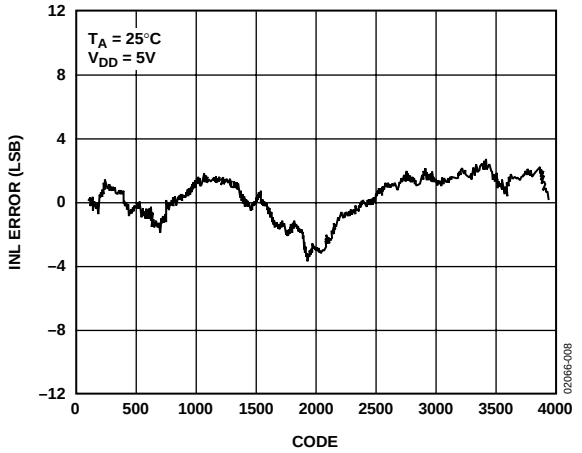

Figure 8. AD5326 INL

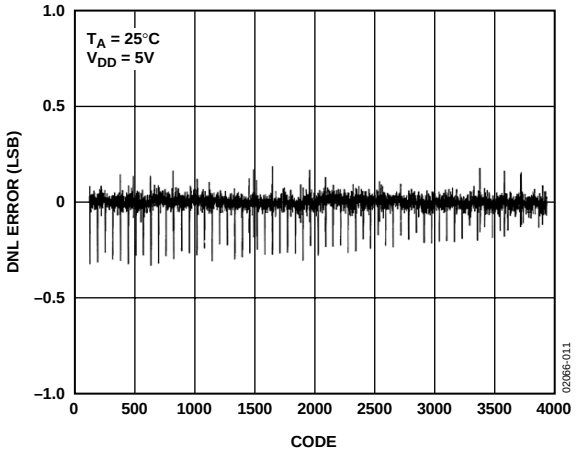

Figure 11. AD5326 DNL

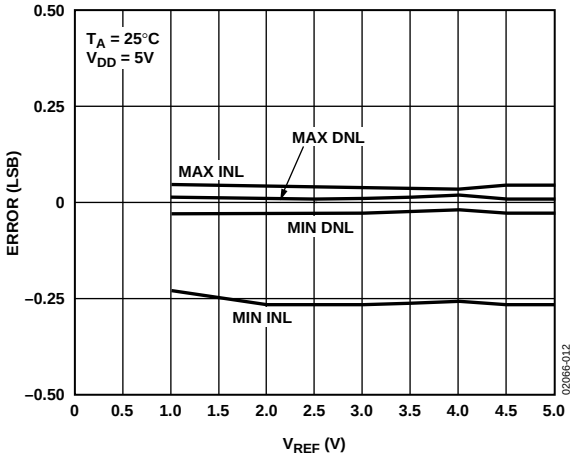

Figure 12. AD5306 INL and DNL Error vs. V_{REF}

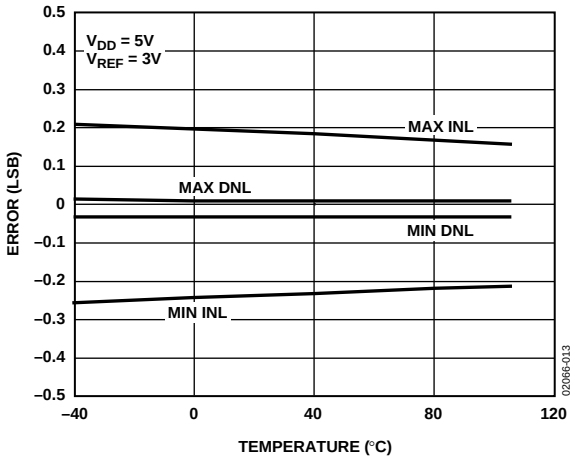

Figure 13. AD5306 INL and DNL Error vs. Temperature

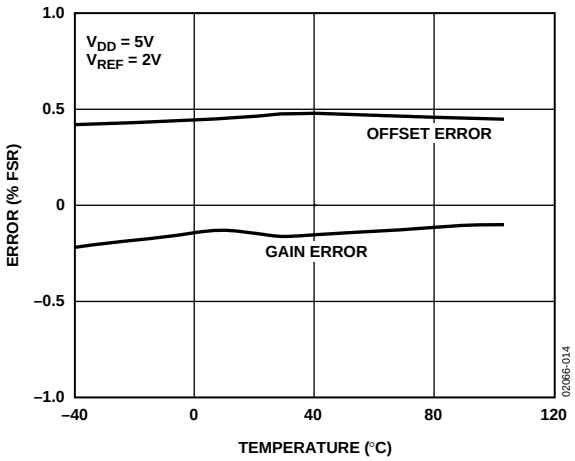

Figure 14. AD5306 Offset Error and Gain Error vs. Temperature

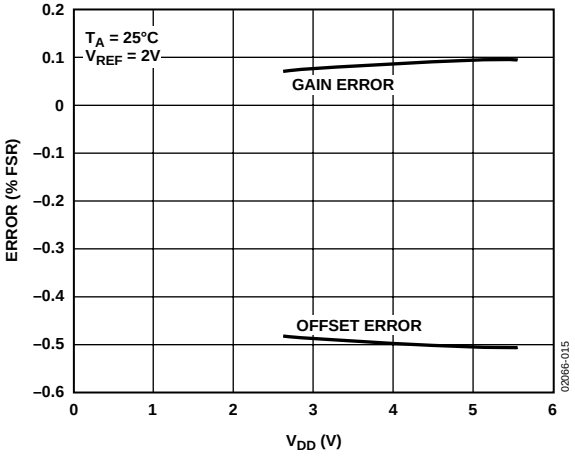

Figure 15. Offset Error and Gain Error vs. V_{DD}

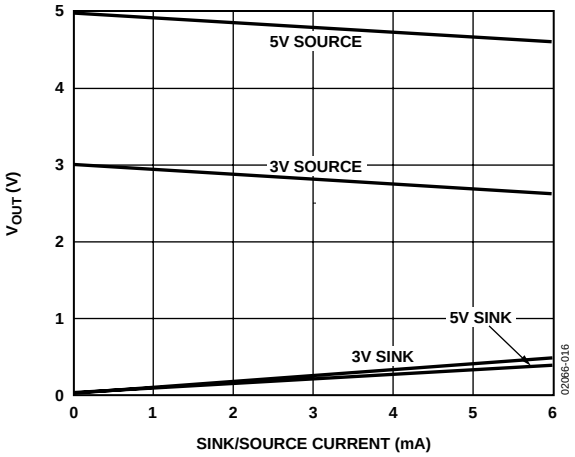

Figure 16. V_{OUT} vs. Source and Sink Current Capability

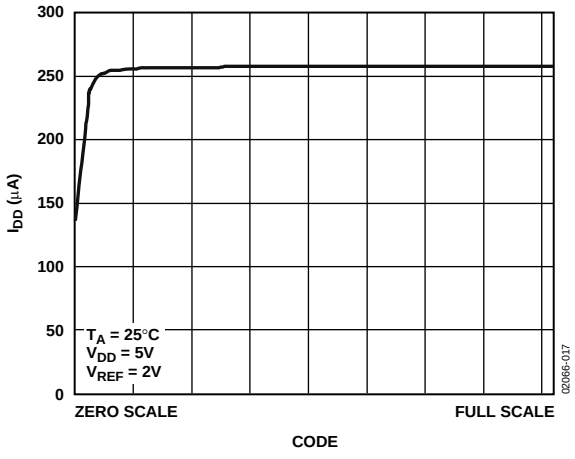

Figure 17. Supply Current vs. DAC Code

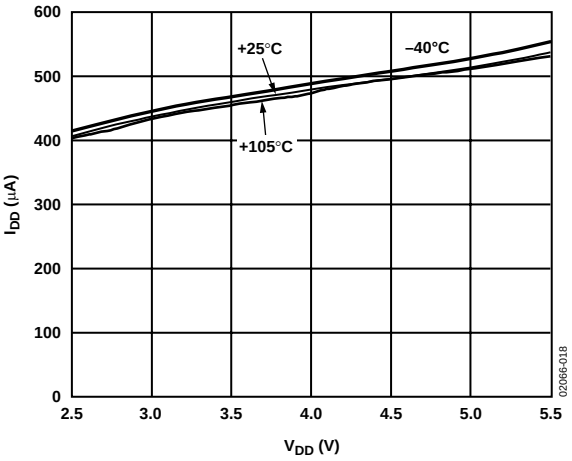

Figure 18. Supply Current vs. Supply Voltage

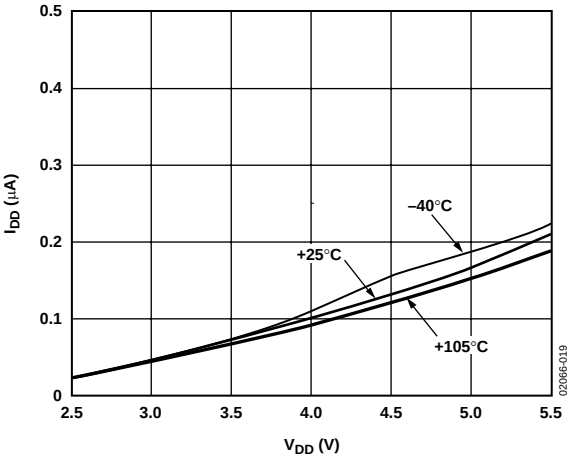

Figure 19. Power-Down Current vs. Supply Voltage

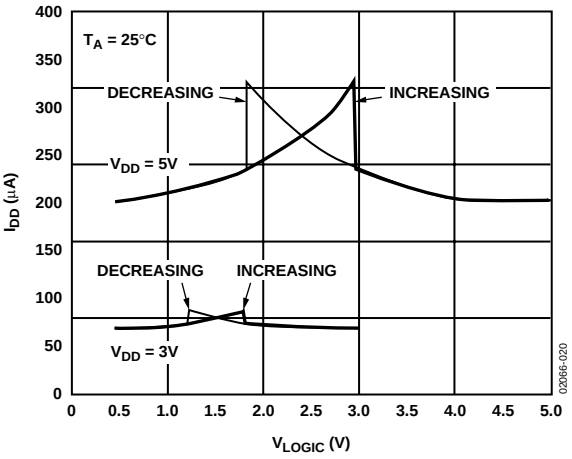

Figure 20. Supply Current vs. Logic Input Voltage for SDA and SCL Voltage Increasing and Decreasing

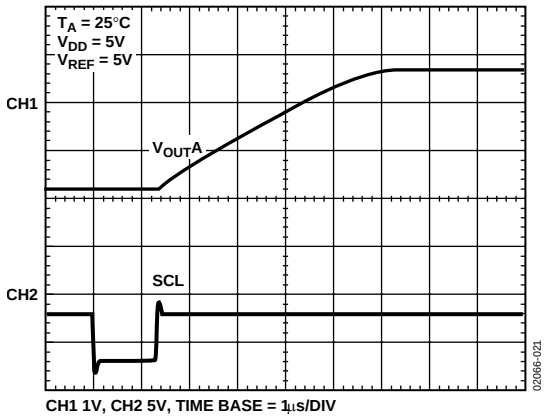

Figure 21. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

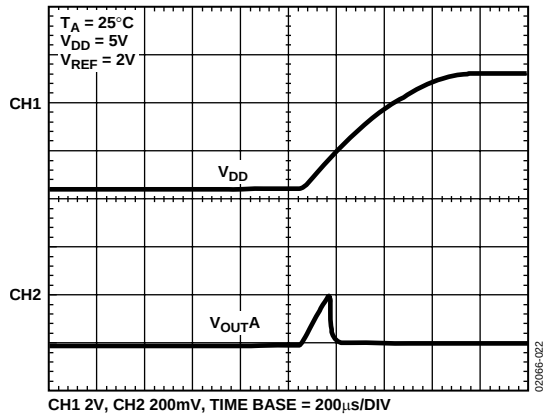

Figure 22. Power-On Reset to 0 V

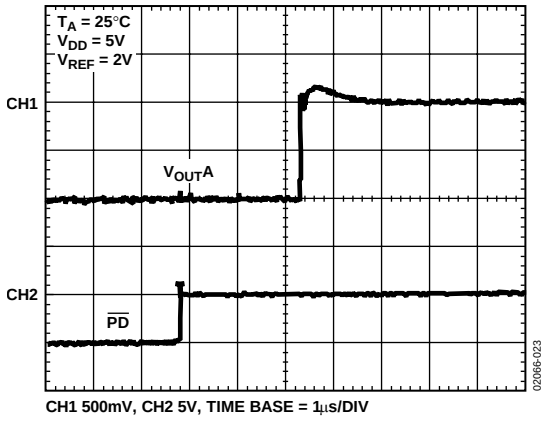

Figure 23. Exiting Power-Down to Midscale

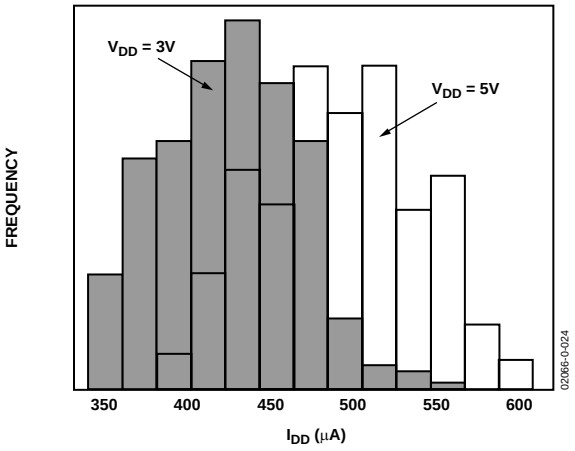

Figure 24. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

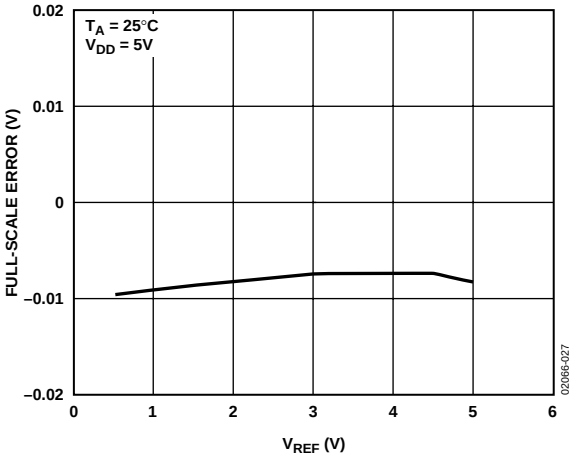

Figure 27. Full-Scale Error vs. V_{REF}

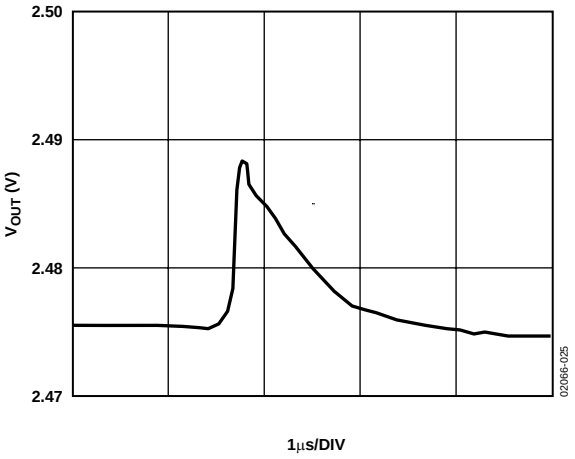

Figure 25. AD5326 Major Code Transition Glitch Energy

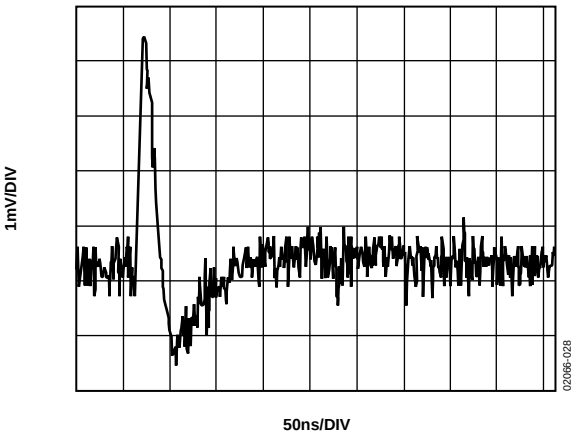

Figure 28. DAC-to-DAC Crosstalk

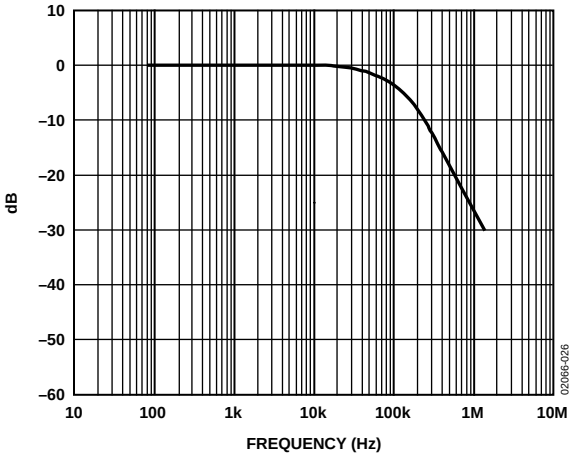

Figure 26. Multiplying Bandwidth (Small-Signal Frequency Response)

FUNCTIONAL DESCRIPTION

The AD5306/AD5316/AD5326 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. Each contains four output buffer amplifiers and is written to via a 2-wire serial interface. They operate from single supplies of 2.5 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. Each DAC is provided with a separate reference input, which can be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from 0.25 V to V_{DD}. The devices have a power-down mode in which all DACs can be turned off completely with a high impedance output.

DIGITAL-TO-ANALOG SECTION

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the corresponding DAC. Figure 29 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal equivalent of the binary code that is loaded to the DAC register:

0 to 255 for AD5306 (8 bits)
0 to 1023 for AD5316 (10 bits)
0 to 4095 for AD5326 (12 bits)

N is the DAC resolution.

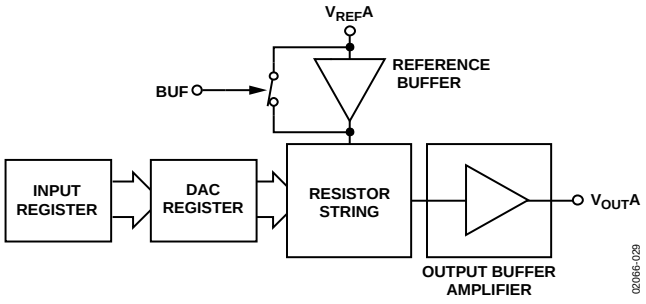

Figure 29. Single DAC Channel Architecture

RESISTOR STRING

The resistor string section is shown in Figure 30. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

DAC REFERENCE INPUTS

Each of the four DACs has a reference pin. The reference inputs are buffered but can also be individually configured as unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However, if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V_{DD}, since there is no restriction due to headroom and footroom of the reference amplifier.

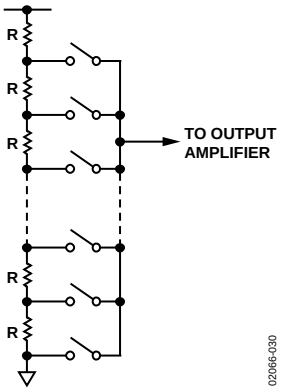

Figure 30. Resistor String

If there is a buffered reference in the circuit (for example, REF192), there is no need to use the on-chip buffers of the AD5306/AD5316/AD5326. In unbuffered mode, the input impedance is still large at typically 180 kΩ per reference input for 0 V to V_{REF} mode and 90 kΩ for 0 V to 2 V_{REF} mode.

The buffered/unbuffered option is controlled by the BUF bit in the control byte. The BUF bit setting applies to whichever DAC is selected in the pointer byte.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on the value of V_{REF}, GAIN, offset error, and gain error. If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 V_{REF}. Because of clamping, however, the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD} in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in the plot in Figure 16.

The slew rate is 0.7 V/µs with a half-scale settling time to 0.5 LSB (at eight bits) of 6 µs.

POWER-ON RESET

The AD5306/AD5316/AD5326 have a power-on reset function so that they power up in a defined state. The power-on state is

- Normal operation
- Reference inputs unbuffered
- 0 V to V_{REF} output range
- Output voltage set to 0 V

Both input and DAC registers are filled with 0s and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

SERIAL INTERFACE

The AD5306/AD5316/AD5326 are controlled via an I²C-compatible serial bus. These devices are connected to this bus as slave devices; that is, no clock is generated by the AD5306/AD5316/AD5326 DACs. This interface is SMBus-compatible at V_{DD} < 3.6 V.

The AD5306/AD5316/AD5326 has a 7-bit slave address. The five MSBs are 00011, and the two LSBs are determined by the state of the A0 and A1 pins. The facility to make hardwired changes to A0 and A1 allows the user to have up to four of these devices on one bus.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit. This bit determines whether data is read from or written to the slave device.

   The slave whose address corresponds to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read from or written to, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse; that is, the SDA line remains high. The master then brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a stop condition.

READ/WRITE SEQUENCE

For the AD5306/AD5316/AD5326, all write access sequences and most read sequences begin with the device address (with R/$\overline{W}$ = 0) followed by the pointer byte. This pointer byte specifies the data format and determines that DAC is being accessed in the subsequent read/write operation (see Figure 1). In a write operation, the data follows immediately. In a read operation, the address is resent with R/$\overline{W}$ = 1, and the data is then read back. However, it is also possible to perform a read operation by sending only the address with R/$\overline{W}$ = 1. The previously loaded pointer settings are then used for the readback operation.

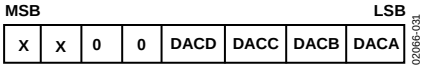

Figure 31. Pointer Byte

POINTER BYTE BITS

Table 6 describes the individual bits that make up the pointer byte.

Table 6. Pointer Byte Bits

Bit	Description
X	Don't care bits.
0	Reserved bits. Must be set to 0.
DACD	1: The following data bytes are for DAC D.
DACC	1: The following data bytes are for DAC C.
DACB	1: The following data bytes are for DAC B.
DACA	1: The following data bytes are for DAC A.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide. Data is loaded into the device as two data bytes on the serial data line, SDA, under the control of the serial clock input, SCL. The timing diagram for this operation is shown in Figure 2. The two data bytes consist of four control bits followed by 8, 10, or 12 bits of DAC data, depending on the device type. The first bits loaded are the control bits: GAIN, BUF, $\overline{CLR}$, and $\overline{PD}$; the remaining bits are left-justified DAC data bits, starting with the MSB (see Figure 32).

Table 7. Input Shift Register Control Bits

Bit	Description
GAIN	0: Output range for that DAC set at 0 V to V_{REF}. 1: Output range for that DAC set at 0 V to 2 V_{REF}.
BUF	0: Reference input for that DAC is unbuffered. 1: Reference input for that DAC is buffered.
$\overline{CLR}$	0: All DAC registers and input registers are filled with 0s on completion of the write sequence. 1: Normal operation.
$\overline{PD}$	0: On completion of the write sequence, all four DACs go into power-down mode. The DAC outputs enter a high impedance state. 1: Normal operation.

DEFAULT READBACK CONDITIONS

All pointer byte bits power up to 0. Therefore, if the user initiates a readback without first writing to the pointer byte, no single DAC channel has been specified. In this case, the default readback bits are all 0 except for the $\overline{CLR}$ bit and the $\overline{PD}$ bit, which are 1.

MULTIPLE DAC WRITE SEQUENCE

Because there are individual bits in the pointer byte for each DAC, it is possible to write the same data and control bits to two, three, or four DACs simultaneously by setting the relevant bits to 1.

MULTIPLE DAC READBACK SEQUENCE

If the user attempts to read back data from more than one DAC at a time, the part reads back the power-on condition of GAIN, BUF, and data bits (all 0), and the current state of $\overline{CLR}$ and $\overline{PD}$.

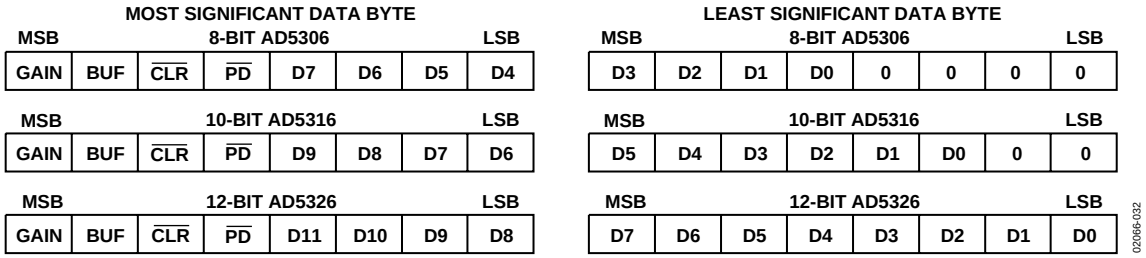

Figure 32. Data Formats for Write and Readback

WRITE OPERATION

When writing to the AD5306/AD5316/AD5326 DACs, the user must begin with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte is followed by the pointer byte, which is also acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 33. A stop condition follows.

READ OPERATION

When reading data back from the AD5306/AD5316/AD5326 DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte is usually followed by the pointer byte, which is also acknowledged by the DAC. Following this, there is a repeated start condition by the master, and the address is resent with R/$\overline{W}$ = 1. This is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 34. A stop condition follows.

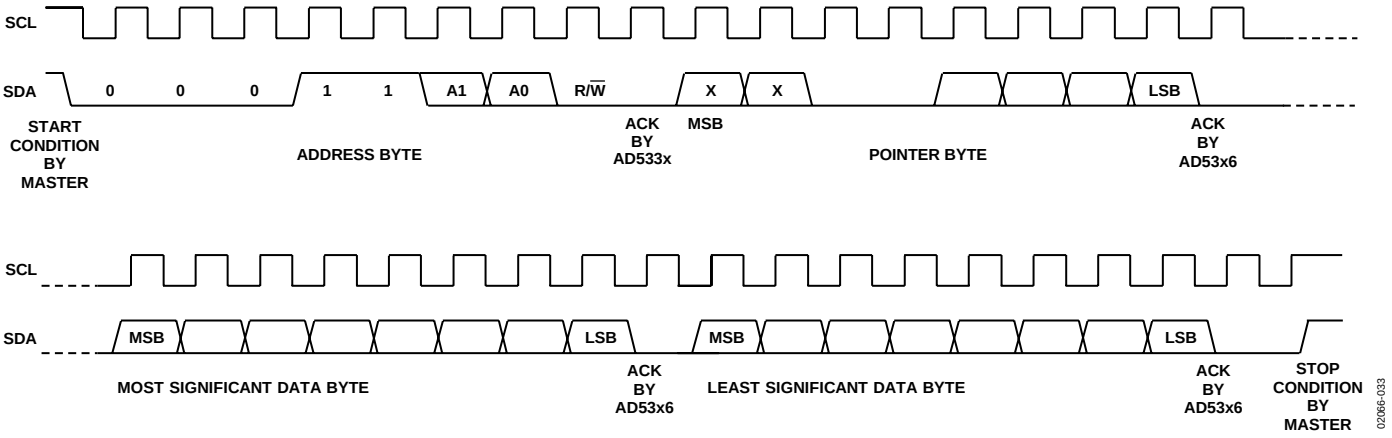

Figure 33. Write Sequence

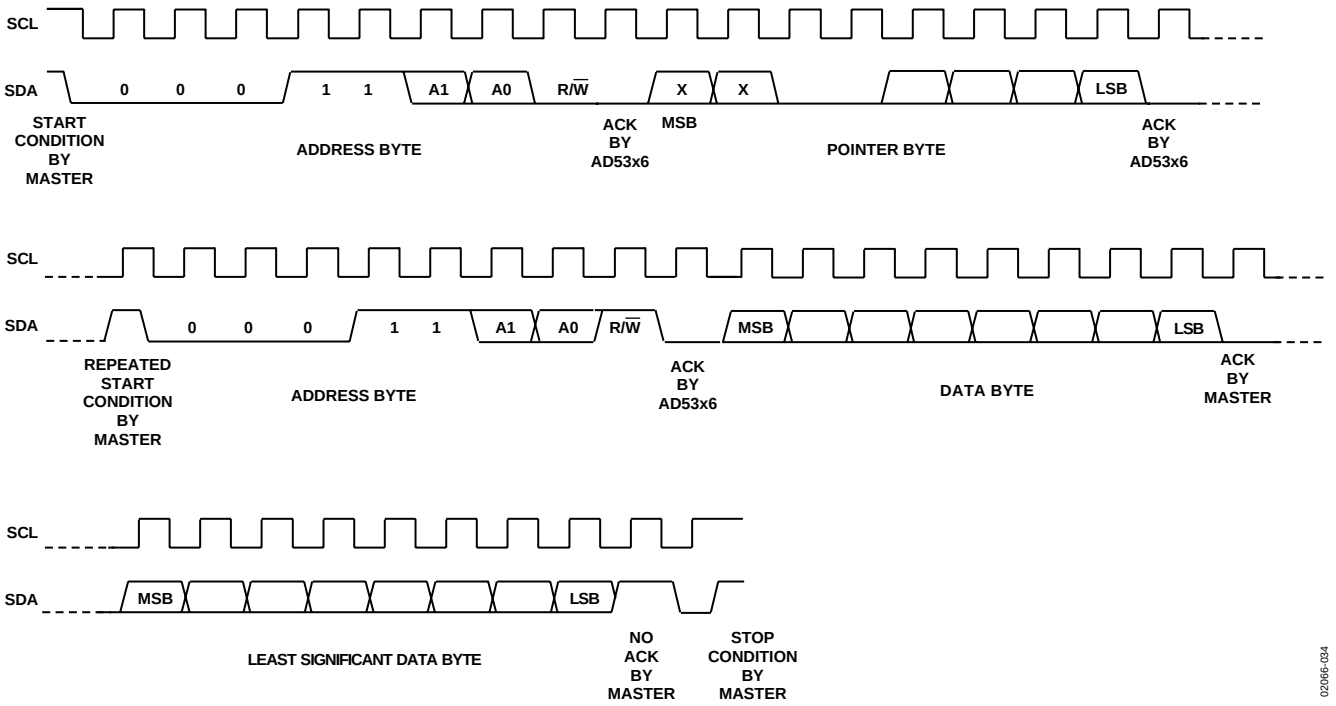

Figure 34. Readback Sequence

However, if the master sends an ACK and continues clocking SCL (no stop is sent), the DAC retransmits the same two bytes of data on SDA. This allows continuous readback of data from the selected DAC register.

Alternatively, the user can send a start followed by the address with R/$\overline{W}$ = 1. In this case, the previously loaded pointer settings are used and readback of data can start immediately.

DOUBLE-BUFFERED INTERFACE

The AD5306/AD5316/AD5326 DACs have double-buffered interfaces consisting of two banks of registers: input registers and DAC registers. The input registers are connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC registers contain the digital code used by the resistor strings.

Access to the DAC registers is controlled by the $\overline{\text{LDAC}}$ pin. When $\overline{\text{LDAC}}$ is high, the DAC registers are latched and the input registers can change state without affecting the contents of the DAC registers. When $\overline{\text{LDAC}}$ is low, however, the DAC registers become transparent and the contents of the input registers are transferred to them.

Double-buffering is useful if the user requires simultaneous updating of all DAC outputs. The user may write to each of the input registers individually and then, by pulsing the $\overline{\text{LDAC}}$ input low, all outputs update simultaneously.

These parts contain an extra feature whereby a DAC register is not updated unless its input register has been updated since the last time that $\overline{\text{LDAC}}$ was low. Normally, when $\overline{\text{LDAC}}$ is low, the DAC registers are filled with the contents of the input registers. In the AD5306/AD5316/AD5326, the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

LOAD DAC INPUT $\overline{\text{LDAC}}$

$\overline{\text{LDAC}}$ transfers data from the input registers to the DAC registers and, therefore, updates the outputs. The $\overline{\text{LDAC}}$ function enables double-buffering of the DAC data, GAIN, and BUF. There are two $\overline{\text{LDAC}}$ modes: synchronous mode and asynchronous mode.

In synchronous mode, the DAC registers are updated after new data is read in on the rising edge of the eighth SCL pulse. $\overline{\text{LDAC}}$ can be tied permanently low or pulsed as in Figure 2.

In asynchronous mode, the outputs are not updated at the same time the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input registers.

POWER-DOWN MODE

The AD5306/AD5316/AD5326 have very low power consumption, dissipating typically at 1.2 mW with a 3 V supply and 2.5 mW with a 5 V supply. Power consumption can be reduced further when the DACs are not in use by putting them into power-down mode, which is selected by setting the $\overline{\text{PD}}$ pin low or by setting Bit 12 ($\overline{\text{PD}}$) of the data-word to 0.

When the $\overline{\text{PD}}$ pin is high and the $\overline{\text{PD}}$ bit is set to 1, all DACs work normally with a typical power consumption of 500 μA at 5 V (400 μA at 3 V). In power-down mode, however, the supply current falls to 300 nA at 5 V (90 nA at 3 V) when all DACs are powered down. Not only does the supply current drop, but each output stage is internally switched from the output of its amplifier, making it open-circuit. This has the advantage that the outputs are three-state while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifiers. The output stage is shown in Figure 35.

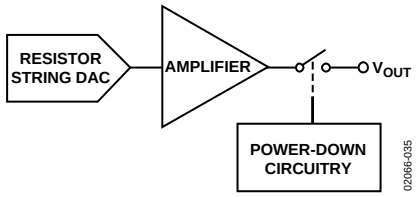

Figure 35. Output Stage During Power-Down

The bias generator, output amplifiers, resistor strings, and all other associated linear circuitry are shut down when power-down mode is activated. However, the contents of the registers are unaffected when in power-down. In fact, it is possible to load new data into the input registers and DAC registers during power-down. The DAC outputs update as soon as the $\overline{\text{PD}}$ pin goes high or the $\overline{\text{PD}}$ bit is reset to 1. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs for V_{DD} = 3 V. This is the time from the rising edge of the eighth SCL pulse or from the rising edge of $\overline{\text{PD}}$ to when the output voltage deviates from its power-down voltage (see Figure 23).

APPLICATIONS

TYPICAL APPLICATION CIRCUIT

The AD5306/AD5316/AD5326 can be used with a wide range of reference voltages where the devices offer full one-quadrant multiplying capability over a reference range of 0 V to V_{DD}. More typically, these devices are used with a fixed precision-reference voltage. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference is the AD589, a 1.23 V band gap reference. Figure 36 shows a typical setup for the AD5306/AD5316/AD5326 when using an external reference. Note that A0 and A1 can be high or low.

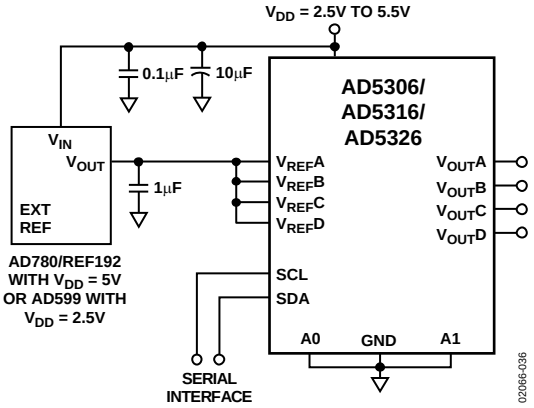

Figure 36. AD5306/AD5316/AD5326 Using a 2.5 V External Reference

DRIVING V_{DD} FROM THE REFERENCE VOLTAGE

If an output range of 0 V to V_{DD} is required when the reference inputs are configured as unbuffered, the simplest solution is to connect the reference inputs to V_{DD}. Because this supply may be noisy and somewhat inaccurate, the AD5306/AD5316/AD5326 may be powered from the reference voltage, for example, using a 5 V reference such as the REF195. The REF195 outputs a steady supply voltage for the AD5306/AD5316/AD5326. The typical current required from the REF195 is 500 µA supply current and approximately 112 µA to supply the reference inputs, if unbuffered. This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10 kΩ load on each output) is

612 µA + (5 V/10 kΩ) = 2.6 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 5.2 ppm (26 µV) for the 2.6 mA current drawn from it. This corresponds to a 0.0013 LSB error at eight bits and a 0.021 LSB error at 12 bits.

BIPOLAR OPERATION USING THE AD5306/AD5316/AD5326

The AD5306/AD5316/AD5326 are designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 37. This circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

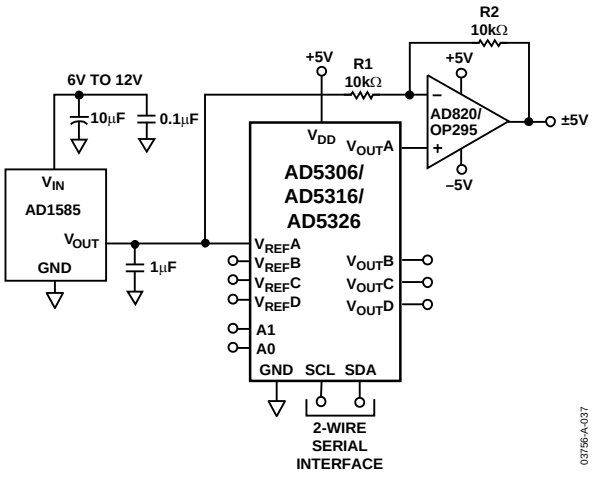

Figure 37. Bipolar Operation with the AD5306/AD5316/AD5326

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = \left[\frac{\left(REFIN \times D / 2^N\right) \times \left(R1 + R2\right)}{R1}\right] - REFIN \times \left(R2 / R1\right)$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
REFIN is the reference voltage input.

With *REFIN* = 5 V, *R1* = *R2* = 10 kΩ,

$$V_{OUT} = (10 \times D/2^N) - 5 \text{ V}$$

MULTIPLE DEVICES ON ONE BUS

Figure 38 shows four AD5306 devices on the same serial bus. Each has a different slave address since the states of the A0 and A1 pins are different. This allows each of 16 DACs to be written to or read from independently.

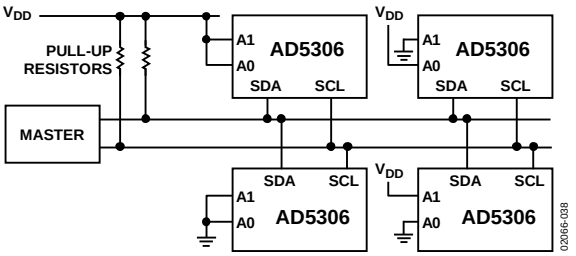

Figure 38. Multiple AD5306 Devices on One Bus

AD5306/AD5316/AD5326 AS A DIGITALLY PROGRAMMABLE WINDOW DETECTOR

A digitally programmable upper/lower limit detector using two of the DACs in the AD5306/AD5316/AD5326 is shown in Figure 39. The upper and lower limits for the test are loaded to DACs A and B, which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, an LED indicates the fail condition. Similarly, DAC C and DAC D can be used for window detection on a second V_{IN} signal.

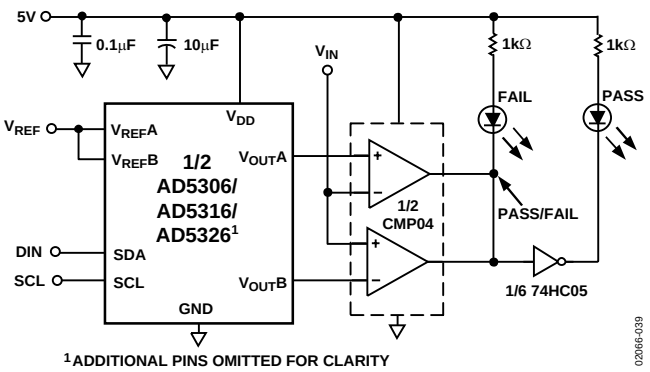

Figure 39. Window Detection

COARSE AND FINE ADJUSTMENT USING THE AD5306/AD5316/AD5326

Two of the DACs in the AD5306/AD5316/AD5326 can be paired together to form a coarse and fine adjustment function, as shown in Figure 40. DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 changes the relative effect of the coarse and fine adjustments. With the resistor values and external reference shown, the output amplifier has unity gain for the DAC A output; therefore, the output range is 0 V to 2.5 V − 1 LSB. For DAC B, the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range of 19 mV. Similarly, DAC C and DAC D can be paired together for coarse and fine adjustment.

The circuit in Figure 40 is shown with a 2.5 V reference, but reference voltages up to V_{DD} may be used. The op amps indicated allow a rail-to-rail output swing.

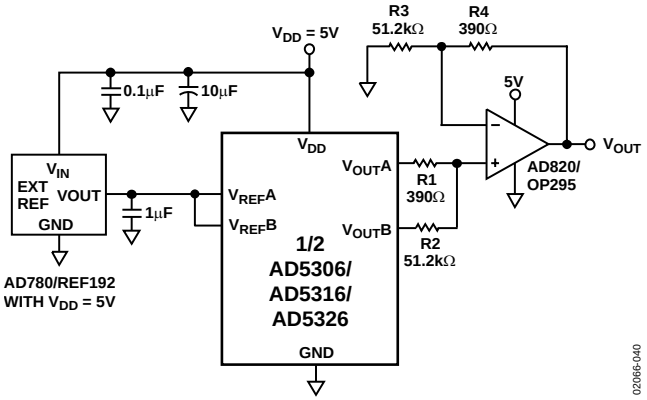

Figure 40. Coarse/Fine Adjustment

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5306/AD5316/AD5326 is mounted should be designed so the analog and digital sections are separated and confined to certain areas of the board.

If the AD5306/AD5316/AD5326 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. The AD5306/AD5316/AD5326 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5306/AD5316/AD5326 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Components with fast-switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other parts of the board, and they should never be run near the reference inputs. A ground line routed between the SDA and SCL lines helps to reduce crosstalk between them. Although a ground line is not required on a multilayer board because there is a separate ground plane, separating the lines helps.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is the best method, but its use is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

Table 8. Overview of AD53xx Serial Devices[1]

Part No.	Resolution	No. of DACs	DNL	Interface	Settling Time (µs)	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI	4	SOT-23, MSOP	6, 8
AD5310	10	1	±0.5	SPI	6	SOT-23, MSOP	6, 8
AD5320	12	1	±1.0	SPI	8	SOT-23, MSOP	6, 8
AD5301	8	1	±0.25	2-wire	6	SOT-23, MSOP	6, 8
AD5311	10	1	±0.5	2-wire	7	SOT-23, MSOP	6, 8
AD5321	12	1	±1.0	2-wire	8	SOT-23, MSOP	6, 8
DUALS							
AD5302	8	2	±0.25	SPI	6	MSOP	8
AD5312	10	2	±0.5	SPI	7	MSOP	8
AD5322	12	2	±1.0	SPI	8	MSOP	8
AD5303	8	2	±0.25	SPI	6	TSSOP	16
AD5313	10	2	±0.5	SPI	7	TSSOP	16
AD5323	12	2	±1.0	SPI	8	TSSOP	16
QUADS							
AD5304	8	4	±0.25	SPI	6	MSOP	10
AD5314	10	4	±0.5	SPI	7	MSOP	10
AD5324	12	4	±1.0	SPI	8	MSOP	10
AD5305	8	4	±0.25	2-Wire	6	MSOP	10
AD5315	10	4	±0.5	2-Wire	7	MSOP	10
AD5325	12	4	±1.0	2-Wire	8	MSOP	10
AD5306	8	4	±0.25	2-Wire	6	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8	TSSOP	16
AD5307	8	4	±0.25	SPI	6	TSSOP	16
AD5317	10	4	±0.5	SPI	7	TSSOP	16
AD5327	12	4	±1.0	SPI	8	TSSOP	16
OCTALS							
AD5308	8	8	±0.25	SPI	6	TSSOP	16
AD5318	10	8	±0.5	SPI	7	TSSOP	16
AD5328	12	8	±1.0	SPI	8	TSSOP	16

[1] Visit www.analog.com/support/standard_linear/selection_guides/AD53xx.html for more information.

Table 9. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time (µs)	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6	Yes	Yes		Yes	TSSOP	20
AD5331	10	±0.5	1	7		Yes		Yes	TSSOP	20
AD5340	12	±1.0	1	8	Yes	Yes		Yes	TSSOP	24
AD5341	12	±1.0	1	8	Yes	Yes	Yes	Yes	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6				Yes	TSSOP	20
AD5333	10	±0.5	2	7	Yes	Yes		Yes	TSSOP	24
AD5342	12	±1.0	2	8	Yes	Yes		Yes	TSSOP	28
AD5343	12	±1.0	1	8			Yes	Yes	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6		Yes		Yes	TSSOP	24
AD5335	10	±0.5	2	7			Yes	Yes	TSSOP	24
AD5336	10	±0.5	4	7		Yes		Yes	TSSOP	28
AD5344	12	±1.0	4	8					TSSOP	28