Current Output/Serial Input, 16-/14-Bit DACs

Data Sheet

AD5543/AD5553

FEATURES

- 16-bit resolution AD5543
- 14-bit resolution AD5553
- ±1 LSB DNL
- ±1 LSB INL
- Low noise: 12 nV/√Hz
- Low power: I_{DD} = 10 µA
- 0.5 µs settling time
- 4-quadrant multiplying reference input
- 2 mA full-scale current ± 20%, with V_{REF} = 10 V
- Built-in R_{FB} facilitates voltage conversion
- 3-wire interface
- Ultracompact 8-lead MSOP and 8-lead SOIC packages

APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Industrial control programmable logic controllers

GENERAL DESCRIPTION

The AD5543/AD5553 are precision 16-/14-bit, low power, current output, small form factor digital-to-analog converters (DACs). They are designed to operate from a single 5 V supply with a ±10 V multiplying reference.

The applied external reference, V_{REF}, determines the full-scale output current. An internal feedback resistor (R_{FB}) facilitates the R-2R and temperature tracking for voltage conversion when combined with an external operational amplifier.

A serial data interface offers high speed, 3-wire microcontroller-compatible inputs using serial data in (SDI), clock (CLK), and chip select ($\overline{CS}$).

The AD5543/AD5553 are packaged in ultracompact (3 mm × 4.7 mm) 8-lead MSOP and 8-lead SOIC packages.

FUNCTIONAL BLOCK DIAGRAM

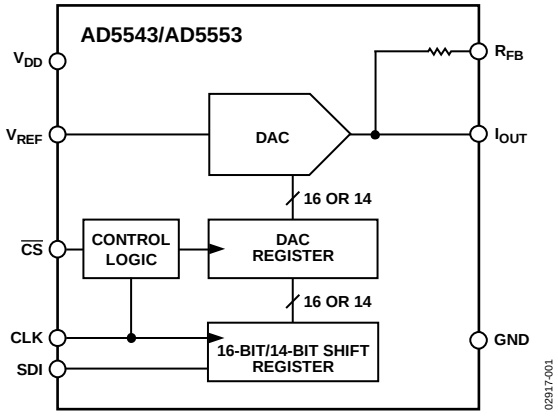

Figure 1.

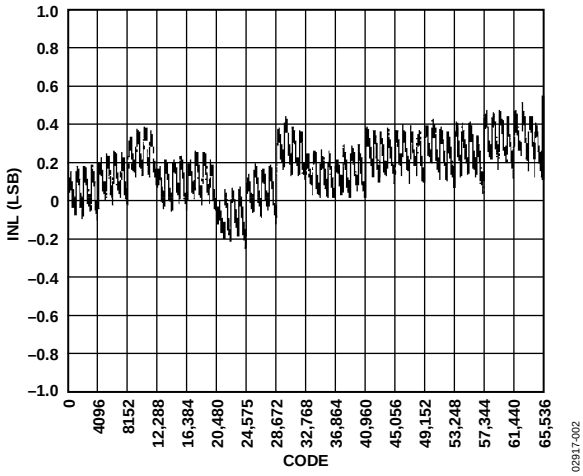

Figure 2. Integral Nonlinearity (INL)

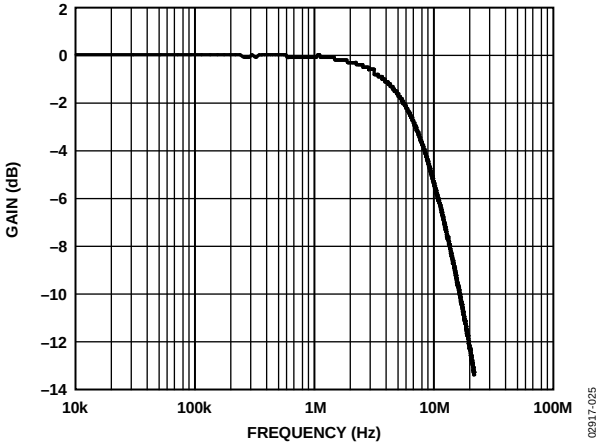

Figure 3. Reference Multiplying Bandwidth

Rev. H Document Feedback

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4/2010—Rev. C to Rev. D

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10/2009—Rev. B to Rev. C

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7/2009—Rev. A to Rev. B

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2/2003—Rev. 0 to Rev. A

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12/2002—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, I_{OUT} = virtual GND, GND = 0 V, V_{REF} = 10 V, T_A = full operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	5 V ± 10%	Unit
STATIC PERFORMANCE[1]				
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153 µV when V_{REF} = 10 V (AD5543)	16	Bits
		1 LSB = $V_{REF}/2^{14}$ = 610 µV when V_{REF} = 10 V (AD5553)	14	Bits
Relative Accuracy	INL	Grade: AD5553C	±1	LSB max
		Grade: AD5543C	±1	LSB max
		Grade: AD5543B	±2	LSB max
Differential Nonlinearity (DNL)	DNL	Monotonic	±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0x0000, T_A = 25°C	10	nA max
		Data = 0x0000, T_A = T_A maximum	20	nA max
Full-Scale Gain Error	G_{FSE}	Data = 0xFFFF	±1/±4	mV typ/max
Full-Scale Temperature Coefficient[2]	TCV_{FS}		1	ppm/°C typ
REFERENCE INPUT				
V_{REF} Range	V_{REF}		−15/+15	V min/max
Input Resistance	R_{REF}		5	kΩ typ[3]
Input Capacitance[2]	C_{REF}		5	pF typ
ANALOG OUTPUT				
Output Current	I_{OUT}	Data = 0xFFFF for AD5543	2	mA typ
		Data = 0x3FFF for AD5553		
Output Capacitance[2]	C_{OUT}	Code dependent	200	pF typ
LOGIC INPUTS AND OUTPUT				
Logic Input Low Voltage	V_{IL}		0.8	V max
Logic Input High Voltage	V_{IH}		2.4	V min
Input Leakage Current	I_{IL}		10	µA max
Input Capacitance[2]	C_{IL}		10	pF max
INTERFACE TIMING[2, 4]		See Figure 4 and Figure 5		
Clock Input Frequency	f_{CLK}		50	MHz
Clock Width High	t_{CH}		10	ns min
Clock Width Low	t_{CL}		10	ns min
$\overline{CS}$ to Clock Setup	t_{CSS}		0	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		10	ns min
Data Setup	t_{DS}		5	ns min
Data Hold	t_{DH}		10	ns min
SUPPLY CHARACTERISTICS				
Power Supply Range	$V_{DD\ RANGE}$		4.5/5.5	V min/max
Positive Supply Current	I_{DD}	Logic inputs = 0 V	10	µA max
Power Dissipation	P_{DISS}	Logic inputs = 0 V	0.055	mW max
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%	0.006	%/% max

Parameter	Symbol	Test Conditions/Comments	5 V ± 10%	Unit
AC CHARACTERISTICS[4]				
Output Voltage Settling Time	t_S	To ±0.1% of full scale, Data = 0x0000 to 0xFFFF to 0x0000 for AD5543 Data = 0x0000 to 0x3FFF to 0x0000 for AD5553	0.5	µs typ
Reference Multiplying Bandwidth (BW)	BW	V_{REF} = 100 mV rms, data = 0xFFFF	6.6	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0 V, data = 0x7FFF to 0x8000 for AD5543	7	nV-sec
Feedthrough Error	V_{OUT}/V_{REF}	Data = 0x0000, V_{REF} = 100 mV rms, same channel	−83	dB
Digital Feedthrough	Q	C_S = 1 and f_{CLK} = 1 MHz	7	nV-sec
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, data = 0xFFFF, f = 1 kHz	−103	dB typ
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz	12	nV/√Hz

[1] All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5543 R_{FB} terminal is tied to the amplifier output. The +IN operational amplifier is grounded, and the DAC I_{OUT} is tied to the −IN operational amplifier. Typical values represent average readings measured at 25°C.
[2] These parameters are guaranteed by design and are not subject to production testing.
[3] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier except for THD where an AD8065 was used.
[4] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

TIMING DIAGRAMS

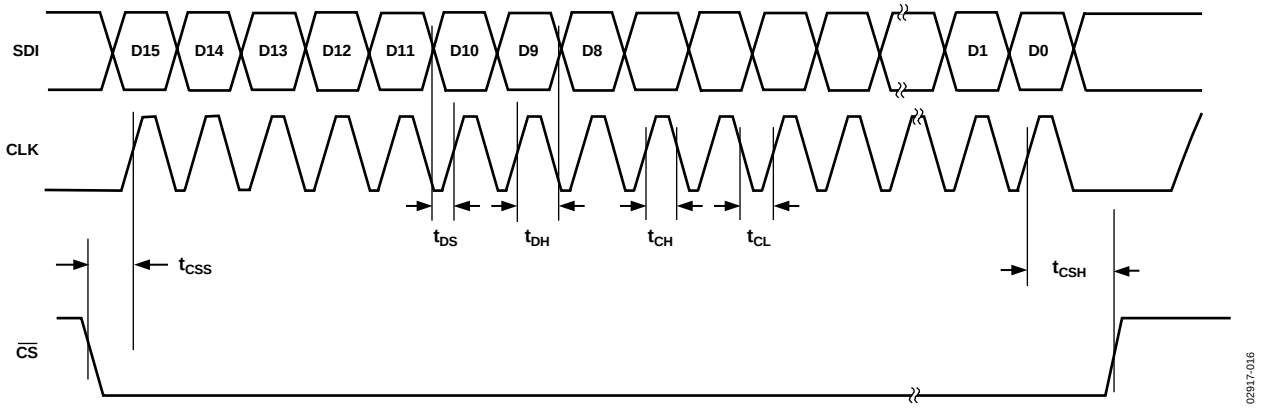


Figure 4. AD5543 Timing Diagram

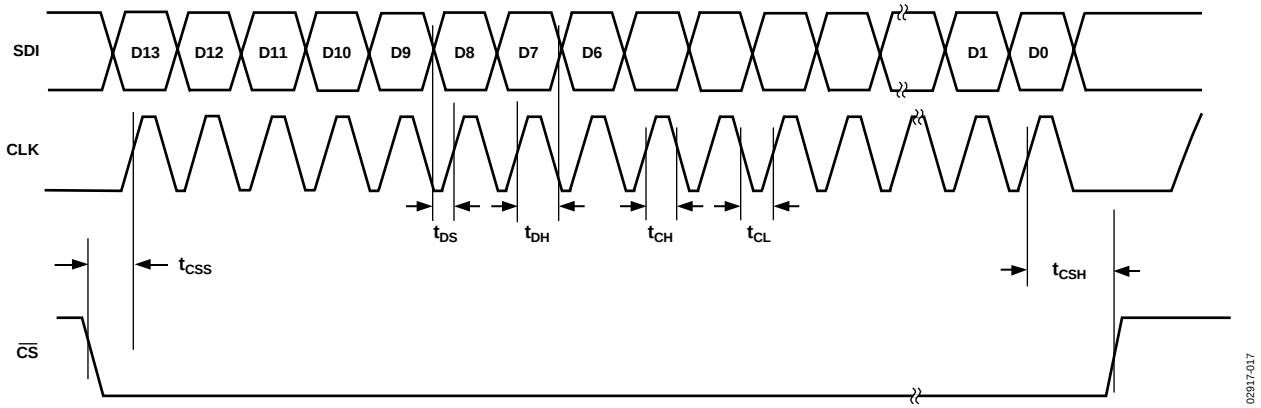


Figure 5. AD5553 Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +8 V
V_{REF} to GND	−18 V to +18 V
Logic Inputs to GND	−0.3 V to +8 V
V(I_{OUT}) to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies	±50 mA
Package Power Dissipation	$(T_{J\,Max} - T_A)/\theta_{JA}$
Thermal Resistance, θ_{JA}	
8-Lead Surface Mount (MSOP)	150°C/W
8-Lead Surface Mount (SOIC)	100°C/W
Maximum Junction Temperature ($T_{J\,Max}$)	150°C
Operating Temperature Range	
Model B and Model C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
R-8, RM-8 (Vapor Phase, 60 sec)	215°C
R-8, RM-8 (Infrared, 15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

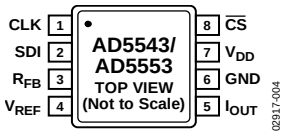


Figure 6. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input. Positive edge triggered, clocks data into shift register.
2	SDI	Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R_{FB}	Internal Matching Feedback Resistor. This pin connects to an external operational amplifier for voltage output.
4	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code.
5	I_{OUT}	DAC Current Output. This pin connects to the inverting terminal of the external precision I-to-V operational amplifier for voltage output.
6	GND	Analog and Digital Ground.
7	V_{DD}	Positive Power Supply Input. Specified range of operation at 5 V ± 10%.
8	$\overline{CS}$	Chip Select. Active low digital input. Transfers shift register data to DAC register on rising edge. See Table 4 for operation.

Table 4. Control Logic Truth Table

CLK	$\overline{CS}$	Serial Shift Register Function	DAC Register
X	H	No effect	Latched
↑+[1]	L	Shift register data advanced one bit	Latched
X[1]	H	No effect	Latched
X[1]	↑+[1]	Shift register data transferred to DAC register	New data loaded from serial register

[1] ↑+ = positive logic transition; X means don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

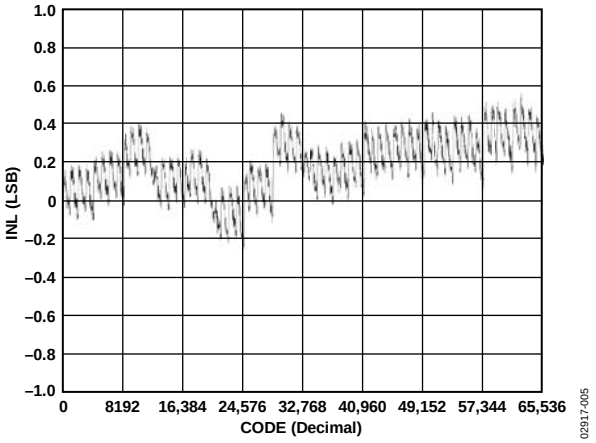


Figure 7. AD5543 INL Error

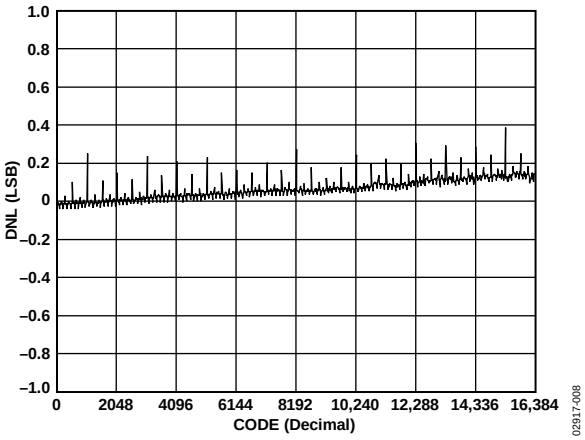


Figure 10. AD5553 DNL Error

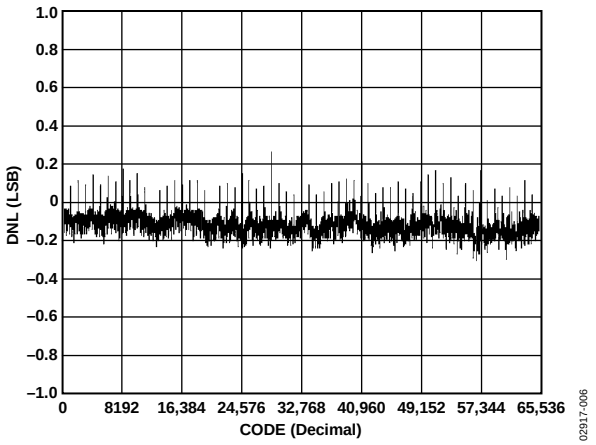


Figure 8. AD5543 DNL Error

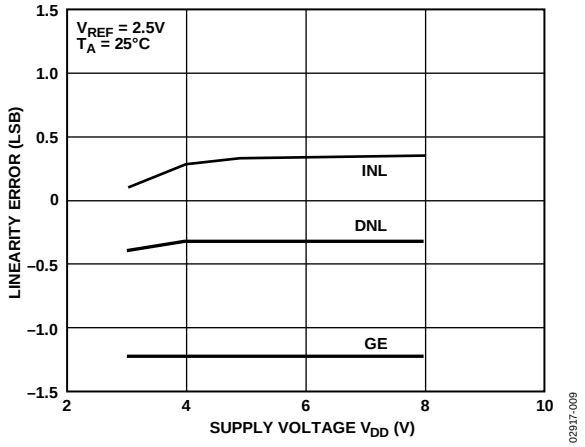


Figure 11. Linearity Error vs. V_{DD}

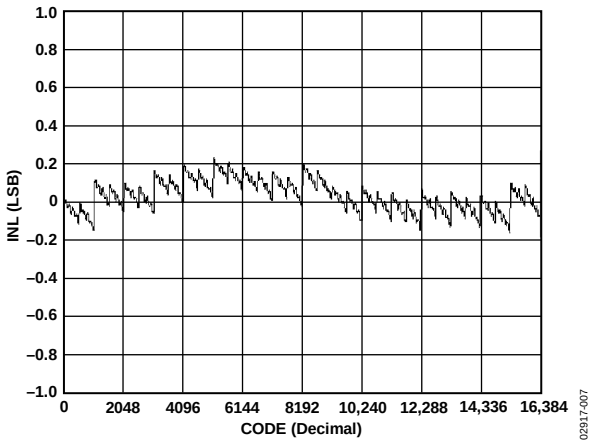


Figure 9. AD5553 INL Error

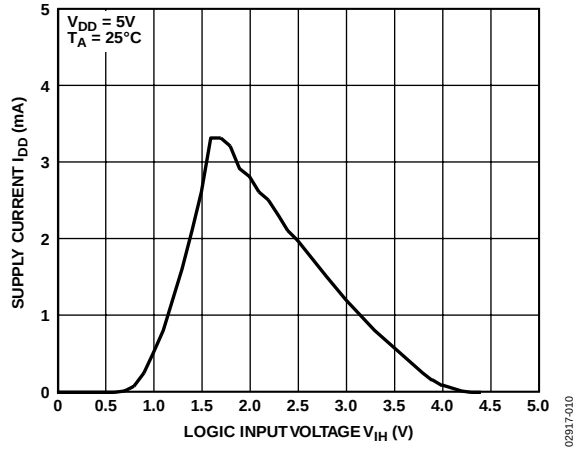


Figure 12. Supply Current vs. Logic Input Voltage

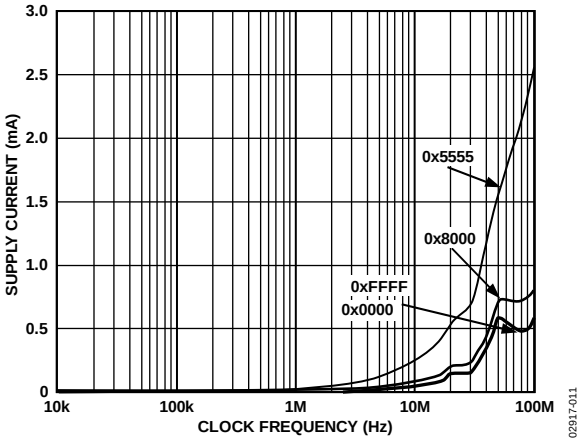


Figure 13. AD5543 Supply Current vs. Clock Frequency

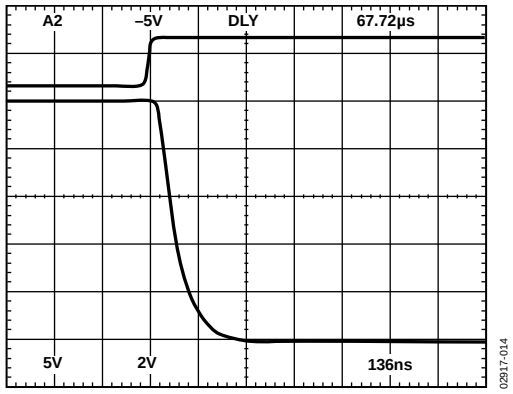


Figure 16. Settling Time

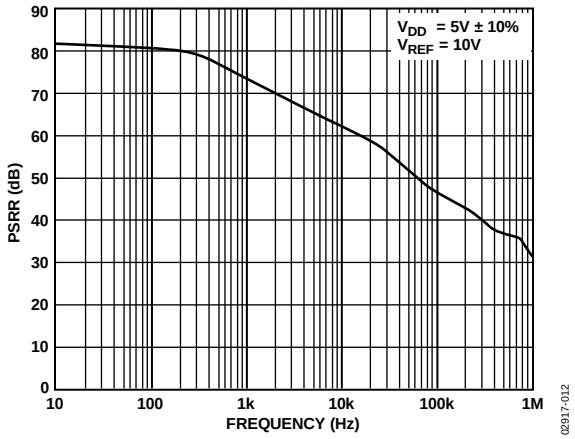


Figure 14. Power Supply Rejection Ratio (PSRR) vs. Frequency

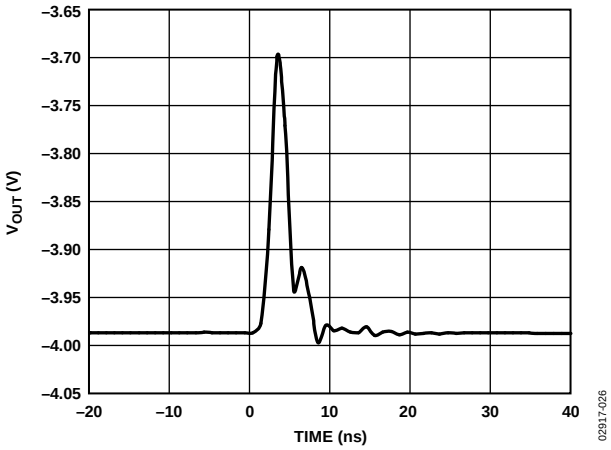


Figure 17. Midscale Transition and Digital Feedthrough

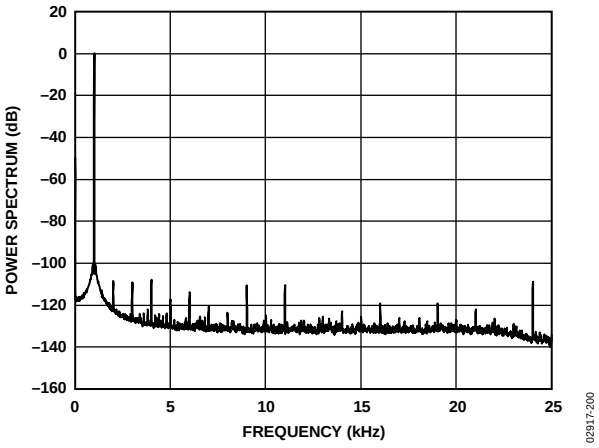


Figure 15. AD5543/AD5553 Analog Total Harmonic Distortion (THD)

CIRCUIT OPERATION

The AD5543/AD5553 contain a 16-/14-bit current output, DACs, serial input registers, and DAC registers. Both converters use a 3-wire serial data interface.

DAC SECTION

The DAC architecture uses a current steering R-2R ladder design. Figure 18 shows the typical equivalent DAC structure. The DAC contains a matching feedback resistor for use with an external operational amplifier (see Figure 19). With R_{FB} and I_{OUT} terminals connected to the operational amplifier output and inverting node, respectively, a precision voltage output is achieved as

$$V_{OUT} = -V_{REF} \times D/65{,}536 \text{ (AD5543)} \quad (1)$$

$$V_{OUT} = -V_{REF} \times D/16{,}384 \text{ (AD5553)} \quad (2)$$

Note that the output voltage polarity is the opposite of the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal logic to drive the on and off states of the DAC switches.

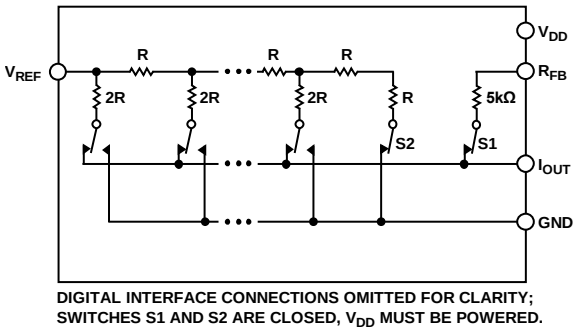


Figure 18. Equivalent R-2R DAC Circuit

Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

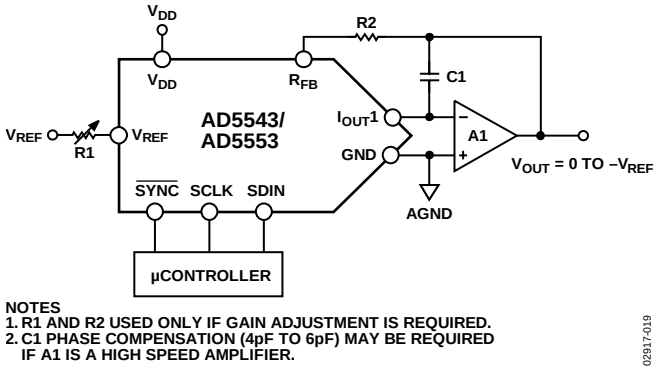


Figure 19. Voltage Output Configuration

These DACs are also designed to accommodate ac reference input signals. The AD5543 accommodates input reference voltages in the range of −12 V to +12 V. The reference voltage inputs exhibit a constant nominal input resistance value of 5 kΩ ± 30%. The DAC output (I_{OUT}) is code dependent, producing various resistances and capacitances. External amplifier choice must take into account the variation in impedance generated by the AD5543 on the inverting input node of the amplifier. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. To maintain good analog performance, power supply bypassing of 0.01 µF to 0.1 µF ceramic or chip capacitors, in parallel with a 1 µF tantalum capacitor, is recommended. Due to degradation of PSRR in frequency, users must avoid using switching power supplies.

SERIAL DATA INTERFACE

The AD5543/AD5553 use a 3-wire ($\overline{CS}$, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 16-bit data-word format for the AD5543. The MSB is loaded first. Table 5 defines the 16 data-word bits. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK, subject to the data setup-and-hold time requirements that are specified in the interface timing specifications. Only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin is strobed to transfer the serial register data to the DAC register. Because most microcontrollers output serial data in 8-bit bytes, two data bytes can be written to the AD5543/AD5553. After loading the serial register, the rising edge of $\overline{CS}$ transfers the serial register data to the DAC register; during this strobe, the CLK must not be toggled. For the AD5553, with 16-bit clock cycles, the two LSBs are ignored.

ESD PROTECTION CIRCUITS

All logic input pins contain back-biased ESD protection Zener diodes that are connected to ground (DGND) and V_{DD}, as shown in Figure 20.

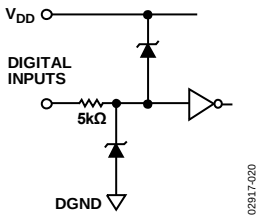


Figure 20. Equivalent ESD Protection Circuits

PCB LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length printed circuit board (PCB) layout design. The leads to the input must be as short as possible to minimize infrared drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device must be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors must also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

The PCB metal traces between V_{REF} and R_{FB} must also be matched to minimize gain error.

Table 5. AD5543 Serial Input Register Data Format; Data Loaded MSB First Format

B15 (MSB)	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 6. AD5553 Serial Input Register Data Format; Data Loaded MSB First Format

B13 (MSB)[1]	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

[1] A full 16-bit data-word can be loaded into the AD5553 serial input register, but only the last 14 bits entered are transferred to the DAC register when $\overline{CS}$ returns to logic high.

APPLICATIONS INFORMATION

STABILITY

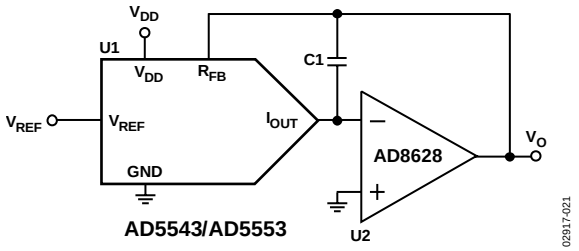


Figure 21. Optional Compensation Capacitor for Gain Peaking Prevention

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the operational amplifier must be connected as close as possible to each other, and proper PCB layout technique must be employed. Because every code change corresponds to a step function, gain peaking may occur if the operational amplifier has limited gain bandwidth product (GBP) and there is excessive parasitic capacitance at the inverting node.

An optional compensation capacitor, C1, can be added for stability, as shown in Figure 21. C1 must be found empirically, but 20 pF is generally adequate for the compensation.

BIPOLAR OUTPUT

The AD5543/AD5553 are inherently 2-quadrant multiplying DACs. That is, they can easily be set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing, which is easily accomplished by using an additional U4 external amplifier configured as a summing amplifier (see Figure 22). In this circuit, the second amplifier, U4, provides a gain of 2 that increases the output span magnitude to 5 V. Biasing the external amplifier with a 2.5 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = −2.5 V) to midscale (V_{OUT} = 0 V) to full-scale (V_{OUT} = +2.5 V).

$$V_{OUT} = (D/32{,}768 - 1) \times V_{REF} \text{ (AD5543)} \quad (3)$$

$$V_{OUT} = (D/8192 - 1) \times V_{REF} \text{ (AD5553)} \quad (4)$$

For the AD5543, the resistance tolerance becomes the dominant error of which users must be aware.

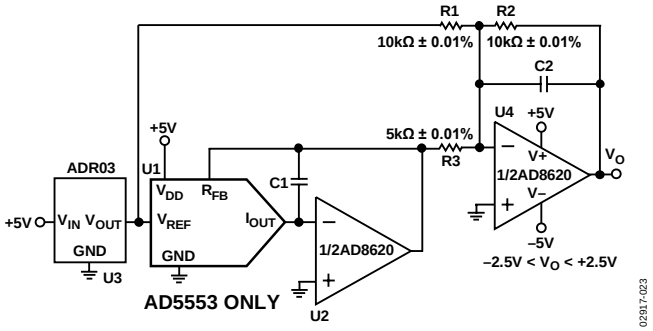


Figure 22. 4-Quadrant Multiplying Application Circuit

PROGRAMMABLE CURRENT SOURCE

Figure 23 shows a versatile V-I conversion circuit using an improved Howland current pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. This circuit can be used in 4 mA to 20 mA current transmitters with up to 500 Ω of load. In Figure 23, it can be shown that if the resistor network is matched, the load current is

$$I_L = \frac{(R2+R3)/R1}{R3} \times V_{REF} \times D \quad (5)$$

R3 in theory can be made small to achieve the current needed within the U3 output current driving capability. This circuit is versatile such that AD8510 can deliver ±20 mA in both directions and the voltage compliance approaches 15 V, which is limited mainly by the supply voltages of U3. However, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes

$$Z_O = \frac{R1'\,R3(R1+R2)}{R1(R2'+R3') - R1'(R2+R3)} \quad (6)$$

If the resistors are perfectly matched, Z_O is infinite, which is desirable, and behaves as an ideal current source. On the other hand, if the resistors are not matched, Z_O can be either positive or negative. Negative can cause oscillation. As a result, C1 is needed to prevent the oscillation. For critical applications, C1 can be found empirically but typically falls in the range of a few picofarads (pF).

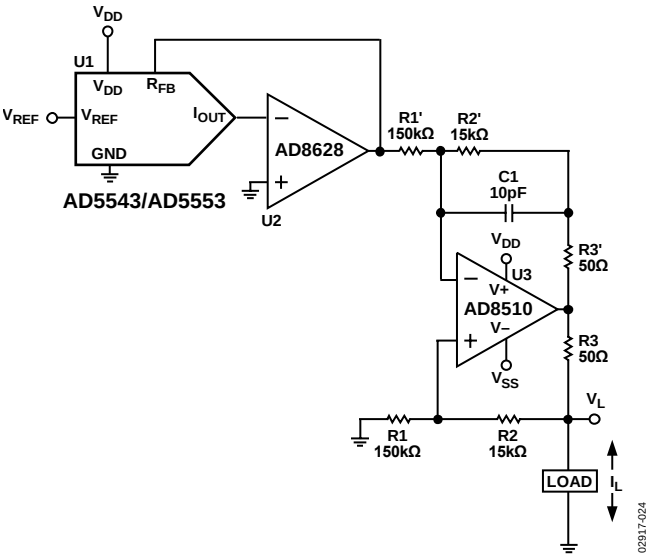


Figure 23. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

REFERENCE SELECTION

When selecting a reference for use with the AD5543/AD5553 and other devices in this series of current output DACs, pay attention to the output voltage temperature coefficient reference. Choosing a precision reference with a low output temperature coefficient minimizes error sources. Table 7 lists some of the references available from Analog Devices, Inc., that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current steering mode is an amplifier with low input bias currents and low input offset voltage. Because of the code dependent output resistance of the DAC, the input offset voltage of an operational amplifier is multiplied by the variable gain of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error, which, if large enough, can cause the DAC to be nonmonotonic.

The input bias current of an operational amplifier also generates an offset at the voltage output because of the bias current flowing in the feedback resistor, R_{FB}.

Common-mode rejection of the operational amplifier is important in voltage switching circuits because it produces a code dependent error at the voltage output of the circuit.

Provided that the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output operational amplifier. To obtain minimum settling time in this configuration, minimize capacitance at the V_{REF} node (the voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

Analog Devices offers a wide range of amplifiers for both precision dc and ac applications, as listed in Table 8 and Table 9.

Table 7. Suitable Analog Devices Precision References

Part No.	Output Voltage (V)	Initial Tolerance (%)	Maximum Temperature Drift (ppm/°C)	I_{SS} (mA)	Output Noise (µV p-p)	Packages
ADR01	10	0.05	3	1	20	SOIC-8
ADR01	10	0.05	9	1	20	TSOT-5, SC70-5
ADR02	5.0	0.06	3	1	10	SOIC-8
ADR02	5.0	0.06	9	1	10	TSOT-5, SC70-5
ADR03	2.5	0.1	3	1	6	SOIC-8
ADR03	2.5	0.1	9	1	6	TSOT-5, SC70-5
ADR06	3.0	0.1	3	1	10	SOIC-8
ADR06	3.0	0.1	9	1	10	TSOT-5, SC70-5
ADR420	2.048	0.05	3	0.5	1.75	SOIC-8, MSOP-8
ADR421	2.50	0.04	3	0.5	1.75	SOIC-8, MSOP-8
ADR423	3.00	0.04	3	0.5	2	SOIC-8, MSOP-8
ADR425	5.00	0.04	3	0.5	3.4	SOIC-8, MSOP-8
ADR431	2.500	0.04	3	0.8	3.5	SOIC-8, MSOP-8
ADR435	5.000	0.04	3	0.8	8	SOIC-8, MSOP-8
ADR391	2.5	0.16	9	0.12	5	TSOT-5
ADR395	5.0	0.10	9	0.12	8	TSOT-5

Table 8. Suitable Analog Devices Precision Operational Amplifier

Part No.	Supply Voltage (V)	V_{OS} Maximum (µV)	I_B Maximum (nA)	0.1 Hz to 10 Hz Noise (µV p-p)	Supply Current (µA)	Packages
OP1177	±2.5 to ±15	60	2	0.4	500	MSOP-8, SOIC-8
AD8675	±5 to ±18	75	2	0.1	2300	MSOP-8, SOIC-8
AD8671	±5 to ±15	75	12	0.077	3000	MSOP-8, SOIC-8
ADA4004-1	±5 to ±15	125	90	0.1	2000	SOIC-8, SOT-23-5
AD8603	1.8 to 5	50	0.001	2.3	40	TSOT-5
AD8607	1.8 to 5	50	0.001	2.3	40	MSOP-8, SOIC-8
AD8605	2.7 to 5	65	0.001	2.3	1000	WLCSP-5, SOT-23-5
AD8615	2.7 to 5	65	0.001	2.4	2000	TSOT-5
AD8616	2.7 to 5	65	0.001	2.4	2000	MSOP-8, SOIC-8

Table 9. Suitable Analog Devices High Speed Operational Amplifier

Part No.	Supply Voltage (V)	BW at ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Max) (µV)	I_B (Max) (nA)	Packages
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23-5
AD8066	5 to 24	145	180	1500	0.006	SOIC-8, MSOP-8
AD8021	5 to 24	490	120	1000	10,500	SOIC-8, MSOP-8
AD8038	3 to 12	350	425	3000	750	SOIC-8, SC70-5
ADA4899-1	5 to 12	600	310	35	100	LFCSP-8, SOIC-8
AD8057	3 to 12	325	1000	5000	500	SOT-23-5, SOIC-8
AD8058	3 to 12	325	850	5000	500	SOIC-8, MSOP-8
AD8061	2.7 to 8	320	650	6000	350	SOT-23-5, SOIC-8
AD8062	2.7 to 8	320	650	6000	350	SOIC-8, MSOP-8
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC-8, PDIP-8

EVALUATION BOARD

The EVAL-AD5543 is used in conjunction with an SDP1Z system development platform board available from Analog Devices, which is purchased separately from the evaluation board. The USB to serial peripheral interface (SPI) communication to the AD5543 is completed using this Blackfin-based development board. The software offers a waveform generator.

SYSTEM DEVELOPMENT PLATFORM

The system development platform (SDP) is a hardware and software evaluation tool for use in conjunction with product evaluation boards. The SDP board is based on the Blackfin ADSP-BF527 processor with USB connectivity to the PC through a USB 2.0 high speed port. For more information about this device, see the system development platform web page.

AD5543/AD5553 TO SPORT INTERFACE

The Analog Devices SDP has one SPORT serial port. The SPORT interface is used to control the AD5543/AD5553, allowing clock frequencies up to 30 MHz.

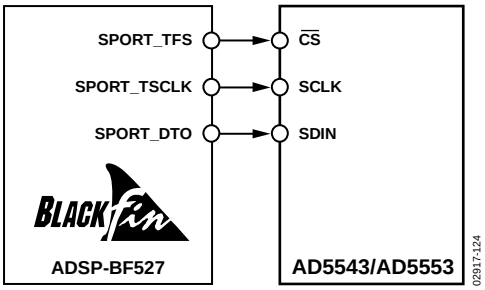


Figure 24. AD5543/AD5553 to SPORT Interface

WAVEFORM GENERATOR

The evaluation board software offers a waveform generator to show every change introduced and transmitted to the output.

OPERATING THE EVALUATION BOARD

The evaluation board requires ±12 V and +5 V supplies. The +12 V V_{DD} and V_{SS} are used to power the output amplifier, while the +5 V is used to power the DAC (V_{DD1}).

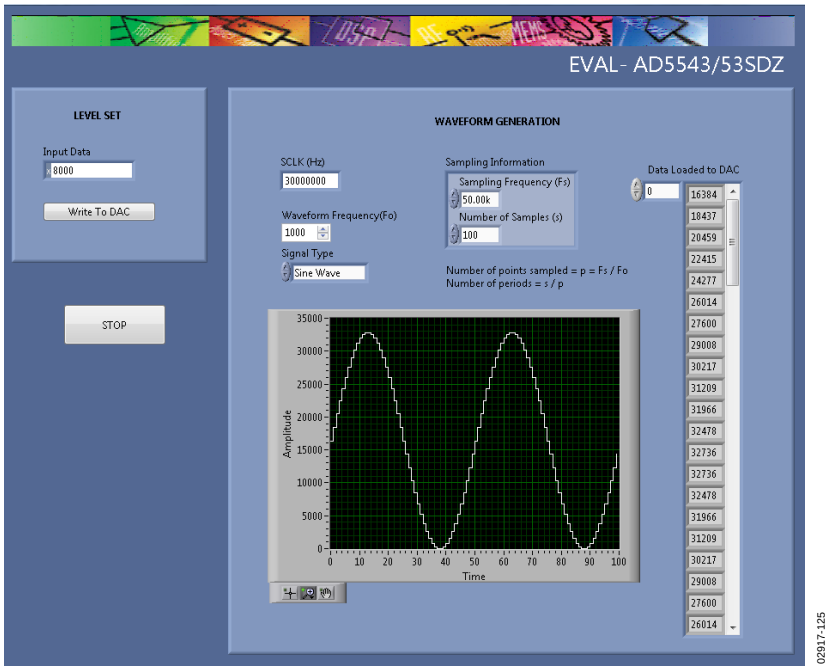


Figure 25. Evaluation Board Software—Waveform Generator

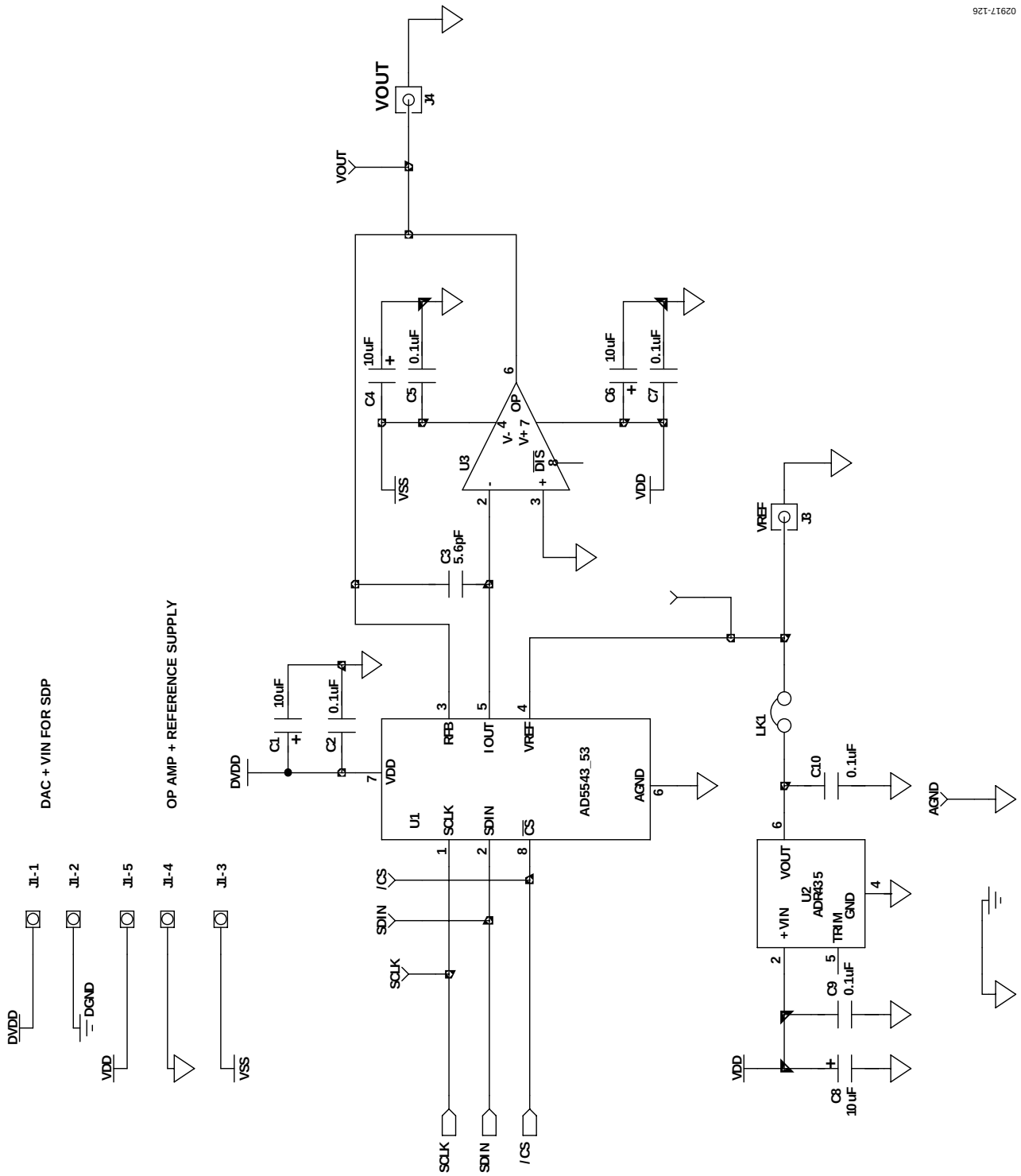


Figure 26. Schematic of AD5543/AD5553 Evaluation Board

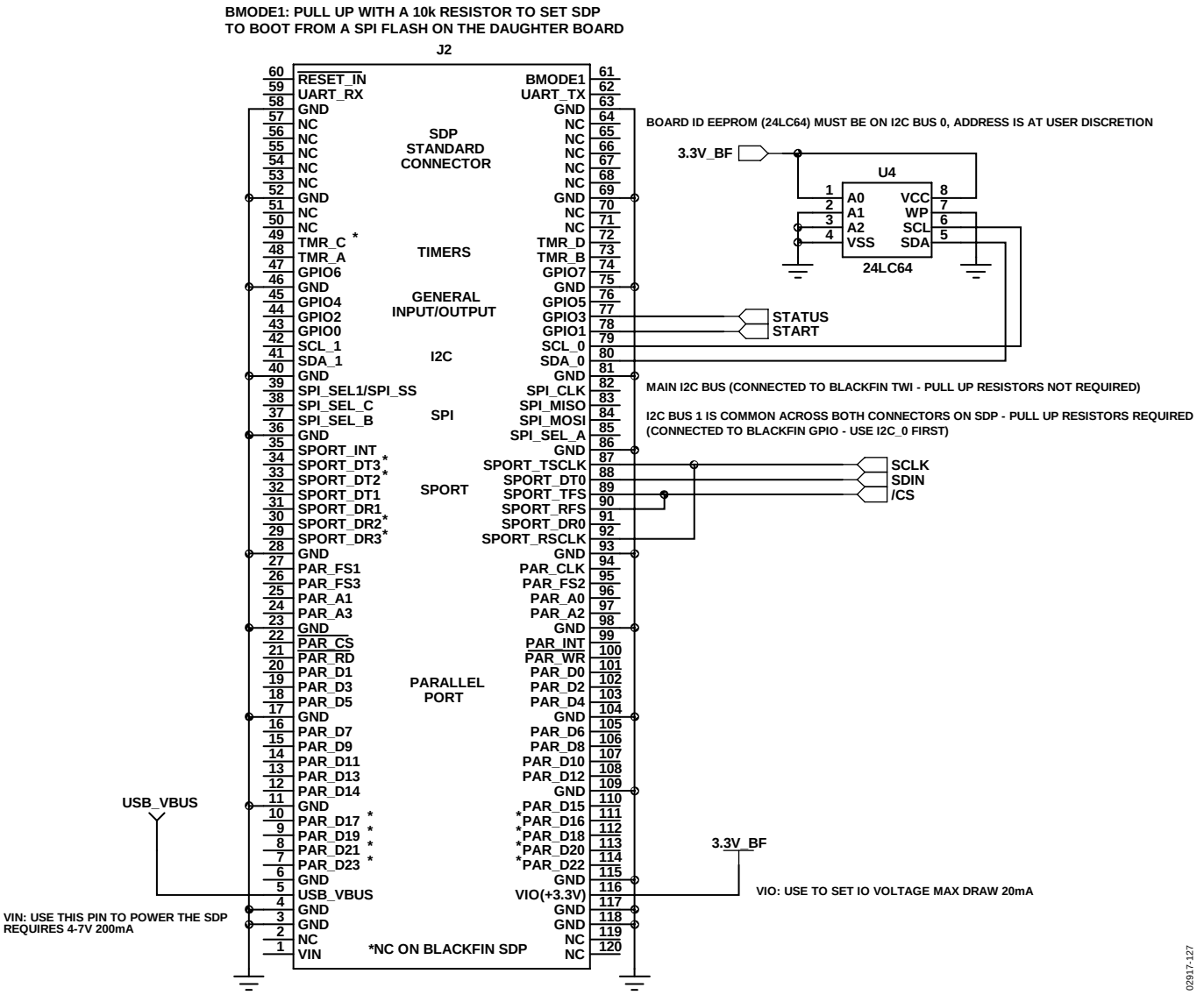


Figure 27. Schematic of SDP Interface

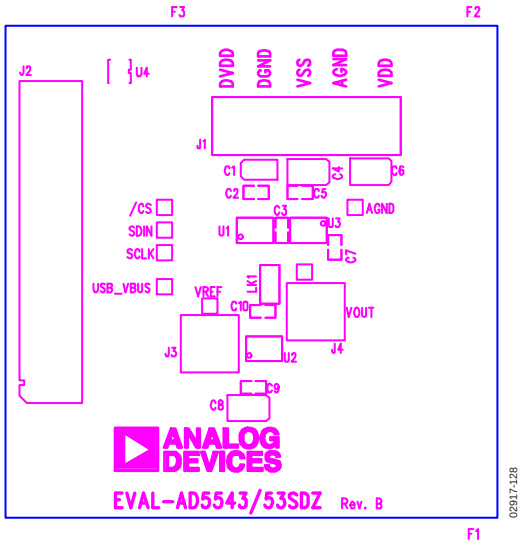


Figure 28. Silkscreen—Component Side View (Top Layer)

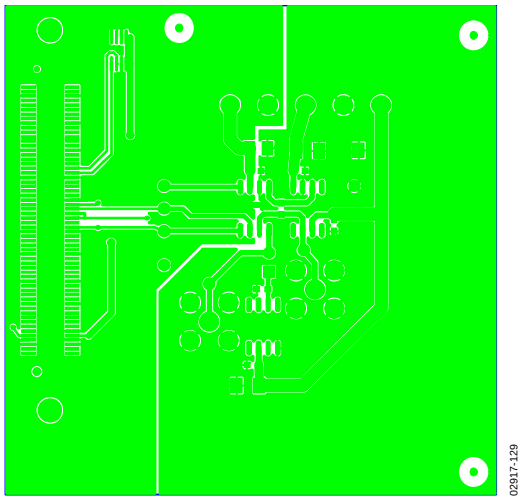


Figure 29. Component Side Artwork

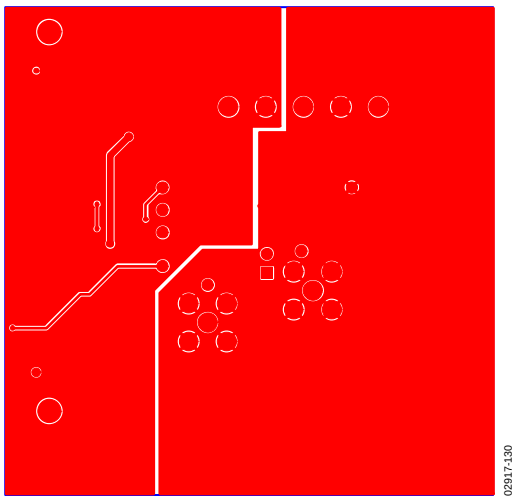


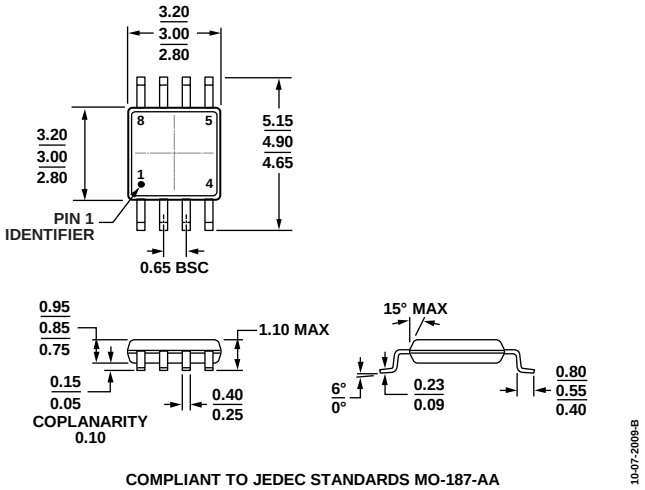
Figure 30. Solder Side Artwork

BILL OF MATERIALS

Table 10.

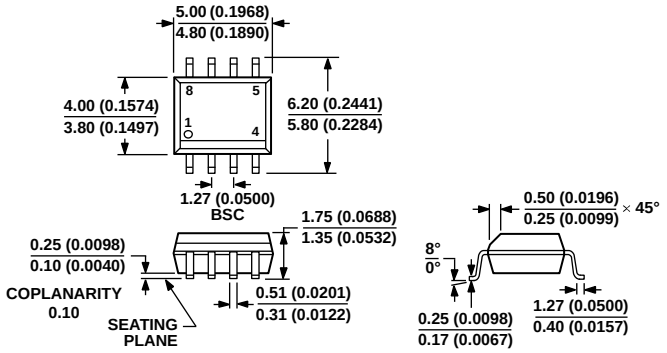
Name	Part Description	Value	PCB Decal	Part Description
$\overline{CS}$	Test point		Test point	Red test point
AGND	Test point		Test point	Black test point
C1	Capacitor+	10 µF	RTAJ_A	10 V SMD tantalum capacitor
C2	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
C3	Capacitor	5.6 pF	C0603	Multilayer ceramic capacitor
C4	Capacitor+	10 µF	RTAJ_B	16 V tantalum capacitor
C5	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
C6	Capacitor+	10 µF	RTAJ_B	16 V tantalum capacitor
C7	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
C8	Capacitor+	10 µF	RTAJ_B	16 V tantalum capacitor
C9	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
C10	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
C11	Capacitor	10 µF	C0805	10 V 10 µF ceramic capacitor 10% X5R 0805
C12	Capacitor	0.1 µF	C0603	50 V X7R ceramic capacitor
GL1	Ground link		Component link	Copper short
J1	CON\POWER5		CON\POWER5	5-pin terminal block
J2	SDP-STANDARD-CONN		CON-120/FX8-120S-SV	120-way connector, 0.6 mm pitch, receptacle
J3	SMB		SMB	Straight PCB mount SMB jack—50 Ω
J4	SMB		SMB	Straight PCB mount SMB jack—50 Ω
SCLK	Test point		Test point	Red test point
SDIN	Test point		Test point	Red test point
U1	AD5543/AD5553		SO8NB	Digital-to-analog converter
U2	ADR435		SO8NB	5 V reference
U3	AD8038		SO8NB	Single operational amplifier 8-pin
U4	24LC64		MSO8	64K I^2C serial EEPROM MSOP8
USB_VBUS	Test point		Test point	Black test point
VOUT	Test point		Test point	Red test point
VREF	Test point		Test point	Red test point
X1	MTHOLE-3MM		MTHOLE-3MM	3 mm NPTH hole
X2	MTHOLE-3MM		MTHOLE-3MM	3 mm NPTH hole

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 31. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 32. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)