Data Sheet

AD5592R

8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, SPI Interface

FEATURES

- 8-channel, configurable ADC/DAC/GPIO
- Configurable as any combination of
  - 8 × 12-bit DAC channels
  - 8 × 12-bit ADC channels
  - 8 × general-purpose digital input/output pins
- Integrated temperature sensor
- SPI interface
- 2.7 V to 5.5 V power supply
- 1.8 V logic compatibility (AD5592R-1)
- Available in
  - 16-ball, 2 mm × 2 mm WLCSP
  - 16-lead, 3 mm × 3 mm LFCSP
  - 16-lead TSSOP
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- Control and monitoring
- General-purpose analog and digital inputs/outputs

GENERAL DESCRIPTION

The AD5592R/AD5592R-1 have eight I/Ox pins (I/O0 to I/O7) that can be independently configured as digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/Ox pin is configured as an analog output, it is driven by a 12-bit DAC. The output range of the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. When an I/Ox pin is configured as an analog input, it is connected to a 12-bit ADC via an analog multiplexer. The input range of the ADC is 0 V to V_{REF} or 0 V to 2 × V_{REF}. The ADC has a total throughput rate of 400 kSPS. The I/Ox pins can also be configured as digital, general-purpose input or output (GPIO) pins. The state of the GPIO pins can be set or read back by accessing the GPIO write data register or the GPIO read configuration register, respectively, via a serial peripheral interface (SPI) write or read operation.

The AD5592R/AD5592R-1 have an integrated 2.5 V, 20 ppm/°C reference, which is turned off by default, and an integrated temperature indicator, which gives an indication of the die temperature. The temperature value is read back as part of an ADC read sequence.

The AD5592R/AD5592R-1 are available in 16-ball, 2 mm × 2 mm WLCSP, 16-lead, 3 mm × 3 mm LFCSP, and 16-lead TSSOP. The AD5592R/AD5592R-1 operate over a temperature range of −40 °C (T_A) to +125 °C (T_J).

Table 1. Related Products

Part No.	Description
AD5593R	AD5592R equivalent with V_{LOGIC} and $\overline{RESET}$ pins and an I^2C interface

FUNCTIONAL BLOCK DIAGRAM

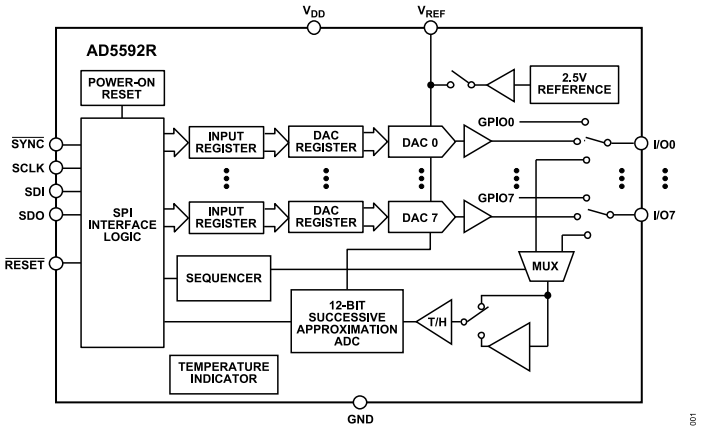

Figure 1. AD5592R Functional Block Diagram

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REVISION HISTORY

7/2023—Rev. G to Rev. H

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FUNCTIONAL BLOCK DIAGRAM (AD5592R-1)

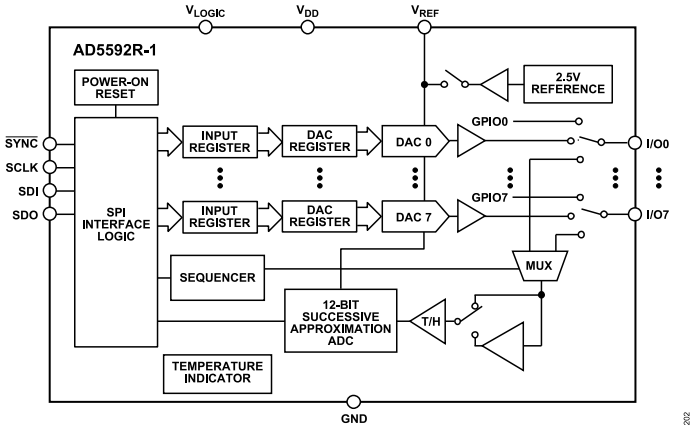

Figure 2. AD5592R-1 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, V_{LOGIC} = 2.7 V to 5.5 V (AD5592R-1 only), V_{REF} = 2.5 V (external), R_L = 2 kΩ to GND, C_L = 200 pF to GND, typical values are at T_A = 25°C, unless otherwise noted. Typical specifications are verified by characterization, not production tested.

Table 2.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
TEMPERATURE RANGE					
Specified Performance[2]	−40		+105	°C	
	−40		+125	°C	AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
ADC PERFORMANCE					f_{IN} = 10 kHz sine wave
Resolution		12		Bits	
Input Range	0		V_{REF}	V	When using the internal ADC buffer, there is a dead band of 0 V to 5 mV
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−2		+2	LSB	
	−2.5		+2.5	LSB	V_{DD} = 5.5 V, input range = 0 V to V_{REF}, AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error			±5	mV	
Gain Error			0.3	% FSR	
Throughput Rate[3]			400	kSPS	
			350	kSPS	AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
Track Time (t_{TRACK})[3, 4]	500			ns	
Conversion Time (t_{CONV})[3, 4]			2	µs	
		2	2.36	µs	AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
Signal-to-Noise Ratio (SNR)		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 5.5 V, input range = 0 V to V_{REF}
		61		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Signal-to-Noise-and-Distortion (SINAD) Ratio		69		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		67		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		60		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Total Harmonic Distortion (THD)		−91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		−89		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		−72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Peak Harmonic or Spurious Noise (SFDR)		91		dB	V_{DD} = 2.7 V, input range = 0 V to V_{REF}
		91		dB	V_{DD} = 3.3 V, input range = 0 V to V_{REF}
		72		dB	V_{DD} = 5.5 V, input range = 0 V to 2 × V_{REF}
Aperture Delay[3]		15		ns	V_{DD} = 3 V
		12		ns	V_{DD} = 5 V
Aperture Jitter[3]		50		ps	
Channel-to-Channel Isolation		−95		dB	f_{IN} = 5 kHz
Input Capacitance		45		pF	
Full Power Bandwidth		8.2		MHz	At 3 dB
		1.6		MHz	At 0.1 dB
DAC PERFORMANCE[5]					
Resolution		12		Bits	
Output Range	0		V_{REF}	V	
	0		2 × V_{REF}	V	
Integral Nonlinearity (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	
Offset Error	−3		+3	mV	
Offset Error Drift[3]		8		µV/°C	

SPECIFICATIONS

Table 2. (Continued)

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
Gain Error			±0.2	% FSR	Output range = 0 V to V_{REF}
			±0.1	% FSR	Output range = 0 V to 2 × V_{REF}
Zero Code Error		0.65	2	mV	
Total Unadjusted Error		±0.03	±0.25	% FSR	Output range = 0 V to V_{REF}
		±0.015	±0.1		Output range = 0 V to 2 × V_{REF}
Capacitive Load (C_L) Stability[3]			2	nF	R_L = ∞
			10	nF	R_L = 1 kΩ
Resistive Load (R_L)	1			kΩ	
Short-Circuit Current		25		mA	
DC Crosstalk[3]	−4		+4	µV	Due to single channel, full-scale output change
DC Output Impedance		0.2		Ω	
DC Power Supply Rejection Ratio (PSRR)[3]		0.15		mV/V	DAC code = midscale, V_{DD} = 3 V ± 10% or 5 V ± 10%
Load Impedance at Rails[6]		25		Ω	
Load Regulation		200		µV/mA	V_{DD} = 5 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
		200		µV/mA	V_{DD} = 3 V ± 10%, DAC code = midscale, −10 mA ≤ I_{OUT} ≤ +10 mA
Power-Up Time		7		µs	Coming out of power-down mode, V_{DD} = 5 V
DAC AC SPECIFICATIONS					
Slew Rate		1.25		V/µs	Measured from 10% to 90% of full scale
Settling Time		6		µs	¼ scale to ¾ scale settling to 1 LSB
DAC Glitch Impulse		2		nV-sec	
DAC to DAC Crosstalk		1		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		1		nV-sec	
Digital Feedthrough		0.1		nV-sec	
Multiplying Bandwidth		240		kHz	DAC code = full scale, output range = 0 V to V_{REF}
Output Voltage Noise Spectral Density		200		nV/√Hz	DAC code = midscale, output range = 0 V to 2 × V_{REF}, measured at 10 kHz
Signal-to-Noise Ratio (SNR)		81		dB	
Peak Harmonic or Spurious Noise (SFDR)		77		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	
Total Harmonic Distortion (THD)		−76		dB	
REFERENCE INPUT					
V_{REF} Input Voltage	1		V_{DD}	V	
DC Leakage Current	−1		+1	µA	No I/Ox pins configured as DACs
Reference Input Impedance		12		kΩ	DAC output range = 0 V to 2 × V_{REF}
		24		kΩ	DAC output range = 0 V to V_{REF}
REFERENCE OUTPUT					
V_{REF} Output Voltage	2.495	2.5	2.505	V	T_A = 25°C
	2.485	2.5	2.515	V	T_A = 25°C, AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
V_{REF} Temperature Coefficient		20		ppm/°C	
Capacitive Load (C_L) Stability		5		µF	R_L = 2 kΩ
Output Impedance[3]		0.15		Ω	V_{DD} = 2.7 V
		0.7		Ω	V_{DD} = 5 V
Output Voltage Noise		10		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density		240		nV/√Hz	T_A = 25°C, f = 10 kHz, C_L = 10 nF

SPECIFICATIONS

Table 2. (Continued)

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
Line Regulation		20		µV/V	T_A = 25°C, sweeping V_{DD} from 2.7 V to 5.5 V
		10		µV/V	T_A = 25°C, sweeping V_{DD} from 2.7 V to 3.3 V
Load Regulation					
Sourcing		210		µV/mA	T_A = 25°C, −5 mA ≤ load current ≤ +5 mA
Sinking		120		µV/mA	T_A = 25°C, −5 mA ≤ load current ≤ +5 mA
Output Current Load Capability		±5		mA	V_{DD} ≥ 3 V
GPIO OUTPUT					
I_{SOURCE}, I_{SINK}		1.6		mA	
Output Voltage					
High (V_{OH})	V_{DD} − 0.2			V	I_{SOURCE} = 1 mA
Low (V_{OL})			0.4	V	I_{SINK} = 1 mA
GPIO INPUT					
Input Voltage					V_{DD} = 2.7 V to 5.5 V
High (V_{IH})	0.7 × V_{DD}			V	
Low (V_{IL})			0.3 × V_{DD}	V	
Input Capacitance		20		pF	
Hysteresis		0.2		V	
Input Current		±1		µA	
LOGIC INPUTS					
AD5592R Input Voltage					V_{DD} = 2.7 V to 5.5 V
High (V_{INH})	0.7 × V_{DD}			V	
Low (V_{INL})			0.3 × V_{DD}	V	
AD5592R-1 Input Voltage					
High (V_{INH})	0.7 × V_{LOGIC}			V	V_{LOGIC} = 2.7 V to 5.5 V
	0.9 × V_{LOGIC}				V_{LOGIC} = 1.8 V to 2.7 V
Low (V_{INL})			0.3 × V_{LOGIC}	V	V_{LOGIC} = 2.7 V to 5.5 V
			0.1 × V_{LOGIC}		V_{LOGIC} = 1.8 V to 2.7 V
Input Current (I_{IN})	−1		+1	µA	Typically 10 nA, $\overline{RESET}$ = 1 µA typical
Input Capacitance (C_{IN})			10	pF	
LOGIC OUTPUT (SDO)					
Output High Voltage (V_{OH})					I_{SOURCE} = 200 µA
AD5592R	V_{DD} − 0.2			V	V_{DD} = 2.7 V to 5.5 V
AD5592R-1	V_{LOGIC} − 0.2				V_{LOGIC} = 2.7 V to 5.5 V
	V_{LOGIC} − 0.1				V_{LOGIC} = 1.8 V to 2.7 V
Output Low Voltage (V_{OL})					I_{SINK} = 200 µA
AD5592R			0.4	V	V_{DD} = 2.7 V to 5.5 V
AD5592R-1			0.4	V	V_{LOGIC} = 2.7 V to 5.5 V
			0.2	V	V_{LOGIC} = 1.8 V to 2.7 V
Floating-State Output Capacitance		10		pF	
TEMPERATURE SENSOR[3]					
Resolution		12		Bits	
Operating Range[2]	−40		+105	°C	
	−40		+125	°C	AD5592RWBCPZ-RL7 and AD5592RWBCPZ-1-RL7
Accuracy		±3		°C	5 sample averaging
Track Time			5	µs	ADC buffer enabled
			20	µs	ADC buffer disabled
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	

SPECIFICATIONS

Table 2. (Continued)

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
I_{DD}			2.7	mA	Digital inputs = 0 V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0 V to 2 × V_{REF} for DACs and ADCs
Power-Down Mode			3.5	µA	
V_{DD} = 5 V (Normal Mode)		1.6		mA	I/O0 to I/O7 are DACs, internal reference, gain = 2
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 2
		2.4		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2
		1		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 2
		0.75		mA	I/O0 to I/O7 are ADCs, external reference, gain = 2
		0.5		mA	I/O0 to I/O7 are general-purpose outputs
		0.5		mA	I/O0 to I/O7 are general-purpose inputs
		0.5		mA	I/O0 to I/O3 are general-purpose outputs, I/O4 to I/O7 are general-purpose inputs
V_{DD} = 3 V (Normal Mode)		1.1		mA	I/O0 to I/O7 are DACs, internal reference, gain = 1
		1		mA	I/O0 to I/O7 are DACs, external reference, gain = 1
		1.1		mA	I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1
		0.78		mA	I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1
		0.75		mA	I/O0 to I/O7 are ADCs, internal reference, gain = 1
		0.5		mA	I/O0 to I/O7 are ADCs, external reference, gain = 1
		0.45		mA	I/O0 to I/O7 are general-purpose outputs
		0.45		mA	I/O0 to I/O7 are general-purpose inputs
V_{LOGIC}	1.62		V_{DD}	V	AD5592R-1 only
I_{LOGIC}			3	µA	AD5592R-1 only

[1] All specifications expressed in decibels are referred to full-scale input (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise noted.

[2] The minimum is the ambient temperature (T_A) and the maximum is the junction temperature (T_J).

[3] Guaranteed by design and characterization; not production tested.

[4] See Figure 5.

[5] DC specifications tested with the outputs unloaded, unless otherwise noted. Linearity calculated using a code range of 8 to 4095. There is an upper dead band of 10 mV when $V_{REF} = V_{DD}$.

[6] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 34).

TIMING CHARACTERISTICS

Guaranteed by design and characterization, not production tested; all input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; $T_A = T_{A, MIN}$ to $T_{A, MAX}$, unless otherwise noted.

Table 3. AD5592R Timing Characteristics

Parameter	2.7 V ≤ V_{DD} < 3 V	3 V ≤ V_{DD} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	50	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time

SPECIFICATIONS

Table 3. AD5592R Timing Characteristics (Continued)

Parameter	2.7 V ≤ V_{DD} < 3 V	3 V ≤ V_{DD} ≤ 5.5 V	Unit	Test Conditions/Comments
t_4	15	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
	1.65	1.65	µs max	$\overline{SYNC}$ falling edge to SCLK falling edge setup time[1]
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for register write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	25	25	ns max	SCLK rising edge to SDO valid
t_{11}	250	250	ns min	$\overline{RESET}$ low pulse width (not shown in Figure 4)

[1] When reading an ADC conversion (see Figure 5).

Table 4. AD5592R-1 Timing Characteristics

Parameter	1.62 V ≤ V_{LOGIC} < 3 V	3 V ≤ V_{LOGIC} ≤ 5.5 V	Unit	Test Conditions/Comments
t_1	33	20	ns min	SCLK cycle time, write operation
	100	50	ns min	SCLK cycle time, read operation
t_2	16	10	ns min	SCLK high time
t_3	16	10	ns min	SCLK low time
t_4	15	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
	1.65	1.65	µs max	$\overline{SYNC}$ to SCLK falling edge setup time[1]
t_5	7	7	ns min	Data setup time
t_6	5	5	ns min	Data hold time
t_7	15	10	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	30	30	ns min	Minimum $\overline{SYNC}$ high time for write operations
	60	60	ns min	Minimum $\overline{SYNC}$ high time for register read operations
t_9	0	0	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge
t_{10}	56	25	ns max	SCLK rising edge to SDO valid

[1] When reading an ADC conversion (see Figure 5).

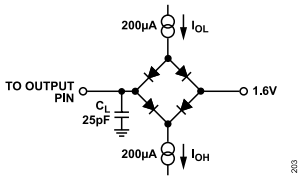

Figure 3. Load Circuit for Logic Output (SDO) Timing Specifications

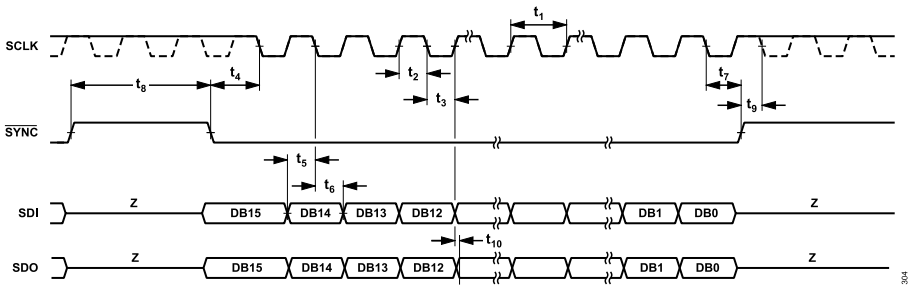

Figure 4. Serial Read and Write Timing Diagram

SPECIFICATIONS

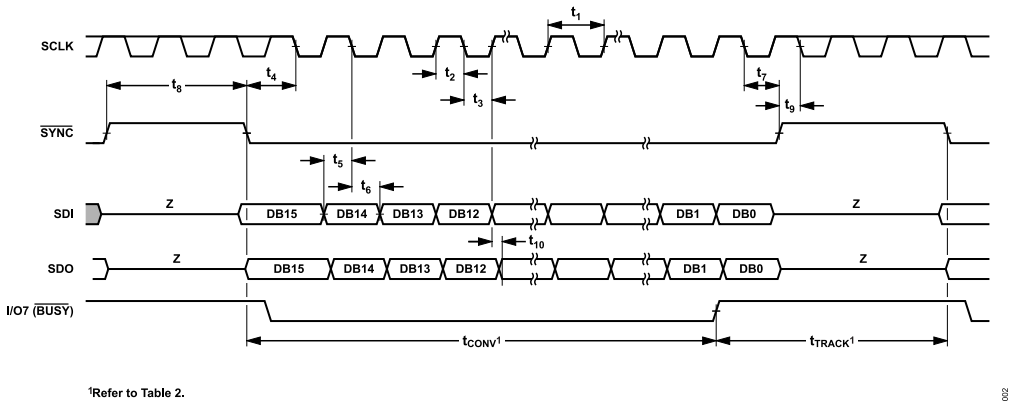

Figure 5. ADC Conversion Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to + 7 V
V_{LOGIC} to GND	−0.3 V to + 7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R	
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
AD5592R-1	
Digital Input Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40 °C (T_A) to +125 °C (T_J)
Storage Temperature Range	−65 °C to +150 °C
Junction Temperature (T_J max)	150 °C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal characteristics are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. Thermal resistance values specified in Table 6 are simulated based on JEDEC specifications using a 2S2P thermal test board (see JEDEC JESD51), except for $\theta_{JC\text{-}TOP}$, which uses a JEDEC 1S test board.

θ_{JA} is the junction to ambient thermal resistance, measured in a JEDEC natural convection environment.

θ_{JC} is the junction to case thermal resistance, measured at the center of the package top surface, with an infinite heat sink attached to the package surface.

θ_{JB} is the junction to board thermal resistance, measured at a point on the board 1mm from the package edge, along the package centerline, measured in a JEDEC θ_{JB} environment.

Ψ_{JB} is the junction to board thermal characterization parameter, measured in a JEDEC natural convection environment.

Ψ_{JT} is the junction to package top thermal characterization parameter, measured in a JEDEC natural convection environment.

Do not use θ_{JA}, θ_{JC}, and θ_{JB} thermal resistances to perform direct calculation/measurement of the die temperature because doing so results in incorrect values. The thermal resistances assume 100% of the power that is dissipated along the specified path between the measurement points. The thermal resistances are directly dependent on the PCB design and environment.

If direct measurement of the package is required, the Ψ_{JT} and Ψ_{JB} values must be used because they more accurately reflect the true thermal dissipation paths.

θ_{JC} must only be used where an external heat sink is attached directly to the package.

System level thermal simulation is highly recommended.

For more details about the thermal resistances, refer to *JEDEC51-12: Guidelines for Reporting and Using Electronic Package Thermal Information*.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	$\theta_{JC\text{-}TOP}$	Ψ_{JT}	Ψ_{JB}	Unit
CP-16-32	92.4	39.6	48.2	0.9	37.4	°C/W
RU-16	127	60.2	42.2	2.6	59.1	°C/W
CB-16-3	103.2	64	0	0	78	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD5592R/AD5592R-1

Table 7. AD5592R/AD5592R-1, 16-Ball WLCSP, 16-Lead LFCSP, and 16-Lead TSSOP

ESD Model	Withstand Voltage (V)	Class
HBM	1000	1C
FICDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

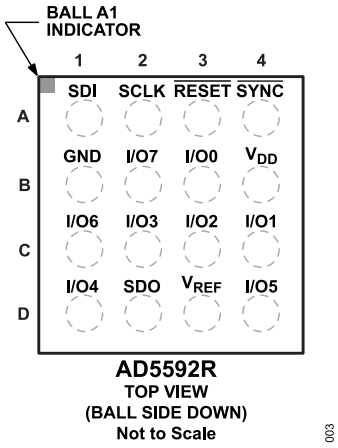

Figure 6. AD5592R 16-Ball WLCSP Pin Configuration

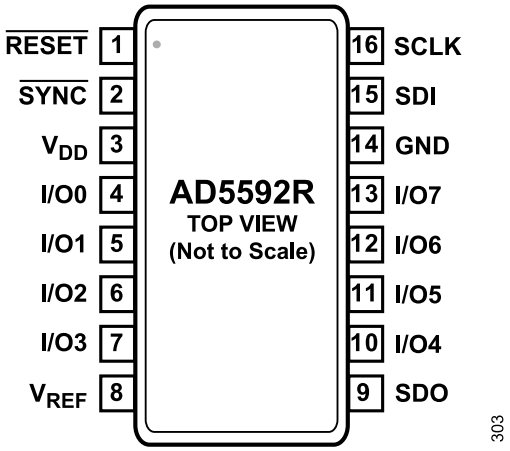

Figure 8. AD5592R 16-Lead TSSOP Pin Configuration

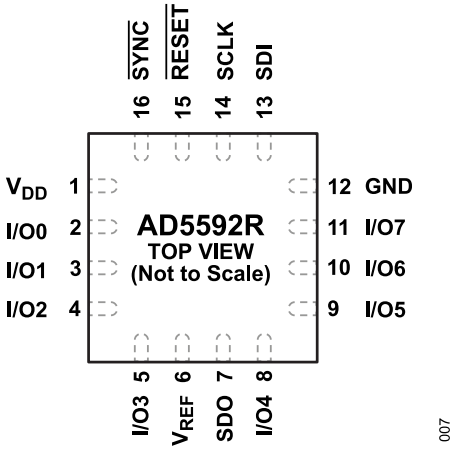

Figure 7. AD5592R 16-Lead LFCSP Pin Configuration

Table 8. AD5592R Pin Function Descriptions

Pin No.				
WLCSP	LFCSP	TSSOP	Mnemonic	Description
A1	13	15	SDI	Data In. Logic input. Data that is to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
A2	14	16	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R.
A3	15	1	$\overline{\text{RESET}}$	Asynchronous Reset Pin. Tie this pin high for normal operation. When this pin is brought low, the AD5592R is reset to its default configuration.
A4	16	2	$\overline{\text{SYNC}}$	Synchronization. Active low control input. $\overline{\text{SYNC}}$ is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 16 clocks.
B1	12	14	GND	Ground Reference Point for All Circuitry on the AD5592R.
B2	11	13	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 11 and Table 12). I/O7 can also be configured as a $\overline{\text{BUSY}}$ signal to indicate when an ADC conversion is taking place (see Table 22).
B3, C4, C3, C2, D1, D4, C1	2, 3, 4, 5, 8, 9, 10	4, 5, 6, 7, 10, 11, 12	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 11 and Table 12).
B4	1	3	V_{DD}	Power Supply Input. The AD5592R operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 8. AD5592R Pin Function Descriptions (Continued)

Pin No.				
WLCSP	LFCSP	TSSOP	Mnemonic	Description
D2	7	9	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
D3	6	8	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

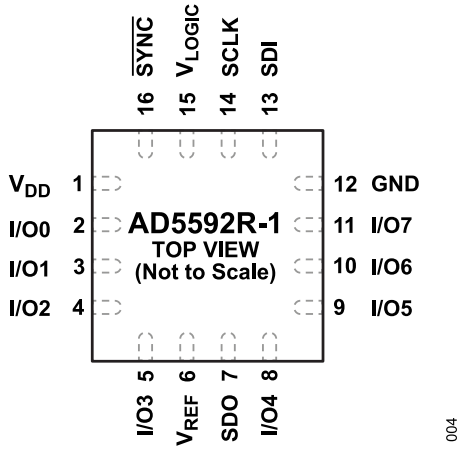

Figure 9. AD5592R-1 16-Lead LFCSP Pin Configuration

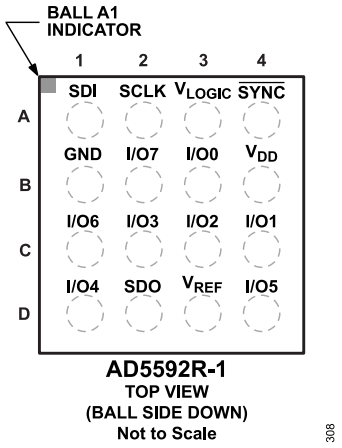

Figure 10. AD5592R-1 16-Ball WLCSP Pin Configuration

Table 9. AD5592R-1 Pin Function Descriptions

Pin No.			
LFCSP	WLCSP	Mnemonic	Description
1	B4	V_{DD}	Power Supply Input. The AD5592R-1 operates from 2.7 V to 5.5 V, and this pin must be decoupled with a 0.1 µF capacitor to GND.
2 to 5, 8 to 10	B3, C4, C3, C2, D1, D4, C1	I/O0 to I/O6	Input/Output 0 Through Input/Output 6. These pins can be independently configured as DACs, ADCs, or general-purpose digital inputs or outputs. The function of each pin is determined by programming the I/Ox pin configuration registers (see Table 11 and Table 12).
6	D3	V_{REF}	Reference Input/Output. When the internal reference is enabled, the 2.5 V reference voltage is available on this pin. A 0.1 µF capacitor connected from the V_{REF} pin to GND is recommended to achieve the specified performance from the AD5592R-1. When the internal reference is disabled, an external reference must be applied to this pin. The voltage range for the external reference is 1 V to V_{DD}.
7	D2	SDO	Data Out. Logic output. The conversion results from the ADC, register reads, and temperature sensor information are provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The MSB is placed on the SDO pin on the falling edge of $\overline{SYNC}$. Because the SCLK can idle high or low, the next bit is clocked out on the first rising edge of SCLK that follows a falling edge SCLK while $\overline{SYNC}$ is low (see Figure 4).
11	B2	I/O7	Input/Output 7. This pin can be configured as a DAC, ADC, or general-purpose digital input or output. The function of this pin is determined by programming the I/Ox pin configuration registers (see Table 11 and Table 12). I/O7 can also be configured as a $\overline{BUSY}$ signal to indicate when an ADC conversion is taking place (see Table 22).
12	B1	GND	Ground Reference Point for All Circuitry on the AD5592R-1.
13	A1	SDI	Data In. Logic input. Data to be written to the DACs and control registers is provided on this input and is clocked into the register on the falling edge of SCLK.
14	A2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz when writing to the DACs. SCLK has a maximum speed of 20 MHz when performing a conversion or clocking data from the AD5592R-1.
15	A3	V_{LOGIC}	Interface Power Supply. The voltage of this pin ranges from 1.62 V to 5.5 V.
16	A4	$\overline{SYNC}$	Synchronization. Active low control input. $\overline{SYNC}$ is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, data is transferred in on the falling edges of the next 16 clocks.

TYPICAL PERFORMANCE CHARACTERISTICS

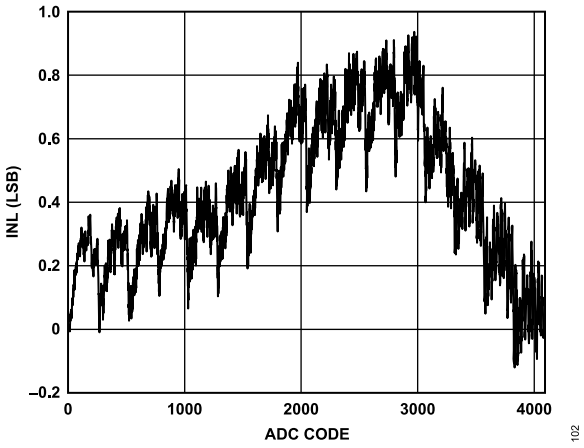

Figure 11. ADC INL, V_{DD} = 5.5 V

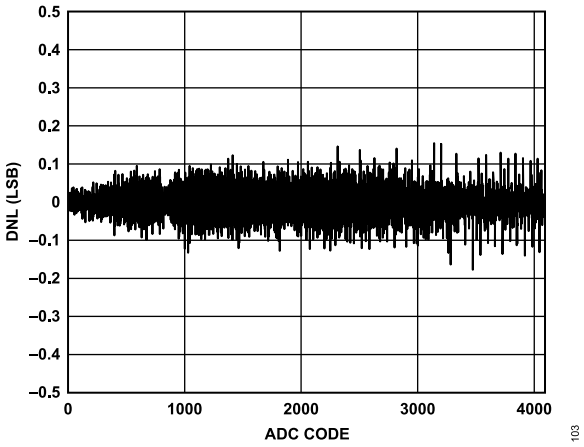

Figure 12. ADC DNL, V_{DD} = 5.5 V

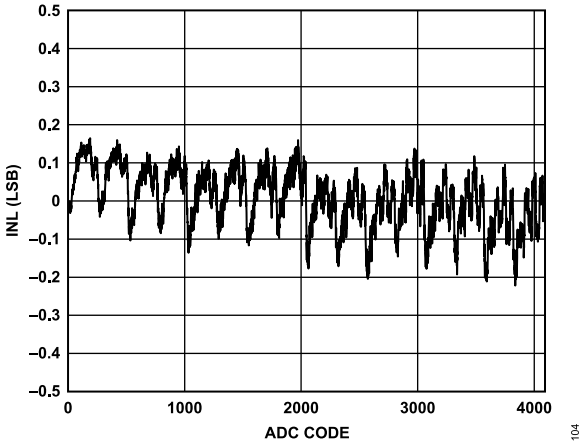

Figure 13. ADC INL, V_{DD} = 2.7 V

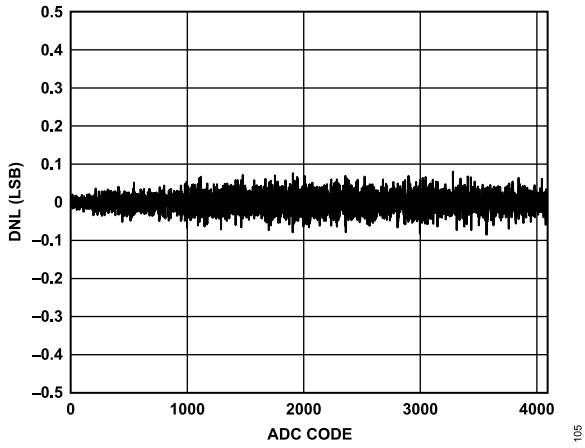

Figure 14. ADC DNL, V_{DD} = 2.7 V

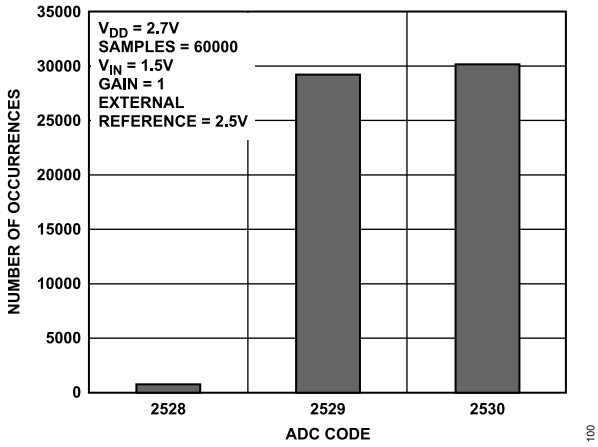

Figure 15. Histogram of ADC Codes, V_{DD} = 2.7 V

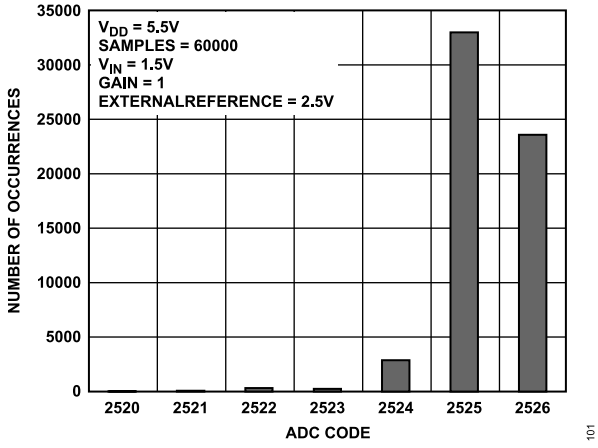

Figure 16. Histogram of ADC Codes, V_{DD} = 5.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

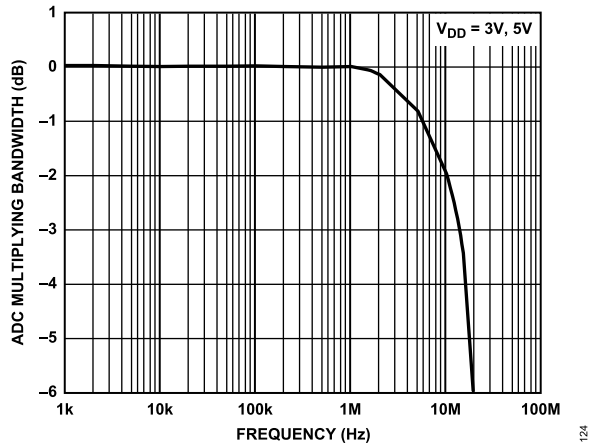

Figure 17. ADC Multiplying Bandwidth

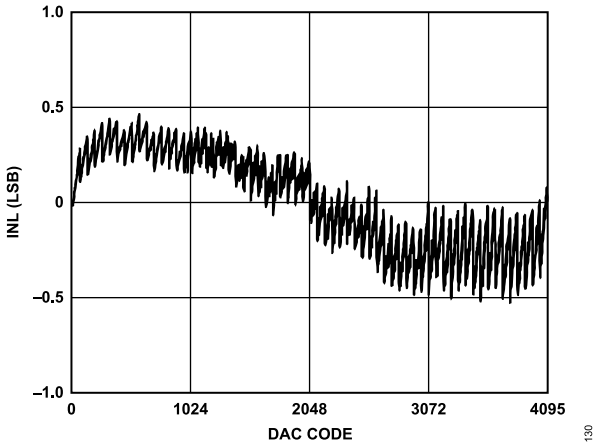

Figure 18. DAC INL

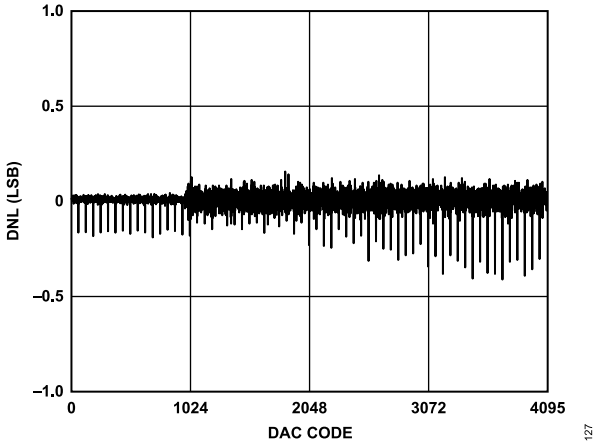

Figure 19. DAC DNL

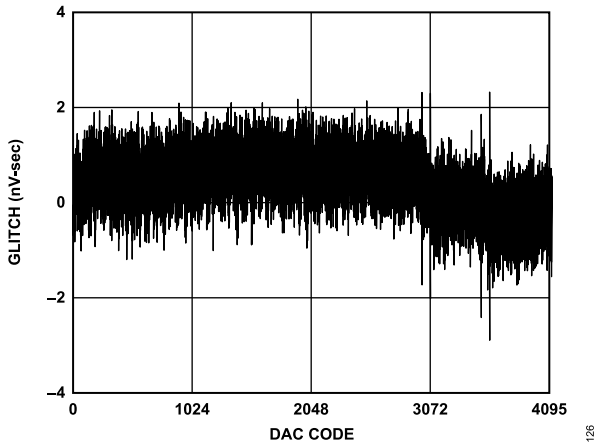

Figure 20. DAC Adjacent Code Glitch

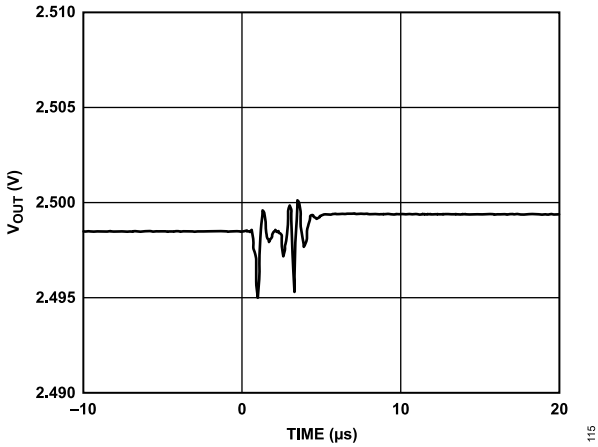

Figure 21. DAC Digital-to-Analog Glitch (Rising)

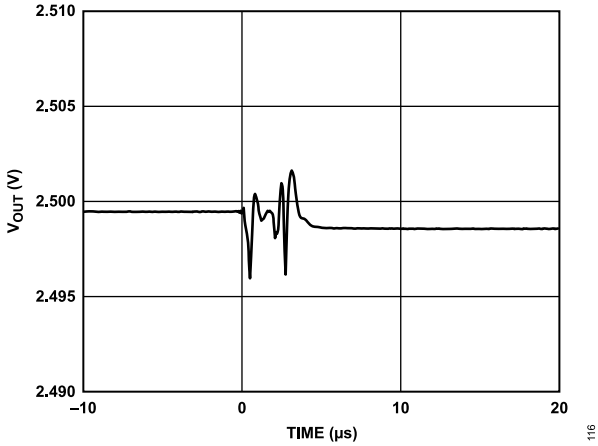

Figure 22. DAC Digital-to-Analog Glitch (Falling)

TYPICAL PERFORMANCE CHARACTERISTICS

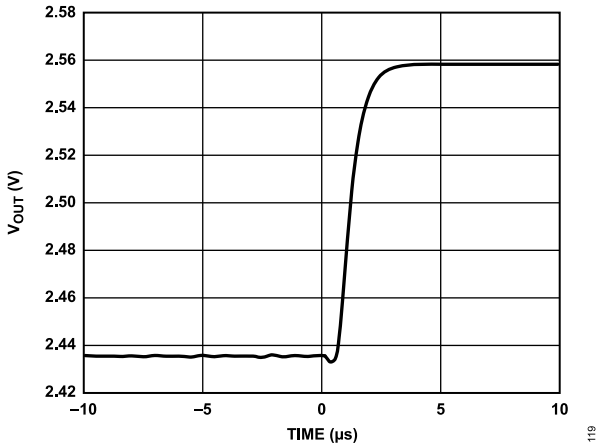

Figure 23. DAC Settling Time (100 Code Change, Rising Edge)

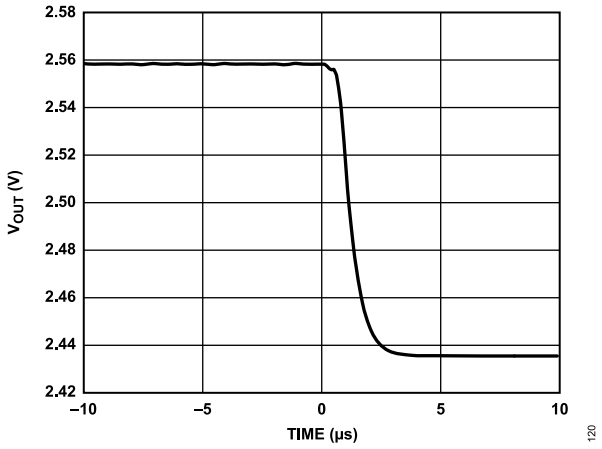

Figure 24. DAC Settling Time (100 Code Change, Falling Edge)

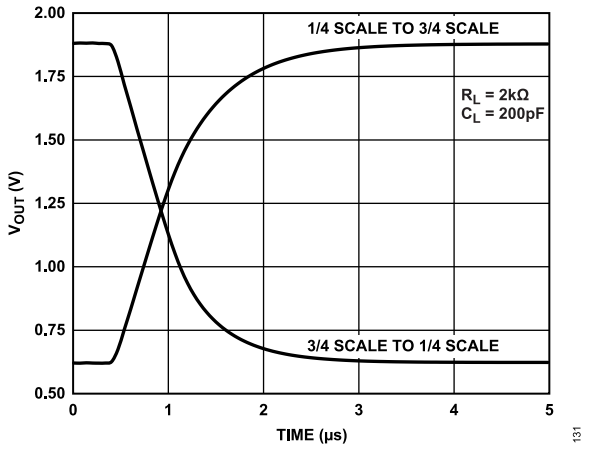

Figure 25. DAC Settling Time, Output Range = 0 V to V_{REF}

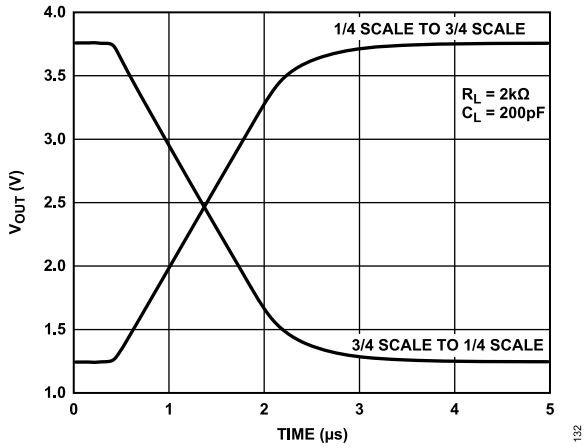

Figure 26. DAC Settling Time, Output Range = 0 V to 2 × V_{REF}

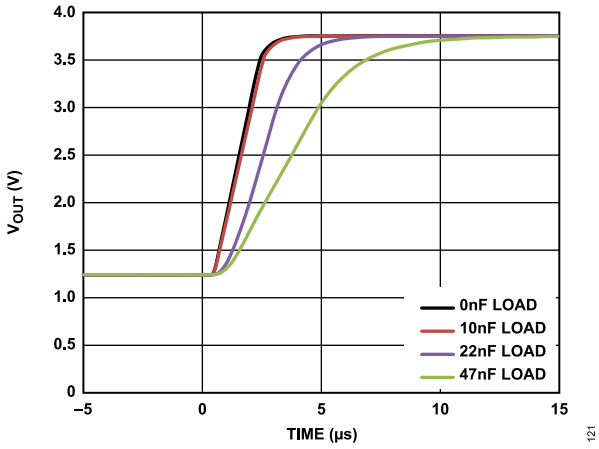

Figure 27. DAC Settling Time for Various Capacitive Loads

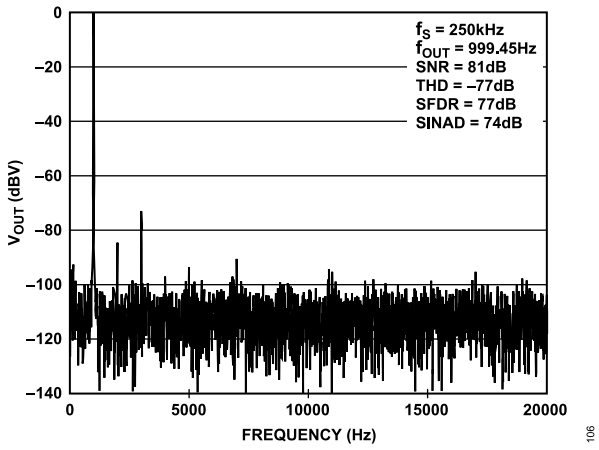

Figure 28. DAC Sine Wave Output, Output Range = 0 V to 2 × V_{REF}, Bandwidth = 0 Hz to 20 kHz

TYPICAL PERFORMANCE CHARACTERISTICS

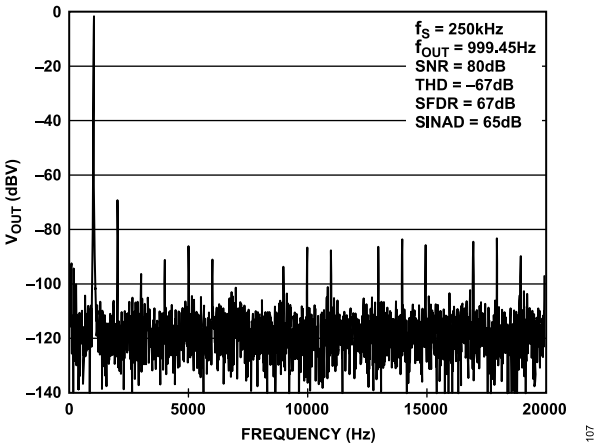

Figure 29. DAC Sine Wave Output, Output Range = 0 V to V_{REF}, Bandwidth = 0 Hz to 20 kHz

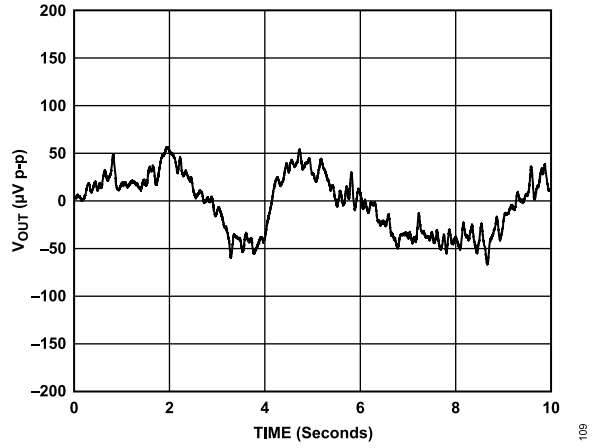

Figure 30. DAC 1/f Noise with External Reference

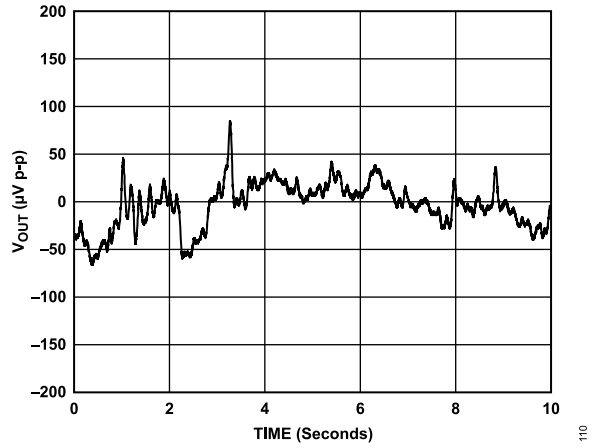

Figure 31. DAC 1/f Noise with Internal Reference

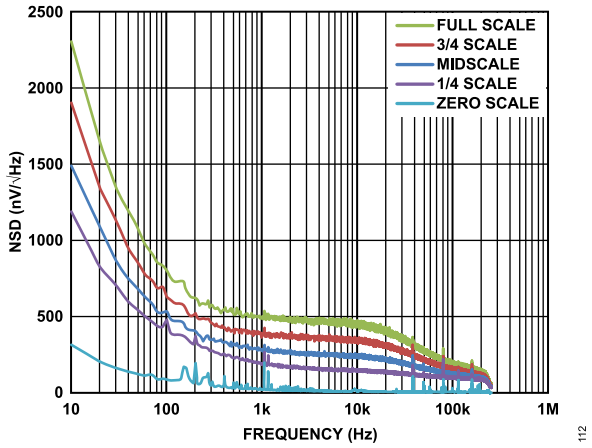

Figure 32. DAC Output Noise Spectral Density (NSD)

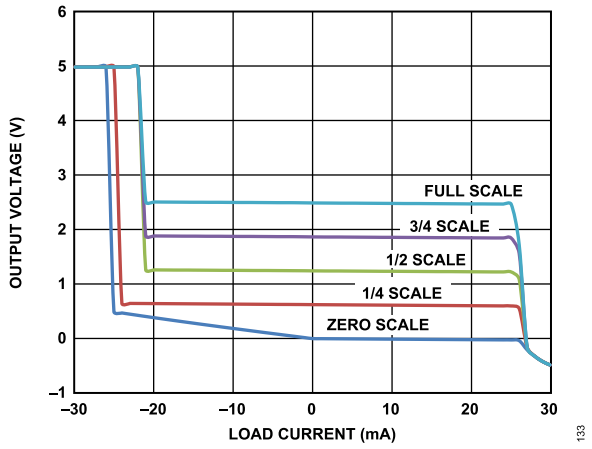

Figure 33. DAC Output Sink and Source Capability, Output Range = 0 V to V_{REF}

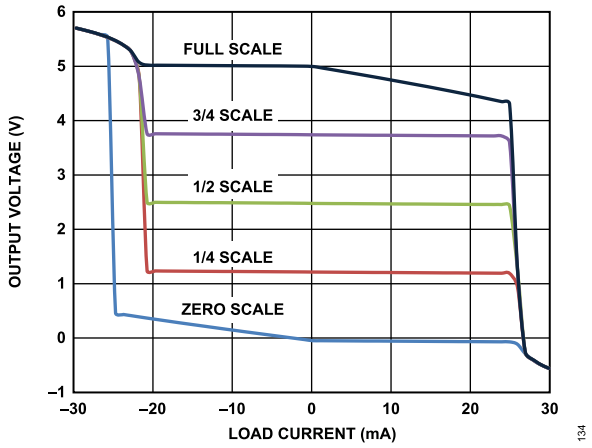

Figure 34. DAC Output Sink and Source Capability, Output Range = 0 V to 2 × V_{REF}

TYPICAL PERFORMANCE CHARACTERISTICS

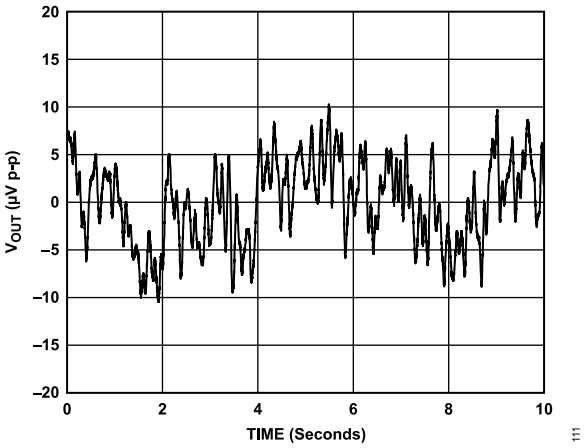

Figure 35. Internal Reference 1/f Noise

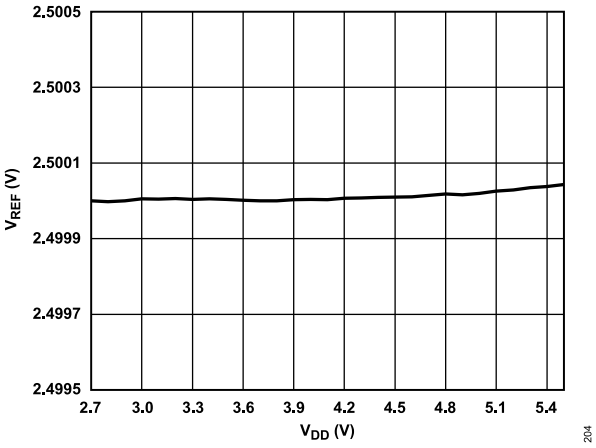

Figure 37. Reference Line Regulation

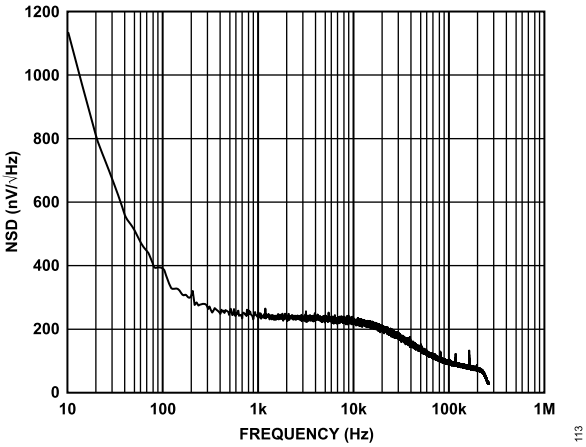

Figure 36. Reference Noise Spectral Density (NSD)

TERMINOLOGY

ADC TERMINOLOGY

Integral Nonlinearity (INL)

INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The end-points of the transfer function are zero scale, a point that is 1 LSB below the first code transition, and full scale, a point that is 1 LSB above the last code transition.

Differential Nonlinearity (DNL)

DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

Offset error is the deviation of the first code transition (00 … 000) to (00 … 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match

Offset error match is the difference in offset error between any two channels.

Gain Error

Gain error is the deviation of the last code transition (111 … 110) to (111 … 111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error has been adjusted out.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale, 5 kHz sine wave signal to all non-selected ADC input channels and determining how much that signal is attenuated in the selected channel. This specification is the worst case across all ADC channels for the AD5592R/AD5592R-1.

Track-and-Hold Acquisition Time

The track-and-hold amplifier enters hold mode on the falling edge of $\overline{SYNC}$ and returns to track mode when the conversion is complete. The track-and-hold acquisition time is the minimum time required for the track-and-hold amplifier to remain in track mode for its output to reach and settle to within ±1 LSB of the applied input signal, given a step change to the input signal.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the measured ratio of signal-to-noise-and-distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$SINAD\ (\text{dB}) = 6.02N + 1.76 \quad (1)$$

Thus, for a 12-bit converter, SINAD is 74 dB.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD5592R/AD5592R-1, it is defined as

$$THD\ (dB) = 20 \times \log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1} \quad (2)$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

DAC TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 18.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 19.

Zero Code Error

Zero code error is a measurement of the output error when zero code (0x000) is loaded to the DAC register. Ideally, the output is 0 V. The zero code error is always positive in the AD5592R/AD5592R-1 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero code error is expressed in mV.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

TERMINOLOGY

Gain Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error

Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV, in the linear region of the transfer function. Offset error can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for a full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change and is measured from the rising edge of $\overline{SYNC}$.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FF to 0x800).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough

Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC maintained at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa), then executing software LDAC (see Table 21), and monitoring the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth; the multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The voltage reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as follows:

$$TC = \left[\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(NOM)} \times Temp\ Range}\right] \times 10^6 \quad (3)$$

where:

$V_{REF(MAX)}$ is the maximum reference output measured over the total temperature range.

$V_{REF(MIN)}$ is the minimum reference output measured over the total temperature range.

$V_{REF(NOM)}$ is the nominal reference output voltage, 2.5 V.

Temp Range is the specified temperature range of −40°C to +125°C.

THEORY OF OPERATION

The AD5592R/AD5592R-1 are 8-channel configurable analog and digital input/output ports. The AD5592R/AD5592R-1 have eight pins that can be independently configured as a 12-bit DAC output channel, a 12-bit ADC input channel, a digital input pin, or a digital output pin.

The function of each pin is determined by programming the ADC, DAC, or GPIO configuration registers as appropriate. See the Configuring the AD5592R/AD5592R-1 section and Table 12 for more information.

DAC SECTION

The AD5592R/AD5592R-1 contain eight 12-bit DACs and implement a segmented string DAC architecture with an internal output buffer. Figure 38 shows the internal block diagram of the DAC architecture.

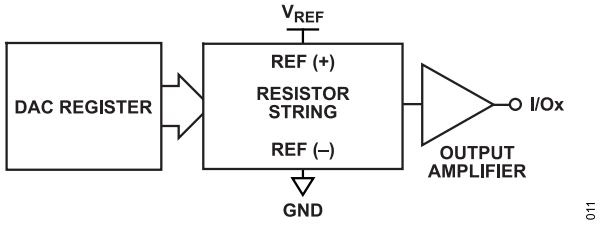

Figure 38. Internal Block Diagram of the DAC Architecture

The DAC channels have a shared gain bit that sets the output range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. Because the gain bit is shared by all channels, it is not possible to set different output ranges on a per channel basis. The input coding to the DAC is straight binary. The ideal output voltage is given by

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D}{2^N}\right) \quad (4)$$

where:
D is the decimal equivalent of the binary code (0 to 4095) that is loaded to the DAC register.
G = 1 for an output range of 0 V to V_{REF}, or *G* = 2 for an output range of 0 V to 2 × V_{REF}. *N* = 12.

Resistor String

The simplified segmented resistor string DAC structure is shown in Figure 39. The code loaded to the DAC register determines the switch on the string that is connected to the output buffer.

Because each resistance in the string has the same value, R, the string DAC is guaranteed monotonic.

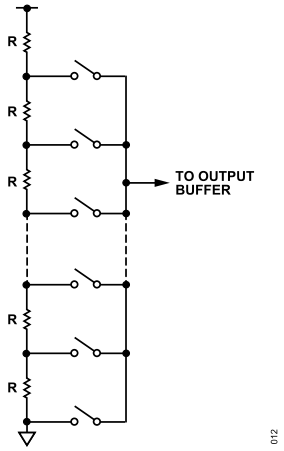

Figure 39. Simplified Resistor String Structure

Output Buffer

The output buffer is designed as an input/output rail-to-rail buffer. The output buffer can drive 2 nF capacitance with a 1 kΩ resistor in parallel. The slew rate is 1.25 V/µs with a ¼ to ¾ scale settling time of 6 µs. By default, the DAC outputs update directly after data has been written to the input register. The LDAC register is used to delay the updates until additional channels have been written to, if required. See the Readback and LDAC Mode Register section for more information.

DAC Output Range

The DAC output voltage range can be configured to 0 V to V_{REF} (gain = 1) or 0 V to 2 × V_{REF} (gain = 2) using the DAC range bit of the general-purpose control register, as shown in Figure 40 and Figure 41, respectively. When V_{REF} = V_{DD}, the 0 V to 2 × V_{REF} range does not allow the DAC to swing the output beyond V_{DD}.

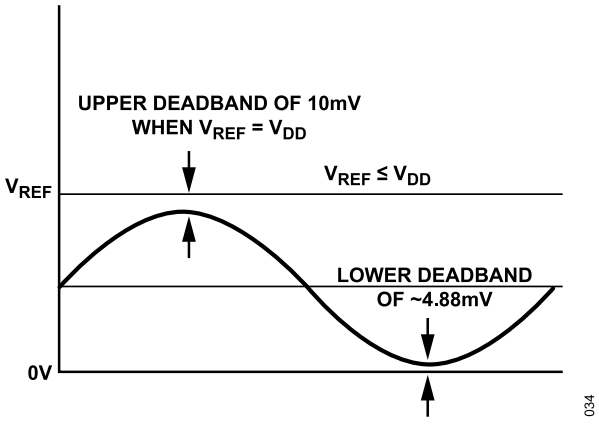

Figure 40. Output Voltage Range of the DAC with Gain = 1 (Unloaded Condition)

THEORY OF OPERATION

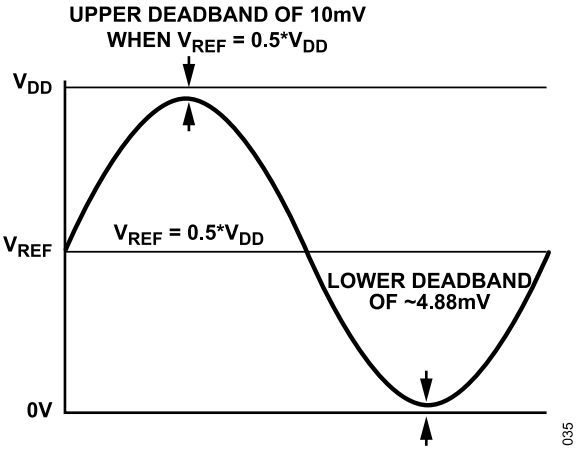

Figure 41. Output Voltage Range of the DAC with Gain = 2 (Unloaded Condition)

When $V_{REF} = V_{DD}$ for gain = 1 or $V_{REF} = 0.5 \times V_{DD}$ for gain = 2, there is an upper dead band of 10 mV at the DAC channel output in unloaded conditions. Additionally, there is a lower dead band of ~4.88 mV at the DAC channel output in unloaded conditions. When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the DAC channel. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV.

ADC SECTION

The 12-bit, single-supply ADC is capable of throughput rates of 400 kSPS. The ADC is preceded by a multiplexer that switches selected I/Ox pins to the ADC. A sequencer is included to automatically switch the multiplexer to the next selected channel. Channels are selected for conversion by writing to the ADC sequence register. When the write to the ADC sequence register has completed, the first channel in the conversion sequence is put into track mode. Allow each channel to track the input signal for a minimum of 500 ns. The first $\overline{SYNC}$ falling edge following the write to the ADC sequence register begins the conversion of the first channel in the sequence. The next $\overline{SYNC}$ falling edge starts a conversion on the second channel in the sequence and also begins to clock the first ADC result onto the serial interface. ADC data is clocked out of the AD5592R/AD5592R-1 in a 16-bit frame. Bit 15 is 0 to indicate that the data contains ADC data, Bits[14:12] are the binary representation of the ADC address, and Bits[11:0] represent the ADC result (see Table 30).

Each conversion takes 2 µs, and the conversion must be completed before another conversion is initiated. Only write to the AD5592R/AD5592R-1 when no conversion is taking place. I/O7 can be configured as a $\overline{BUSY}$ signal to indicate when a conversion is taking place. $\overline{BUSY}$ goes low while a conversion is in progress, and high when an ADC result is available. The ADC has an input range selection bit (Bit 5 in the General-Purpose Control Register section, Table 17), which sets the input range as 0 V to V_{REF} or 0 V to 2 × V_{REF}. All input channels share the same range. The output coding of the ADC is straight binary. It is possible to set each I/Ox pin as both a DAC and an ADC. When an I/Ox pin is set as both a DAC and an ADC, the primary function is that of the DAC. If the pin is selected for inclusion in an ADC conversion sequence, the voltage on the pin is converted and made available via the serial interface, allowing the DAC voltage to be monitored.

Calculating ADC Input Current

The current flowing into the I/Ox pins configured as ADC inputs vary with the sampling rate (f_S), the voltage difference between successive channels (V_{DIFF}), and whether buffered or unbuffered mode is used. Figure 42 shows a simplified version of the ADC input structure. When a new channel is selected for conversion, the 5.8 pF capacitor must be charged or discharged of the voltage that was on the previously selected channel. The time required by the charge or discharge depends on the voltage difference between the two channels. This affects the input impedance of the multiplexer and therefore the input current flowing into the I/Ox pins. In buffered mode, Switch S1 is open and Switch S2 is closed, in which case the U1 buffer is directly driving the 23.1 pF capacitor, and its charging time is negligible. In unbuffered mode, Switch S1 is closed and Switch S2 is closed. In unbuffered mode, the 23.1 pF capacitor must be charged from the I/Ox pins, which contributes to the input current. For applications where the ADC input current is too high, an external input buffer may be required. The choice of buffer is a function of the particular application.

Calculate the input current for buffered mode as follows:

$$f_S \times C \times V_{DIFF} + 1\ nA$$

where:
f_S is the ADC sample rate in Hertz.
C is the sampling capacitance in Farads.
V_{DIFF} is the voltage change between successive channels.
1 nA is the dc leakage current associated with buffered mode.

Calculate the input current for unbuffered mode as follows:

$$f_S \times C \times V_{DIFF}$$

An example solution is as follows: for the ADC input current in buffered mode, where I/O0 = 0.5 V, I/O1 = 2 V, and f_S = 10 kHz,

$$(10{,}000 \times 5.8 \times 10^{-12} \times 1.5) + 1\ nA = 88\ nA$$

Under the same conditions, the ADC input current in unbuffered mode is as follows:

$$(10{,}000 \times 28.9 \times 10^{-12} \times 1.5) = 433.5\ nA$$

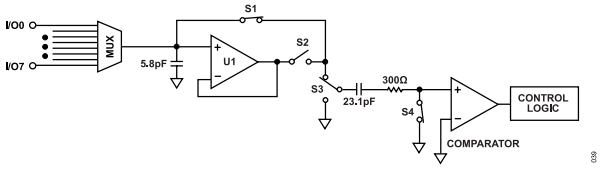

Figure 42. ADC Input Structure

THEORY OF OPERATION

GPIO SECTION

Each of the eight I/Ox pins can be configured as a general-purpose digital input pin by programming the GPIO read configuration register (see the GPIO Read Configuration Register section) or as a digital output pin by programming the GPIO write configuration register (see the GPIO Write Configuration Register section). When an I/Ox pin is configured as an output, the pin can be set high or low by programming the GPIO write data register (see the GPIO Write Data Register section). Logic levels for general-purpose outputs are relative to V_{DD} and GND. When an I/Ox pin is configured as an input, its status can be determined by setting Bit 10 in the GPIO read configuration register. The next SPI operation clocks out the state of the GPIO pins. When an I/Ox pin is set as an output, it is possible to read its status by also setting it as an input pin. When reading the status of the I/Ox pins set as inputs, the status of an I/Ox pin set as both an input and output pin is also returned.

INTERNAL REFERENCE

The AD5592R/AD5592R-1 contain an on-chip 2.5 V reference. The reference is powered down by default and is enabled by setting Bit 9 in the power-down/reference control register (see the Power-Down/Reference Control Register section). When the on-chip reference is powered up, the reference voltage appears on the V_{REF} pin and may be used as a reference source for other components. When the internal reference is used, it is recommended to decouple the internal reference to GND using a 100 nF capacitor. It is recommended that the internal reference be buffered before using it elsewhere in the system. When the reference is powered down, an external reference must be connected to the V_{REF} pin. Suitable external reference sources for the AD5592R/AD5592R-1 include the AD780, AD1582, ADR431, REF193, and ADR391.

$\overline{\text{RESET}}$ FUNCTION

The AD5592R has an asynchronous $\overline{\text{RESET}}$ pin. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ resets all registers to their default values and reconfigures the I/Ox pins to their default values (85 kΩ pull-down to GND). The reset function takes 250 µs maximum; do not write new data to the AD5592R during this time. The AD5592R has a software reset that performs the same function as the $\overline{\text{RESET}}$ pin. The reset function is activated by writing 0x5AC to the software reset register (see the Software Reset Register section).

TEMPERATURE INDICATOR

The AD5592R/AD5592R-1 contain an integrated temperature indicator, which can be read to provide an estimation of the die temperature. The temperature reading can be used in fault detection where a sudden rise in die temperature may indicate a fault condition such as a shorted output. Temperature readback is enabled by setting Bit 8 in the ADC sequence register (see the ADC Sequence Register section) to 1. The temperature result is then added to the ADC sequence. The temperature result has an address of 0b1000 (see the Temperature Reading Format section, Table 31); take care that this result is not confused with the readback from the DAC0 channel. The temperature conversion takes 5 µs with the ADC buffer enabled and 20 µs when the buffer is disabled. Calculate the temperature by using the following formulae:

For ADC gain = 1,

$$Temperature\ (°C) = 25 + \frac{(ADC\ Code - (0.5 / V_{REF}) \times 4095)}{(2.654 \times (2.5 / V_{REF}))}$$

For ADC gain = 2,

$$Temperature\ (°C) = 25 + \frac{(ADC\ Code - (0.5 / (2 \times V_{REF})) \times 4095)}{(1.327 \times (2.5 / V_{REF}))}$$

The range of codes returned by the ADC when reading from the temperature indicator is approximately 645 to 1084 (for ADC gain = 1), corresponding to a temperature between −40°C (T_A) and +125°C (T_J). The accuracy of the temperature indicator, averaged over five samples, is typically 3°C.

SERIAL INTERFACE

The AD5592R/AD5592R-1 have a serial interface ($\overline{SYNC}$, SCLK, SDI, and SDO), which is compatible with SPI standards, as well as with most DSPs. The input shift register is 16 bits wide (see Table 10). The MSB (Bit 15) determines what type of write function is required. When Bit 15 is 0, a write to the control register is selected. The control register address is selected by Bits[14:11]. Bits[10:9] are reserved and are 0s. Bits[8:0] set the data that is written to the selected control register. When Bit 15 is 1, data is written to a DAC channel (assuming that channel has been set to be a DAC). Bits[14:12] select which DAC is addressed. Bits[11:0] are the 12-bit data loaded to the selected DAC, with Bit 11 being the MSB of the DAC data. Table 13 shows the control register map for the AD5592R/AD5592R-1. The register map allows the operation of each of the I/Ox pins to be configured. ADCs can be selected for inclusion in sampling sequences. DACs can be updated individually or simultaneously (see the LDAC Mode Operation section). GPIO settings are also controlled via the register map.

Table 10. Input Shift Register Format

MSB															LSB
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Control register address				0	0	Control register data								
1	DAC address				12-bit DAC data										

SERIAL INTERFACE

POWER-UP TIME

When power is applied to the AD5592R/AD5592R-1, the power-on reset block begins to configure the device and to load the registers with their default values. The configuration process takes 250 µs; do not write to any of the registers during this time.

WRITE MODE

Figure 4 shows the read and write timing for the AD5592R/AD5592R-1. A write sequence begins by bringing the $\overline{SYNC}$ line low. Data on SDI is clocked into the 16-bit shift register on the falling edge of SCLK. After the 16th falling clock edge, the last data bit is clocked in. $\overline{SYNC}$ is brought high, and the programmed function is executed (that is, a change in a DAC input register or a change in a control register). $\overline{SYNC}$ must be brought high for a minimum of 20 ns before the next write. All interface pins must be operated close to the V_{DD} or V_{LOGIC} rails to minimize power consumption in the digital input buffers.

READ MODE

The AD5592R/AD5592R-1 allow data readback from the ADCs and control registers via the serial interface. ADC conversions are automatically clocked out on the serial interface as part of a sequence or as a single ADC conversion. Reading from a register first requires a write to the readback and LDAC mode register to select the register to read back. The contents of the selected register are clocked out on the next 16 SCLKs following a falling edge of $\overline{SYNC}$. Note that due to timing requirements of t_{10} (25 ns), the maximum speed of the SPI interface during a read operation must not exceed 20 MHz.

During the ADC conversion cycle, only the ADC conversion result and the temperature reading results can be read back and all other read requests are ignored.

CONFIGURING THE AD5592R/AD5592R-1

The AD5592R/AD5592R-1 I/Ox pins are configured by writing to a series of configuration registers. The control registers are accessed when the MSB of a serial write is 0, as shown in Table 10. The control register map for the AD5592R/AD5592R-1 is shown in Table 13. At power-up, the I/Ox pins are configured as 85 kΩ pull-down resistors connected to GND.

The input/output channels of the AD5592R/AD5592R-1 can be configured to operate as DAC outputs, ADC inputs, digital outputs, digital inputs, three-state, or connected to GND with 85 kΩ pull-down resistors. When configured as digital outputs, the I/Ox pins have the additional option of being configured as push/pull or open-drain. The input/output channels are configured by writing to the appropriate configuration registers, as shown in Table 11 and Table 12 (see the Register Map section). To assign a particular function to an input/output channel, the user writes to the appropriate register and sets the corresponding bit to 1. For example, setting Bit 0 in the DAC configuration register to 1 configures I/O0 as a DAC (see Table 19). See the Register Map section for details.

In the event that the bit for an input/output channel is set in multiple configuration registers, the input/output channel takes the function dictated by the last write operation. The exceptions to this rule are that an I/Ox pin can be set as both a DAC and an ADC or as a digital input and output. When an I/Ox pin is configured as a DAC and ADC, its primary function is as a DAC, and the ADC can measure the voltage being provided by the DAC. This feature can monitor the output voltage to detect short circuits or overload conditions.

When a pin is configured as both a general-purpose input and output, the primary function is as an output pin. This configuration allows the status of the output pin to be determined by reading the GPIO register. Figure 43 shows a typical configuration example where I/O0 and I/O1 are configured as ADCs, I/O2 and I/O3 are configured as DACs, I/O4 is a general-purpose output pin, I/O5 is a general-purpose input pin, and I/O6 and I/O7 are three-state.

The general-purpose control register (see the General-Purpose Control Register section) also contains other functions associated with the DAC and ADC, such as the lock configuration bit. When the lock configuration (IO_LOCK) bit is set to 1, any writes to the pin configuration registers are ignored, thus preventing the function of the I/Ox pins from being changed.

The I/Ox pins can be reconfigured at any time when the AD5592R/AD5592R-1 is in an idle state, that is, no ADC conversions are taking place and no registers are being read back. The lock configuration bit must also be 0.

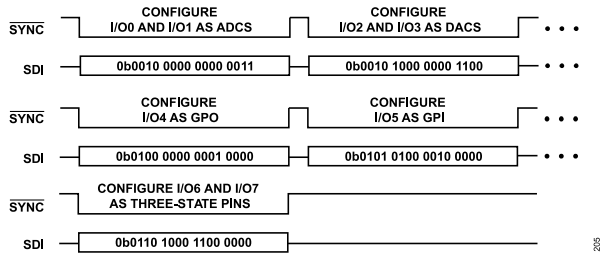

Figure 43. Typical Configuration Example

Table 11. I/Ox Pin Configuration Registers

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Register address				Reserved			IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0

SERIAL INTERFACE

Table 12. Bit Descriptions for the I/Ox Pin Configuration Registers

Bit(s)	Bit Name	Description
15	MSB	Set this bit to 0.
[14:11]	Register address	Selects which pin configuration register is addressed. 0100: ADC pin configuration. 0101: DAC pin configuration. 0110: pull-down configuration (default condition at power-up). 1000: GPIO write configuration. 1010: GPIO read configuration. 1100: GPIO open-drain configuration. 1101: three-state configuration.
[10:8]	Reserved	Reserved. Set these bits to 0.
[7:0]	IO7 to IO0	Enable register function on selected I/Ox pin. 0: no function selected. 1: set the selected I/Ox pin to the register function.

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GENERAL-PURPOSE CONTROL REGISTER

The general-purpose control register (see the General-Purpose Control Register section) enables or disables certain functions associated with the DAC, ADC, and I/Ox pin configuration (see Table 17). The general-purpose control register sets the gain of the DAC and ADC. Bit 5 sets the input range for the ADC, and Bit 4 sets the output range of the DAC.

The general-purpose control register also enables/disables the ADC buffer and precharge function (see the ADC Section section for more details). The register can also be used to lock the I/Ox pin configuration to prevent accidental change. When Bit 7 (IO_LOCK bit) is set to 1, writes to the configuration registers are ignored.

DAC WRITE OPERATION

To set a pin as a DAC, set the appropriate bit in the DAC pin configuration register to 1 (see Table 19). For example, setting Bit 0 to 1 enables I/O0 as a DAC output. Data is written to a DAC when the MSB (Bit 15) of the serial write is 1. Bits[14:12] determine which DAC is addressed, and Bits[11:0] contain the 12-bit data to be written to the DAC, as shown in Table 29. Data is written to the selected DAC input register. Data written to the input register can be automatically copied to the DAC register, if required. Data is transferred to the DAC register based on the setting of the LDAC mode register (see Table 21).

LDAC Mode Operation

When the LDAC mode bits (Bits[1:0]) are 00 respectively, new data is automatically transferred from the input register to the DAC register, and the analog output updates. When the LDAC mode bits are 01, data remains in the input register. This LDAC mode allows writes to input registers without affecting the analog outputs. When the input registers have been loaded with the desired values, setting the LDAC mode bits to 10 transfers the values in the input registers to the DAC registers, and the analog outputs update simultaneously. The LDAC mode bits then revert back to 01, assuming their previous setting was 01 (see Table 21).

DAC READBACK

The input register of each DAC can be read back via the SPI interface. Reading back the DAC register value can be used to confirm that the data was received correctly before writing to the LDAC register, or to check what value was last loaded to a DAC. Data can only be read back from a DAC when there is no ADC conversion sequence taking place.

To read back a DAC input register, it is first necessary to enable the readback function and select which DAC register is required. This is achieved by writing to the DAC read back register (see Table 15). Set the Bits[4:3] to 11 to enable the readback function. Bits[2:0] select which DAC data is required. The DAC data is clocked out of the AD5592R/AD5592R-1 on the subsequent SPI operation. Figure 44 shows an example of setting I/O3, configured as a DAC, to midscale. The input data is then read back. Bits[14:12] contain the address of the DAC register being read back, and Bit 15 is 1 (see Table 32).

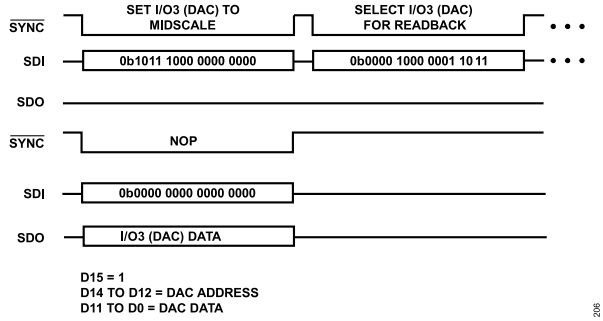


Figure 44. DAC Readback Operation

ADC OPERATION

To set a pin as an ADC, set the appropriate bit in the ADC pin configuration register to 1 (see Table 18). For example, setting Bit 0 to 1 enables I/O0 as an ADC input. The ADC channels of the AD5592R/AD5592R-1 operate as a traditional multichannel ADC, where each serial transfer selects the next channel for conversion. Writing to the ADC sequence register (see the ADC Sequence Register section and Table 16) selects the ADC channels to be included in the sequence, and the REP bit determines if the sequence is repeated. The $\overline{\text{SYNC}}$ signal is used to frame the write to the converter on the SDI pin. The data that appears on the SDO pin during the initial write to the ADC sequence register is invalid. When the sequence register is written to, the ADC begins to track the first channel in the sequence. Tracking takes 500 ns; do not initiate a conversion until this time has passed. The next $\overline{\text{SYNC}}$ falling edge initiates a conversion on the selected channel. The subsequent $\overline{\text{SYNC}}$ falling edge begins clocking out the ADC result and also initiates the next conversion. The ADC operates with one cycle latency. Thus, the conversion result corresponding to each conversion is available one serial read cycle after the cycle in which the conversion was initiated. Note that for a valid ADC conversion, the first falling edge of SCLK must occur within the time t_4 (mentioned in Table 3 and Table 4) after every falling edge of $\overline{\text{SYNC}}$ (see Figure 5).

If more than one channel is selected in the ADC sequence register, the ADC converts all selected channels sequentially in ascending order on successive $\overline{\text{SYNC}}$ falling edges. Once all the selected channels in the sequence register are converted, the ADC repeats the sequence if the REP bit is set. If the REP bit is clear, the ADC goes three-state. Figure 45 to Figure 48 show typical ADC modes of operation. I/O7 can be configured as a $\overline{\text{BUSY}}$ output pin to indicate when a conversion result is available. $\overline{\text{BUSY}}$ goes low while a conversion takes place and goes high when the conversion result is available. The conversion result is clocked out on the SDO pin on the following read/write operation. For an ADC conversion, Bit 15 is 0, Bits[14:12] contain the ADC address, and Bits[11:0] contain the

SERIAL INTERFACE

12-bit conversion result, as shown in the ADC Conversion Result Format section, Table 30.

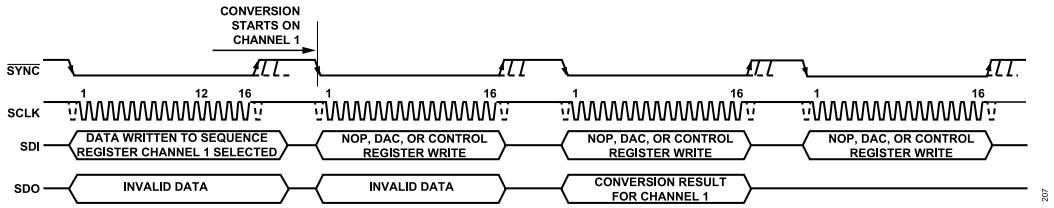


Figure 45. Single-Channel ADC Conversion Sequence, No Repeat

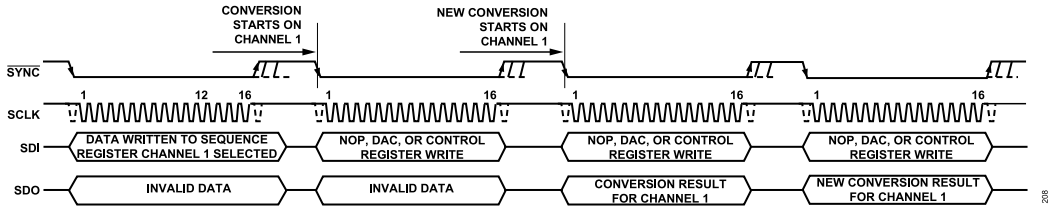


Figure 46. Single-Channel, Repeating, ADC Conversion Sequence

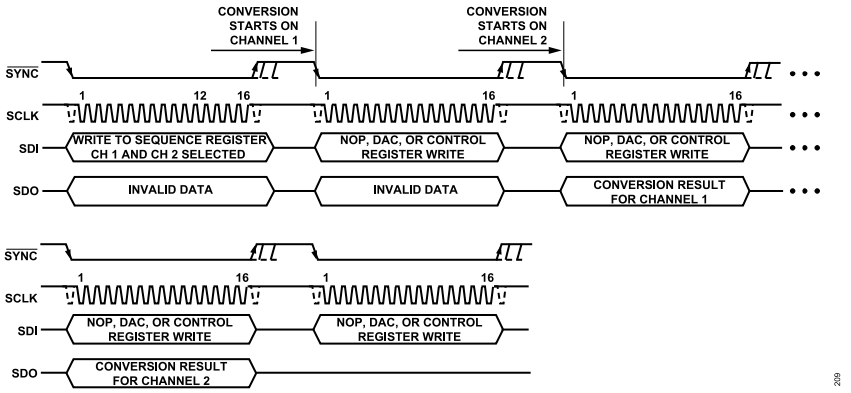


Figure 47. Multichannel ADC Conversion Sequence, No Repeat

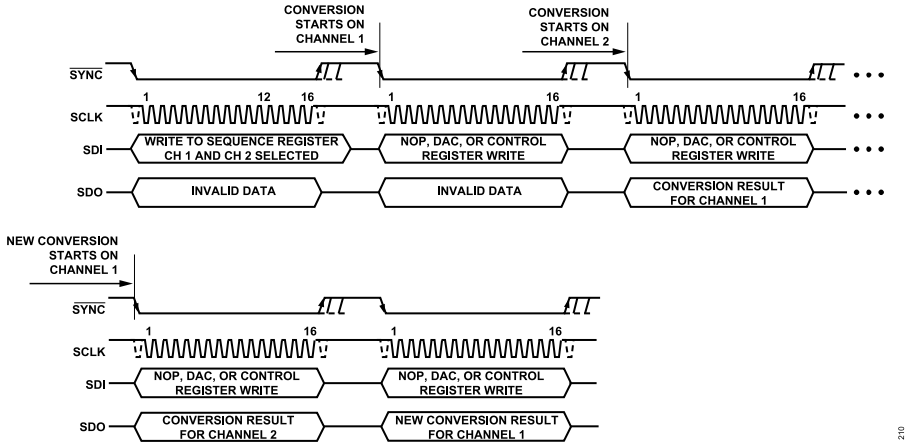


Figure 48. Multichannel, Repeating, ADC Conversion Sequence

SERIAL INTERFACE

Changing an ADC Sequence

The channels included in an ADC sequence can be changed by first stopping an existing conversion sequence (see Figure 49). The ADC conversion sequence is stopped by clearing the REP, TEMP, and ADC7 to ADC0 bits in the ADC sequence register (see the ADC Sequence Register section) to 0.

As the command to stop the sequence is written, an ADC conversion is also taking place. This conversion must finish before a new sequence can be written to the ADC sequence register. Allow a minimum of 2 µs between starting the write to end the current sequence and starting the write to select a new sequence. After selecting the new sequence, allow an ADC track time of 500 ns before initiating the next conversion.

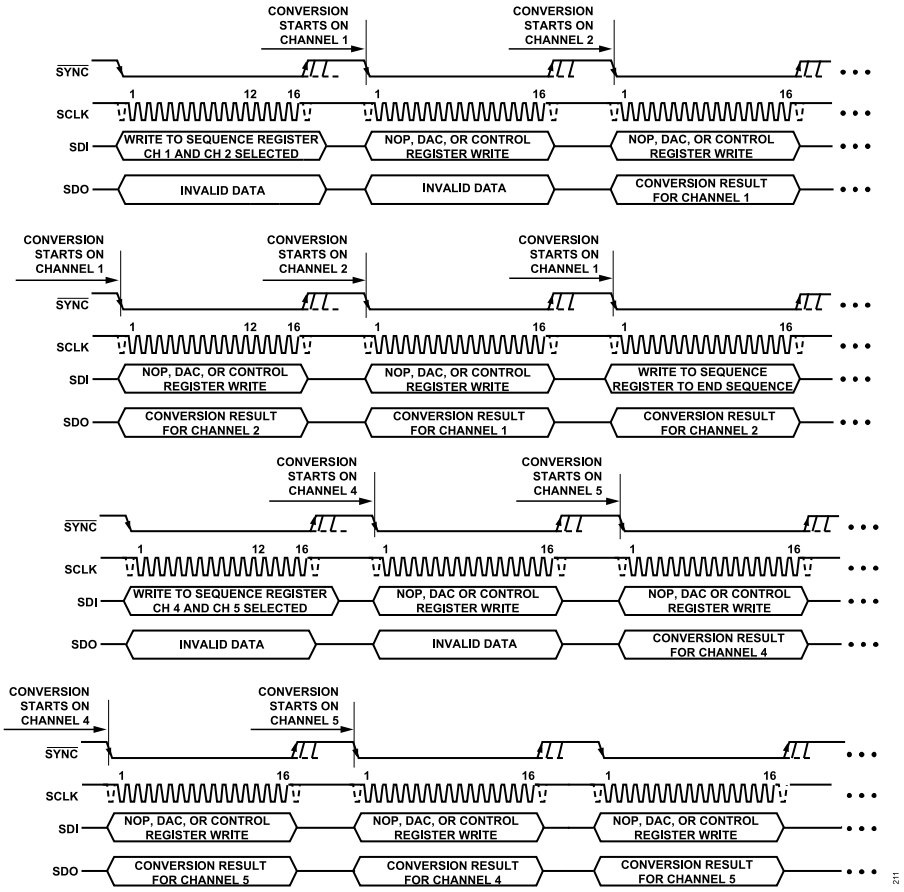


Figure 49. Changing a Multichannel, Repeating, ADC Conversion Sequence

SERIAL INTERFACE

ADC Conversion Result

For every selected channel in the ADC sequencer, the ADC conversion result is clocked out on SDO in the format given in Table 30. The ADC channel address is provided along with the 12-bit ADC data for every valid ADC conversion result. Use the ADC channel address while assigning the ADC data for further processing.

GPIO OPERATION

Each of the I/Ox pins of the AD5592R/AD5592R-1 can operate as a general-purpose, digital input or output pin. The function of the pins is determined by writing to the appropriate bit in the GPIO read configuration register (see the GPIO Read Configuration Register section) and the GPIO write configuration register (see the GPIO Write Configuration Register section).

Setting Pins as Outputs

To set a pin as a general-purpose output, set the appropriate bit in the GPIO write configuration register to 1 (see Table 22). For example, setting Bit 0 to 1 enables I/O0 as a general-purpose output. The state of the output pin is controlled by setting or clearing the bits in the GPIO write data register (see the GPIO Write Data Register section and Table 23). A data bit is ignored if it is written to a location that is not configured as an output.

The outputs can be independently configured as push/pull or open-drain outputs. When in a push/pull configuration, the output is driven to V_{DD} or GND, as determined by the data in the GPIO write data register. To set a pin as an open-drain output, set the appropriate bit in the GPIO open-drain configuration register to 1 (see the GPIO Open-Drain Configuration Register section and Table 26). When in an open-drain configuration, the output is driven to GND when a data bit in the GPIO write data register sets the pin low. When the pin is set high, the output is not driven and must be pulled high by an external resistor. Open-drain configuration allows for multiple output pins to be tied together. If all the pins are normally high, the open-drain configuration allows for one pin to pull down the others pins. This method is commonly used where multiple pins are used to trigger an alarm or an interrupt pin.

To change the state of the I/Ox pins, a write to the GPIO write data register (see the GPIO Write Data Register section) is required. Setting a bit to 1 gives a Logic 1 on the selected output. Clearing a bit to 0 gives a Logic 0 on the selected output.

Setting Pins as Inputs

To set a pin as a general-purpose input, set the appropriate bit in the GPIO read configuration register to 1 (see the GPIO Read Configuration Register section and Table 24). For example, setting Bit 0 to 1 enables I/O0 as a general-purpose input. To read the state of the general-purpose inputs, write to the GPIO read configuration register to set Bit 10 to 1 and also any of Bits[7:0] that correspond to a general-purpose input pin. The following SPI operation clocks out the state of any pins set as general-purpose inputs. Figure 50 shows an example where I/O4 to I/O7 are set as general-purpose inputs. I/O3 is assumed to be a DAC. To read the status of I/O7 to I/O4, Bit 10 and Bits[7:4] are set to 1. To read the status of I/O5 and I/O4, only Bit 10, Bit 5, and Bit 4 need to be set to 1. The status of I/O7 and I/O6 are not read, and Bits[7:6] are read as 0. Figure 50 also has a write to a DAC to show that other operations can be included when reading the status of the general-purpose pins.

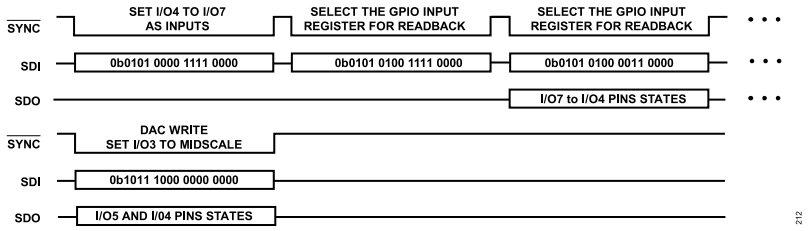


Figure 50. Configuring and Reading General-Purpose Input Pins

SERIAL INTERFACE

THREE-STATE PINS

The I/Ox pins can be set to three-state by writing to the three-state configuration register, as shown in the Three-State Configuration Register section and Table 27.

85 KΩ PULL-DOWN RESISTOR PINS

The I/Ox pins can be connected to GND via a pull-down resistor (85 kΩ) by setting the appropriate bits in the pull-down configuration register, as shown in the Pull-Down Configuration Register section and Table 20.

POWER-DOWN MODE

The AD5592R/AD5592R-1 have a power configuration register to reduce the power consumption when certain functions are not needed. The power-down register allows any channels set as DACs to be individually placed in a power-down state. When in a power-down state, the DAC outputs are three-state. When a DAC channel is put back into normal mode, the DAC output returns to its previous value. The internal reference and its buffer are powered down by default and are enabled by setting the EN_REF bit in the power-down register. The internal reference voltage then appears at the V_{REF} pin.

There is no dedicated power-down function for the ADC, but the ADC is automatically powered down if none of the I/Ox pins are selected as ADCs. The PD_ALL bit powers down all the DACs, the reference and its buffer, and the ADC simultaneously. The Power-Down/Reference Control Register section shows the power-down register.

RESET FUNCTION

The AD5592R/AD5592R-1 can be reset to their default conditions by writing to the software reset register, as shown in the Software Reset Register section and Table 28. This write resets all registers to their default values and reconfigures the I/Ox pins to their default values (85 kΩ pull-down resistor to GND). The reset function takes 250 µs maximum; do not write new data to the AD5592R/AD5592R-1 during this time. The AD5592R has a $\overline{\text{RESET}}$ pin that performs the same function. For normal operation, $\overline{\text{RESET}}$ is tied high. A falling edge on $\overline{\text{RESET}}$ triggers the reset function.

READBACK AND LDAC MODE REGISTER

The values contained in the AD5592R/AD5592R-1 registers can be read back to ensure that the registers are correctly set up. The register readback is initiated by writing to the configuration register readback and LDAC mode register (see the Configuration Register Readback and LDAC Mode Register section and Table 21) with Bit 6 set to 1. Bits[5:2] select which register is to be read back. The register data is clocked out of the AD5592R/AD5592R-1 on the next SPI transfer.

Bits[1:0] of the configuration register readback and LDAC mode register select the LDAC mode. The LDAC mode determines if data written to a DAC input register is also transferred to the DAC register. See the LDAC Mode Operation section for details of the LDAC mode function.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5592R/AD5592R-1 is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal. The devices require a 16-bit data-word with data valid on the falling edge of SCLK.

AD5592R/AD5592R-1 TO SPI INTERFACE

The SPI interface of the AD5592R/AD5592R-1 is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 51 shows the AD5592R/AD5592R-1 connected to the Analog Devices, Inc., ADSP-BF531 Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5592R/AD5592R-1.

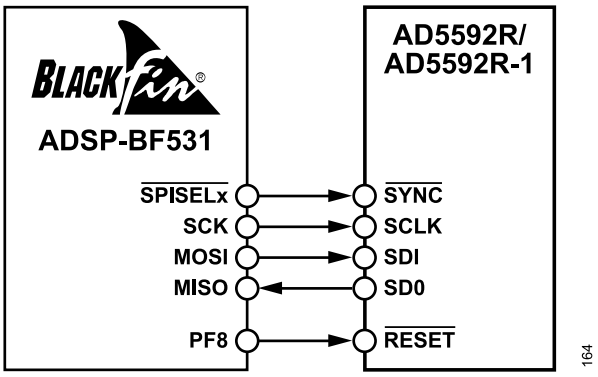


Figure 51. ADSP-BF531 SPI Interface

AD5592R/AD5592R-1 TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has two serial ports (SPORT). Figure 52 shows how a SPORT interface can be used to control the AD5592R/AD5592R-1. The ADSP-BF527 has an SPI port that can also be used. This method is the same as when using the ADSP-BF531.

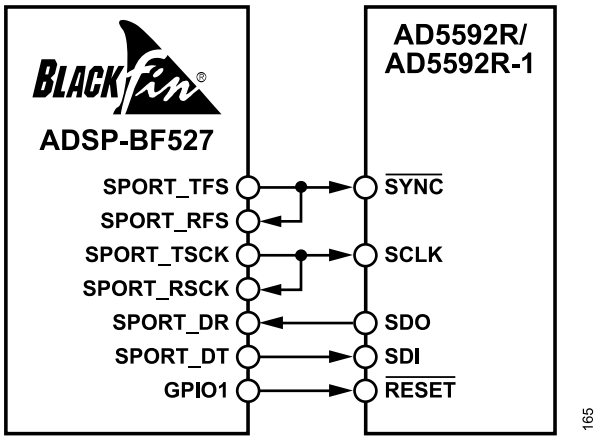


Figure 52. ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board (PCB) on which the AD5592R or the AD5592R-1 is mounted must be designed so that the AD5592R/AD5592R-1 lie on the analog plane.

The AD5592R/AD5592R-1 must have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI). Ceramic capacitors, for example, provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

REGISTER MAP

The AD5592R/AD5592R-1 has programmable user configuration registers that are used to configure the device. Table 13 shows a complete list of the user configuration registers. See the Register Details: AD5592R/AD5592R-1 Control Register Map section for details about the functions of each of the bits.

The Data Format Details: AD5592R/AD5592R-1 ADC and DAC Readback section provides data formats for the ADC and the DAC readback.

REGISTER SUMMARY: AD5592R/AD5592R-1 CONTROL REGISTER MAP

Table 13. AD5592R/AD5592R-1 Control Register Summary

MSB Bit 15	Address Bits[14:11]	Register Name	Register Description	Default Value Bits[10:0]
0	0000	NOP	NOP. No operation.	0x000
0	0001	DAC_RD	DAC Readback Register. Selects and enables DAC readback.	0x000
0	0010	ADC_SEQ	ADC Sequence Register. Selects ADCs for conversion.	0x000
0	0011	GEN_CTRL_REG	General-Purpose Control Register. DAC and ADC control register.	0x000
0	0100	ADC_CONFIG	ADC Pin Configuration Register. Selects which pins are ADC inputs.	0x000
0	0101	DAC_CONFIG	DAC Pin Configuration Register. Selects which pins are DAC outputs.	0x000
0	0110	PULLDWN_CONFIG	Pull-Down Configuration Register. Selects which pins have an 85 kΩ pull-down resistor to GND.	0x0FF
0	0111	CONFIG_READ_AND_LDAC	Configuration Register readback and LDAC Mode Register. Selects the operation of the Load DAC (LDAC) function and/or which configuration register is read back.	0x000
0	1000	GPIO_CONFIG[1]	GPIO Write Configuration Register. Selects which pins are general-purpose outputs.	0x000
0	1001	GPIO_OUTPUT	GPIO Write Data Register. Writes data to the general-purpose outputs.	0x000
0	1010	GPIO_INPUT	GPIO Read Configuration Register. Selects which pins are general-purpose inputs	0x000
0	1011	PD_REF_CTRL	Power-Down/Reference Control Register. Powers down DACs and enables/disables the reference.	0x000
0	1100	GPIO_OPENDRAIN_CONFIG	GPIO Open-Drain Configuration Register. Selects open-drain or push/pull for general-purpose outputs.	0x000
0	1101	IO_TS_CONFIG	Three-State Configuration Register. Selects which pins are three-state.	0x000
0	1111	SW_RESET	Software Reset. Resets the AD5592R/AD5592R-1.	0x000
1	XXX[2]	DAC_WR	DAC Write. Writes to addressed DAC register.	0x000

[1] This register is also used to set I/O7 as a $\overline{\text{BUSY}}$ output.

[2] Bits[14:12] represent the DAC register address.

REGISTER MAP

REGISTER DETAILS: AD5592R/AD5592R-1 CONTROL REGISTER MAP

NOP Register

Name: NOP

No operation.

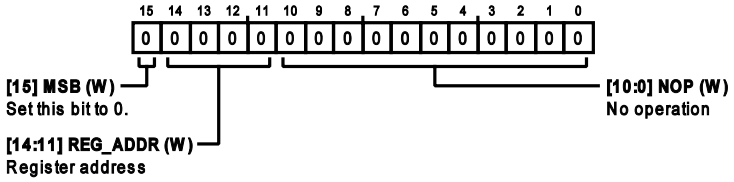


Table 14. Bit Descriptions for NOP

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address.	0x0
[10:0]	NOP	No operation.	0x0

DAC Readback Register

Name: DAC_RD

Selects and enables DAC readback.

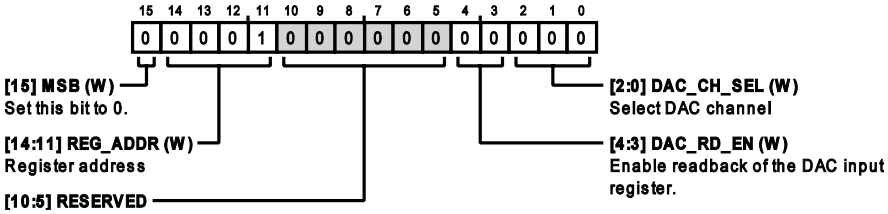


Table 15. Bit Descriptions for DAC_RD

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0001.	0x1
[10:5]	RESERVED	Reserved. Set this bit to 0.	0x0
[4:3]	DAC_RD_EN	Enable readback of the DAC input register. 0: DAC register readback disabled. 1: DAC register readback enabled.	0x0
[2:0]	DAC_CH_SEL	Select DAC channel. 000: DAC0. 001: DAC1. 010: DAC2. 011: DAC3. 100: DAC4. 101: DAC5. 110: DAC6.	0x0

REGISTER MAP

Table 15. Bit Descriptions for DAC_RD (Continued)

Bits	Bit Name	Description	Default Value
		111: DAC7.	

ADC Sequence Register

Name: ADC_SEQ

Selects ADCs for conversion.

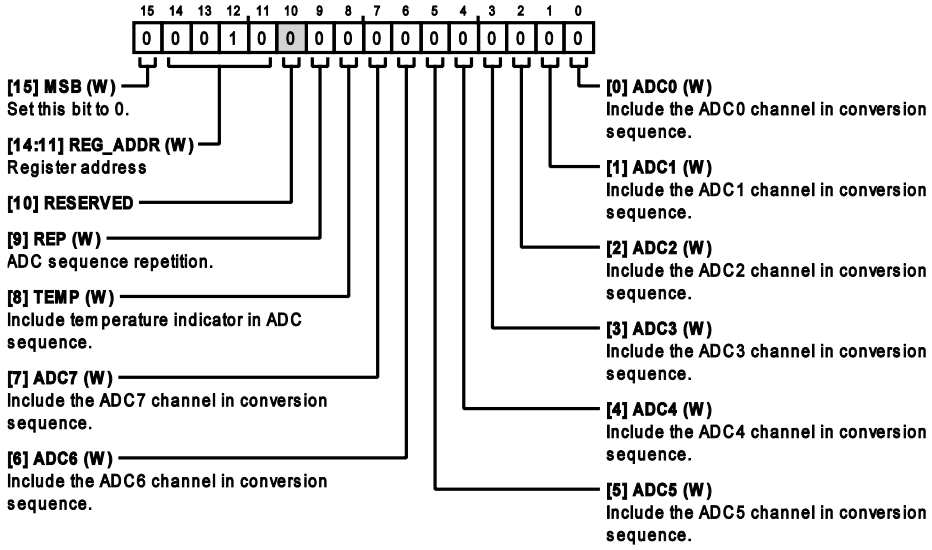


Table 16. Bit Descriptions for ADC_SEQ

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0010.	0x2
10	RESERVED	Reserved. Set this bit to 0.	0x0
9	REP	ADC sequence repetition. 0: Sequence repetition disabled. 1: Sequence repetition enabled.	0x0
8	TEMP	Include temperature indicator in ADC sequence. 0: Disable temperature indicator readback. 1: Enable temperature indicator readback.	0x0
7	ADC7	Include the ADC7 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
6	ADC6	Include the ADC6 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
5	ADC5	Include the ADC5 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
4	ADC4	Include the ADC4 channel in conversion sequence.	0x0

REGISTER MAP

Table 16. Bit Descriptions for ADC_SEQ (Continued)

Bits	Bit Name	Description	Default Value
		0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	
3	ADC3	Include the ADC3 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
2	ADC2	Include the ADC2 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
1	ADC1	Include the ADC1 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0
0	ADC0	Include the ADC0 channel in conversion sequence. 0: The selected ADC channel is not included in the conversion sequence. 1: Include the selected ADC channel in the conversion sequence.	0x0

General-Purpose Control Register

Name: GEN_CTRL_REG

DAC and ADC control register.

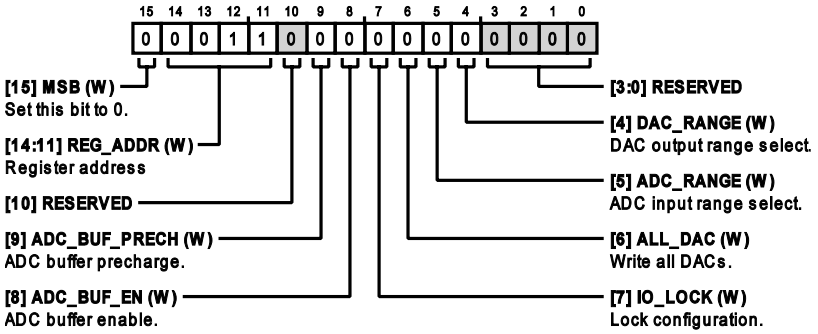


Table 17. Bit Descriptions for GEN_CTRL_REG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0011.	0x3
10	RESERVED	Reserved. Set this bit to 0.	0x0
9	ADC_BUF_PRECH	ADC buffer precharge. 0: ADC buffer is not used to precharge the ADC. If the ADC buffer is enabled, it is always powered up. 1: ADC buffer is used to precharge the ADC. If the ADC buffer is enabled, it is powered up while the conversion takes place and then powered down until the next conversion takes place.	0x0
8	ADC_BUF_EN	ADC buffer enable. 0: ADC buffer is disabled. 1: ADC buffer is enabled.	0x0
7	IO_LOCK	Lock configuration. 0: The contents of the I/Ox pin configuration register can be changed.	0x0

REGISTER MAP

Table 17. Bit Descriptions for GEN_CTRL_REG (Continued)

Bits	Bit Name	Description	Default Value
		1: The contents of the I/Ox pin configuration register cannot be changed.	
6	ALL_DAC	Write all DACs. 0: For future DAC writes, the DAC address bits determine which DAC is written to. 1: For future DAC writes, the DAC address bits are ignored, and all channels configured as DACs are updated with the same data.	0x0
5	ADC_RANGE	ADC input range select. 0: ADC gain is 0 V to V_{REF}. 1: ADC gain is 0 V to 2 × V_{REF}.	0x0
4	DAC_RANGE	DAC output range select. 0: DAC output range is 0 V to V_{REF}. 1: DAC output range is 0 V to 2 × V_{REF}.	0x0
[3:0]	RESERVED	Reserved. Set these bits to 0b0000.	0x0

ADC Pin Configuration Register

Name: ADC_CONFIG

Selects which pins are ADC inputs.

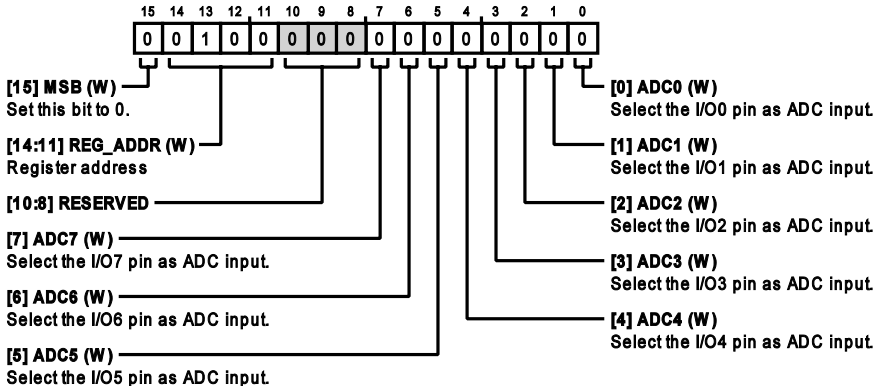


Table 18. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0100.	0x4
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	ADC7	Select the I/O7 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
6	ADC6	Select the I/O6 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
5	ADC5	Select the I/O5 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
4	ADC4	Select the I/O4 pin as ADC input.	0x0

REGISTER MAP

Table 18. Bit Descriptions for ADC_CONFIG (Continued)

Bits	Bit Name	Description	Default Value
		0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	
3	ADC3	Select the I/O3 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
2	ADC2	Select the I/O2 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
1	ADC1	Select the I/O1 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0
0	ADC0	Select the I/O0 pin as ADC input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is an ADC input.	0x0

DAC Pin Configuration Register

Name: DAC_CONFIG

Selects which pins are DAC outputs.

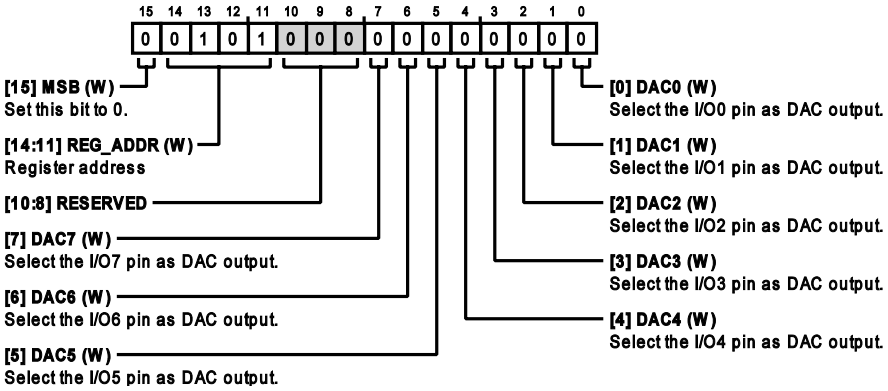


Table 19. Bit Descriptions for DAC_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0101.	0x5
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	DAC7	Select the I/O7 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
6	DAC6	Select the I/O6 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
5	DAC5	Select the I/O5 pin as DAC output.	0x0

REGISTER MAP

Table 19. Bit Descriptions for DAC_CONFIG (Continued)

Bits	Bit Name	Description	Default Value
		0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	
4	DAC4	Select the I/O4 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
3	DAC3	Select the I/O3 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
2	DAC2	Select the I/O2 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
1	DAC1	Select the I/O1 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0
0	DAC0	Select the I/O0 pin as DAC output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a DAC output.	0x0

Pull-Down Configuration Register

Name: PULLDWN_CONFIG

Selects which pins have an 85 kΩ pull-down resistor to GND.

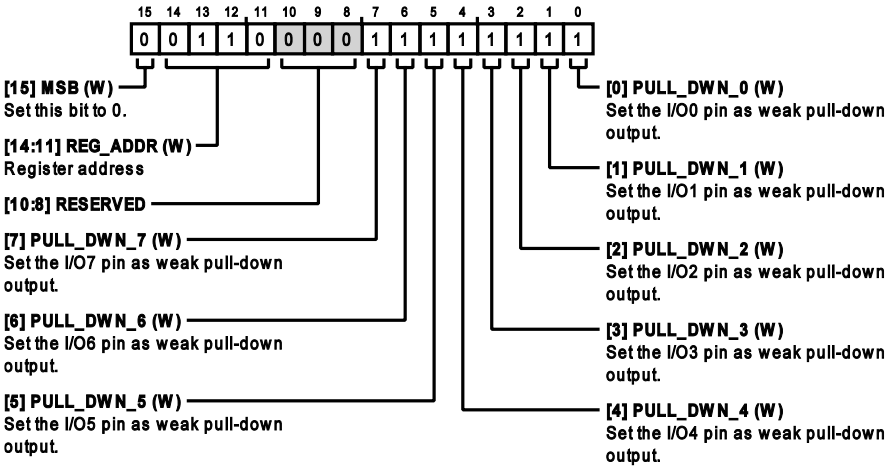


Table 20. Bit Descriptions for PULLDWN_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0110.	0x6
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	PULL_DWN_7	Set the I/O7 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers.	0x1

REGISTER MAP

Table 20. Bit Descriptions for PULLDWN_CONFIG (Continued)

Bits	Bit Name	Description	Default Value
		1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	
6	PULL_DWN_6	Set the I/O6 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
5	PULL_DWN_5	Set the I/O5 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
4	PULL_DWN_4	Set the I/O4 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
3	PULL_DWN_3	Set the I/O3 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
2	PULL_DWN_2	Set the I/O2 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
1	PULL_DWN_1	Set the I/O1 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1
0	PULL_DWN_0	Set the I/O0 pin as weak pull-down output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is connected to GND via an 85 kΩ pull-down resistor.	0x1

Configuration Register Readback and LDAC Mode Register

Name: CONFIG_READ_AND_LDAC

Selects the operation of the Load DAC (LDAC) function and/or which configuration register is read back.

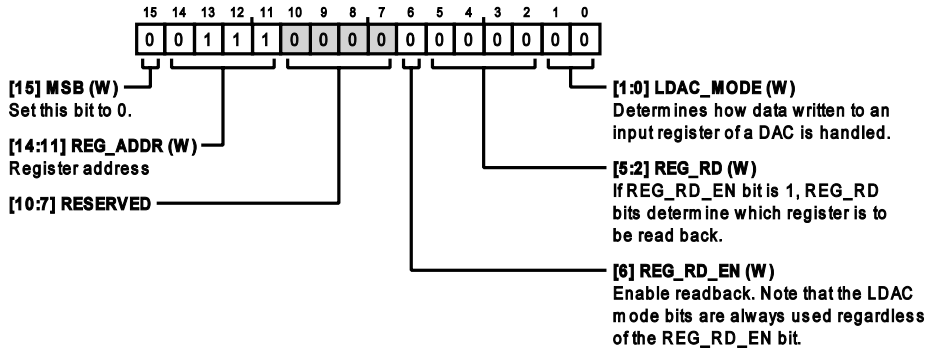


Table 21. Bit Descriptions for CONFIG_READ_AND_LDAC

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b0111.	0x7
[10:7]	RESERVED	Reserved. Set these bits to 0b0000.	0x0

REGISTER MAP

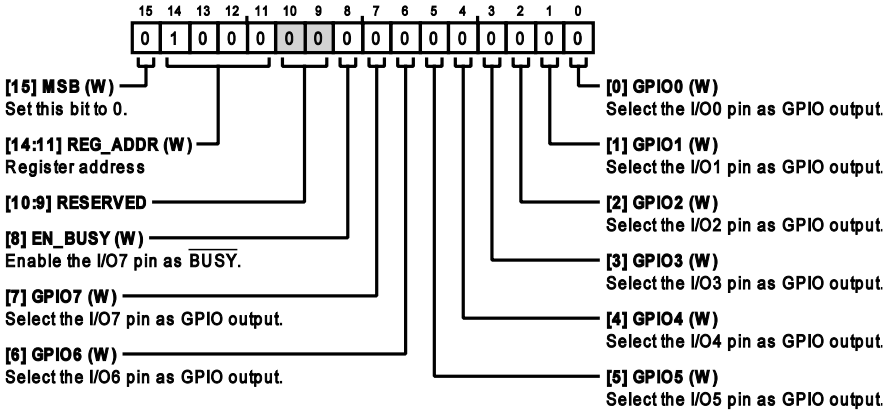
Table 21. Bit Descriptions for CONFIG_READ_AND_LDAC (Continued)

Bits	Bit Name	Description	Default Value
6	REG_RD_EN	Enable Configuration Register readback. Note that the LDAC mode bits are always used regardless of the REG_RD_EN bit. 0: No readback is initiated. 1: REG_RD bits select which register is read back. REG_RD_EN automatically clears when the read is complete.	0x0
[5:2]	REG_RD	If REG_RD_EN bit is 1, REG_RD bits determine which register is to be read back. 0000: NOP. 0001: DAC readback. 0010: ADC sequence. 0011: General-purpose configuration. 0100: ADC pin configuration. 0101: DAC pin configuration. 0110: Pull-down configuration. 0111: LDAC configuration. 1000: GPIO write configuration. 1001: GPIO write data. 1010: GPIO read configuration. 1011: Power-down and reference control. 1100: Open-drain configuration. 1101: Three-state pin configuration. 1111: Software reset.	0x0
[1:0]	LDAC_MODE	Determines how data written to an input register of a DAC is handled. 00: Data written to an input register is immediately copied to a DAC register, and the DAC output updates. 01: Data written to an input register is not copied to a DAC register. The DAC output is not updated. 10: Data in the input registers is copied to the corresponding DAC registers. When the data has been transferred, the DAC outputs are updated simultaneously.	0x0

GPIO Write Configuration Register

Name: GPIO_CONFIG

Selects which pins are general-purpose outputs. This register is used to set I/O7 as a $\overline{\text{BUSY}}$ output.



REGISTER MAP

Table 22. Bit Descriptions for GPIO_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1000.	0x8
[10:9]	RESERVED	Reserved. Set these bits to 0b00.	0x0
8	EN_BUSY	Enable the I/O7 pin as $\overline{\text{BUSY}}$. 0: I/O7 is not configured as $\overline{\text{BUSY}}$. 1: I/O7 pin is configured as $\overline{\text{BUSY}}$. GPIO7 must be set to 1 to enable the I/O7 pin as an output.	0x0
7	GPIO7	Select the I/O7 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
6	GPIO6	Select the I/O6 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
5	GPIO5	Select the I/O5 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
4	GPIO4	Select the I/O4 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
3	GPIO3	Select the I/O3 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
2	GPIO2	Select the I/O2 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
1	GPIO1	Select the I/O1 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0
0	GPIO0	Select the I/O0 pin as GPIO output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose output pin.	0x0

GPIO Write Data Register

Name: GPIO_OUTPUT

Writes data to the general-purpose outputs.

REGISTER MAP

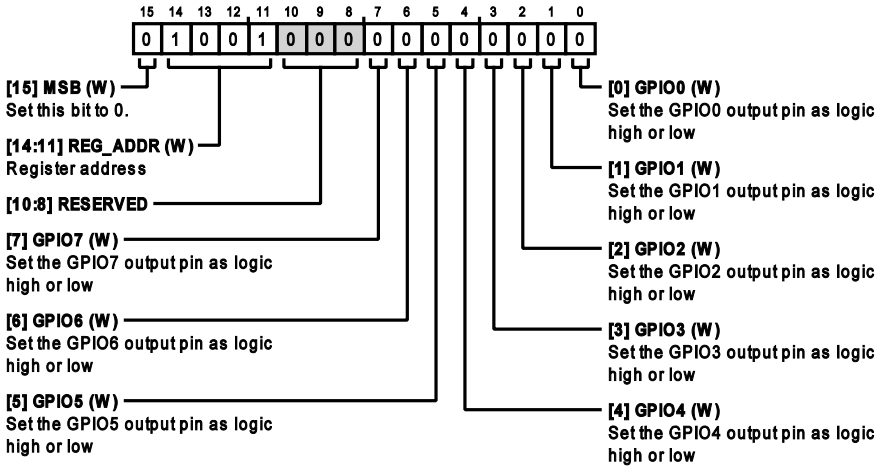


Table 23. Bit Descriptions for GPIO_OUTPUT

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1001.	0x9
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	GPIO7	Set the GPIO7 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
6	GPIO6	Set the GPIO6 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
5	GPIO5	Set the GPIO5 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
4	GPIO4	Set the GPIO4 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
3	GPIO3	Set the GPIO3 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
2	GPIO2	Set the GPIO2 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
1	GPIO1	Set the GPIO1 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0
0	GPIO0	Set the GPIO0 output pin as logic high or low. 0: The I/O pin is a Logic 0 output. 1: The I/O pin is a Logic 1 output.	0x0

REGISTER MAP

GPIO Read Configuration Register

Name: GPIO_INPUT

Selects which pins are general-purpose inputs.

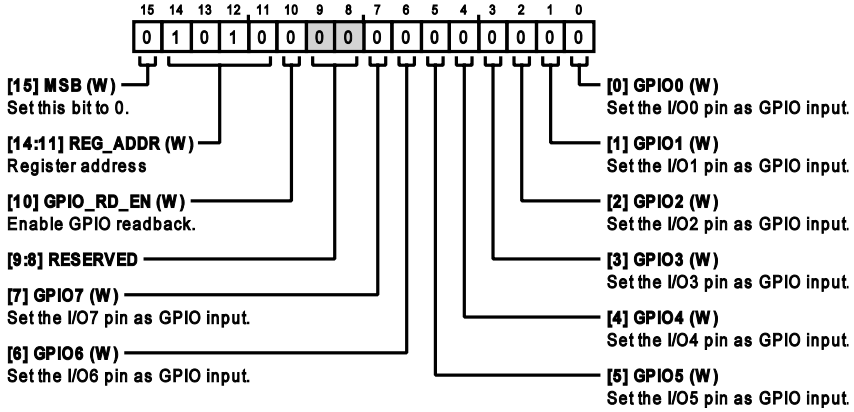


Table 24. Bit Descriptions for GPIO_INPUT

Bits	Bit Name	Description	Default value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1010.	0xA
10	GPIO_RD_EN	Enable GPIO readback. 0: GPIO7 to GPIO0 bits determine which pins are set as general-purpose inputs. 1: The next SPI operation clocks out the state of the GPIO pins.	0x0
[9:8]	RESERVED	Reserved. Set these bits to 0b00.	0x0
7	GPIO7	Set the I/O7 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
6	GPIO6	Set the I/O6 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
5	GPIO5	Set the I/O5 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
4	GPIO4	Set the I/O4 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
3	GPIO3	Set the I/O3 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
2	GPIO2	Set the I/O2 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0
1	GPIO1	Set the I/O1 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0

REGISTER MAP

Table 24. Bit Descriptions for GPIO_INPUT (Continued)

Bits	Bit Name	Description	Default value
0	GPIO0	Set the I/O0 pin as GPIO input. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a general-purpose input pin.	0x0

Power-Down/Reference Control Register

Name: PD_REF_CTRL

Powers down DACs and enables/disables the reference.

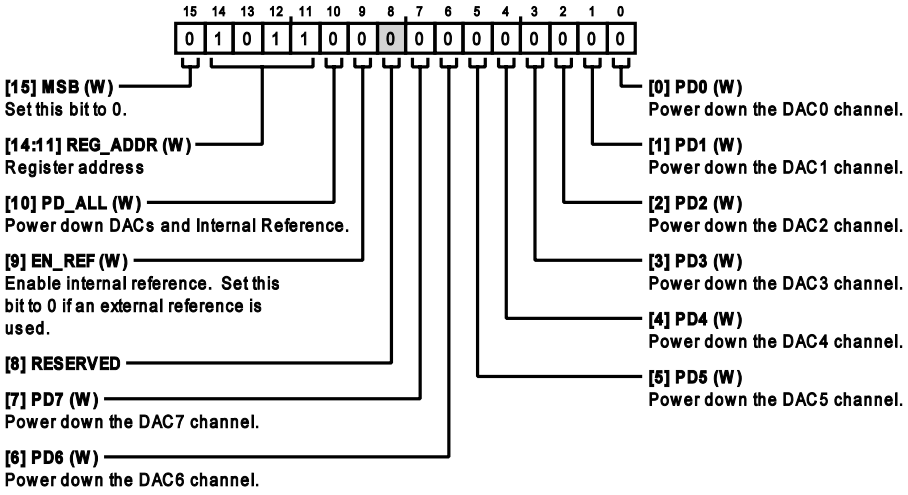


Table 25. Bit Descriptions for PD_REF_CTRL

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1011.	0xB
10	PD_ALL	Power down DACs and Internal Reference. 0: The reference and DACs power-down states are determined by EN_REF and PD7 to PD0 bits. 1: The reference, DACs and ADC are powered down.	0x0
9	EN_REF	Enable internal reference. Set this bit to 0 if an external reference is used. 0: The reference and its buffer are powered down. 1: The reference and its buffer are powered up. The reference is available on the V_{REF} pin.	0x0
8	RESERVED	Reserved. Set this bit to 0.	0x0
7	PD7	Power down the DAC7 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
6	PD6	Power down the DAC6 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
5	PD5	Power down the DAC5 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0

REGISTER MAP

Table 25. Bit Descriptions for PD_REF_CTRL (Continued)

Bits	Bit Name	Description	Default Value
4	PD4	Power down the DAC4 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
3	PD3	Power down the DAC3 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
2	PD2	Power down the DAC2 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
1	PD1	Power down the DAC1 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0
0	PD0	Power down the DAC0 channel. 0: The channel is in normal operating mode. 1: The channel is powered down if it is configured as a DAC.	0x0

GPIO Open-Drain Configuration Register

Name: GPIO_OPENDRAIN_CONFIG

Selects open-drain or push/pull for general-purpose outputs. The selected I/Ox pin must be set as digital output pin in the GPIO_CONFIG register.

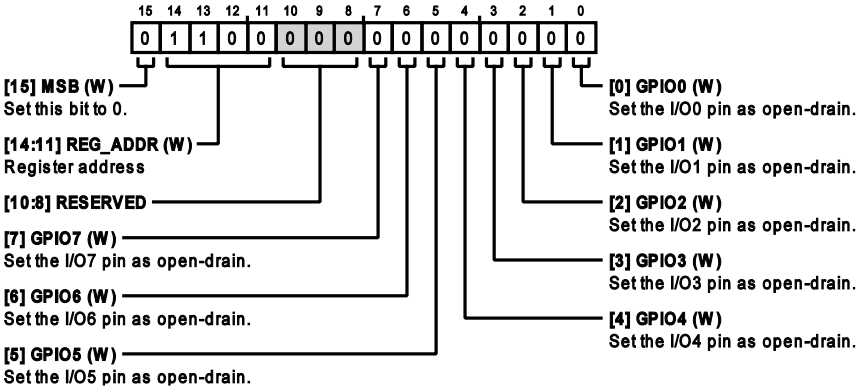


Table 26. Bit Descriptions for GPIO_OPENDRAIN_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1100.	0xC
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	GPIO7	Set the I/O7 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
6	GPIO6	Set the I/O6 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0

REGISTER MAP

Table 26. Bit Descriptions for GPIO_OPENDRAIN_CONFIG (Continued)

Bits	Bit Name	Description	Default Value
5	GPIO5	Set the I/O5 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
4	GPIO4	Set the I/O4 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
3	GPIO3	Set the I/O3 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
2	GPIO2	Set the I/O2 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
1	GPIO1	Set the I/O1 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0
0	GPIO0	Set the I/O0 pin as open-drain. 0: The I/O pin is a push/pull output pin. 1: The I/O pin is an open-drain output pin.	0x0

Three-State Configuration Register

Name: IO_TS_CONFIG

Selects which pins are three-state.

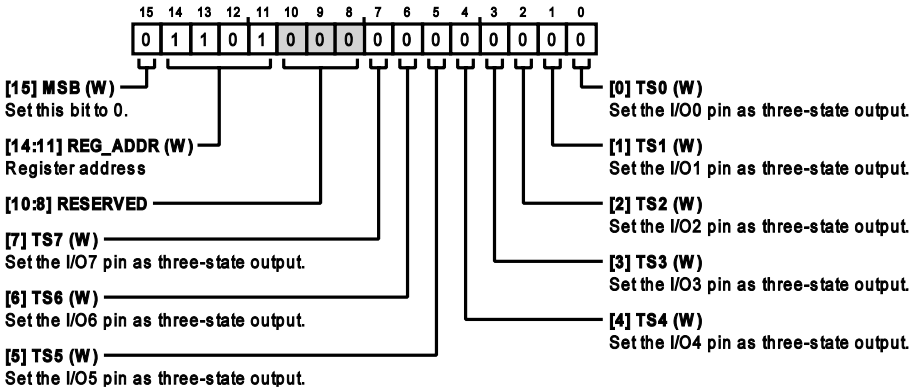


Table 27. Bit Descriptions for IO_TS_CONFIG

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1101.	0xD
[10:8]	RESERVED	Reserved. Set these bits to 0b000.	0x0
7	TS7	Set the I/O7 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0

REGISTER MAP

Table 27. Bit Descriptions for IO_TS_CONFIG (Continued)

Bits	Bit Name	Description	Default Value
6	TS6	Set the I/O6 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
5	TS5	Set the I/O5 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
4	TS4	Set the I/O4 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
3	TS3	Set the I/O3 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
2	TS2	Set the I/O2 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
1	TS1	Set the I/O1 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0
0	TS0	Set the I/O0 pin as three-state output. 0: The I/O pin function is determined by the pin configuration registers. 1: The I/O pin is a three-state output pin.	0x0

Software Reset Register

Name: SW_RESET

Resets the AD5592R/AD5592R-1.

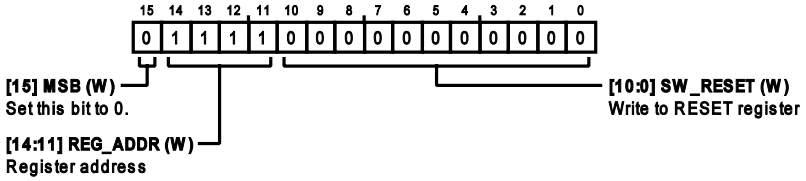


Table 28. Bit Descriptions for SW_RESET

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 0.	0x0
[14:11]	REG_ADDR	Register address. Set these bits to 0b1111.	0xF
[10:0]	SW_RESET	Write to RESET register. 10110101100: Reset the AD5592R/AD5592R-1.	0x0

DAC Write Register

Name: DAC_WR

Writes to addressed DAC register.

REGISTER MAP

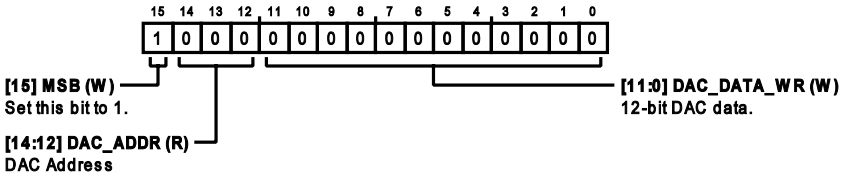


Table 29. Bit Descriptions for DAC_WR

Bits	Bit Name	Description	Default Value
15	MSB	Set this bit to 1.	0x1
[14:12]	DAC_ADDR	DAC Address. 000: DAC0. 001: DAC1. 010: DAC2. 011: DAC3. 100: DAC4. 101: DAC5. 110: DAC6. 111: DAC7.	0x0
[11:0]	DAC_DATA_WR	12-bit DAC data.	0x0

DATA FORMAT DETAILS: AD5592R/AD5592R-1 ADC AND DAC READBACK

ADC Conversion Result Format

Name: ADC_RESULT

ADC Conversion Result.

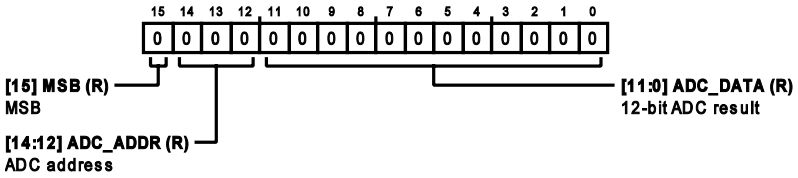


Table 30. Bit Descriptions for ADC_RESULT

Bits	Bit Name	Description
15	MSB	MSB. This bit is read as 0 during ADC channel readback.
[14:12]	ADC_ADDR	ADC address. 000: ADC0. 001: ADC1. 010: ADC2. 011: ADC3. 100: ADC4. 101: ADC5. 110: ADC6. 111: ADC7.
[11:0]	ADC_DATA	12-bit ADC result.

REGISTER MAP

Temperature Reading Format

Name: TMP_SENSE_RESULT

Temperature Reading.

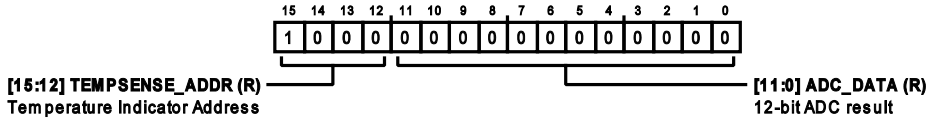


Table 31. Bit Descriptions for TMP_SENSE_RESULT

Bits	Bit Name	Description
[15:12]	TEMPSENSE_ADDR	Temperature Indicator Address. The address is 0b1000 for the temperature reading readback.
[11:0]	ADC_DATA	12-bit ADC result.

DAC Data Read Back Format

Name: DAC_DATA_RD

Read back the 12-bit DAC Input Register Data.

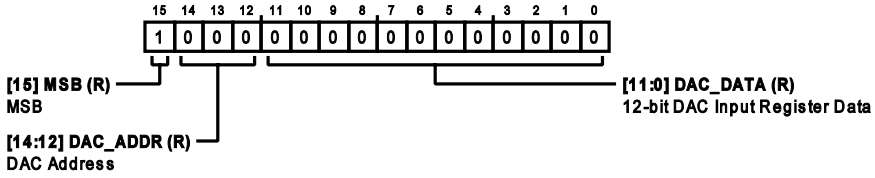


Table 32. Bit Descriptions for DAC_DATA_RD

Bits	Bit Name	Description
15	MSB	MSB. This bit is read as 1 during DAC register read back.
[14:12]	DAC_ADDR	DAC Address. 000: DAC0. 001: DAC1. 010: DAC2. 011: DAC3. 100: DAC4. 101: DAC5. 110: DAC6. 111: DAC7.
[11:0]	DAC_DATA	12-bit DAC Input Register Data.

OUTLINE DIMENSIONS

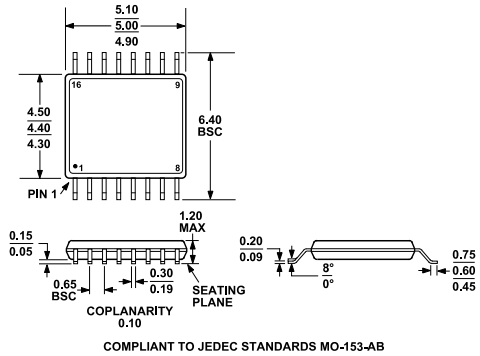


Figure 53. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

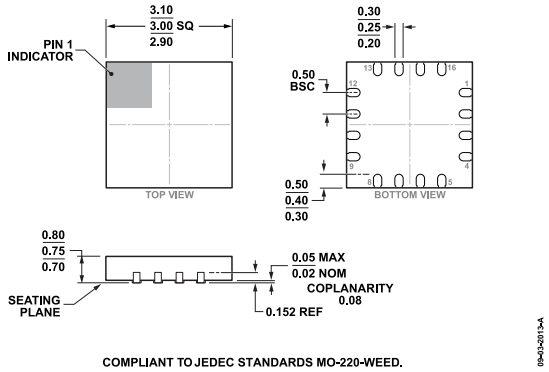


Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-32)
Dimensions shown in millimeters

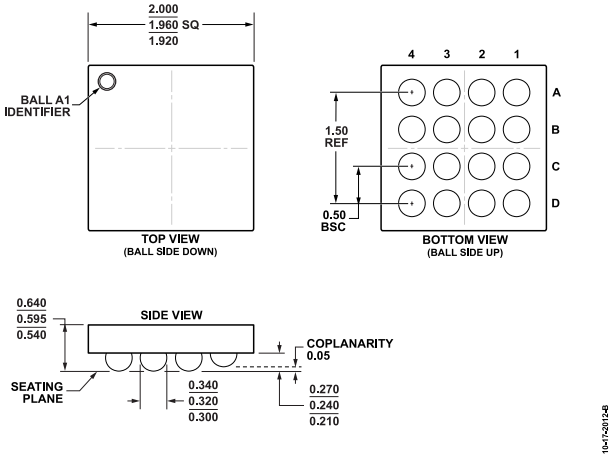


Figure 55. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-3)
Dimensions shown in millimeters