Quad 16-/14-/12-Bit *nano*DAC+ with 2 ppm/°C Reference, I²C Interface

Data Sheet

AD5696R/AD5695R/AD5694R

FEATURES

High relative accuracy (INL): ±2 LSB maximum at 16 bits
Low drift 2.5 V reference: 2 ppm/°C typical
Tiny package: 3 mm × 3 mm, 16-lead LFCSP
Total unadjusted error (TUE): ±0.1% of FSR maximum
Offset error: ±1.5 mV maximum
Gain error: ±0.1% of FSR maximum
High drive capability: 20 mA, 0.5 V from supply rails
User selectable gain of 1 or 2 (GAIN pin)
Reset to zero scale or midscale (RSTSEL pin)
1.8 V logic compatibility
Low glitch: 0.5 nV-sec
400 kHz I²C-compatible serial interface
Low power: 3.3 mW at 3 V
2.7 V to 5.5 V power supply
−40°C to +105°C temperature range

APPLICATIONS

Optical transceivers
Base-station power amplifiers
Process control (PLC I/O cards)
Industrial automation
Data acquisition systems

GENERAL DESCRIPTION

The AD5696R/AD5695R/AD5694R family are low power, quad, 16-/14-/12-bit buffered voltage output DACs. The devices include a 2.5 V, 2 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and exhibit less than 0.1% FSR gain error and 1.5 mV offset error performance. The devices are available in a 3 mm × 3 mm LFCSP and a TSSOP package.

The AD5696R/AD5695R/AD5694R also incorporate a power-on reset circuit and a RSTSEL pin that ensures that the DAC outputs power up to zero scale or midscale and remain there until a valid write takes place. Each part contains a per-channel power-down feature that reduces the current consumption of the device to 4 µA at 3 V while in power-down mode.

The AD5696R/AD5695R/AD5694R use a versatile 2-wire serial interface that operates at clock rates up to 400 kHz, and includes a V_{LOGIC} pin intended for 1.8 V/3 V/5 V logic.

FUNCTIONAL BLOCK DIAGRAM

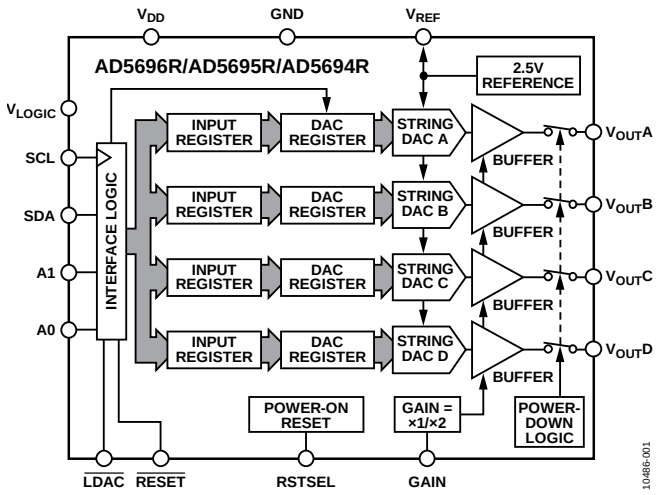

Figure 1.

Table 1. Quad *nano*DAC+ Devices

Interface	Reference	16-Bit	14-Bit	12-Bit
SPI	Internal	AD5686R	AD5685R	AD5684R
	External	AD5686		AD5684
I²C	Internal	AD5696R	AD5695R	AD5694R
	External	AD5696		AD5694

PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).
   AD5696R (16-bit): ±2 LSB maximum.
   AD5695R (14-bit): ±1 LSB maximum.
   AD5694R (12-bit): ±1 LSB maximum.
2. Low Drift 2.5 V On-Chip Reference.
   2 ppm/°C typical temperature coefficient.
   5 ppm/°C maximum temperature coefficient.
3. Two Package Options.
   3 mm × 3 mm, 16-lead LFCSP.
   16-lead TSSOP.

Rev. D **Document Feedback**

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4/2012—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. R_L = 2 kΩ; C_L = 200 pF.

Table 2.

Parameter	A Grade[1]			B Grade[1]			Unit	Test Conditions/Comments
	Min	Typ	Max	Min	Typ	Max		
STATIC PERFORMANCE[2]								
AD5696R								
Resolution	16			16			Bits	
Relative Accuracy		±2	±8		±1	±2	LSB	Gain = 2
		±2	±8		±1	±3		Gain = 1
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design
AD5695R								
Resolution	14			14			Bits	
Relative Accuracy		±0.5	±4		±0.5	±1	LSB	
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design
AD5694R								
Resolution	12			12			Bits	
Relative Accuracy		±0.12	±2		±0.12	±1	LSB	
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design
Zero-Code Error		0.4	4		0.4	1.5	mV	All zeros loaded to DAC register
Offset Error		+0.1	±4		+0.1	±1.5	mV	
Full-Scale Error		+0.01	±0.2		+0.01	±0.1	% of FSR	All ones loaded to DAC register
Gain Error		±0.02	±0.2		±0.02	±0.1	% of FSR	
Total Unadjusted Error		±0.01	±0.25		±0.01	±0.1	% of FSR	External reference; gain = 2; TSSOP
			±0.25			±0.2	% of FSR	Internal reference; gain = 1; TSSOP
Offset Error Drift[3]		±1			±1		µV/°C	
Gain Temperature Coefficient[3]		±1			±1		ppm	Of FSR/°C
DC Power Supply Rejection Ratio[3]		0.15			0.15		mV/V	DAC code = midscale; V_{DD} = 5 V ± 10%
DC Crosstalk[3]								
		±2			±2		µV	Due to single channel, full-scale output change
		±3			±3		µV/mA	Due to load current change
		±2			±2		µV	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{REF}	0		V_{REF}	V	Gain = 1
	0		2 × V_{REF}	0		2 × V_{REF}	V	Gain = 2, see Figure 30
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 1 kΩ
Resistive Load[4]	1			1			kΩ	
Load Regulation		80			80		µV/mA	5 V ± 10%, DAC code = midscale; −30 mA ≤ I_{OUT} ≤ 30 mA
		80			80		µV/mA	3 V ± 10%, DAC code = midscale; −20 mA ≤ I_{OUT} ≤ 20 mA
Short-Circuit Current[5]		40			40		mA	
Load Impedance at Rails[6]		25			25		Ω	See Figure 30
Power-Up Time		2.5			2.5		µs	Coming out of power-down mode; V_{DD} = 5 V

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
REFERENCE OUTPUT								
Output Voltage[7]	2.4975		2.5025	2.4975		2.5025	V	At ambient
Reference TC[8, 9]		5	20		2	5	ppm/°C	See the Terminology section
Output Impedance[3]		0.04			0.04		Ω	
Output Voltage Noise[3]		12			12		µV p-p	0.1 Hz to 10 Hz
Output Voltage Noise Density[3]		240			240		nV/√Hz	At ambient; f = 10 kHz, C_L = 10 nF
Load Regulation Sourcing[3]		20			20		µV/mA	At ambient
Load Regulation Sinking[3]		40			40		µV/mA	At ambient
Output Current Load Capability[3]		±5			±5		mA	V_{DD} ≥ 3 V
Line Regulation[3]		100			100		µV/V	At ambient
Thermal Hysteresis[3]		125			125		ppm	First cycle
		25			25		ppm	Additional cycles
LOGIC INPUTS[3]								
Input Current			±2			±2	µA	Per pin
V_{INL}, Input Low Voltage			0.3 × V_{LOGIC}			0.3 × V_{LOGIC}	V	
V_{INH}, Input High Voltage	0.7 × V_{LOGIC}			0.7 × V_{LOGIC}			V	
Pin Capacitance		2			2		pF	
LOGIC OUTPUTS (SDA)[3]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 3 mA
Floating State Output Capacitance		4			4		pF	
POWER REQUIREMENTS								
V_{LOGIC}	1.62		5.5	1.62		5.5	V	
I_{LOGIC}			3			3	µA	
V_{DD}	2.7		5.5	2.7		5.5	V	Gain = 1
V_{DD}	V_{REF} + 1.5		5.5	V_{REF} + 1.5		5.5	V	Gain = 2
I_{DD}								V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V to 5.5 V
Normal Mode[10]		0.59	0.7		0.59	0.7	mA	Internal reference off
		1.1	1.3		1.1	1.3	mA	Internal reference on, at full scale
All Power-Down Modes[11]		1	4		1	4	µA	−40°C to +85°C
			6			6	µA	−40°C to +105°C

[1] Temperature range: A and B grade: −40°C to +105°C.
[2] DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when V_{REF} = V_{DD} with gain = 1 or when V_{REF}/2 = V_{DD} with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280 (AD5696R), 64 to 16,320 (AD5695R), and 12 to 4080 (AD5694R).
[3] Guaranteed by design and characterization; not production tested.
[4] Channel A and Channel B can have a combined output current of up to 30 mA. Similarly, Channel C and Channel D can have a combined output current of up to 30 mA up to a junction temperature of 110°C.
[5] V_{DD} = 5 V. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature may impair device reliability.
[6] When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = 25 Ω × 1 mA = 25 mV (see Figure 30).
[7] Initial accuracy presolder reflow is ±750 µV; output voltage includes the effects of preconditioning drift. See the Internal Reference Setup section.
[8] Reference is trimmed and tested at two temperatures and is characterized from −40°C to +105°C.
[9] Reference temperature coefficient calculated as per the box method. See the Terminology section for further information.
[10] Interface inactive. All DACs active. DAC outputs unloaded.
[11] All DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 3.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments[3]
Output Voltage Settling Time					
AD5696R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
AD5695R		5	8	µs	¼ to ¾ scale settling to ±2 LSB
AD5694R		5	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		0.8		V/µs	
Digital-to-Analog Glitch Impulse		0.5		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.13		nV-sec	
Digital Crosstalk		0.1		nV-sec	
Analog Crosstalk		0.2		nV-sec	
DAC-to-DAC Crosstalk		0.3		nV-sec	
Total Harmonic Distortion[4]		−80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
Output Noise Spectral Density		300		nV/√Hz	DAC code = midscale, 10 kHz; gain = 2, internal reference
Output Noise		6		µV p-p	0.1 Hz to 10 Hz
SNR		90		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SFDR		83		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz
SINAD		80		dB	At ambient, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical at 25°C.
[4] Digitally generated sine wave at 1 kHz.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V; 1.62 V ≤ V_{LOGIC} ≤ 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. [1]

Table 4.

Parameter[2]	Min	Max	Unit	Conditions/Comments
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100		ns	$t_{SU,DAT}$, data setup time
t_6[3]	0	0.9	µs	$t_{HD,DAT}$, data hold time
t_7	0.6		µs	$t_{SU,STA}$, setup time for repeated start
t_8	0.6		µs	$t_{SU,STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus free time between a stop and a start condition
t_{10}	0	300	ns	t_R, rise time of SCL and SDA when receiving
t_{11}	20 + 0.1C_B[4]	300	ns	t_F, fall time of SDA and SCL when transmitting/ receiving
t_{12}	20		ns	$\overline{\text{LDAC}}$ pulse width
t_{13}	400		ns	SCL rising edge to $\overline{\text{LDAC}}$ rising edge
t_{SP}[5]	0	50	ns	Pulse width of suppressed spike
C_B[4]		400	pF	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization; not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of SCL's falling edge.
[4] C_B is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.
[5] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns.

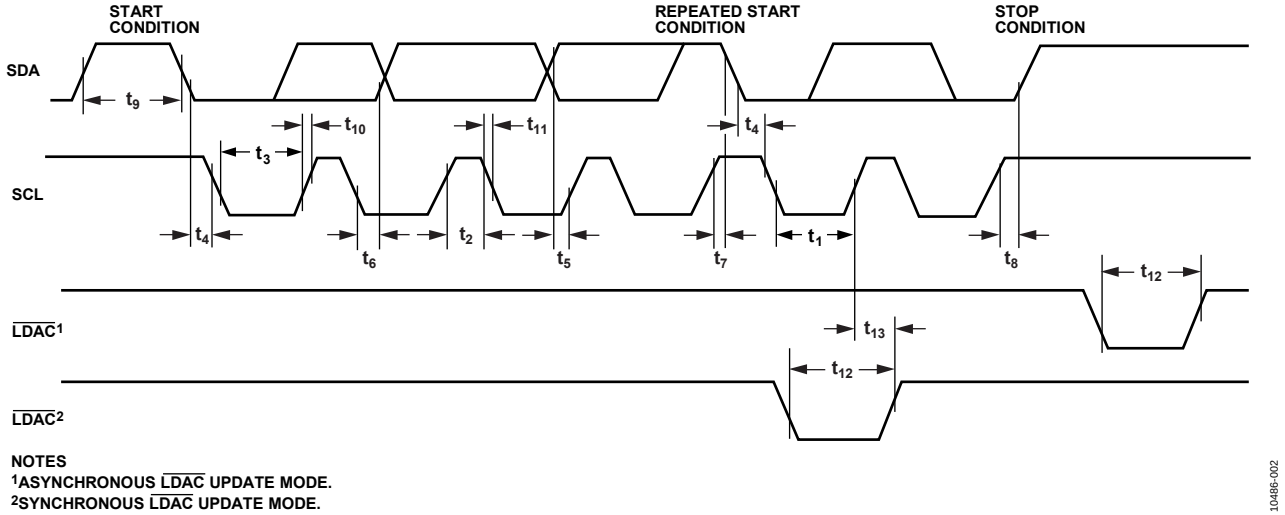


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{LOGIC} to GND	−0.3 V to +7 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND[1]	−0.3 V to V_{LOGIC} + 0.3 V
SDA and SCL to GND	−0.3 V to +7 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	125°C
16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board)	70°C/W
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	260°C

[1] Excluding SDA and SCL.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

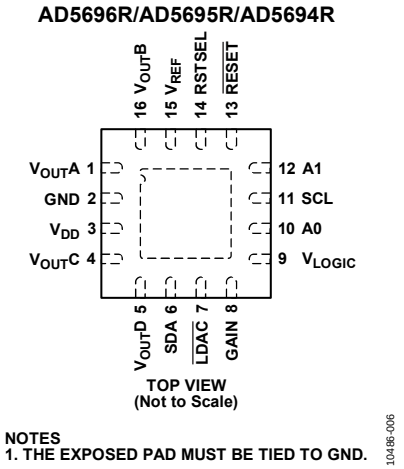


Figure 3. 16-Lead LFCSP Pin Configuration

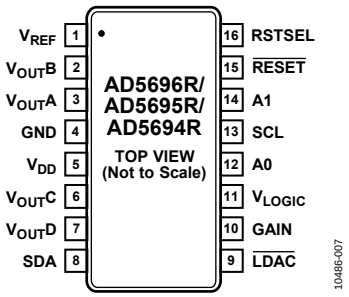


Figure 4. 16-Lead TSSOP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
LFCSP	**TSSOP**	**Mnemonic**	**Description**
1	3	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	4	GND	Ground Reference Point for All Circuitry on the Part.
3	5	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	6	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	7	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
6	8	SDA	Serial Data Input. This pin is used in conjunction with the SCL line to clock data into or out of the 24-bit input shift register. SDA is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
7	9	$\overline{LDAC}$	$\overline{LDAC}$ can be operated in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. This pin can also be tied permanently low.
8	10	GAIN	Span Set Pin. When this pin is tied to GND, all four DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{LOGIC}, all four DACs output a span of 0 V to 2 × V_{REF}.
9	11	V_{LOGIC}	Digital Power Supply. Voltage ranges from 1.62 V to 5.5 V.
10	12	A0	Address Input. Sets the first LSB of the 7-bit slave address.
11	13	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 24-bit input register.
12	14	A1	Address Input. Sets the second LSB of the 7-bit slave address.
13	15	$\overline{RESET}$	Asynchronous Reset Input. The $\overline{RESET}$ input is falling edge sensitive. When $\overline{RESET}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{RESET}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. If the pin is forced low at power-up, the POR circuit does not initialize correctly until the pin is released.
14	16	RSTSEL	Power-On Reset Pin. Tying this pin to GND powers up all four DACs to zero scale. Tying this pin to V_{LOGIC} powers up all four DACs to midscale.
15	1	V_{REF}	Reference Voltage. The AD5696R/AD5695R/AD5694R have a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	2	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
17	N/A	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

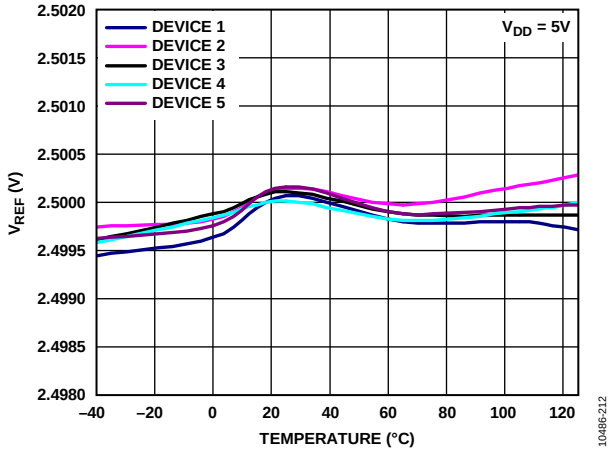


Figure 5. Internal Reference Voltage vs. Temperature (Grade B)

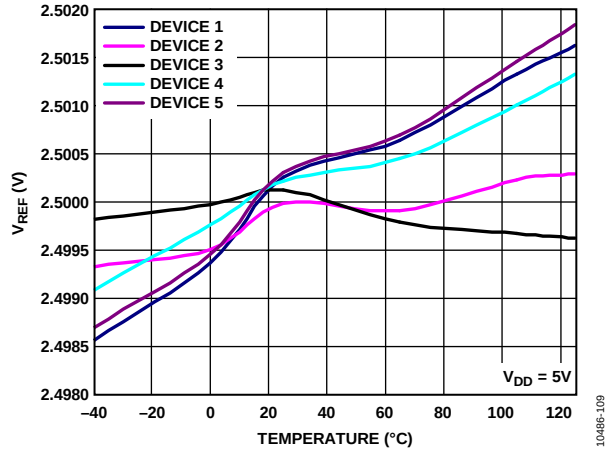


Figure 6. Internal Reference Voltage vs. Temperature (Grade A)

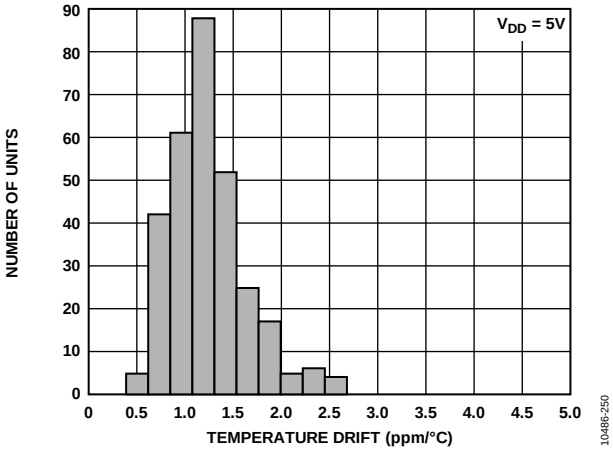


Figure 7. Reference Output Temperature Drift Histogram

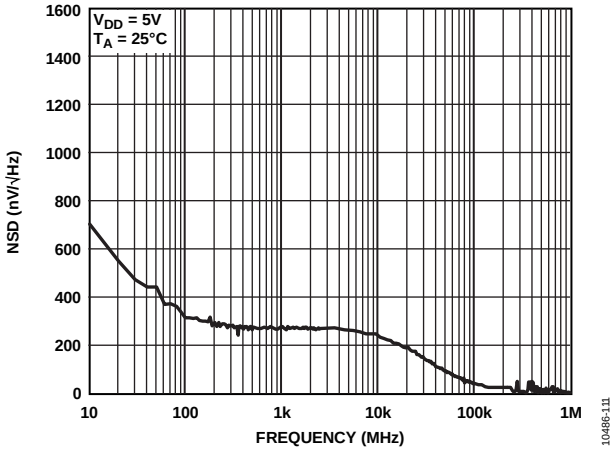


Figure 8. Internal Reference Noise Spectral Density vs. Frequency

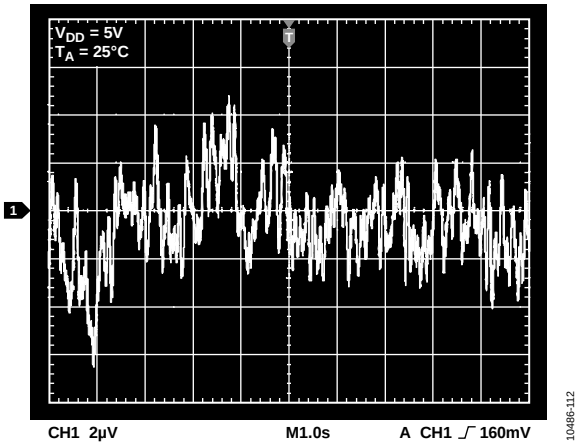


Figure 9. Internal Reference Noise, 0.1 Hz to 10 Hz

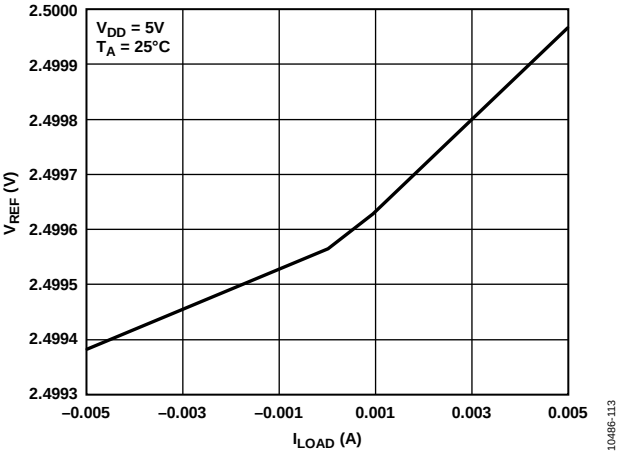


Figure 10. Internal Reference Voltage vs. Load Current

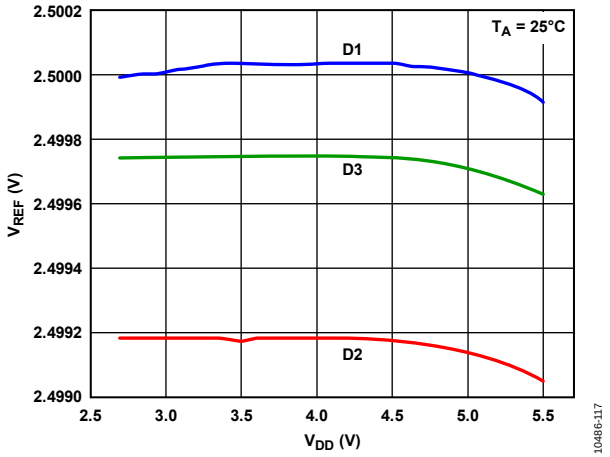


Figure 11. Internal Reference Voltage vs. Supply Voltage

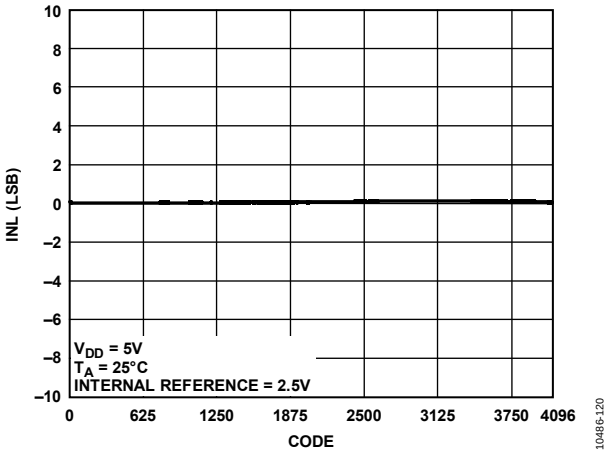


Figure 14. AD5694R INL

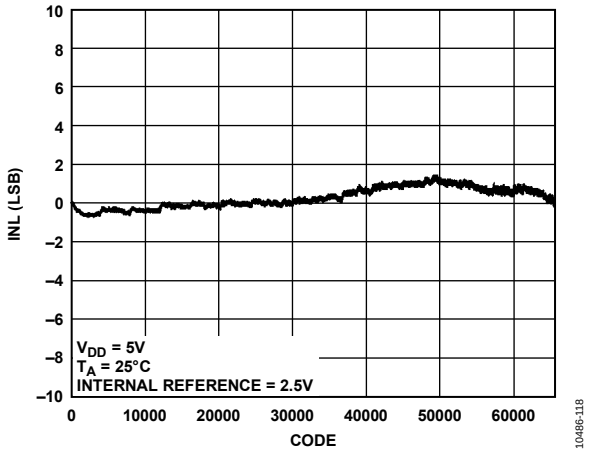


Figure 12. AD5696R INL

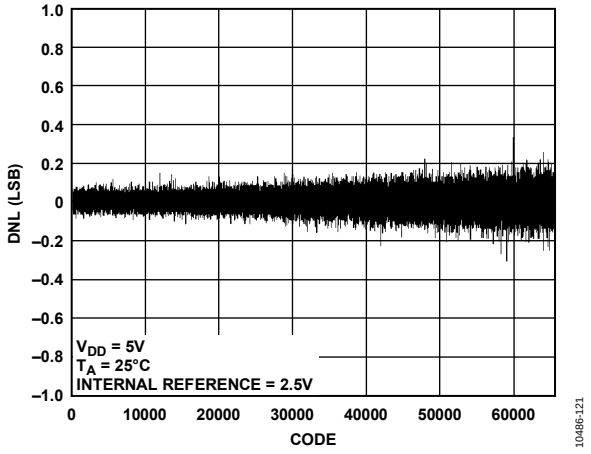


Figure 15. AD5696R DNL

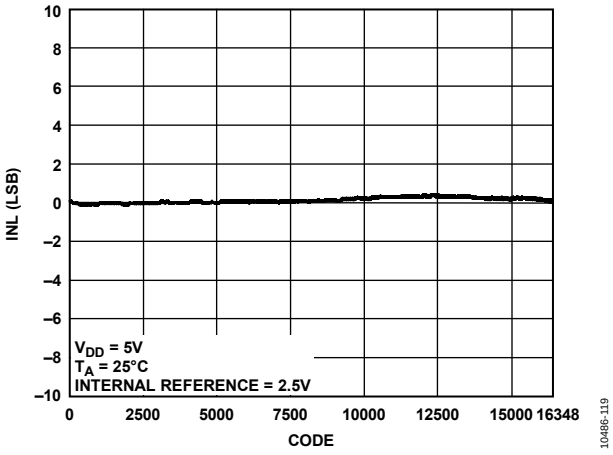


Figure 13. AD5695R INL

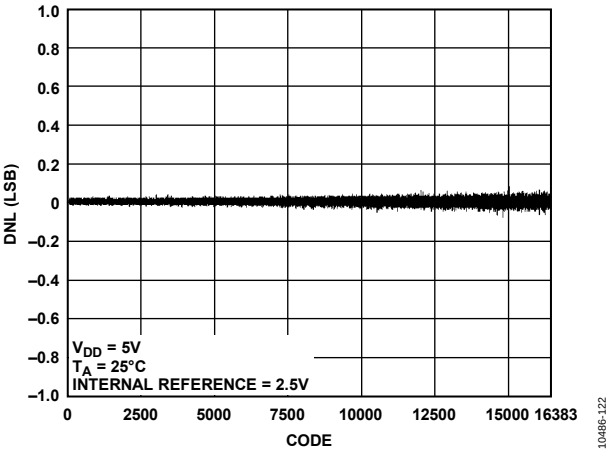


Figure 16. AD5695R DNL

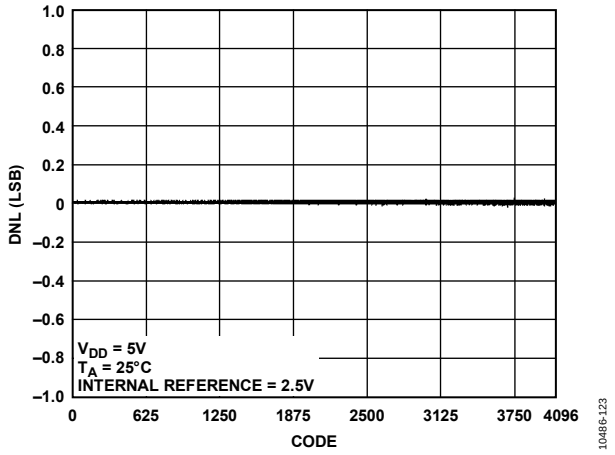


Figure 17. AD5694R DNL

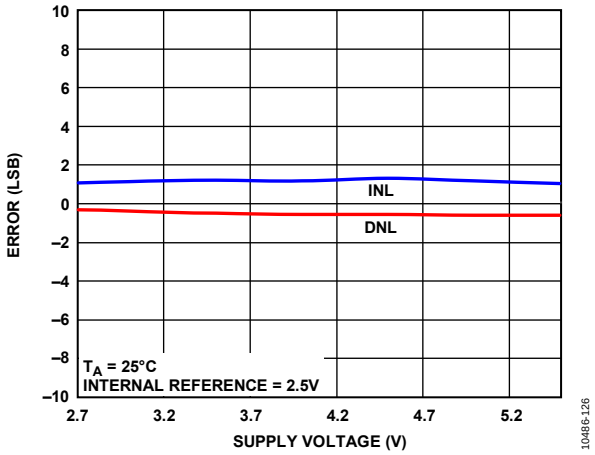


Figure 20. INL Error and DNL Error vs. Supply Voltage

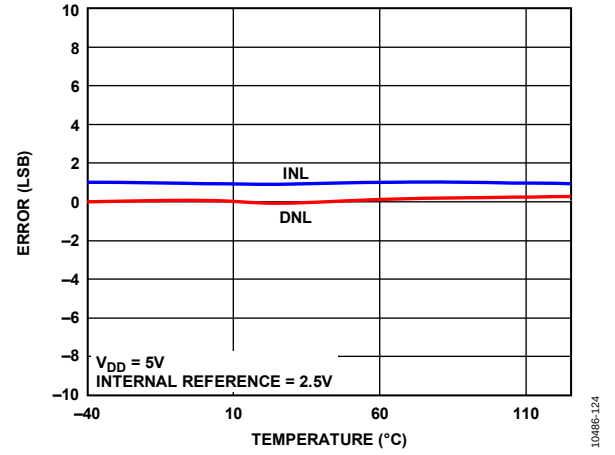


Figure 18. INL Error and DNL Error vs. Temperature

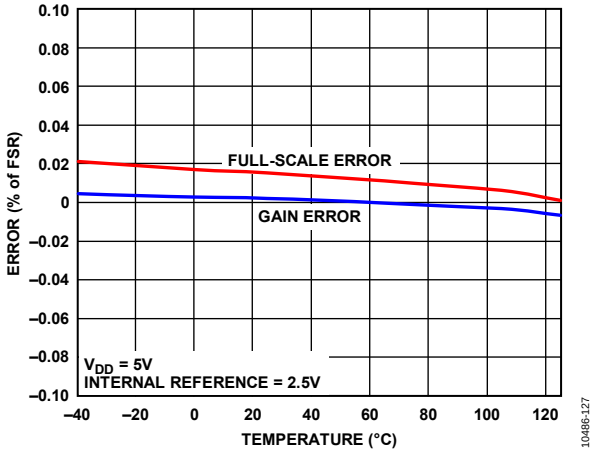


Figure 21. Gain Error and Full-Scale Error vs. Temperature

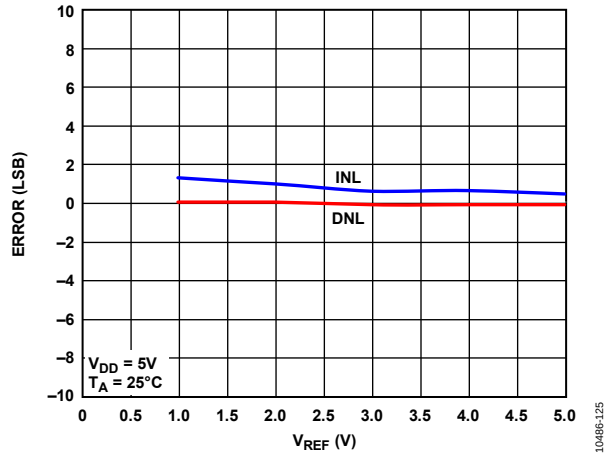


Figure 19. INL Error and DNL Error vs. V_{REF}

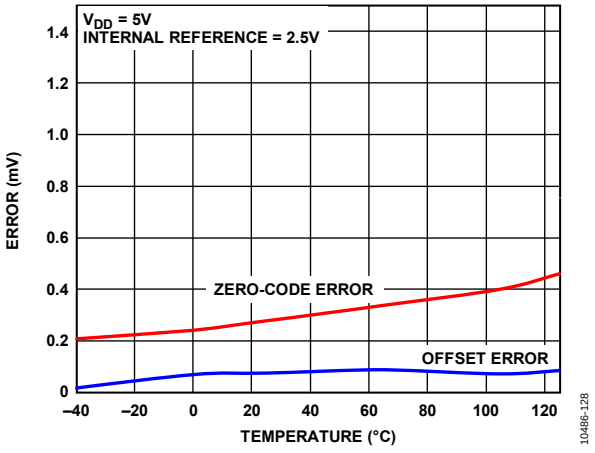


Figure 22. Zero-Code Error and Offset Error vs. Temperature

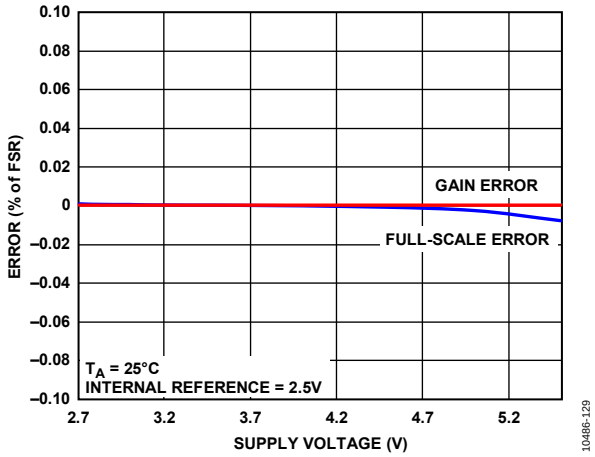


Figure 23. Gain Error and Full-Scale Error vs. Supply

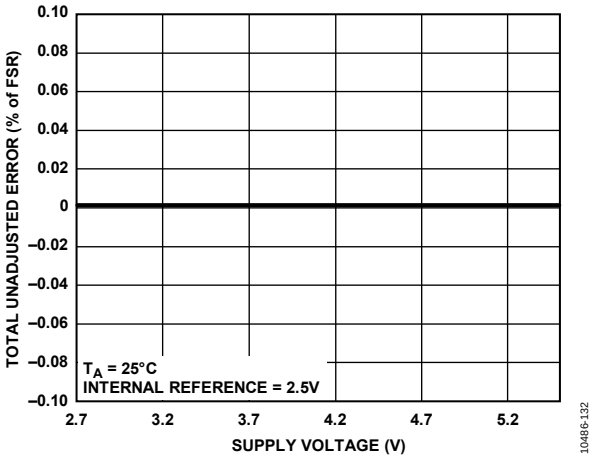


Figure 26. TUE vs. Supply, Gain = 1

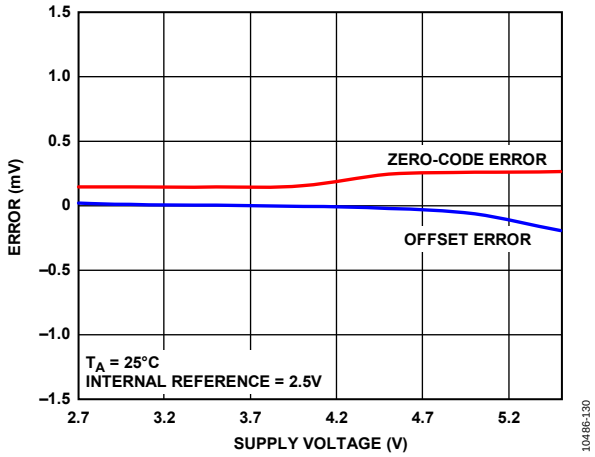


Figure 24. Zero-Code Error and Offset Error vs. Supply

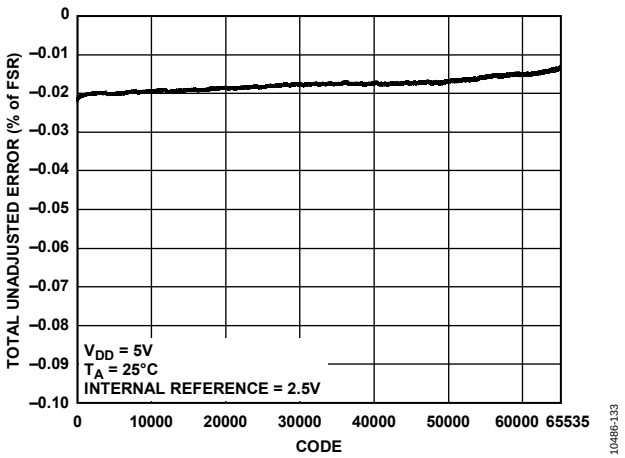


Figure 27. TUE vs. Code

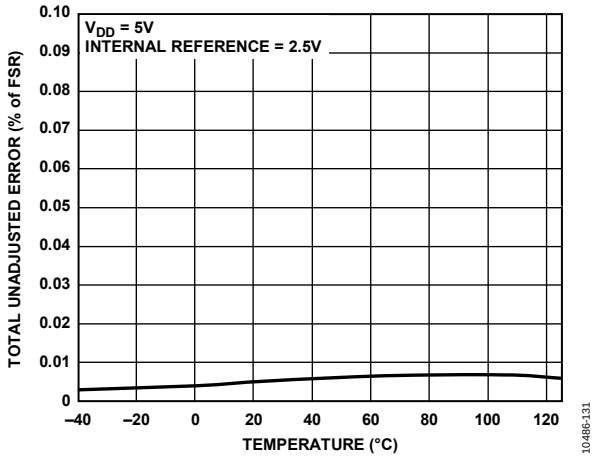


Figure 25. TUE vs. Temperature

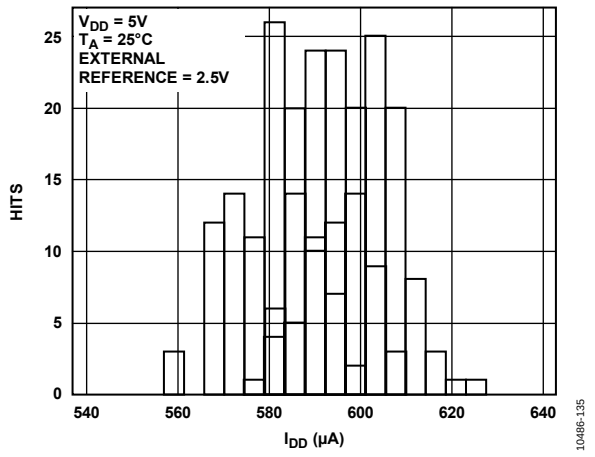


Figure 28. I_{DD} Histogram with External Reference, 5 V

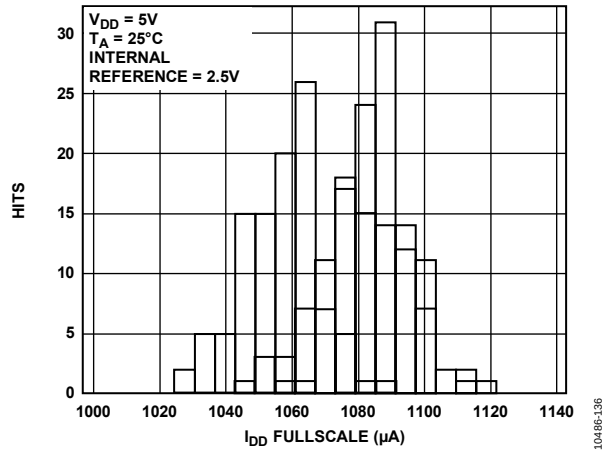


Figure 29. I_{DD} Histogram with Internal Reference, V_{REFOUT} = 2.5 V, Gain = 2

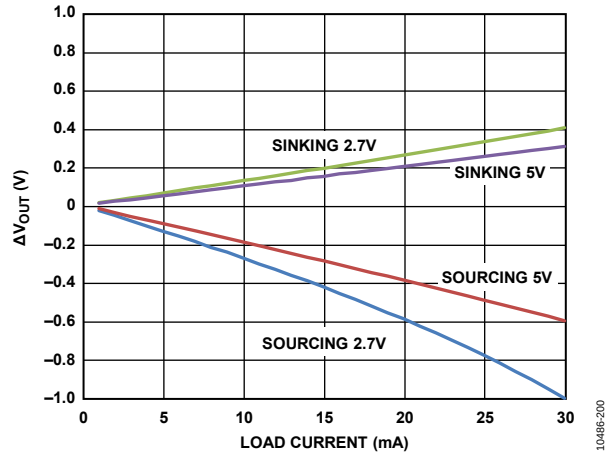


Figure 30. Headroom/Footroom vs. Load Current

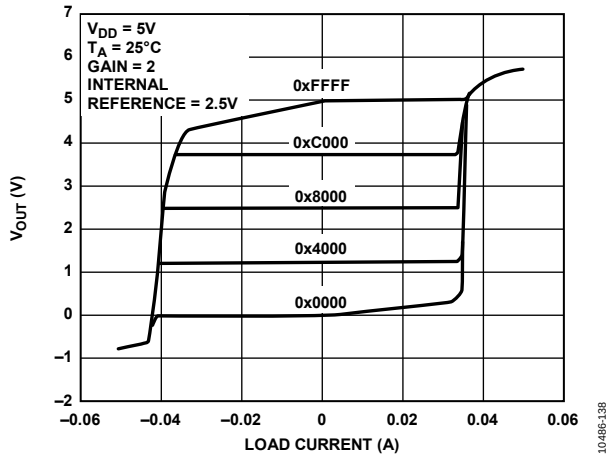


Figure 31. Source and Sink Capability at 5 V

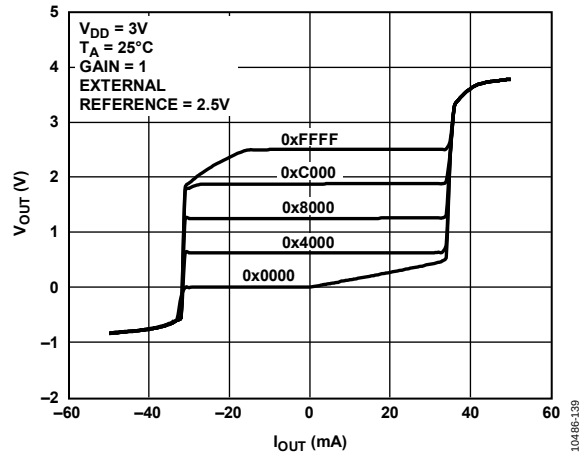


Figure 32. Source and Sink Capability at 3 V

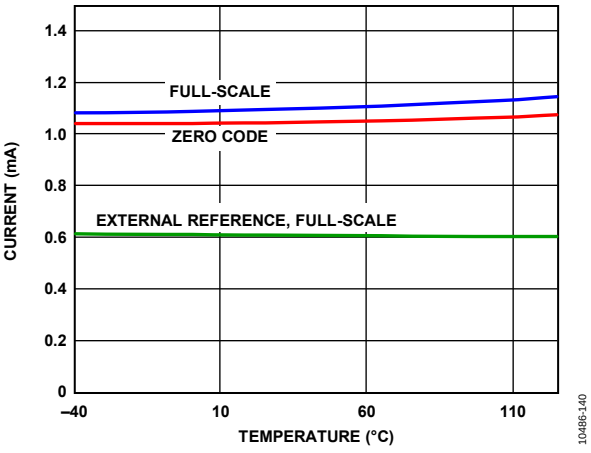


Figure 33. Supply Current vs. Temperature

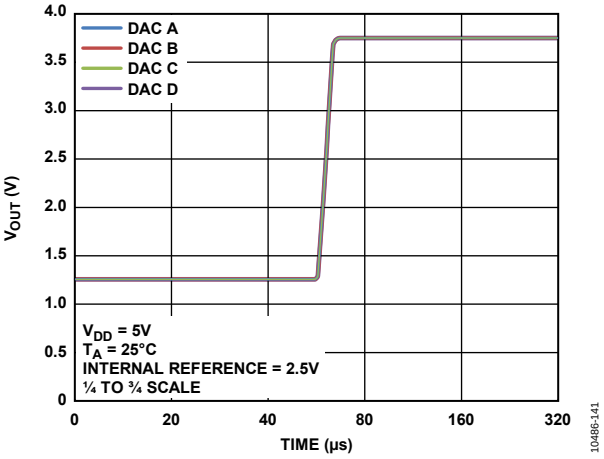


Figure 34. Settling Time, 5.25 V

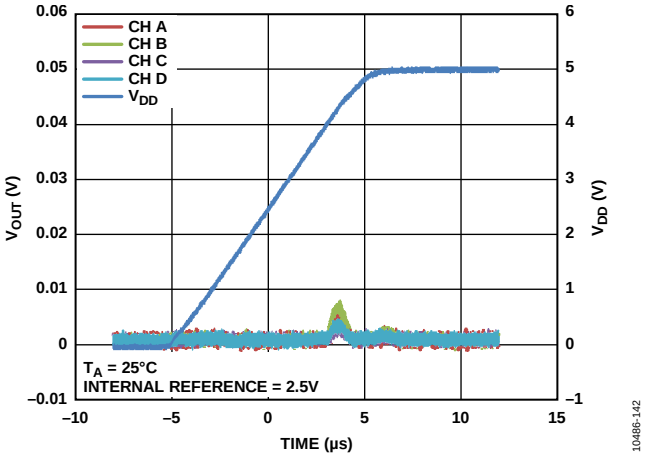


Figure 35. Power-On Reset to 0 V

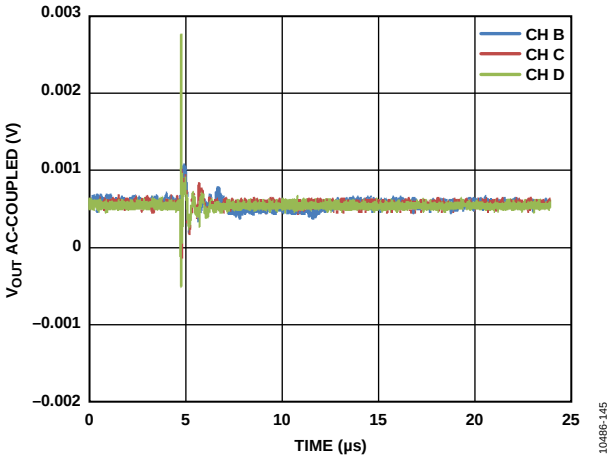


Figure 38. Analog Crosstalk, Channel A

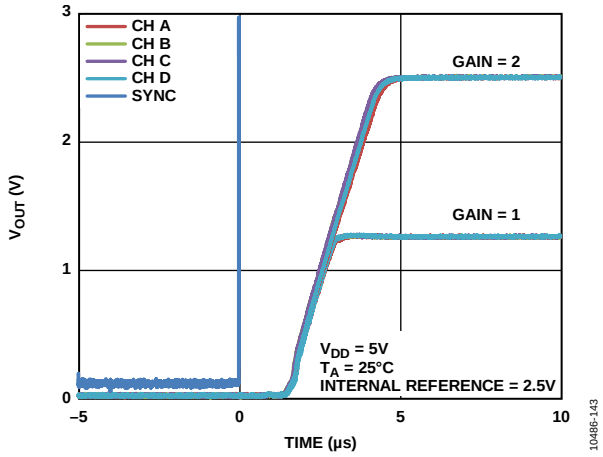


Figure 36. Exiting Power-Down to Midscale

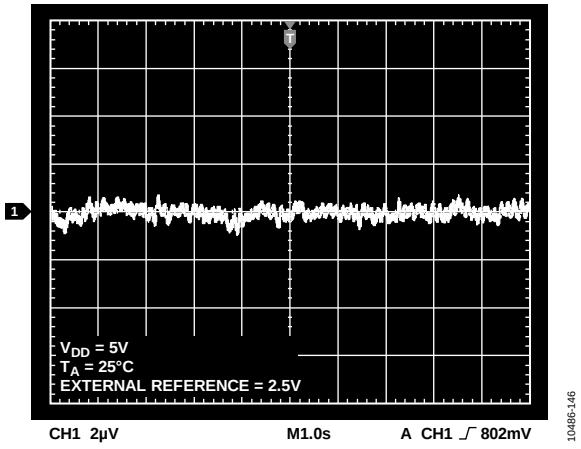


Figure 39. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

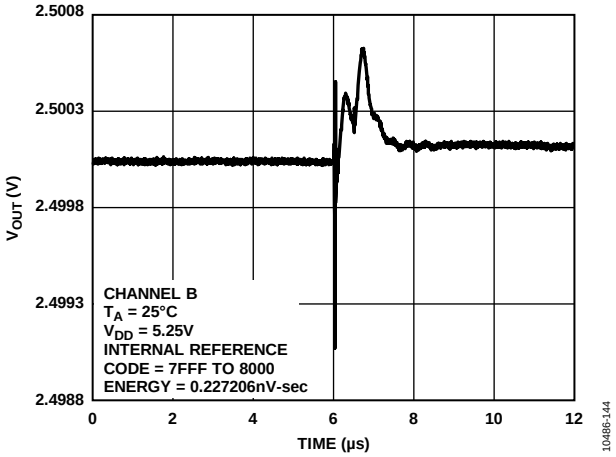


Figure 37. Digital-to-Analog Glitch Impulse

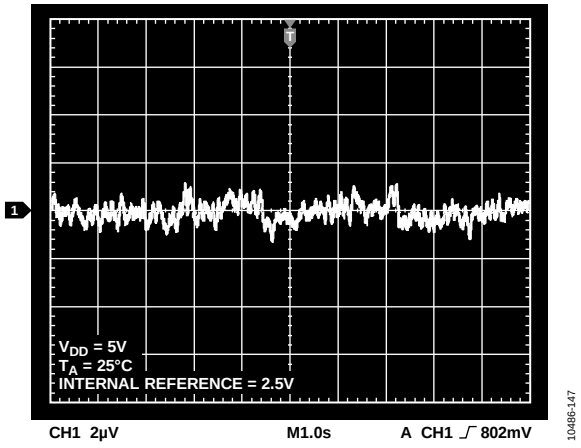


Figure 40. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

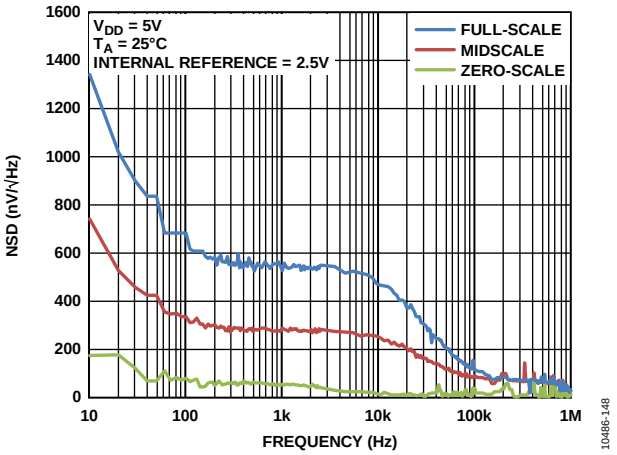


Figure 41. Noise Spectral Density

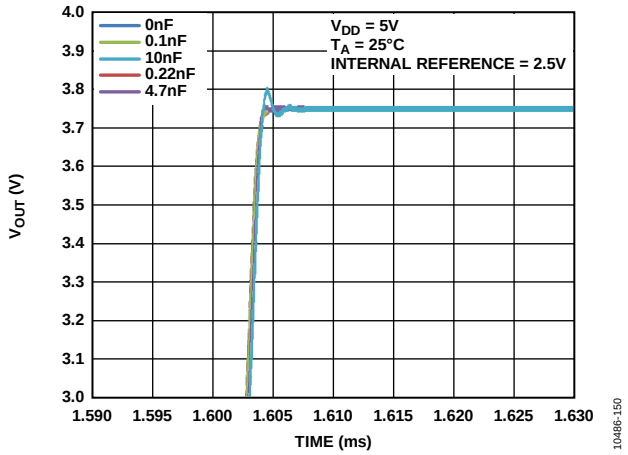


Figure 43. Settling Time vs. Capacitive Load

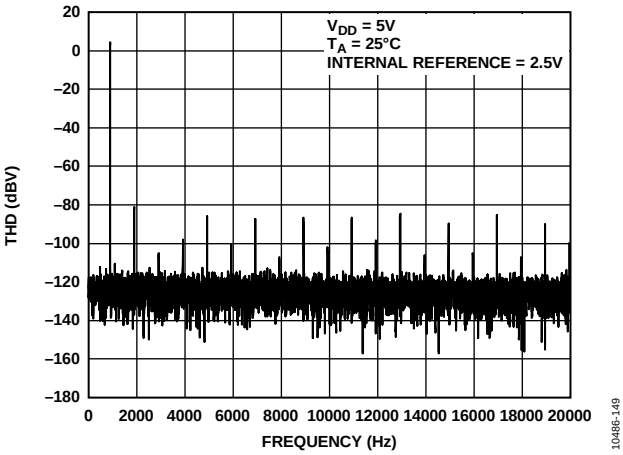


Figure 42. Total Harmonic Distortion at 1 kHz

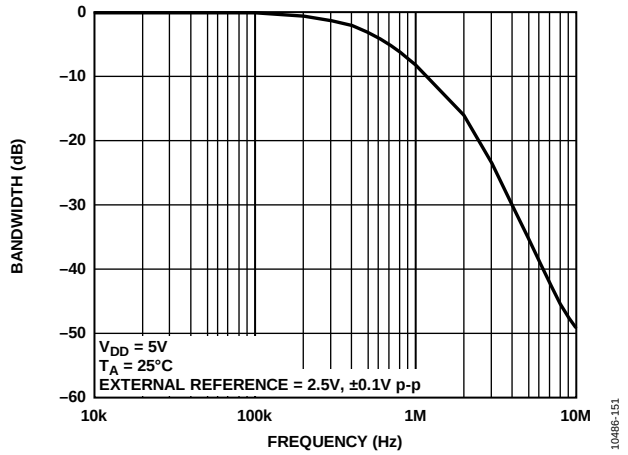


Figure 44. Multiplying Bandwidth, External Reference = 2.5 V, ±0.1 V p-p, 10 kHz to 10 MHz

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 12.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 15.

Zero-Code Error
Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5696R because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 22.

Full-Scale Error
Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range (% of FSR). A plot of full-scale error vs. temperature can be seen in Figure 21.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift
This is a measurement of the change in offset error with a change in temperature. It is expressed in µV/°C.

Gain Temperature Coefficient
This is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/°C.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5696R with Code 512 loaded in the DAC register. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2 V, and V_{DD} is varied by ±10%.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 37).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec, and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Reference Feedthrough
Reference feedthrough is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Noise Spectral Density
This is a measurement of the internally generated random noise. Random noise is characterized as a spectral density (nV/√Hz). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in nV/√Hz. A plot of noise spectral density is shown in Figure 41.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in µV.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in µV/mA.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands while monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

Voltage Reference TC
Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C as follows;

$$TC = \left[\frac{V_{REFmax} - V_{REFmin}}{V_{REFnom} \times TempRange} \right] \times 10^6$$

where:
V_{REFmax} is the maximum reference output measured over the total temperature range.
V_{REFmin} is the minimum reference output measured over the total temperature range.
V_{REFnom} is the nominal reference output voltage, 2.5 V.
TempRange is the specified temperature range of −40°C to +105°C.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5696R/AD5695R/AD5694R are quad 16-/14-/12-bit, serial input, voltage output DACs with an internal reference. The parts operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5696R/AD5695R/AD5694R in a 24-bit word format via a 2-wire serial interface. The AD5696R/AD5695R/AD5694R incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to typically 4 µA.

TRANSFER FUNCTION

The internal reference is on by default. To use an external reference, only a nonreference option is available. Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REF} \times Gain \left[\frac{D}{2^N} \right]$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register as follows:

- 0 to 4,095 for the 12-bit device.
- 0 to 16,383 for the 14-bit device.
- 0 to 65,535 for the 16-bit device.

N is the DAC resolution.

Gain is the gain of the output amplifier and is set to 1 by default. This can be set to ×1 or ×2 using the gain select pin. When this pin is tied to GND, all four DAC outputs have a span from 0 V to V_{REF}. If this pin is tied to V_{DD}, all four DACs output a span of 0 V to 2 × V_{REF}.

DAC ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 45 shows a block diagram of the DAC architecture.

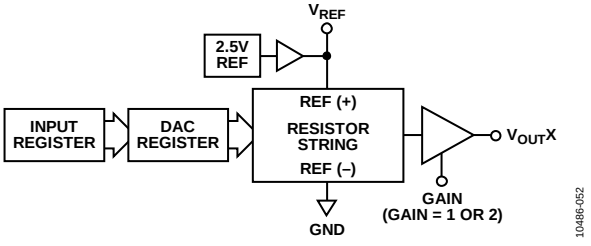


Figure 45. Single DAC Channel Architecture Block Diagram

The resistor string structure is shown in Figure 46. It is a string of resistors, each of Value R. The code loaded to the DAC register determines the node on the string where the voltage is to be tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

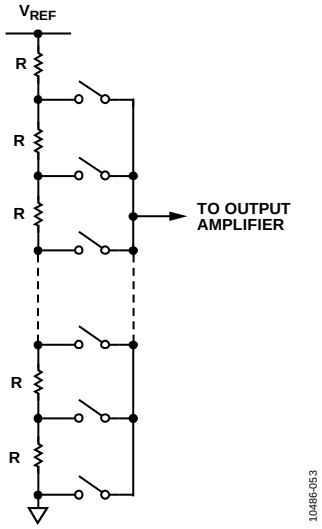


Figure 46. Resistor String Structure

Internal Reference

The AD5696R/AD5695R/AD5694R on-chip reference is on at power-up but can be disabled via a write to a control register. See the Internal Reference Setup section for details.

The AD5696R/AD5695R/AD5694R have a 2.5 V, 2 ppm/°C reference, giving a full-scale output of 2.5 V or 5 V depending on the state of the GAIN pin. The internal reference associated with the device is available at the V_{REF} pin. This buffered reference is capable of driving external loads of up to 10 mA.

Output Amplifiers

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The actual range depends on the value of V_{REF}, the GAIN pin, offset error, and gain error. The GAIN pin selects the gain of the output.

- If this pin is tied to GND, all four outputs have a gain of 1 and the output range is 0 V to V_{REF}.
- If this pin is tied to V_{LOGIC}, all four outputs have a gain of 2 and the output range is 0 V to 2 × V_{REF}.

These amplifiers are capable of driving a load of 1 kΩ in parallel with 2 nF to GND. The slew rate is 0.8 V/µs with a ¼ to ¾ scale settling time of 5 µs.

SERIAL INTERFACE

The AD5696R/AD5695R/AD5694R have 2-wire I²C-compatible serial interfaces (refer to *I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). See Figure 2 for a timing diagram of a typical write sequence. The AD5696R/AD5695R/AD5694R can be connected to an I²C bus as a slave device, under the control of a master device. The AD5696R/AD5695R/AD5694R support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing. Power should not be removed while the device is connected to an active I²C bus.

Input Shift Register

The input shift register of the AD5696R/AD5695R/AD5694R is 24 bits wide. Data is loaded into the device as a 24-bit word under the control of a serial clock input, SCL. The first eight MSBs make up the command byte. The first four bits are the command bits (C3, C2, C1, C0) that control the mode of operation of the device (see Table 7). The last 4 bits of first byte are the address bits (DAC A, DAC B, DAC C, DAC D) (see Table 8).

The data-word comprises 16-bit, 14-bit, or 12-bit input code, followed by four, two, or zero don't care bits for the AD5696R, AD5695R, and AD5694R, respectively (see Figure 47, Figure 48, and Figure 49). These data bits are transferred to the input register on the 24 falling edges of SCL.

Commands can be executed on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected.

Table 7. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Hardware $\overline{\text{LDAC}}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference setup register
1	0	0	0	Reserved
…	…	…	…	Reserved
1	1	1	1	Reserved

Table 8. Address Commands

Address (n)				
DAC D	DAC C	DAC B	DAC A	Selected DAC Channel[1]
0	0	0	1	DAC A
0	0	1	0	DAC B
0	1	0	0	DAC C
1	0	0	0	DAC D
0	0	1	1	DAC A and DAC B[1]
1	1	1	1	All DACs

[1] Any combination of DAC channels can be selected using the address bits.

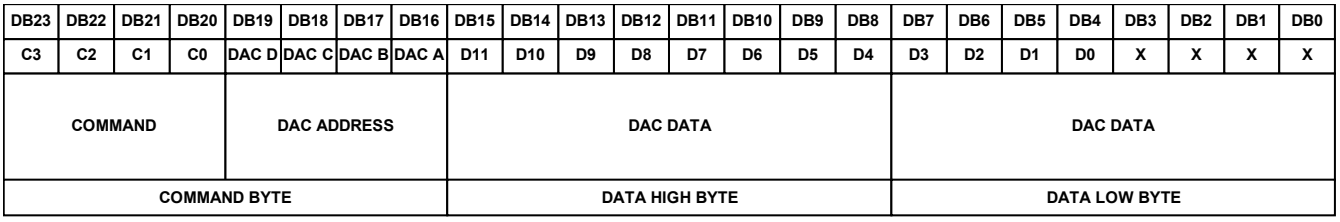


Figure 47. AD5696R Input Shift Register Content

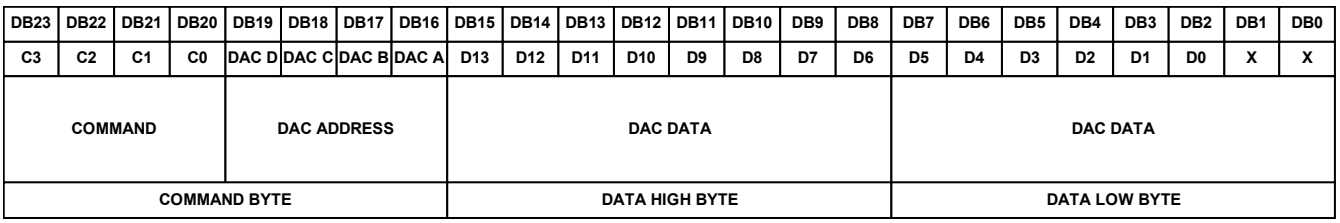


Figure 48. AD5695R Input Shift Register Content

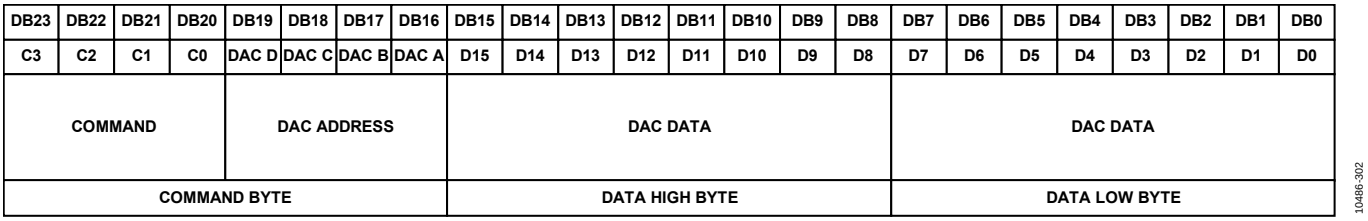


Figure 49. AD5694R Input Shift Register Content

WRITE AND UPDATE COMMANDS

Write to Input Register n (Dependent on $\overline{\text{LDAC}}$)

Command 0001 allows the user to write to each DAC's dedicated input register individually. When $\overline{\text{LDAC}}$ is low, the input register is transparent (if not controlled by the $\overline{\text{LDAC}}$ mask register).

Update DAC Register n with Contents of Input Register n

Command 0010 loads the DAC registers/outputs with the contents of the input registers selected and updates the DAC outputs directly.

Write to and Update DAC Channel n (Independent of $\overline{\text{LDAC}}$)

Command 0011 allows the user to write to the DAC registers and update the DAC outputs directly.

SERIAL OPERATION

The AD5696R/AD5695R/AD5694R each have a 7-bit slave address. The five MSBs are 00011 and the two LSBs (A1, A0) are set by the state of the A0 and A1 address pins. The ability to make hardwired changes to A0 and A1 allows the user to incorporate up to four of these devices on one bus, as outlined in Table 9.

Table 9. Device Address Selection

A0 Pin Connection	A1 Pin Connection	A0	A1
GND	GND	0	0
V_{LOGIC}	GND	1	0
GND	V_{LOGIC}	0	1
V_{LOGIC}	V_{LOGIC}	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the 9th clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the 9th clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5696R/AD5695R/AD5694R, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5696R/AD5695R/AD5694R require two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC with the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 50. All these data bytes are acknowledged by the AD5696R/AD5695R/AD5694R. A stop condition follows.

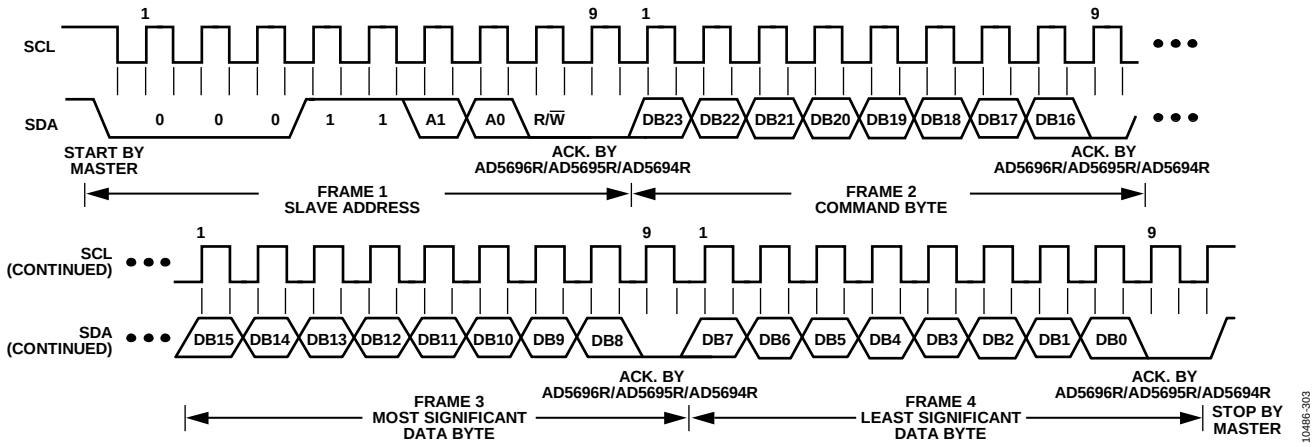


Figure 50. I²C Write Operation

READ OPERATION

When reading data back from the AD5696R DACs, the user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte must be followed by the NOP command operation that sets the internal pointer to the DAC address to read from, which is also acknowledged by the DAC. Following this, there is a repeated start condition by the master and the address is resent with R/$\overline{W}$ = 1. This is acknowledged by the DAC, indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 51. A NACK condition from the master, followed by a STOP condition, completes the read sequence. Default readback is Channel A if more than one DAC is selected.

MULTIPLE DAC READBACK SEQUENCE

The user begins with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte must be followed by the control byte, which is also acknowledged by the DAC. The user configures which channel to start the readback using the control byte. Following this, there is a repeated start condition by the master and the address is resent with R/$\overline{W}$ = 1. This is acknowledged by the DAC, indicating that it is prepared to transmit data. The first two bytes of data are then read from the DAC Input Register n selected using the control byte, most significant byte first as shown in Figure 51. The next two bytes read back are the contents of DAC Input Register n + 1, the next bytes read back are the contents of DAC Input Register n + 2. Data continues to be read from the DAC input registers in this auto-incremental fashion, until a NACK followed by a stop condition follows. If the contents of DAC Input Register D are read out, the next two bytes of data that are read are from the contents of DAC Input Register A.

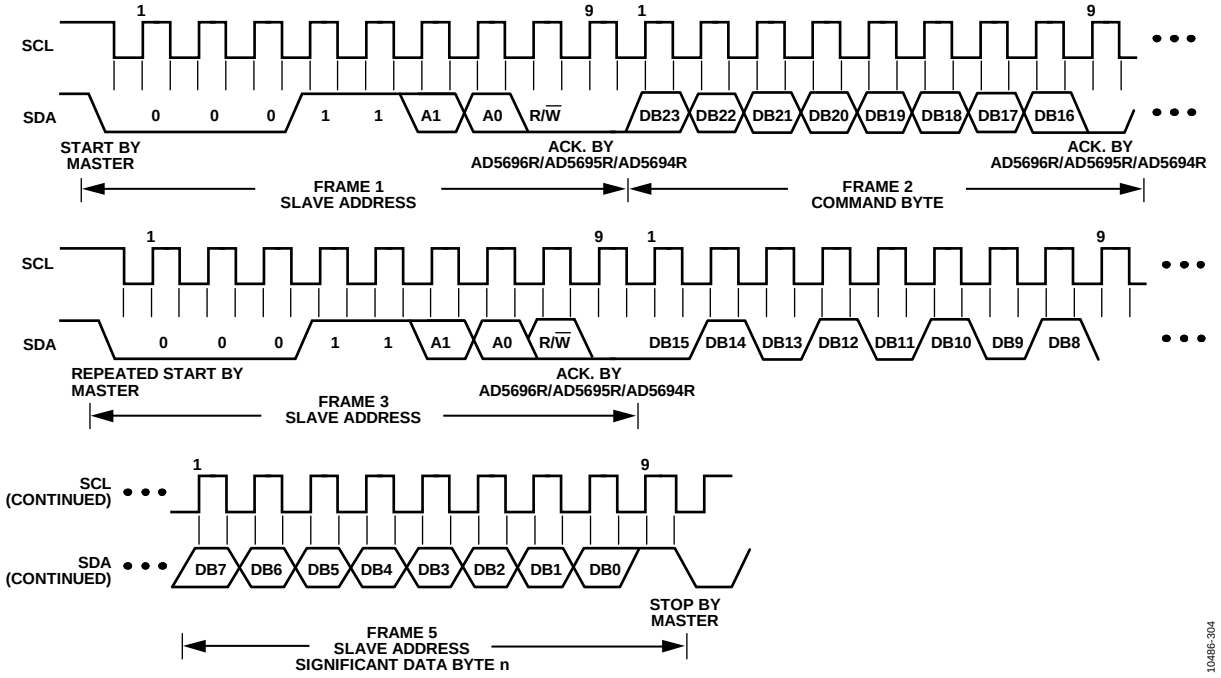


Figure 51. I²C Read Operation

POWER-DOWN OPERATION

The AD5696R/AD5695R/AD5694R contain three separate power-down modes. Command 0100 is designated for the power-down function (see Table 7). These power-down modes are software-programmable by setting eight bits, Bit DB7 to Bit DB0, in the shift register. There are two bits associated with each DAC channel. Table 10 shows how the state of the two bits corresponds to the mode of operation of the device.

Table 10. Modes of Operation

Operating Mode	PDx1	PDx0
Normal Operation	0	0
Power-Down Modes		
1 kΩ to GND	0	1
100 kΩ to GND	1	0
Three-State	1	1

Any or all DACs (DAC A to DAC D) can be powered down to the selected mode by setting the corresponding bits. See Table 11 for the contents of the input shift register during the power-down/power-up operation.

When both Bit PDx1 and Bit PDx0 (where x is the channel selected) in the input shift register are set to 0, the parts work normally with its normal power consumption of 4 mA at 5 V. However, for the three power-down modes, the supply current falls to 4 μA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different power-down options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 52.

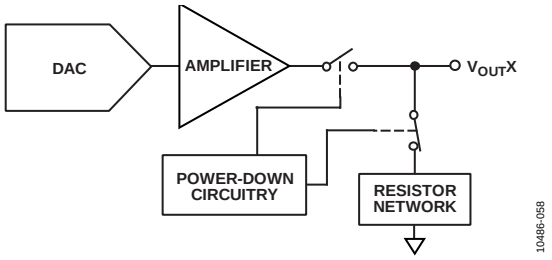


Figure 52. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The DAC register can be updated while the device is in power-down mode. The time required to exit power-down is typically 4.5 μs for V_{DD} = 5 V.

To reduce the current consumption further, the on-chip reference can be powered off. See the Internal Reference Setup section.

Table 11. 24-Bit Input Shift Register Contents of Power-Down/Power-Up Operation[1]

DB23	DB22	DB21	DB20	DB19 to DB16	DB15 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)
0	1	0	0	X	X	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0
Command bits (C3 to C0)				Address bits Don't care		Power-Down Select DAC D		Power-Down Select DAC C		Power-Down Select DAC B		Power-Down Select DAC A	

[1] X = don't care.

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5696R/AD5695R/AD5694R DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the $\overline{\text{LDAC}}$ pin.

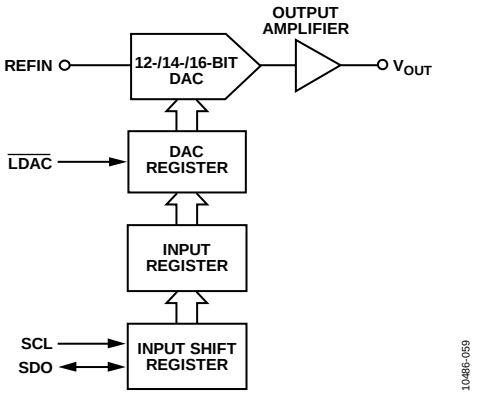


Figure 53. Simplified Diagram of Input Loading Circuitry for a Single DAC

Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)

$\overline{\text{LDAC}}$ is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the 24th clock and the output begins to change (see Table 13).

Deferred DAC Updating ($\overline{\text{LDAC}}$ is Pulsed Low)

$\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by taking $\overline{\text{LDAC}}$ low after the 24th clock. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

$\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for this software $\overline{\text{LDAC}}$ function. Address bits are ignored. Writing to the DAC, using Command 0101, loads the 4-bit $\overline{\text{LDAC}}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wishes to select which channels respond to the $\overline{\text{LDAC}}$ pin.

Table 12. $\overline{\text{LDAC}}$ Overwrite Definition

Load $\overline{\text{LDAC}}$ Register		
$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	$\overline{\text{LDAC}}$ Pin	$\overline{\text{LDAC}}$ Operation
0	1 or 0	Determined by the $\overline{\text{LDAC}}$ pin.
1	X[1]	DAC channels update and override the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 1.

[1] X = don't care.

The $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 12). Setting the $\overline{\text{LDAC}}$ bits (DB0 to DB3) to 0 for a DAC channel means that this channel's update is controlled by the hardware $\overline{\text{LDAC}}$ pin.

Table 13. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table[1]

Commands	Description	Hardware $\overline{\text{LDAC}}$ Pin State	Input Register Contents	DAC Register Contents
0001	Write to Input Register n (dependent on $\overline{\text{LDAC}}$)	V_{LOGIC}	Data update	No change (no update)
		GND[2]	Data update	Data update
0010	Update DAC Register n with contents of Input Register n	V_{LOGIC}	No change	Updated with input register contents
		GND	No change	Updated with input register contents
0011	Write to and update DAC Channel n	V_{LOGIC}	Data update	Data update
		GND	Data update	Data update

[1] A high to low hardware $\overline{\text{LDAC}}$ pin transition always updates the contents of the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.
[2] When LDAC is permanently tied low, the LDAC mask bits are ignored.

HARDWARE RESET ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the $\overline{\text{RESET}}$ select pin. It is necessary to keep $\overline{\text{RESET}}$ low for a minimum amount of time to complete the operation (see Figure 2). When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{\text{RESET}}$ pin is low. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function (see Table 7). Any events on $\overline{\text{LDAC}}$ during a power-on reset are ignored. If the $\overline{\text{RESET}}$ pin is pulled low at power-up, the device does not initialize correctly until the pin is released.

RESET SELECT PIN (RSTSEL)

The AD5696R/AD5695R/AD5694R contain a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this is outside the linear region of the DAC; by connecting the RSTSEL pin high, V_{OUT} powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC.

INTERNAL REFERENCE SETUP

The on-chip reference is on at power-up by default. To reduce the supply current, this reference can be turned off by setting software programmable bit, DB0, in the control register. Table 14 shows how the state of the bit corresponds to the mode of operation. Command 0111 is reserved for setting up the internal reference (see Figure 6). Table 14 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device during internal reference setup.

Table 14. Reference Setup Register

Internal Reference Setup Register (DB0)	Action
0	Reference on (default)
1	Reference off

SOLDER HEAT REFLOW

As with all IC reference voltage circuits, the reference value experiences a shift induced by the soldering process. Analog Devices, Inc., performs a reliability test called precondition to mimic the effect of soldering a device to a board. The output voltage specification quoted previously includes the effect of this reliability test.

Figure 54 shows the effect of solder heat reflow (SHR) as measured through the reliability test (precondition).

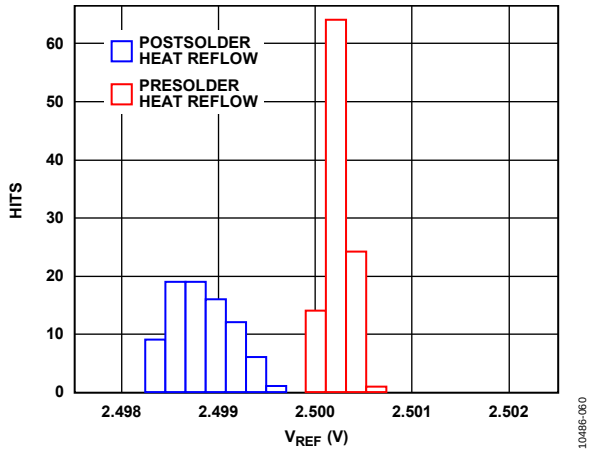


Figure 54. SHR Reference Voltage Shift

LONG-TERM TEMPERATURE DRIFT

Figure 55 shows the change in the V_{REF} (ppm) value after 1000 hours at 25°C ambient temperature.

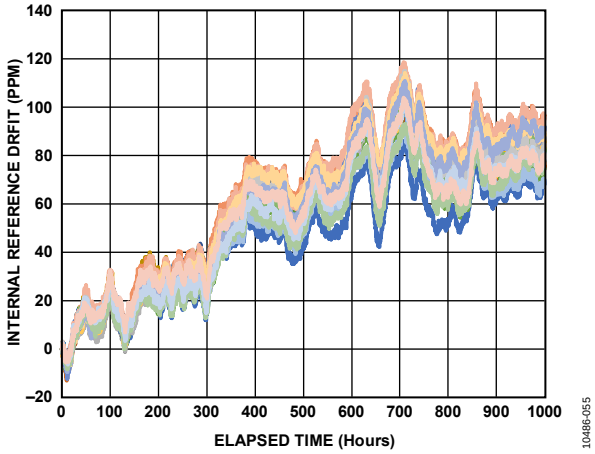


Figure 55. Reference Drift Through to 1000 Hours

THERMAL HYSTERESIS

Thermal hysteresis is the voltage difference induced on the reference voltage by sweeping the temperature from ambient to cold, to hot and then back to ambient.

Thermal hysteresis data is shown in Figure 56. It is measured by sweeping temperature from ambient to −40°C, then to +105°C, and returning to ambient. The V_{REF} delta is then measured between the two ambient measurements and shown in blue in Figure 56. The same temperature sweep and measurements were immediately repeated and the results are shown in red in Figure 56.

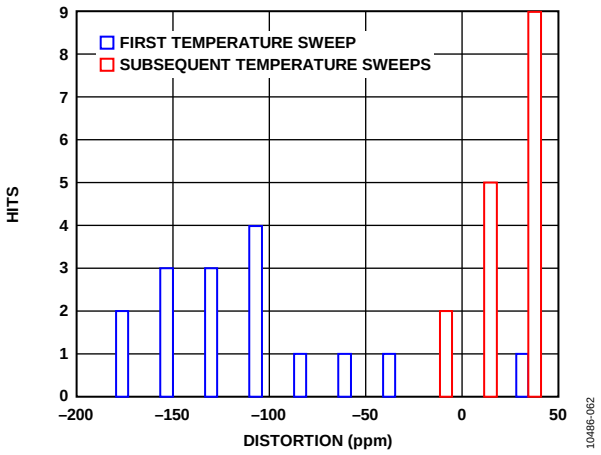


Figure 56. Thermal Hysteresis

Table 15. 24-Bit Input Shift Register Contents for Internal Reference Setup Command[1]

DB23 (MSB)	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0 (LSB)
0	1	1	1	X	X	X	X	X	1/0
Command bits (C3 to C0)				Address bits (A2 to A0)				Don't care	Reference setup register

[1] X = don't care.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5696R/AD5695R/AD5694R is via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 2-wire interface consisting of a clock signal and a data signal.

AD5696R/AD5695R/AD5694R TO ADSP-BF531 INTERFACE

The I²C interface of the AD5696R/AD5695R/AD5694R is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 57 shows the AD5696R/AD5695R/AD5694R connected to the Analog Devices Blackfin® DSP. The Blackfin has an integrated I²C port that can be connected directly to the I²C pins of the AD5696R/AD5695R/AD5694R.

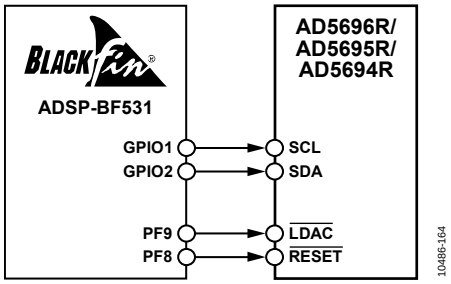


Figure 57. ADSP-BF531 Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5696R/AD5695R/AD5694R are mounted should be designed so that the AD5696R/AD5695R/AD5694R lie on the analog plane.

The AD5696R/AD5695R/AD5694R should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The AD5696R/AD5695R/AD5694R LFCSP models have an exposed paddle beneath the device. Connect this paddle to the GND supply for the part. For optimum performance, use special considerations to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, solder the exposed paddle on the bottom of the package to the corresponding thermal land paddle on the PCB. Design thermal vias into the PCB land paddle area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 58) to provide a natural heat sinking effect.

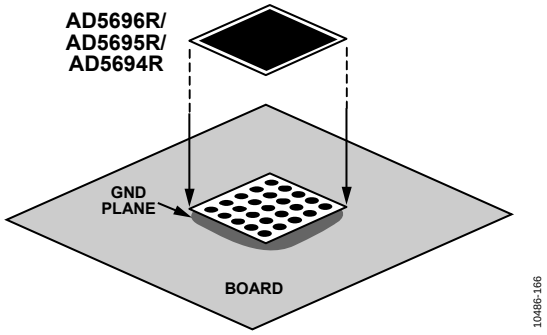


Figure 58. Paddle Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *i*Coupler® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5696R/AD5695R/AD5694R makes the part ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 59 shows a 4-channel isolated interface to the AD5696R/AD5695R/AD5694R using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

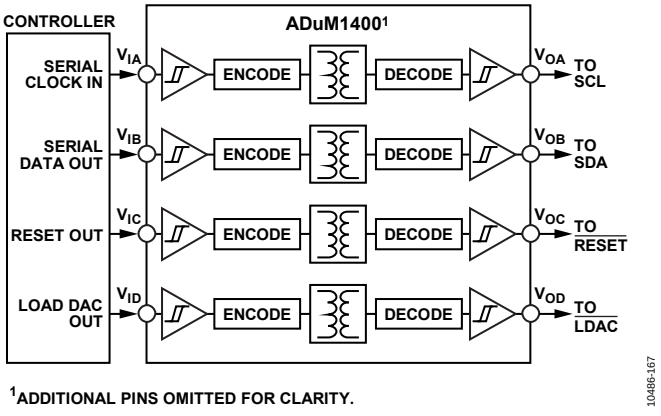
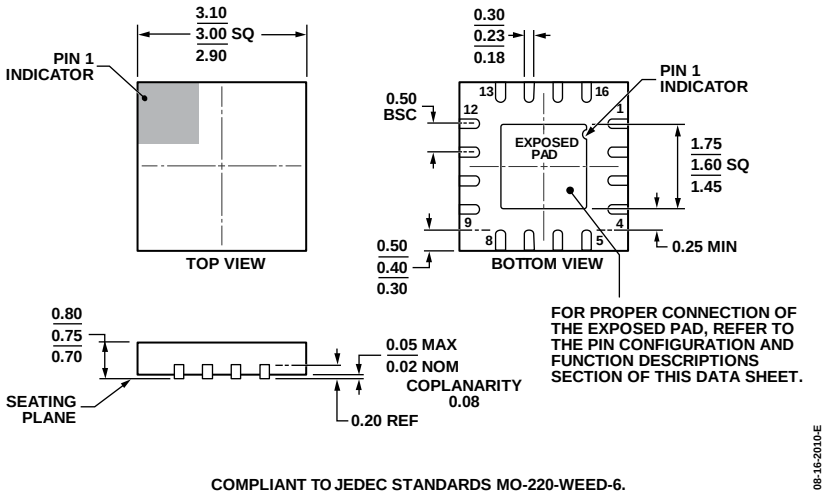


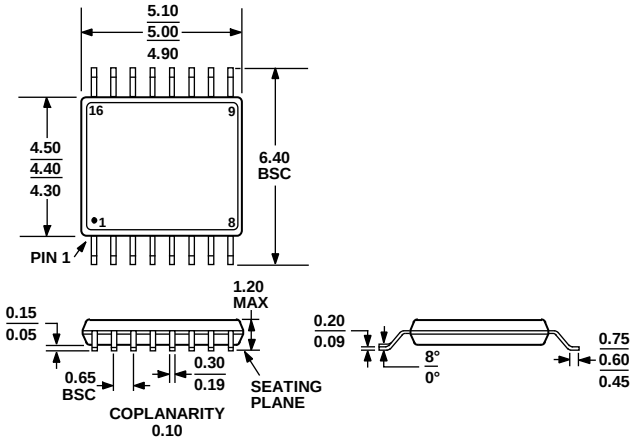
Figure 59. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 60. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 61. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters