REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add Mode of transportation and quantity column under paragraph 6.3. Update document paragraphs to current requirements. - ro	18-06-04	C. SAFFLE
B	Update document to current requirements. - ro	23-09-20	J. ESCHMEYER
C	Update paragraph 6.3 by deleting AD7923SRU-EP-RL7 and replacing with AD7923SRUZ-EP-RL7. - ro	23-12-11	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A

Original date of drawing

YY-MM-DD
12-12-20

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 4 CHANNEL, 200 kSPS, 12 BIT ANALOG-TO-DIGITAL CONVERTER WITH SEQUENCER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/12647
REV C		PAGE 1 OF 16

AMSC N/A

5962-V019-24

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4 channel, 200 kilo samples per second (kSPS) 12 bit analog to digital with sequencer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12647	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD7923	4 channel, 200 kSPS 12 bit analog to digital with sequencer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153-AB	Plastic thin shrink small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog power supply voltage (AV_{DD}) to analog ground (AGND)	-0.3 V to +7 V
Logic power supply input (VDRIVE) to GND	-0.3 V to AV_{DD} + 0.3 V
Analog input voltage to AGND	-0.3 V to AV_{DD} + 0.3 V
Digital input voltage to AGND	-0.3 V to 7 V
Digital output voltage to AGND	-0.3 V to AV_{DD} + 0.3 V
Reference input (REFIN) to AGND	-0.3 V to AV_{DD} + 0.3 V
Input current to any pin except supplies	±10 m A 2/
Power dissipation (PD)	450 mW
Junction temperature range (T_J)	150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature, soldering :	
Vapor phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Lead free temperature, soldering reflow	260(+0) °C
Electrostatic discharge (ESD)	1.5 kV
Thermal impedance, junction to case(θ_{JC})	27.6°C/W
Thermal impedance, junction to ambient (θ_{JA})	150.4°C/W

1.4 Recommended operating conditions. 3/

Supply voltage (AV_{DD}) range	+2.7 V to +5.25 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch up.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Load circuit for digital output timing specifications. The load circuit for digital output timing specifications shall be as shown in figure 1.

3.5.2 Case outline. The case outline shall be as shown in 1.2.2 and figure 2.

3.5.3 Terminal connections. The terminal connections shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance.		f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz					
Signal to (noise + distortion)	SINAD	At 5 V	-40°C to +85°C	01	70		dB
			+85°C to +125°C		69		
		At 3 V	-40°C to +125°C		69		
Signal to noise ratio	SNR		-55°C to +125°C	01	70		dB
Total harmonic distortion	THD	At 5 V	-55°C to +125°C	01		-77	dB
		At 3 V				-73	
Peak harmonic or spurious noise	SFDR	At 5 V	-55°C to +125°C	01		-78	dB
		At 3 V				-76	
Intermodulation distortion (IMD).		f_A = 40.1 kHz, f_B = 41.5 kHz					
Second order terms			-55°C to +125°C	01	-90 typical		dB
Third order terms			-55°C to +125°C	01	-90 typical		dB
Aperture delay			-55°C to +125°C	01	10 typical		ns
Aperture jitter			-55°C to +125°C	01	50 typical		ps
Channel to channel isolation		f_{IN} = 400 kHz	-55°C to +125°C	01	-85 typical		dB
Full power bandwidth	FPBW	3 dB	-55°C to +125°C	01	8.2 typical		MHz
		0.1 dB			1.6 typical		
DC accuracy.							
Resolution			-55°C to +125°C	01	12		Bits
Integral nonlinearity			-55°C to +125°C	01		±1	LSB
Differential nonlinearity		Guaranteed no missed codes to 12 bits	-55°C to +125°C	01	-0.9	+1.5	LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC accuracy – continued.							
0 V to REF_{IN} input range		Straight binary output coding					
Offset error			-55°C to +125°C	01		±8	LSB
Offset error match			-55°C to +125°C	01		±0.5	LSB
Gain error			-55°C to +125°C	01		±1.5	LSB
Gain error match			-55°C to +125°C	01		±0.5	LSB
0 V to 2 x REF_{IN} input range.		-REF_{IN} to +REF_{IN} biased about REF_{IN}	with two's complement output coding offset				
Positive gain error			-55°C to +125°C	01		±1.5	LSB
Positive gain error match			-55°C to +125°C	01		±0.5	LSB
Zero code error			-55°C to +125°C	01		±8	LSB
Zero code error match			-55°C to +125°C	01		±0.5	LSB
Negative gain error			-55°C to +125°C	01		±1	LSB
Negative gain error match			-55°C to +125°C	01		±0.5	LSB
Analog input.							
Input voltage range	V_{IN}	Range bit set to 1	-55°C to +125°C	01	0	REF_{IN}	V
		Range bit set to 0, AV_{DD} = 4.75 V to 5.25 V			0	2 x REF_{IN}	
DC leakage current			-55°C to +125°C	01		±1	µA
Input capacitance	C_{IN}		-55°C to +125°C	01	20 typical		pF
Reference input.							
REF_{IN} input voltage		±1% specified performance	-55°C to +125°C	01	2.5		V
DC leakage current			-55°C to +125°C	01		±1	µA
REF_{IN} input impedance		f_{SAMPLE} = 200 kSPS	-55°C to +125°C	01	36 typical		kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic inputs.							
Input high voltage	V_{INH}		-55°C to +125°C	01	0.7 x V_{DRIVE}		V
Input low voltage	V_{INL}		-55°C to +125°C	01		0.3 x V_{DRIVE}	V
Input current	I_{IN}	V_{IN} = 0 V or V_{DRIVE}	-55°C to +125°C	01		±1	µA
Input capacitance 3/	C_{IN} +		-55°C to +125°C	01		10	pF
Logic outputs.							
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V	-55°C to +125°C	01	V_{DRIVE} – 0.2		V
Output low voltage	V_{OL}	I_{SINK} = 200 µA	-55°C to +125°C	01		0.4	V
Floating state leakage current			-55°C to +125°C	01		±1	µA
Floating state output capacitance 3/			-55°C to +125°C	01		1	pF
Output coding		Coding bit set to 0	-55°C to +125°C	01	Twos com plement		
		Coding bit set to 1			Straight natural binary		
Conversion rate.							
Conversion time		16 SCLK cycles, SCLK at 20 MHz	-55°C to +125°C	01		800	ns
Track and hold		Sine wave input	-55°C to +125°C	01		300	ns
acquisition time		Full scale step input				300	
Throughput rate			-55°C to +125°C	01		200	kSPS
Power requirements.							
Power supply input	AV_{DD}		-55°C to +125°C	01	2.7	5.25	V
Logic power supply input	V_{DRIVE}		-55°C to +125°C	01	2.7	5.25	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power requirements - co ntinued.							
Power supply current	(I_{DD}).	Digital inputs = 0 V or V_{DRIVE}					
During conversion		AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz	-55°C to +125°C	01		2.7	mA
		AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz				2.0	
Normal mode (static)		AV_{DD} = 2.7 V to 5.25 V, SCLK on or off	-55°C to +125°C	01	600 typical		µA
Normal mode (operational)		AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz, f_{sample} = 200 kSPS	-55°C to +125°C	01		1.5	mA
		AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz, f_{sample} = 200 kSPS				1.2	
Using auto shutdown mode		AV_{DD} = 4.75 V to 5.25 V, f_{sample} = 200 kSPS	-55°C to +125°C	01	900 typical		µA
		AV_{DD} = 2.7 V to 3.6 V, f_{sample} = 200 kSPS			650 typical		
Auto shutdown (static)		SCLK on or off	-55°C to +125°C	01		0.5	µA
Full shutdown mode		SCLK on or off	-55°C to +125°C	01		0.5	µA
Power dissipation.							
Normal mode (operational)		f_{sample} = 200 kSPS, f_{SCLK} = 20 MHz, AV_{DD} = 5 V	-55°C to +125°C	01		7.5	mW
		f_{sample} = 200 kSPS, f_{SCLK} = 20 MHz, AV_{DD} = 3 V				3.6	
Auto shutdown (static)		AV_{DD} = 5 V	-55°C to +125°C	01		2.5	µW
		AV_{DD} = 3 V				1.5	
Full shutdown mode		AV_{DD} = 5 V	-55°C to +125°C	01		2.5	µW
		AV_{DD} = 3 V				1.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification. 5/							
Clock frequency 6/	f_{SCLK}	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	10		kHz
						20	MHz
Convert timing	$t_{CONVERT}$	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	16 x t_{SCLK}		
Minimum quiet time required between $\overline{CS}$ rising edge and start of next conversion	t_{QUIET}	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	50		ns
$\overline{CS}$ to SCLK setup time	t_2	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	10		ns
Delay from $\overline{CS}$ 7/ until DOUT three state disabled	t_3	AV_{DD} = 3 V	-55°C to +125°C	01		35	ns
		AV_{DD} = 5 V				30	
Data access time 7/ after SCLK falling edge	t_4	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01		40	ns
SCLK low pulse width	t_5	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	0.4 x t_{SCLK}		ns
SCLK high pulse width	t_6	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	0.4 x t_{SCLK}		ns
SCLK to DOUT valid hold time	t_7	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	10		ns
SCLK falling edge 8/ to DOUT high impedance	t_8	AV_{DD} = 3 V	-55°C to +125°C	01	15	45	ns
		AV_{DD} = 5 V			15	35	
DIN setup time prior to SCLK falling edge	t_9	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	10		ns
DIN hold time after SCLK falling edge	t_{10}	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing specification - continued. 5/							
16th SCLK falling edge to $\overline{CS}$ high	t_{11}	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01	20		ns
Power up time from full power down / auto shutdown	t_{12}	AV_{DD} = 3 V and 5 V	-55°C to +125°C	01		1	µs

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, and f_{SCLK} = 20 MHz.

3/ Sample tested at 25°C to ensure compliance.

4/ Unless otherwise specified, V_{DD} = 2.7 V to 5.25 V, $V_{DRIVE} \leq AV_{DD}$, and REF_{IN} = 2.5 V.

5/ Sample tested at 25°C to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of AV_{DD}) and timed from a voltage level of 1.6 V, see figure1. The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

6/ The mark/space ratio for the SCLK input is 40 / 60 to 60 / 40.

7/ Measured with the load circuit of figure 1 and defined as the time required for the output to cross 0.4 V or 0.7 V_{DRIVE}.

8/ t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, quoted in the timing characteristics t_8, is the true bus relinquish time of the part and is independent of the bus loading.

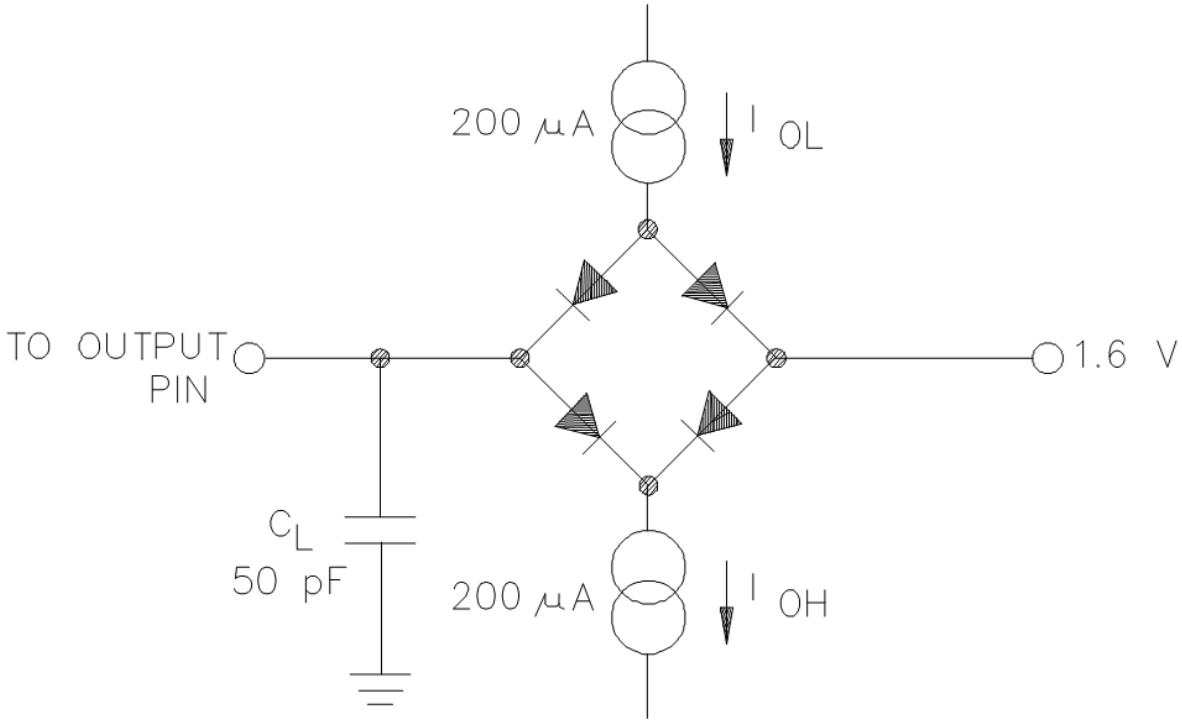

FIGURE 1. Load circuit for digital output timing specifications.

Case X

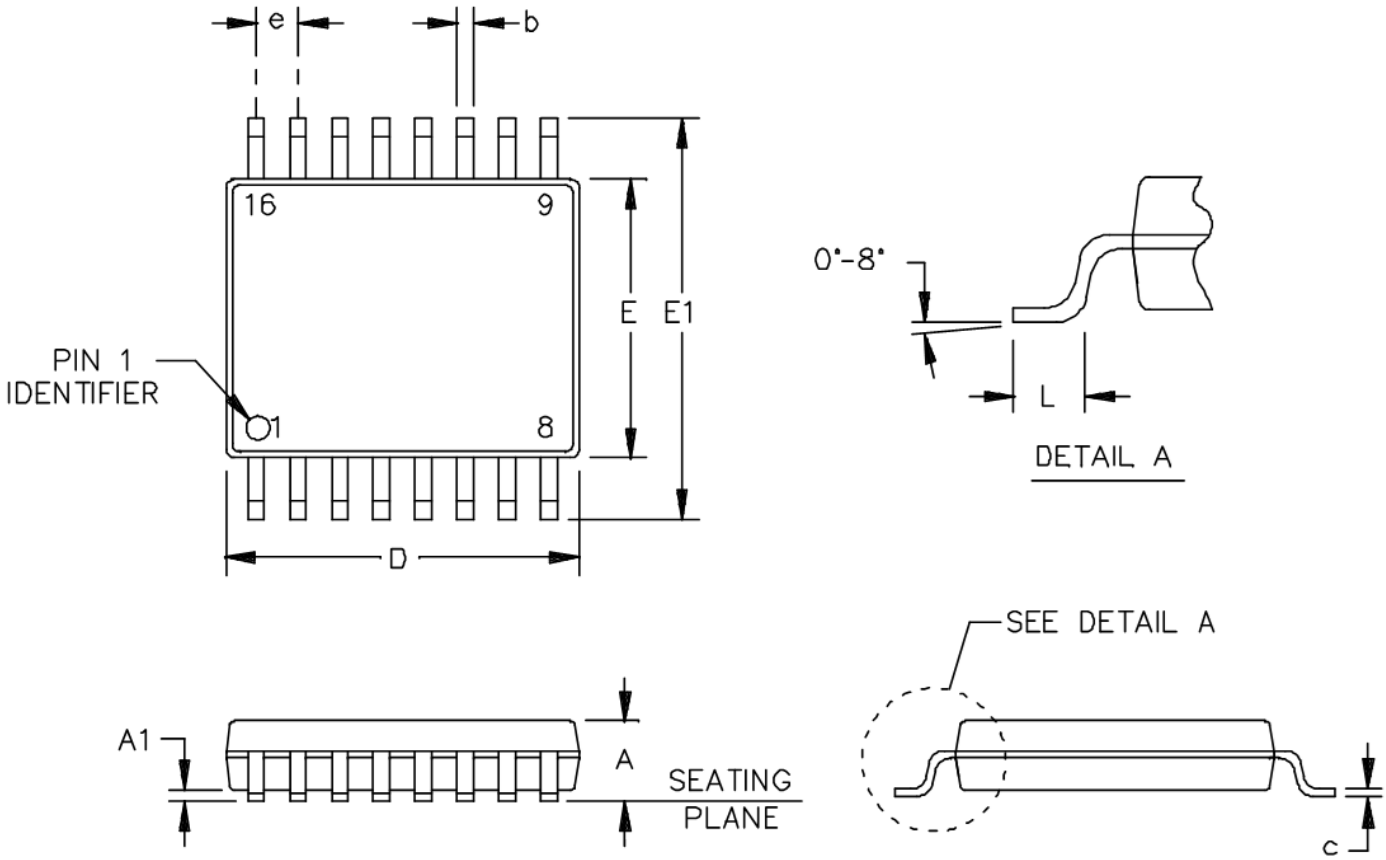

FIGURE 2. Case outline.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.001	.005	0.05	0.15
b	.007	.011	0.19	0.30
c	.003	.007	0.09	0.20
D	.192	.200	4.90	5.10
E	.169	.177	4.30	4.50
E1	.251 BSC		6.40 BSC	
e	.025 BSC		0.65 BSC	
L	.017	.029	0.45	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-153-AB.

FIGURE 2. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	SCLK
2	DIN
3	$\overline{CS}$
4	AGND
5	AV_{DD}
6	AV_{DD}
7	REF_{IN}
8	AGND
9	VIN^3
10	VIN^2
11	VIN^1
12	VIN^0
13	AGND
14	DOUT
15	V_{DRIVE}
16	AGND

FIGURE 3. Terminal connections.

Terminal symbol	Description
SCLK	Serial clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the device conversion process.
DIN	Data in. Logic input. Data to be written to the control register is provided on this input and is clocked into the register on the falling edge of SCLK.
$\overline{CS}$	Chip select. Active low logic input. This input provides the dual function of initiating conversions on the device and framing the serial data transfer.
AGND	Analog ground. Ground reference point for all circuitry on the device. All analog/digital input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
AV_{DD}	Analog power supply input. The AV_{DD} range for the device is from 2.7 V to 5.25 V. For the 0 V to 2 x REF_{IN} range, AV_{DD} should be from 4.75 V to 5.25 V.
REF_{IN}	Reference input for the device. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V $\pm$ 1% for specified performance.
V_{IN}^0 to V_{IN}^3	Analog input 0 through analog input 3. Four single ended analog input channels that are multiplexed into the on chip track and hold. The analog input channel to be converted is selected by using the address bits ADD1 through ADD0 of the control register. The address bits, in conjunction with the SEQ1 and SEQ0 bits, allow the sequencer register to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or 0 V to 2 x REF_{IN} as selected via the RANGE bit in the control register. Any used input channels should be connected to AGND to avoid noise pickup.
DOUT	Data out. Logic out. The conversion result from the device is provided on this output as serial data stream. The device data stream consists of two leading 0's and two address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided by MSB first. The output coding can be selected as straight binary or twos complement via the coding bit in the control register. The bits are clocked out on the device on the SCLK falling edge.
V_{DRIVE}	Logic power supply input. The voltage supplied at this pin determines at which voltage the serial interface of the device operates.

FIGURE 3. Terminal connections - continued.