Data Sheet

AD74115H

Single-Channel, Software Configurable Input and Output with HART Modem

FEATURES

- Single-channel software configurable input and output
- Multiple configurable modes to a single pin
  - Voltage input
  - Current input
  - Voltage output
  - Current output
  - Digital input
  - Digital output
  - 2-wire, 3-wire, or 4-wire RTD measurements
  - Thermocouple measurement
- Overvoltage tolerant on screw terminal facing pins, powered or unpowered
- Auxiliary high voltage sense pins
- 10 ppm/°C reference temperature coefficient
- 16-bit, Σ-Δ ADC with optional 50 Hz and 60 Hz rejection
- 14-bit monotonic DAC
- Unipolar and bipolar capability
- Integrated HART modem
- On-chip diagnostics including open-circuit and short-circuit detection
- Internal temperature sensor, ±5°C accuracy
- SPI-compatible
- Wide power supply range
- Programmable power control
- Temperature range: −40°C to +105°C
- 48-lead LFCSP

APPLICATIONS

- Isolated industrial control systems
- Process control
- Factory automation
- Building control systems

FUNCTIONAL BLOCK DIAGRAM

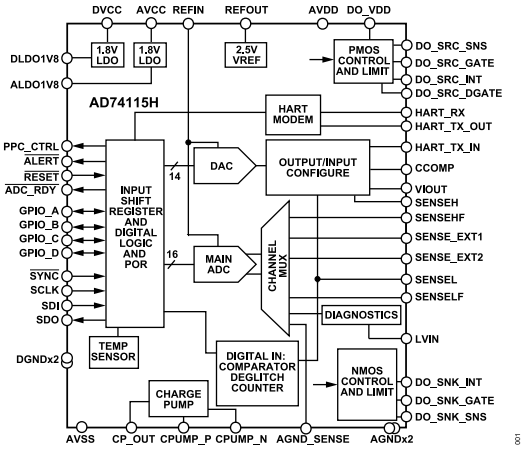

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD74115H is a single-channel, software-configurable, input and output device for industrial control applications. The AD74115H provides a wide range of use cases, integrated on a single chip. These use cases include analog output, analog input, digital output, digital input, resistance temperature detector (RTD), and thermocouple measurement capability. The AD74115H also has an integrated HART modem. A serial peripheral interface (SPI) is used to handle all communications to the device, including communications with the HART modem. The digital input and digital outputs can be accessed via the SPI or the general-purpose input and output (GPIO) pins to support higher speed data rates.

The device features a 16-bit, Σ-Δ analog-to-digital converter (ADC) and a 14-bit digital-to-analog converter (DAC). The AD74115H contains a high accuracy 2.5 V on-chip reference that can be used as the DAC and ADC reference.

Power and isolation can be provided using the ADP1034 companion product. When using the ADP1034 and AD74115H together, programmable power control (PPC) is available on the positive analog supply, AVDD, which allows for an optimized power solution in the end application. An on-chip charge pump can be enabled if unipolar capability is required.

COMPANION PRODUCTS

- **Power and Data Isolation with PPC: ADP1034**
- **Voltage Reference: ADR4525**

Rev. 0

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REVISION HISTORY

8/2022—Revision 0: Initial Version

SPECIFICATIONS

VOLTAGE OUTPUT

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. The sense resistor (R_{SENSE}) = 100 Ω (ideal), the load resistor (R_{LOAD}) = 100 kΩ, and the load capacitor (C_{LOAD}) = 4.7 nF per the recommended configuration. Note that the headroom specification for AVDD and AVSS must be considered when setting supply voltages.

Table 1. Voltage Output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Resolution	14			Bits	
Output Range	0		12	V	
	−12		+12	V	
ACCURACY					
Total Unadjusted Error (TUE)	−0.2		+0.2	%FSR	
TUE at 25°C	−0.1		+0.1	%FSR	
Integral Nonlinearity (INL)	−3.0		+3.0	LSB	
Differential Nonlinearity (DNL)	−1.0		+1.0	LSB	Guaranteed monotonic
Offset Error	−5.5		+5.5	mV	Error with Code 0x0000 loaded to the DAC, 0 V to 12 V range only
Offset Error at 25°C	−3.0		+3.0	mV	0 V to 12 V range only
Bipolar Zero Error	−13		+13	mV	Error with midscale code loaded to the DAC in a ±12 V range
Bipolar Zero Error at 25°C	−13		+13	mV	±12 V range only
Gain Error	−0.2		+0.2	%FSR	
Gain Error 25°C	−0.12		+0.12	%FSR	
OUTPUT CHARACTERISTICS					
Load[1]	1	100		kΩ	
Headroom[1]		2.2		V	Voltage difference required between AVDD and the input and output positive (I/OP) screw terminal to provide 12 V across a 1 kΩ load
Footroom[1]		2.2		V	Voltage difference required between AVSS and the I/OP screw terminal to provide −12 V across a 1 kΩ load
Short-Circuit Current		32		mA	Sourcing and sinking, I_LIMIT bit = 0 (default)
		16		mA	Sourcing and sinking, I_LIMIT bit = 1
Short-Circuit Activation Time[1]		2		ms	Time in short circuit before alert is generated
Maximum Capacitive Load[1]			14	nF	Maximum system capacitance on the I/OP screw terminal, including the recommended 4.7 nF C_{LOAD} when the compensation capacitor (C_{COMP}) is not connected
			2	µF	Maximum system capacitance on the I/OP screw terminal, including the recommended 4.7 nF C_{LOAD} when a C_{COMP} = 220 pF is connected
DC Output Impedance[1]		0.1		Ω	
DC Power Supply Rejection Ratio (PSRR)[1]		90		dB	PSRR measured with a change in AVDD
DYNAMIC PERFORMANCE[1]					
Output Voltage (V_{OUT}) Settling Time		85		µs	11 V step (0.5 V to 11.5 V or 11.5 V to 0.5 V) to ±0.05 % FSR, C_{LOAD} = 4.7 nF, and no C_{COMP} is connected
		110		µs	22 V step (−11 V to +11 V or +11 V to −11 V) to ±0.05 % FSR, C_{LOAD} = 4.7 nF, and no C_{COMP} is connected
Output Voltage Settling Time with CCOMP Connected		400		µs	11 V step (0.5 V to 11.5 V or 11.5 V to 0.5 V) to ±0.05 % FSR, C_{LOAD} = 4.7 nF, and 220 pF C_{COMP} is connected
		400		µs	22 V step (−11 V to +11 V or +11 V to −11 V) to ±0.05 % FSR, C_{LOAD} = 4.7 nF, and 220 pF C_{COMP} is connected

SPECIFICATIONS

Table 1. Voltage Output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Noise (External Reference)					Measured at the I/OP screw terminal, 2.5 V output
Output Noise		0.17		LSB p-p	0.1 Hz to 10 Hz bandwidth, 100 kΩ load
Output Noise Spectral Density					
0 V to 12 V Range		405		nV/√Hz	Measured at 1 kHz, midscale output
−12 V to +12 V Range		815		nV/√Hz	Measured at 1 kHz, midscale output
AC PSRR		65		dB	200 mV at 1 kHz sine wave superimposed on the AVDD supply

[1] Guaranteed by design and characterization.

CURRENT OUTPUT (I_{OUT}) AND I_{OUT} WITH HART

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal), R_{LOAD} = 250 Ω, and C_{LOAD} = 4.7 nF per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

Table 2. Current Output (I_{OUT}) and I_{OUT} with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I_{OUT}					
Resolution	14			Bits	
Output Range	0		25	mA	
ACCURACY					
TUE[1]	−0.2		+0.2	% FSR	
TUE at 25°C[1]	−0.1		+0.1	% FSR	
INL	−3.5		+3.5	LSB	From zero-scale to full-scale
DNL	−1		+1	LSB	Guaranteed monotonic
Offset Error	−15		+15	µA	
Offset Error at 25°C	−8		+8	µA	
Gain Error[1]	−0.2		+0.2	% FSR	
Gain Error at 25°C[1]	−0.1		+0.1	% FSR	
OUTPUT CHARACTERISTICS[2]					
Headroom		3.3		V	Voltage difference required between AVDD and the I/OP screw terminal to source 20 mA
Open Circuit Voltage		AVDD		V	
Sinking Current Limit		3.7		mA	I_LIMIT bit = 0 (default)
		1.2		mA	I_LIMIT bit = 1
Alert Activation Time		2		ms	Time in open or short circuit before alert is generated
Output Impedance		4		MΩ	
DC PSRR		50		nA/V	PSRR measured with a change in AVDD
DYNAMIC PERFORMANCE[2]					
Output Current Settling Time		90		µs	3.2 mA to 23 mA step up or down, time to settle within a window of ±100 µA of final current
Output Current Settling Time (with HART Slew Enabled)		60		ms	With HART slew enabled, 3.2 mA to 23 mA, step up or step down, and time to settle within a window of ±100 µA of final current

SPECIFICATIONS

Table 2. Current Output (I_{OUT}) and I_{OUT} with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Noise					Measured at the I/OP screw terminal with 250 Ω load, 12.5 mA output
Output Noise		0.34		LSB p-p	0.1 Hz to 10 Hz bandwidth
Output Noise Spectral Density		2		nA/√Hz	Measured at 1 kHz, 12.5 mA output
AC PSRR		75		dB	Voltage on the supply at 1 kHz to the voltage across the 250 Ω

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.

[2] Guaranteed by design and characterization.

VOLTAGE INPUT

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal), and C_{LOAD} = 4.7 nF per the recommended configuration. Note that the required input range for AVDD and AVSS must be considered when setting the supply voltages.

Table 3. Voltage Input

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE INPUT					
Input Resolution	16			Bits	
Input Range (SENSELF)	0		12	V	
	−12		+12	V	
ACCURACY[1]					
TUE	−0.1		+0.1	% FSR	
TUE at 25°C	−0.02		+0.02	% FSR	
INL	−4		+4	LSB	
Offset Error	−4		+4	LSB	
Offset Error at 25°C	−2		+2	LSB	
Gain Error	−750		+750	ppm FSR	
Gain Error at 25°C	−330		+330	ppm FSR	
OTHER INPUT SPECIFICATIONS					
Footroom[1]	AVSS + 2			V	
Headroom[1]			AVDD − 0.2	V	
DC PSRR[1]		10		µV/V	PSRR measured with a change in AVDD, AVSS, AVCC, and DVCC
Normal Mode Rejection[1]		80		dB	50 Hz ± 1 Hz and 60 Hz ± 1 Hz
Input Bias Current	−30		+30	nA	As seen from the I/OP screw terminal, ADC is either idle or converting; does not include transient voltage suppressor (TVS) leakage
Input Bias Current at 25°C		±6		nA	

[1] Guaranteed by design and characterization.

SPECIFICATIONS

CURRENT INPUT EXTERNALLY POWERED AND CURRENT INPUT EXTERNALLY POWERED WITH HART

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (Ideal), and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 4. Current Input Externally Powered and Current Input Externally Powered with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUT					
Input Resolution	16			Bits	
Input Range	0		25	mA	Sensed across the external 100 Ω resistor
Screw Terminal Voltage	0			V	
Short-Circuit Current Limit	25		35	mA	Nonprogrammable
ACCURACY					
TUE[1]	−0.1		+0.1	% FSR	
TUE at 25°C[1]	−0.05		+0.05	% FSR	
INL	−4	±2	+4	LSB	Linearity specified from 0.1 mA to 25 mA
Offset Error	−4		+4	LSB	
Offset Error at 25°C	−1.5		+1.5	LSB	
Gain Error[1]	−250		+250	ppm FSR	
Gain Error at 25°C[1]	−150		+150	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[2]		In order of noise			
Input Impedance (Without HART Termination)		165		Ω	Current input, externally powered selected, including 100 Ω R_{SENSE}
Input Impedance (with HART Resistive Termination)	230		330	Ω	Current input, externally powered with HART selected, including 100 Ω R_{SENSE}
Compliance (Without HART Termination)[2]		4.2		V	Current input, externally powered selected, and minimum voltage required at the I/OP screw terminal to sink 25 mA
Compliance (with HART Resistive Termination)[2]		6.6		V	Current input, externally powered with HART selected, and minimum voltage required at the I/OP screw terminal to sink 20 mA

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.

[2] Guaranteed by design and characterization.

CURRENT INPUT LOOP POWERED AND CURRENT INPUT LOOP POWERED WITH HART

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (iIdeal), and C_{LOAD} = 4.7 nF per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

Table 5. Current Input Loop Powered and Current Input Loop Powered with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUTS					
Input Resolution	16			Bits	
Input Range	0		25	mA	Sensed across external 100 Ω resistor
Screw Terminal Voltage			AVDD	V	
NonHART Current Limit	0		25	mA	Programmable current limit, 14-bit resolution
HART Mode Current Limit	23		30	mA	Current input, loop powered with HART enabled, nonprogrammable

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Table 5. Current Input Loop Powered and Current Input Loop Powered with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
TUE[1]	−0.1		+0.1	% FSR	
TUE at 25°C[1]	−0.05		+0.05	% FSR	
INL	−4		+4	LSB	Linearity specified from 0.1 mA to 25 mA range
Offset Error	−4		+4	LSB	
Offset Error at 25°C	−1.5		+1.5	LSB	
Gain Error[1]	−250		+250	ppm FSR	
Gain Error at 25°C[1]	−150		+150	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[2]		In order of noise			
Input Impedance (Without HART Termination)		165		Ω	With current input, loop powered selected, includes 100 Ω R_{SENSE}
Input Impedance (with HART Resistive Termination)	230		330	Ω	With current input, loop powered with HART selected, includes 100 Ω R_{SENSE}
Headroom (Without HART Termination)[2]		3.8		V	Minimum required difference between AVDD and the I/OP screw terminal voltage to source 25 mA, and current input, loop powered selected
Headroom (with HART Resistive Termination)[2]		6.0		V	Minimum required difference between AVDD and the I/OP screw terminal voltage to source 20 mA, and current input, loop powered with HART selected

[1] R_{SENSE} accuracy directly impacts the TUE and gain error.

[2] Guaranteed by design and characterization.

RESISTANCE 2-WIRE MEASUREMENT

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal), and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 6. Resistance 2-Wire Measurement

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0		1	MΩ	2-wire RTD measurements supported
Bias Voltage		2.5		V	
Pull-Up Resistor ($R_{PULL-UP}$)		2.1		kΩ	$R_{PULL-UP}$ is composed of the external 2 kΩ resistor and the external 100 Ω R_{SENSE}
ACCURACY[1]					Refer to Figure 13
Measurement Range					
1 Ω to 50 Ω		0.28		Ω	
50 Ω to 3 kΩ		±0.07, ±0.28		%, Ω	±% of the measured value plus ± fixed error
3 kΩ to 10 kΩ		±0.1		%	±% of the measured value
10 kΩ to 200 kΩ		±1.3		%	±% of the measured value
200 kΩ to 1 MΩ		±6.0		%	±% of the measured value

[1] Guaranteed by design and characterization.

SPECIFICATIONS

3-WIRE RTD MEASUREMENT

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 7. 3-Wire RTD Measuremen

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0.001		4	kΩ	
Programmable Excitation Current		250		µA	The voltage generated across the (reference resistor (R_{REF}) + the RTD resistor (R_{RTD})) must be less than the AVCC voltage (V_{AVCC})
		500		µA	
		750		µA	
		1		mA	
Current Matching					
Excitation Current Matching	−0.5		+0.5	%	For 500 µA, 750 µA, and 1 mA
Current Matching Drift		5		ppm/°C	
Open-Circuit Detect Voltage					Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit
SENSEH		4.0		V	
SENSE_EXT1		2.7		V	
ACCURACY[1]					
Measurement Range					
1 Ω to 40 Ω		±0.036, ±0.023		%, Ω	±% of the measured value plus ± the fixed error, suitable for Pt10, Cu10, or similar, 1 mA excitation current and 104.16 mV ADC range
10 Ω to 400 Ω		±0.037, ±0.037		%, Ω	±% of the measured value, suitable for Pt100 or similar, 1 mA excitation current, and 0.625 V ADC range
100 Ω to 4 kΩ		±0.084, ±0.358		%, Ω	±% of the measured value, suitable for Pt1000, and 500 µA excitation current, and 0 V to 12 V ADC range

[1] Guaranteed by design and characterization.

4-WIRE RTD MEASUREMENT

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 8. 4-Wire RTD Measurement

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0.001		4	kΩ	
Programmable Excitation Current		250		µA	The voltage generated across (R_{REF} + R_{RTD}) must be less than V_{AVCC}
		500		µA	
		750		µA	
		1		mA	
SENSEH Open-Circuit Detect Voltage		4.0		V	Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit

SPECIFICATIONS

Table 8. 4-Wire RTD Measurement

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1]					
Measurement Range					
1 Ω to 40 Ω		±0.036, ±0.006		%, Ω	±% of the measured value plus ± the fixed error, suitable for Pt10, Cu10, or similar, and 1 mA excitation current, and 104.16 mV ADC range
10 Ω to 400 Ω		±0.037, ±0.018		%, Ω	±% of the measured value, suitable for Pt100 or similar, and 1 mA excitation current, and 0.625 V ADC range
100 Ω to 4 kΩ		±0.084, ±0.344		%, Ω	±% of the measured value, suitable for Pt1000, 500 µA excitation current, and 0 V to 12 V ADC range

[1] Guaranteed by design and characterization.

DIGITAL INPUT LOGIC

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 9. Digital Input Logic

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Unbuffered Input Data Rate			200	kHz	The VIOUT pin is driven by a low impedance source, 0 V to 12 V signal, duty cycle: 60:40
Buffered Input Data Rate		20		kHz	The SENSEL pin is driven by a low impedance source, 0 V to 12 V signal, duty cycle: 60:40
Input Voltage Range[1]	−45		+45	V	
Input Resistance		1.3		MΩ	High speed mode
Open-Circuit Detect Current	0.05		0.35	mA	Window for open-circuit detection for compliance with IEC 61131-2 Type 3D
Short-Circuit Detect Current	6			mA	For IEC 61131-2 Type 3D
CURRENT SINK					
Range 0					
Series Resistor Value		2.7		kΩ	
Current Sink Range	0		3.7	mA	Typical programmable current sink to AGND
Current Sink Resolution		120		µA	
Current Sink Accuracy		±2		% FSR	
Current Sink at Decimal Code 20	2.1	2.4		mA	Recommended for IEC 61131-2 Type I and Type III for the I/OP screw terminal > 6 V, DIN_SINK = Decimal Code 20
Current Sink at Decimal 15		1.8		mA	Recommended for IEC 61131-2 Type 3D, DIN_SINK bits = Decimal Code 15
Range 1					
Series Resistor Value		1		kΩ	
Current Sink Range	0		7.4	mA	Typical programmable current sink to AGND
Current Sink Resolution		240		µA	
Current Sink Accuracy		±2		% FSR	
Current Sink at Decimal Code 29	6.1	7.0		mA	Recommended for IEC 61131-2 Type II for the I/OP screw terminal > 7 V, DIN_SINK bits = Decimal Code 29

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Table 9. Digital Input Logic

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE THRESHOLDS MODES					
Threshold Range	AVSS + 2.0		AVDD – 1.5	V	Programmable trip level
AVDD Threshold Mode					
Threshold Resolution		AVDD/50		V	
Hysteresis		AVDD/50		V	
Fixed Threshold Mode					
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Voltage at Decimal Code 55	8.0	8.5	8.8	V	Rising trip point, recommended for IEC 61131-2 Type I, Type II, and Type III, COMP_THRESH bits = Decimal Code 55
Threshold Accuracy		2		% FSR	

[1] Guaranteed by design and characterization.

DIGITAL INPUT LOOP POWERED

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration. Note that the headroom specification for AVDD must be considered when setting supply voltages.

Table 10. Digital Input Loop Powered

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input Data Rate[1]			5	kHz	Unfiltered input, typically dominated by wetting current, load capacitance, and threshold voltage
Dry Contact Wetting Current Range	0		25	mA	Loop powered, programmable current
Headroom[1]		3.3		V	Required voltage difference between AVDD and the I/OP screw terminal to source 20 mA
THRESHOLD MODES					
Threshold Range	AVSS + 2.0		AVDD – 1.5	V	Programmable trip level
AVDD Threshold Mode					
Threshold Resolution		AVDD/50		V	
Hysteresis		AVDD/50		V	
Fixed Threshold Mode					
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Accuracy		2		% FSR	

[1] Guaranteed by design and characterization.

SPECIFICATIONS

DIGITAL OUTPUTS (SOURCING AND SINKING)

DO_VDD = +10 V to +35 V, AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. C_{LOAD} = 4.7 nF per the recommended configuration.

Table 11. Digital Outputs (Sourcing and Sinking)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DO_VDD SUPPLY RANGE	10	24	35	V	
EXTERNAL DIGITAL OUTPUT					Sourcing and sinking
Short Circuit					
Short-Circuit Voltage, $V_{SC}1$	160		240	mV	With a 0.15 Ω set resistor (R_{SET}), the current clamps at 1.3 A
Short-Circuit Voltage, $V_{SC}2$	80		120	mV	With a 0.15 Ω R_{SET}, the current clamps at 667 mA
Short-Circuit Clamp Time[1]		1.2		µs	FET input capacitance (C_{ISS}) < 500 pF, and the time for the short-circuit clamp to engage during a 0 Ω short-circuit
Time Out 1, T1[1]	0.1		100	ms	Typical programmable times
Time Out 2, T2[1]	0.1			ms	Typical programmable times
On and Off Times[1]					
On Time, t_{ON}		20		µs	FET C_{ISS} < 500 pF, and the time from $\overline{SYNC}$ rising edge to settle to 90%
Off Time, t_{OFF}		3		µs	FET C_{ISS} < 500 pF, and the time from the $\overline{SYNC}$ rising edge to FET disable
Gate Drive Voltage					
Current Sourcing	−12	−10	−8	V	The DO_SRC_GATE voltage with respect to DO_VDD
Current Sinking			AVCC	V	The DO_SNK_GATE voltage
DO_SRC_DGATE Current Sink		1		mA	To AVSS, when DO_EXT_MODE is configured for the external source with a smart diode
INTERNAL DIGITAL OUTPUT					
On Resistance, R_{ON}					
Sourcing Mode		7		Ω	
Sinking Mode		3.5		Ω	
Short-Circuit					
Short-Circuit Current 1	220		350	mA	
Short-Circuit Current 2	105		180	mA	
Short-Circuit Clamp Time[1]		2		µs	Time for the short-circuit clamp to engage during a 0 Ω short circuit
Time Out 1, T1[1]	0.018		100	ms	Typical programmable times
Time Out 2, T2[1]	0.018			ms	Typical programmable times
Thermal Shutdown[1]					Thermal shutdown for internal digital output
Disabled Temperature		140		°C	
Reenabled Temperature		130		°C	
On and Off Times[1]					
On Time, t_{ON}		10		µs	Time from the $\overline{SYNC}$ rising edge to settle to 90%
Off Time, t_{OFF}		2		µs	Time from the $\overline{SYNC}$ rising edge to FET disable
PUSH AND PULL MODE[1]					Push and pull timing for the external FET is dependent on the C_{ISS} of the external FET
Output Data Rate					
Internal FETs		50		kHz	
External FETs		10		kHz	

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Table 11. Digital Outputs (Sourcing and Sinking)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Propagation Delay[1]					From the $\overline{\text{SYNC}}$ rising or the GPIO edge (whichever is in use) to a 0.5 V transition on the I/OP screw terminal
Propagation High Time, t_{PH}, and Propagation Low Time, t_{PL}, Internal FETs		4		µs	
t_{PH} and t_{PL}, External FETs		7		µs	FET C_{ISS} < 1 nF
Transition Time[1]					10% to 90% of the transition on the I/OP screw terminal
Rise, t_R, and Fall, t_F, Internal FETs		2		µs	
t_R and t_F External FETs		5		µs	

[1] Guaranteed by design and characterization.

SPECIFICATIONS

ADC SPECIFICATIONS

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration. Note that the required input range for AVDD and AVSS must be considered when setting the supply voltages.

Table 12. ADC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC SPECIFICATIONS					
Resolution	16			Bits	
No Missing Codes[1]	16			Bits	
Conversion Rates[1]					Sample rates vary depending on the number of ADC measurements selected and the use of single or continuous conversion modes
		10		SPS	50 Hz and 60 Hz rejection enabled
		20		SPS	50 Hz and 60 Hz rejection enabled
		1.2		kSPS	50 Hz and 60 Hz rejection disabled
		4.8		kSPS	50 Hz and 60 Hz rejection disabled
		9.6		kSPS	50 Hz and 60 Hz rejection disabled
Absolute Input Voltage[1]	AVSS + 2		AVDD − 0.2	V	
Noise[1]					Refer to Table 28
Common-Mode Rejection Ratio[1]		95		dB	
ADC INPUT RANGES					
0 V to +12 V, ±12V					Typically used to measure the voltage across the I/OP to I/ON screw terminals (I/ON is the input and output negative, and I/OP is the input and output positive), and also used for SENSE_EXT1 and SENSE_EXT2
Range	0		12	V	
	−12		+12	V	
TUE[1]	−0.1		+0.1	% FSR	
INL[1]	−4		+4	LSB	
Offset Error	−4		+4	LSB	
Gain Error	−750		+750	ppm FSR	
0 V to 2.5 V, −2.5 V to 0 V, ±2.5 V					Typically used to measure the current through the R_{SENSE} resistor
Range	0		2.5	V	For current flowing out of the AD74115H through the 100 Ω R_{SENSE}
	−2.5		0	V	For current flowing into the AD74115H across the 100 Ω R_{SENSE}
	−2.5		+2.5	V	Typically used to measure bidirectional current across the 100 Ω R_{SENSE} in voltage output mode
TUE	−0.1		+0.1	% FSR	
INL	−4		+4	LSB	
Offset Error	−4		+4	LSB	
Gain Error	−250		+250	ppm FSR	
0 V to 0.625 V					Typically used to measure 3-wire and 4-wire RTDs
Range	0		0.625	V	
TUE[1]	−0.1		+0.1	% FSR	
INL[1]	−4		+4	LSB	
Offset Error	−10		+10	LSB	
Gain Error	−250		+250	ppm FSR	
±104.16 mV					Typically used to measure thermocouple voltages in voltage input mode
Range	−104.16		+104.16	mV	
TUE[1]	−0.1		+0.1	% FSR	
INL[1]	−4		+4	LSB	

SPECIFICATIONS

Table 12. ADC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Offset Error	−25	+3	+25	LSB	Offset at high temperatures is dominated by leakage through external R_{SENSE}
Gain Error	−500		+500	ppm FSR	
DIAGNOSTICS SPECIFICATIONS					
External Diagnostics					
LVIN Pin 2.5 V Range					
Range	0		2.5	V	
TUE[1]	−0.05		+0.05	% FSR	
INL[1]	−4		+4	LSB	
Offset Error	−4		+4	LSB	
Gain Error	−200		+200	ppm FSR	
Noise[1]					Refer to Table 28
Sense Pins Diagnostics					SENSEL, SENSE_EXT1, and SENSE_EXT2
Accuracy		±0.25		% FSR	
DO Current Sense Accuracy					
External DO		±2		mV	
Internal DO		±5		mA	At 25°C, sourcing and sinking modes
Internal Diagnostics					
Accuracy		±2		%	Percentage of measured value
TEMPERATURE SENSOR[1]					
Accuracy		±5		°C	
Resolution		0.2		°C	

[1] Guaranteed by design and characterization; not production tested.

HART MODEM COMMUNICATIONS

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal), R_{LOAD} = 250 Ω, and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 13. HART Modem Communications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSITION TIME FROM HART POWER DOWN TO NORMAL OPERATING MODE[1]		30		µs	HART modem is powered up via the MODEM_PWRUP bit in the HART_CONFIG register
HART_RX SIGNAL RANGES					
Input Voltage Range	0		2.5	V	
Data Carrier Detect Assert	60	100	110	mV p-p	Range within which assert occurs
High Impedance Devices[1]	120		1500	mV p-p	
Low Impedance Devices[1]	120		800	mV p-p	
HART_TX					
Output Voltage Range					
Current Output	400		600	mV p-p	Measured at the I/OP screw terminal with a current range of 3.2 mA to 23 mA, and a 500 Ω load in current output mode
Current Input	400		800	mV p-p	Measured at the I/OP screw terminal with a current range of 3.2 mA to 23 mA, and a 1 kΩ load in current input (loop powered or externally powered) mode
Mark Frequency		1200		Hz	
Space Frequency		2200		Hz	

SPECIFICATIONS

Table 13. HART Modem Communications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Frequency Error	−1.0		+1.0	%	

[1] Guaranteed by design and characterization; not production tested.

GENERAL SPECIFICATIONS

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 100 Ω (ideal) and C_{LOAD} = 4.7 nF per the recommended configuration.

Table 14. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SPECIFICATIONS					
Reference Input					
Reference Input Voltage		2.5		V	Accuracy of the external reference has an impact on the accuracy of the AD74115H
DC Input Current	−1		+1	µA	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C
Reference Temperature Coefficient[1]			10	ppm/°C	
Output Voltage Drift vs. Time[1]		500		ppm FSR	Drift after 1000 hours, T_A = 85°C
Output Noise[1]		18		µV p-p	0.1 Hz to 10 Hz bandwidth.
Output Noise Spectral Density[1]		95		nV/√Hz	Frequency = 10 kHz
Capacitive Load[1]		22	50	nF	On REFOUT pin
CHARGE PUMP[2]					
Voltage		−DVCC		V	When enabled, the charge pump generates a voltage that is equal to the negative of DVCC
Accuracy		±10		%	
Output Impedance[1]		12.5		Ω	
Power-Up Time[1]		2.2		ms	
FET LEAKAGE COMPENSATION[1]					
Input Voltage Range					Voltage range on the I/OP terminal when leakage compensation is enabled
Sourcing External FET	AVSS + 2		AVDD − 1		Typical input voltage range for leakage compensation
Sinking External FET	0		AVDD − 1		Typical input voltage range for leakage compensation
Voltage Across External Blocking Diode		15		mV	FET leakage compensation enabled, for currents up to 40 µA leakage current in screw terminal
SENSE PINS					SENSEH, SENSEL, SENSEHF, SENSELF, SENSE_EXT1, and SENSE_EXT2
Input Bias Current	−25		+25	nA	
Input Bias Current at 25°C		2		nA	
Input Bias Matching			10	nA	Worst case difference between any of the SENSEHF, SENSELF, SENSE_EXT1, and SENSE_EXT2 pins
High Voltage Buffer Supply Current					
AVDD Current		190		µA	
AVSS Current		190		µA	
High Voltage Buffer Power-Up Time[1]		100		µs	

SPECIFICATIONS

Table 14. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BURNOUT CURRENTS					Programmable source or sink currents
VIOUT Current		1, 10		µA	
SENSE_EXT1 and SENSE_EXT2 Current		0.05, 0.5, 1, 10		µA	
TEMPERATURE ALERT AND RESET[1]					
Temperature Alert		115		°C	Junction temperature, high temperature event flags the alert status and the $\overline{\text{ALERT}}$ pin (if unmasked)
Temperature Alert Accuracy		5		°C	
Temperature Reset		145		°C	Junction temperature, resets the device if over temperature event when the EN_THERM_RST bit =1
Temperature Reset Accuracy		5		°C	
LOGIC INPUTS					SCLK, SDI, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, GPIO_x (as inputs), and PPC_CTRL (as an input)
Input Voltage					
High (V_{IH})	0.7 × DVCC			V	
Low (V_{IL})			0.2 × DVCC	V	
Input Current	−1		+1	µA	Per pin
Input Capacitance[1]		3		pF	Per pin
LOGIC OUTPUTS					
SDO and PPC_CTRL Pins					
Output Low Voltage (V_{OL})			0.4	V	Sink current (I_{SINK}) = 200 µA
Output High Voltage (V_{OH})	DVCC − 0.4			V	Source current (I_{SOURCE}) = 200 µA
High Impedance Leakage Current	−1		+1	µA	SDO pin only
High Impedance Output Capacitance[1]		3		pF	SDO pin only
GPIO_x Pin					As outputs
V_{OL}			0.4	V	Capable of sinking 3 mA
V_{OH}	DVCC − 0.4			V	
Pull-Down Resistance		100		kΩ	
High Impedance Leakage Current	−1		+1	µA	
OPEN-DRAIN LOGIC OUTPUTS					$\overline{\text{ADC\_RDY}}$ and $\overline{\text{ALERT}}$
V_{OL}			0.4	V	Capable of sinking 2.5 mA
High Impedance Leakage Current	−1		+1	µA	
POWER SUPPLY MONITORS					Falling thresholds
AVDD Threshold		5.7		V	
AVSS Threshold		−1.6		V	
AVCC Threshold		4.1		V	
DVCC Threshold		2.0		V	
ALDO1V8 Threshold		1.3		V	
DO_VDD Threshold		9.5		V	
POWER REQUIREMENTS					
Supply Voltages[1]					
AVDD	6	24	28.8	V	Headroom requirements must be met for specific application
AVSS	−18	−15	−2.5	V	Footroom requirements must be met for specific application
DVCC	2.7	3.3	5.5	V	
AVCC	4.5	5.0	5.5	V	
DO_VDD	10		35	V	

SPECIFICATIONS

Table 14. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Supply Quiescent Currents					
AVDD Current	3.5	3.9	4.3	mA	Configured in voltage or current output mode, no load current
	3.1	3.8	4.8	mA	Configured in any RTD or any analog or digital input mode, no load current
	2.8	3.2	3.6	mA	Configured in digital output mode
AVSS Current	3.4	4.3	5.1	mA	Configured in any RTD or any analog or digital input mode
DVCC Current	1.0	1.4	1.7	mA	Configured in any RTD or any analog or digital input mode
AVCC Current	4.0	5.0	6.2	mA	Configured in any RTD or any analog or digital input mode
DO_VDD Current		50		µA	Configured in high Impedance mode
	400		600	µA	Configured in any digital output mode
CONFIGURATION TIMING					
Device Power-Up Time[1]		1		ms	After all supplies are powered up
Device Reset Time[1]		1		ms	Time taken for device reset and calibration memory upload to complete hardware or software reset events after the device is powered up (see Table 15 for pulse width specifications)
Use Case Switch Time[1]		200		µs	Time in use case before changing to another use case
Channel Function Enable Time		200		µs	Wait time after the CH_FUNC_SETUP register is programmed before new DAC codes can be loaded

[1] Guaranteed by design and characterization.

[2] If the charge pump is enabled, connect the CP_OUT pin to AVSS and ensure that there is no other source on AVSS.

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TIMING CHARACTERISTICS

SPI Timing Specifications

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, SDO C_{LOAD} = 30 pF, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted.

Table 15. SPI Timing Specifications

Parameter[1, 2]	Description	DVCC = 2.7 V to 5.5 V	Unit
t_1	SCLK pin cycle time	42	ns min
t_2	SCLK high time	17	ns min
t_3	SCLK low time	17	ns min
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time	21	ns min
t_5	Last SCLK falling edge to $\overline{SYNC}$ rising edge	21	ns min
t_6	$\overline{SYNC}$ high time	450	ns min
t_7	Data setup time	5	ns min
t_8	Data hold time	5	ns min
t_9	$\overline{RESET}$ pulse width	50	µs min
		1[3]	ms max
t_{10}	SCLK rising edge to SDO valid	23	ns max
t_{11}	$\overline{SYNC}$ falling edge to SDO valid (for readback MSB only)	20	ns max
t_{12}	$\overline{SYNC}$ rising edge to SDO tristate	16	ns max
t_{13}	$\overline{SYNC}$ rising edge to DAC output response time	2	µs typ
t_{14}[4]	$\overline{ADC\_RDY}$ pulse	25	µs typ

1 All input signals are specified with t_R= t_F= 5 ns (10% to 90% of the voltage on the DVCC pin (V_{DVCC})) and timed from a voltage level of V_{DVDD}/2.

2 Guaranteed by design and characterization; not production tested.

3 Charge pump voltage decays while in reset.

4 See Figure 53.

SPI Timing Diagram

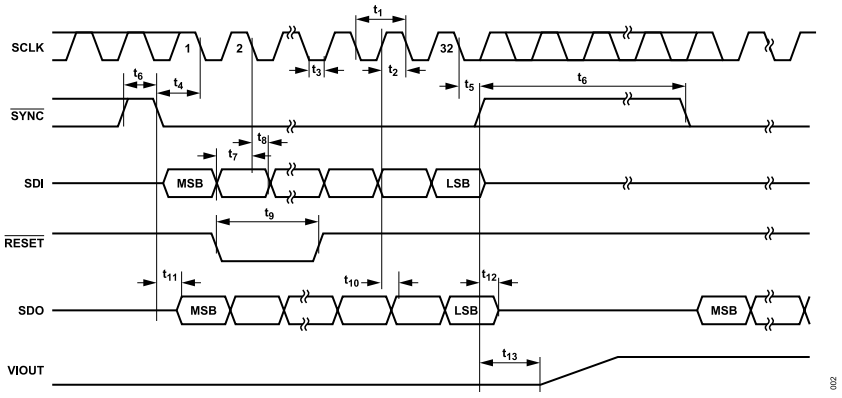

Figure 2. SPI Timing Diagram

SPECIFICATIONS

One-Wire Serial Interface (OWSI) Timing Specifications

AVDD = +6 V to +28.8 V, AVSS = −2.5 V to −18 V, AGND = DGND = 0 V, REFIN = +2.5 V (ideal), DVCC = +2.7 V to +5.5 V, AVCC = +4.5 V to +5.5 V, PPC_CTRL C_{LOAD} = 30 pF, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted.

Table 16. OWSI Timing Specifications

Parameter[1, 2]	Description	Min	Max	Unit
t_{PPC1}	Bit period	4900		ns
t_{PPC2}	Start detect high time	140	260	ns
t_{PPC3}	Start detect low time	140	260	ns
t_{PPC4}	Start detect time (time for two successive pulses)	450	750	ns
t_{PPC5}	Logic low time	300	500	ns
t_{PPC6}	Logic high time	3400	4000	ns
t_{PPC7}	OWSI subordinate control start time	500	2200	ns
t_{PPC8}	OWSI subordinate control end time	2700	4500	ns
t_{PPC9}	Time when the OWSI main takes back control of the bus when there is no OWSI subordinate response	3400	3600	ns
t_{PPC10}	Time when the OWSI main takes back control of the bus when the OWSI subordinate responds by pulling low		2700	ns

[1] All input signals are specified with t_R= fall time t_F = 5 ns (10% to 90% of the voltage on the DVDD pin (V_{DVDD})) and timed from a voltage level of $V_{DVDD}/2$.

[2] Guaranteed by design and characterization; not production tested.

OWSI Timing Diagram

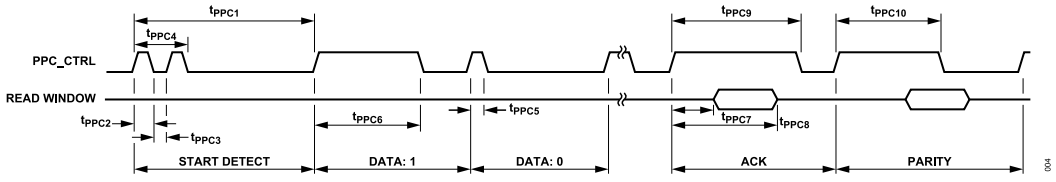

Figure 3. OWSI Timing Diagram for a Successful Transmission

Refer to the One-Wire Serial Interface section for more information.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 17. Absolute Maximum Ratings

Parameter	Rating
AVDD to AGND	−0.3 V to +36 V
AVSS to AGND	−20 V to + 0.3 V
AVDD to AVSS	56 V
DVCC to AGND	−0.3 V to +6 V
AVCC to AGND	−0.3 V to +6 V
DO_VDD to AGND	−0.3 V to +40 V
REFIN and LVIN to AGND	−0.3 V to AVCC + 0.3 V
SENSEH, SENSEHF, SENSEL, SENSELF, SENSE_EXT1, and SENSE_EXT2 to AGND	−50 V to +50 V
VIOUT to AGND	−50 V to +50 V
CCOMP to AGND	−0.3 V to AVCC + 0.3 V
DO_SRC_SNS to DO_VDD	−6 V to +0.3 V
DO_SRC_INT to DGND	−50 V to DO_VDD
DO_SNK_SNS to DGND	−0.3 V to AVCC +0.3V
DO_SNK_INT to DGND	−0.3 V to 50 V
Digital Inputs to DGND ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, SCLK, and SDI)	−0.3 V to DVCC + 0.3 V
Logic Digital Outputs to DGND (GPIO_x[1], SDO, $\overline{\text{ALERT}}$, $\overline{\text{ADC\_RDY}}$, and PPC_CTRL)	−0.3 V to DVCC + 0.3 V
AGND_SENSE to AGND	−0.3 V to +0.3 V
DGND to AGND	−0.3 V to +0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)[2]	125°C
Reflow Profile	JEDEC Industry Standard J-STD-020
Power Dissipation	(T_J maximum − T_A)/θ_{JA}

[1] x = A, B, C, and D.

[2] It is important to manage the power dissipation of the AD74115H to ensure that the maximum T_J is not violated. It is also recommended to enable the thermal shutdown function to avoid damage to the AD74115H.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance. θ_{JC} is the junction to case thermal resistance.

Table 18. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-48-28	28	1.0	°C/W

[1] Based on simulated data using a JEDEC 2S2P thermal test board with a 5 × 5 array of thermal vias in a JEDEC natural convection environment. See JEDEC specification JESD-51 for details.

[2] Measured at the exposed paddle surface with the cold plate in direct contact with the package top surface.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for the AD74115H

Table 19. AD74115H, 48-Lead LFCSP

ESD Model	Withstand Threshold	Class
HBM	3 kV	2

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

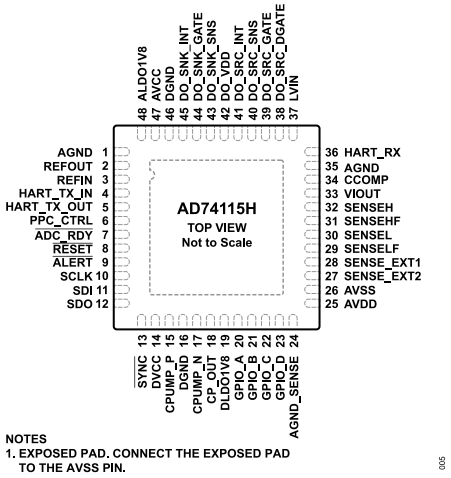

Figure 4. Pin Configuration

Table 20. Pin Function Description

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.
2	REFOUT[1]	Internal 2.5 V Reference Output. The REFOUT pin must be connected to the REFIN pin to use the internal reference.
3	REFIN	2.5 V Reference Input.
4	HART_TX_IN	AC-Coupled HART Transmit Signal.
5	HART_TX_OUT	HART Transmit Signal. Couple this signal to the HART_TX_IN pin using the specified HART coupling capacitor listed in Table 36.
6	PPC_CTRL	Single-Wire Interface Pin to Communicate with the ADP1034. The supply voltage rails from the ADP1034 are configured by SPI writes to the AD74115H and passed to the ADP1034 through this interface.
7	$\overline{\text{ACD\_RDY}}$	Active Low, Open-Drain Output. This pin asserts when a new sequence of ADC conversion results is ready to be read. Connect this pin to a pull-up resistor to the DVDD pin.
8	$\overline{\text{RESET}}$	Hardware Reset Pin. Active low input. This pin resets the AD74115H to the power-on state.
9	$\overline{\text{ALERT}}$	Active Low, Open-Drain Output. This pin asserts low when an alert condition occurs. Read the ALERT_STATUS register when this pin is asserted. Connect this pin to the DVDD pin via a pull-up resistor.
10	SCLK	Serial Interface Clock.
11	SDI	Serial Interface Data In.
12	SDO	Serial Interface Data Out.
13	$\overline{\text{SYNC}}$	Serial Interface Frame Synchronization Pin. Active low input.
14	DVCC[1]	Digital Supply. Decouple this pin with the recommended capacitor listed in Table 36.
15	CPUMP_P	Charge Pump Fly Capacitor Terminal. If using the internal charge pump for unipolar operation, connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin. Pins can be left disconnected if in bipolar mode.
16	DGND	Digital Ground.
17	CPUMP_N	Charge Pump Fly Capacitor Terminal. If using the internal charge pump for unipolar operation, connect the recommended fly capacitor between the CPUMP_P pin and the CPUMP_N pin. Leave these pins disconnected when in bipolar mode.
18	CP_OUT	Charge Pump Output Voltage (Equal to Negative DVCC). When using the charge pump to generate the negative supply, connect the AVSS pin to the CP_OUT pin.
19	DLDO1V8[1]	1.8 V Digital Low Dropout (LDO) Regulator Output. Decouple this pin with the recommended capacitor shown in Table 36. Do not use this pin externally.
20	GPIO_A	General-Purpose Input and Output Pin A. This pin can monitor the digital input comparator result.
21	GPIO_B	General-Purpose Input and Output Pin B. This pin can control the external digital output circuit.
22	GPIO_C	General-Purpose Input and Output Pin C. This pin can control the internal digital output circuit.
23	GPIO_D	General-Purpose Input and Output Pin D.
24	AGND_SENSE	Analog Ground Sense. Tie this pin to the I/ON screw terminal.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 20. Pin Function Description

Pin No.	Mnemonic	Description
25	AVDD[1]	Positive Analog Supply
26	AVSS[1]	Negative Analog Supply.
27	SENSE_EXT2	High Voltage Sense Pin.
28	SENSE_EXT1	High Voltage Sense Pin
29	SENSELF	Filtered Low-Side Sense Pin. SENSELF can be switched to an ADC input. This pin is routed to the I/OP screw terminal side of R_{SENSE} through the off-chip filter.
30	SENSEL	Low-Side Sense Pin. SENSEL closes the loop within the voltage and current output modes. This pin is routed to the I/OP screw terminal side of R_{SENSE}.
31	SENSEHF	Filtered High-Side Sense Pin. SENSEHF can be switched to an ADC input. This pin is routed to the AD74115H side of R_{SENSE} through the off-chip filter.
32	SENSEH	High-Side Sense Pin. SENSEH closes the loop within current output mode. This pin is routed to the AD74115H side of R_{SENSE}.
33	VIOUT	Voltage or Current Force Pin. VIOUT provides a voltage or a current to the I/OP screw terminal.
34	CCOMP	Compensation Capacitor Pin. CCOMP allows the AD74115H to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP pin and the I/O screw terminal.
35	AGND	Analog Ground.
36	HART_RX	HART Receive Pin. Coupled this pin to the I/OP screw terminal with the HART_RX band-pass filter.
37	LVIN	Low Voltage Input Pin. The voltage on LVIN can be measured by selecting the LVIN option in the diagnostics block. The measurement voltage range is 0 V to 2.5 V. For best performance, use an antialiasing filter on this pin.
38	DO_SRC_DGATE	Smart Diode Gate Drive Pin.
39	DO_SRC_GATE	Sourcing Digital Output Gate Drive.
40	DO_SRC_SNS	Sourcing Digital Output Sense Pin. If not using the digital output function with an external FET, tie DO_SRC_SNS to DO_VDD.
41	DO_SRC_INT	Internal Sourcing Digital Output.
42	DO_VDD[1]	Positive Supply for Digital Output Circuit.
43	DO_SNK_SNS	Sinking Digital Output Sense.
44	DO_SNK_GATE	Sinking Digital Output Gate Drive.
45	DO_SNK_INT	Internal Sinking Digital Output.
46	DGND	Digital Ground.
47	AVCC[1]	5 V Analog Supply.
48	ALDO1V8[1]	1.8 V Analog LDO Output. Do not use ALDO1V8 externally.
	Exposed Pad	Exposed Pad. Connect the exposed pad to the AVSS pin.

[1] Connect the recommended decoupling capacitors shown in Table 36.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

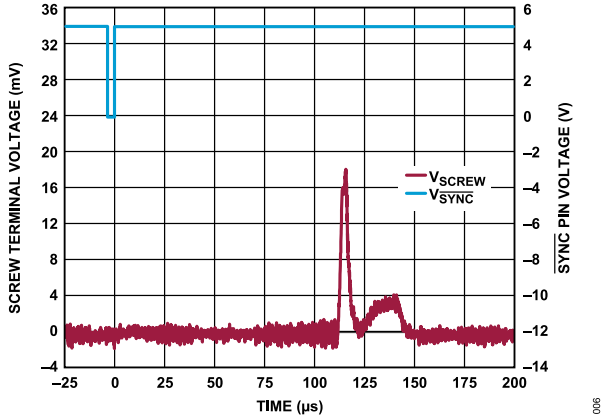

Figure 5. Screw Terminal Voltage (V_{SCREW}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Voltage Output Enabled

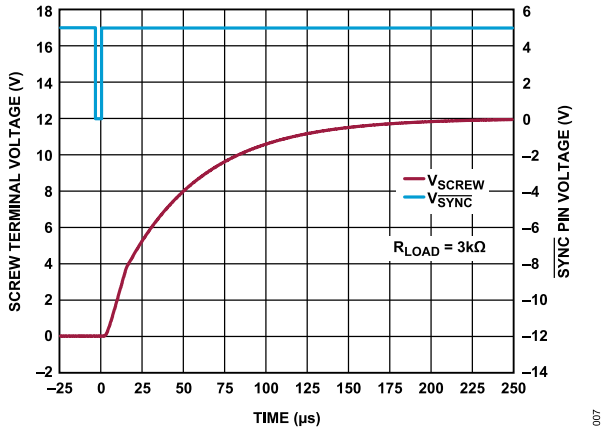

Figure 6. Full-Scale Positive Step with C_{COMP} Connected

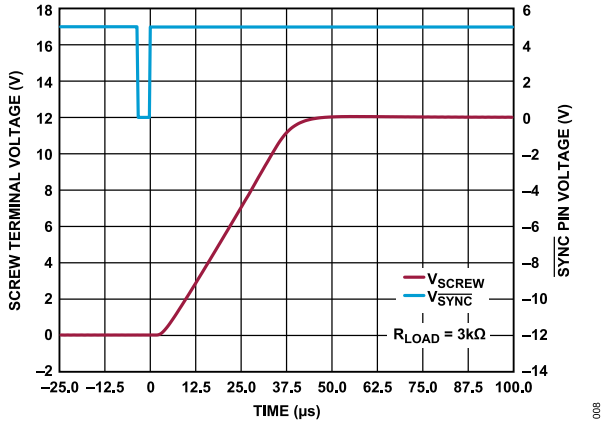

Figure 7. Full-Scale Positive Step Without C_{COMP}

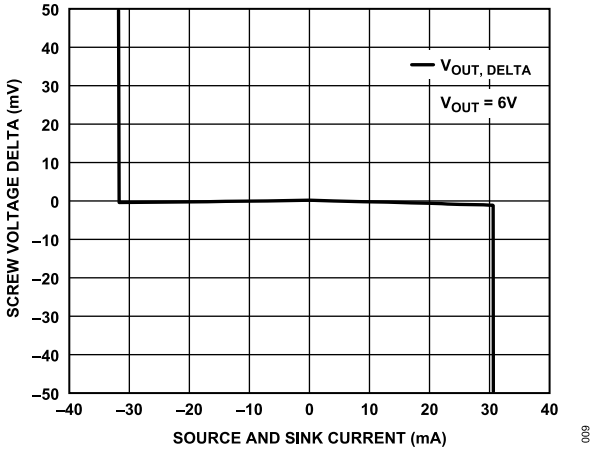

Figure 8. Output Voltage Change ($V_{OUT, DELTA}$) vs. Source and Sink Current

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT OUTPUT (I_{OUT})

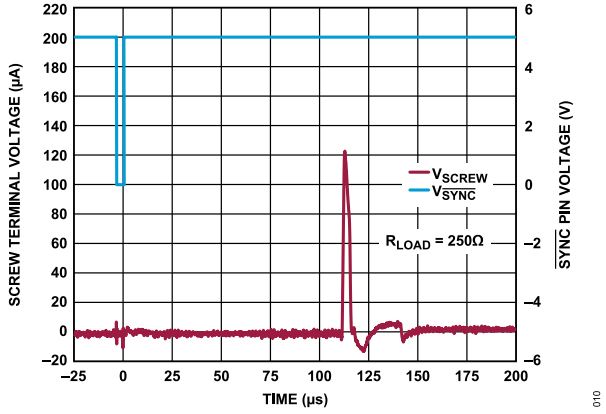

Figure 9. Screw Terminal Voltage (V_{SCREW}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Current Output Enable

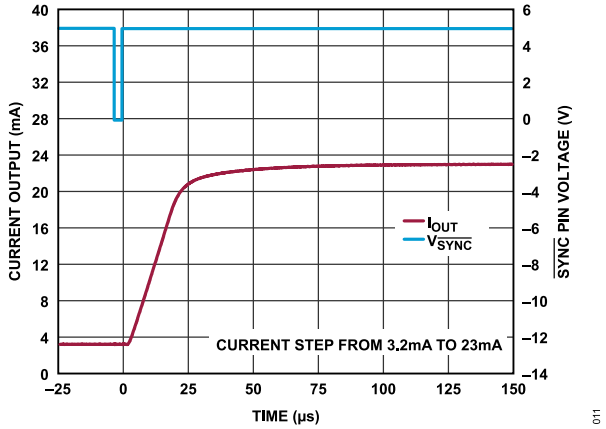

Figure 10. Current Output (I_{OUT}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time

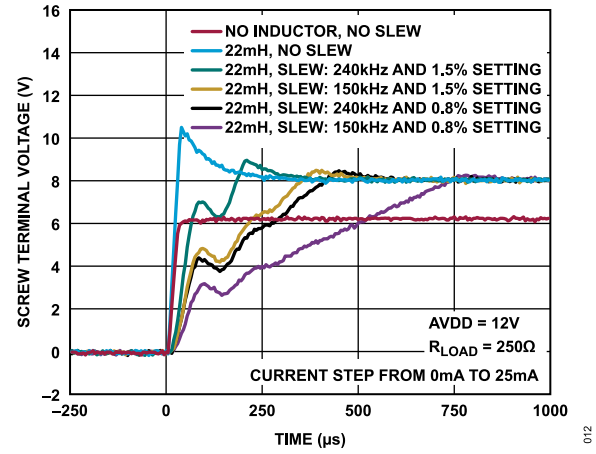

Figure 11. I_{OUT} Settling Time with Inductive Load and with and Without Slew Rate Enabled

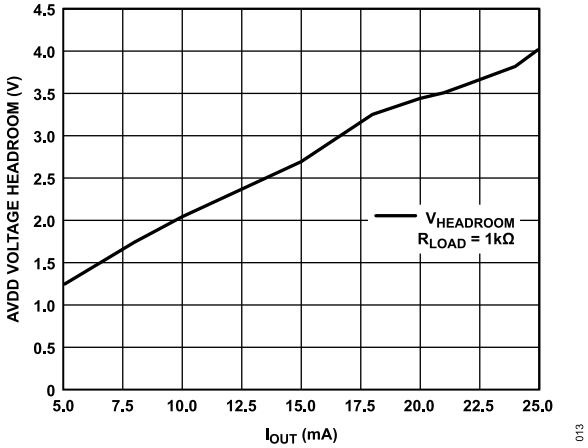

Figure 12. AVDD Voltage Headroom vs. I_{OUT}

TYPICAL PERFORMANCE CHARACTERISTICS

RESISTANCE MEASUREMENT

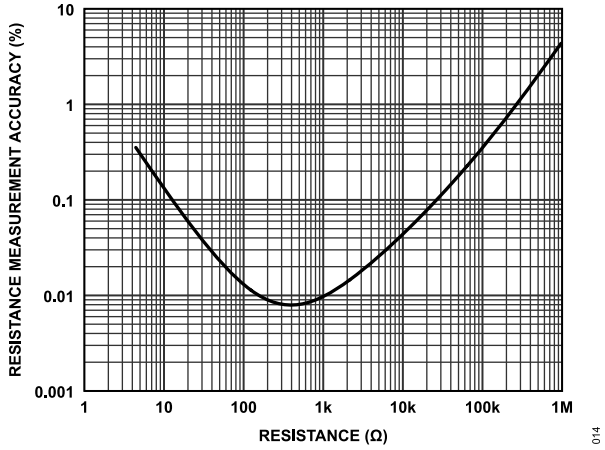

Figure 13. 2-Wire Resistance Measurement Accuracy

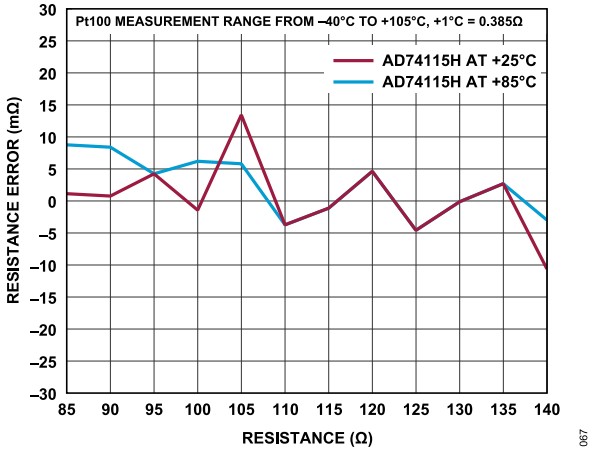

Figure 16. 4-Wire RTD Measurement Error

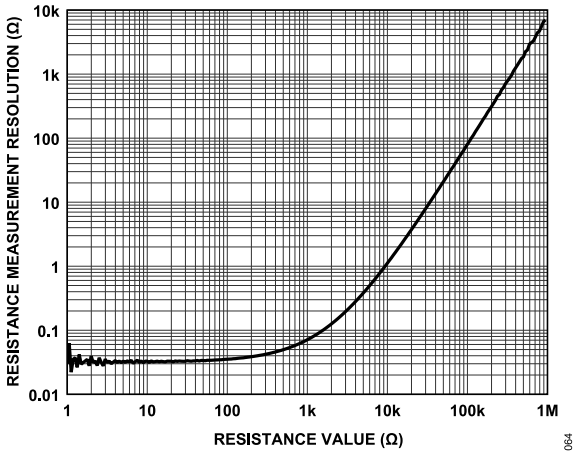

Figure 14. Resistance Measurement Resolution vs. Resistance Value

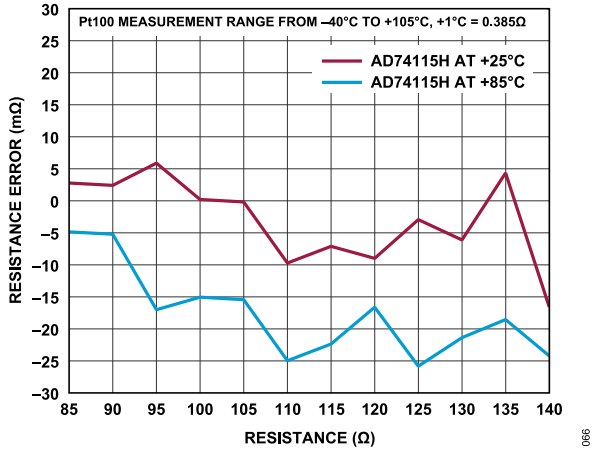

Figure 15. 3-Wire RTD Measurement Error

TYPICAL PERFORMANCE CHARACTERISTICS

REFERENCE

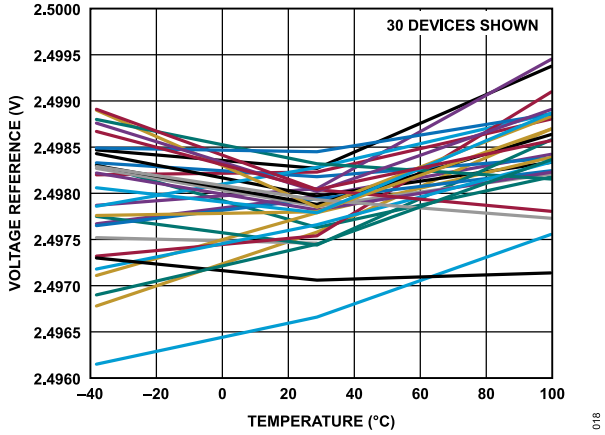

Figure 17. Voltage Reference vs. Temperature

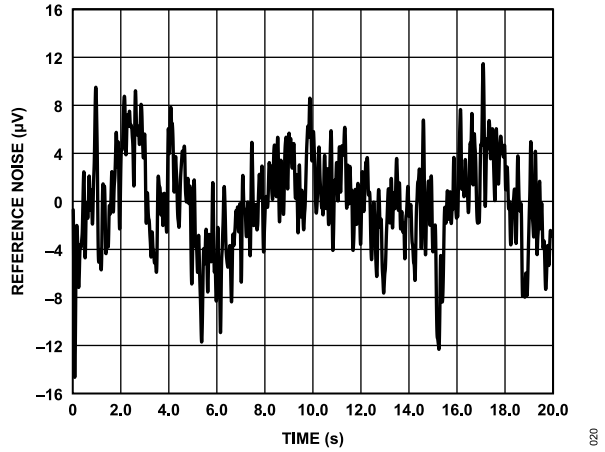

Figure 18. Peak-to-Peak Noise (0.1 Hz to 10 Hz Bandwidth)

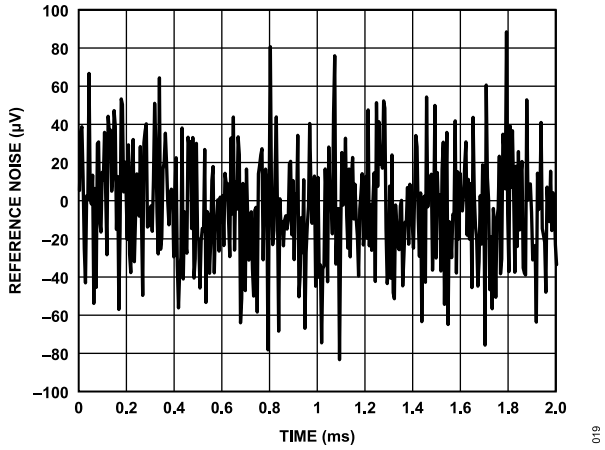

Figure 19. Peak-to-Peak Noise (100 kHz Bandwidth)

TYPICAL PERFORMANCE CHARACTERISTICS

ADC

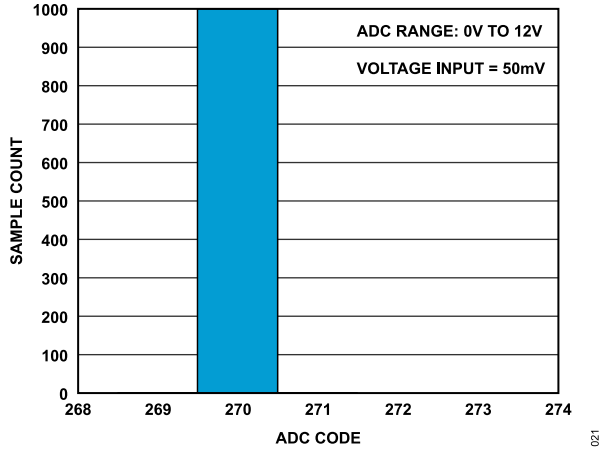

Figure 20. ADC Noise Histogram with Output Data Rate (ODR) = 10 SPS

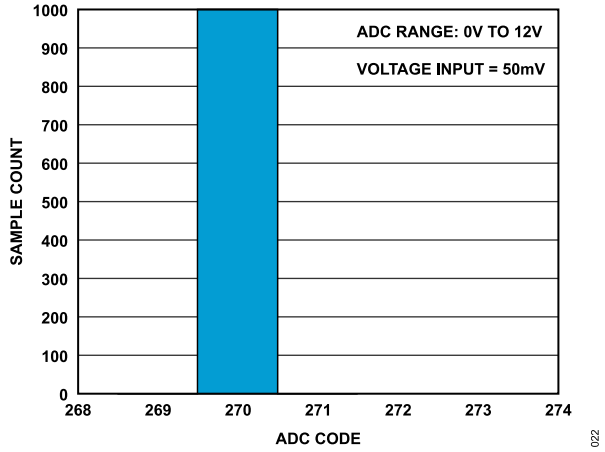

Figure 21. ADC Noise Histogram with ODR = 20 SPS

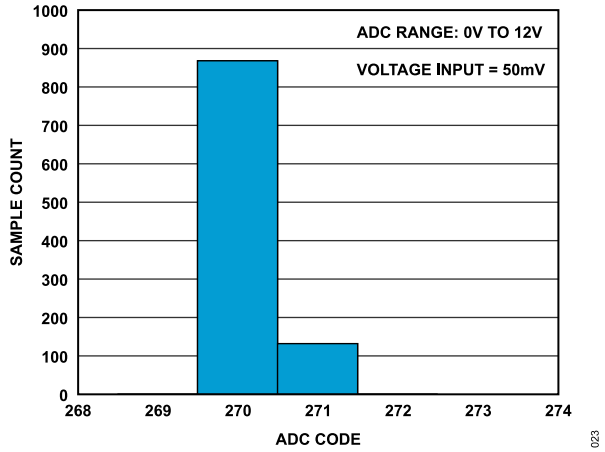

Figure 22. ADC Noise Histogram with ODR = 1.2 kSPS

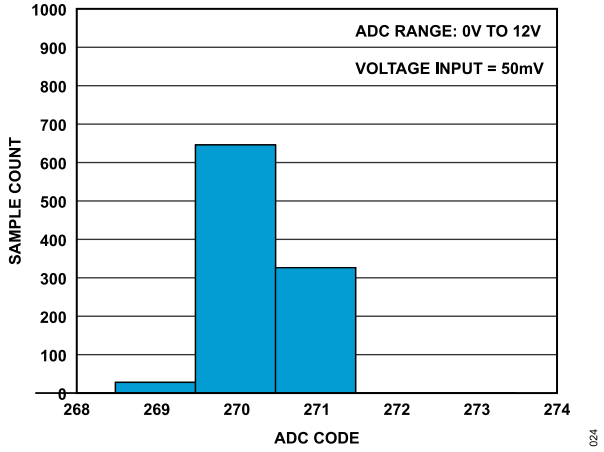

Figure 23. ADC Noise Histogram with ODR = 4.8 kSPS

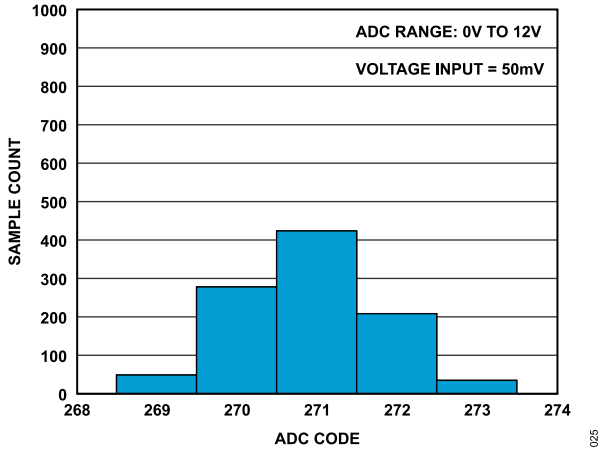

Figure 24. ADC Noise Histogram with ODR = 9.6 kSPS

TYPICAL PERFORMANCE CHARACTERISTICS

DIGITAL OUTPUT

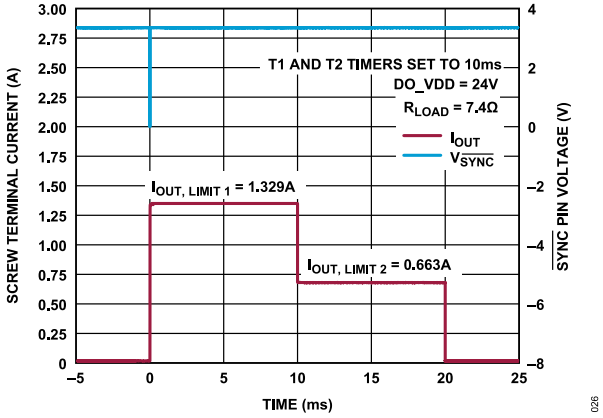

Figure 25. Digital Output Programmable Short-Circuit Activation

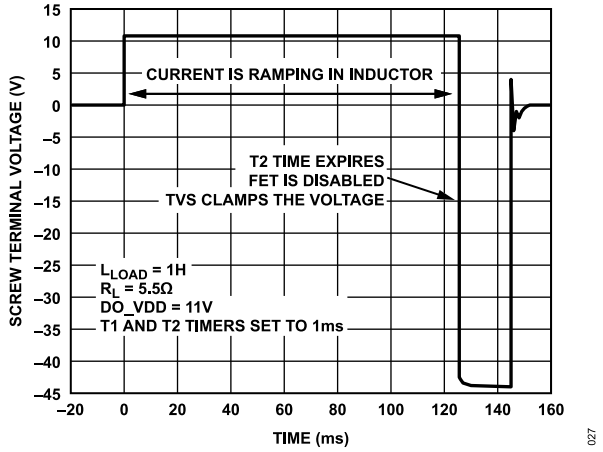

Figure 26. Demagnetization Strategy for Inductive Loads (L_{LOAD})

TYPICAL PERFORMANCE CHARACTERISTICS

HART—I_{OUT} MODE

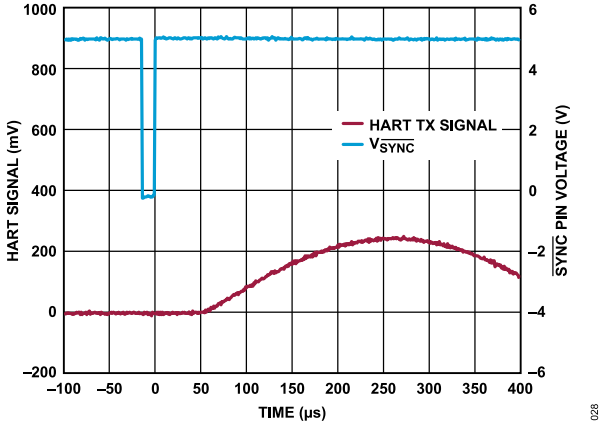

Figure 27. Carrier Start Time

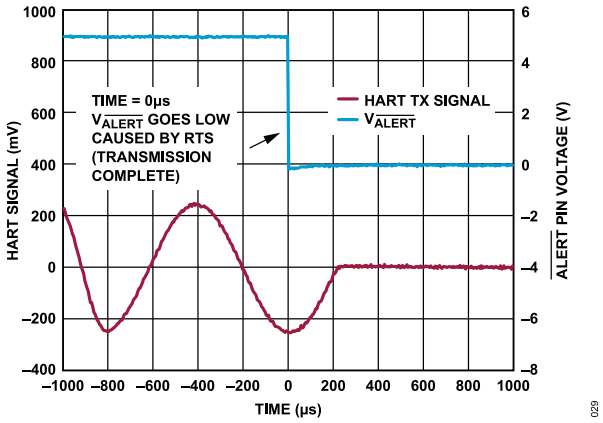

Figure 28. Carrier Stop Time

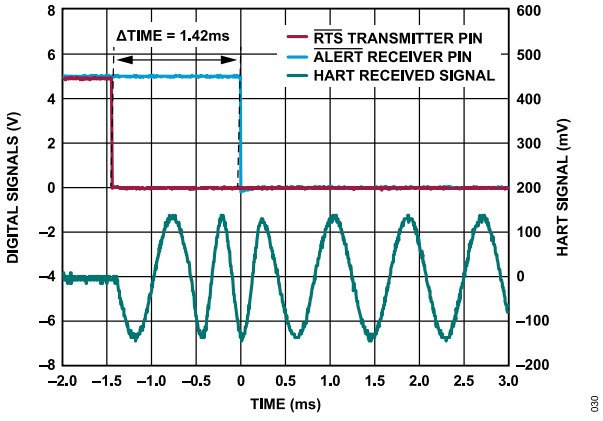

Figure 29. Carrier Detect On Time (Assertion of ALERT Pin)

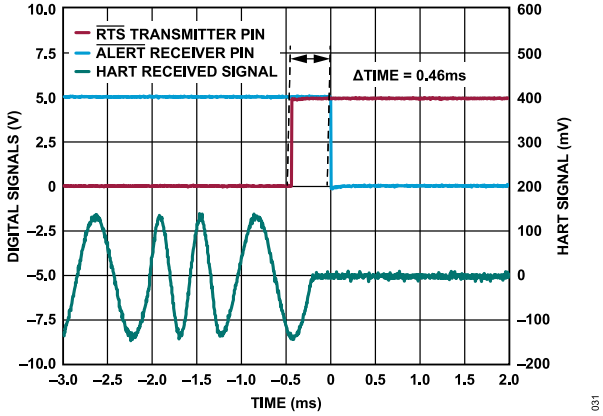

Figure 30. Carrier Detect Off Time (Till ALERT Pin Change to High)

TYPICAL PERFORMANCE CHARACTERISTICS

OTHERS

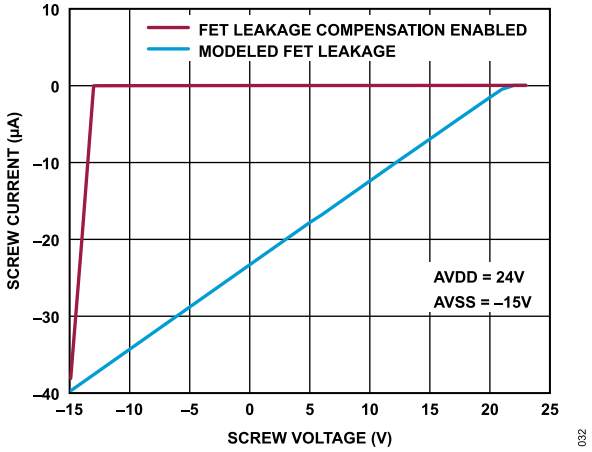

Figure 31. Function of Current Leakage Compensation

TERMINOLOGY

ADC Offset Error

For unipolar input ranges, ADC offset error is the deviation in LSBs from the zero-scale code (0x0000) when inputs are shorted, 0 V.

For bipolar input ranges, ADC offset error is the deviation in LSBs from the midscale code (0x8000) when inputs are shorted, 0 V.

ADC Gain Error

Gain error applies to both unipolar and bipolar ranges. Gain error is a measure of the span error of the ADC.

For input ranges, gain error is defined as the full-scale error minus the zero-scale error. The error is expressed in ppm FSR.

DAC Offset Error

Offset error is the deviation of the analog output from the ideal zero-scale output when the DAC output register is loaded with 0x0. The offset error is expressed in mV.

DAC Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal midscale output of 0 V when the DAC output register is loaded with 0x2000. This error applies only to bipolar output ranges.

DAC Gain Error

Gain error is a measure of the span error of the DAC. This error is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR.

Total Unadjusted Error (TUE)

TUE is the maximum deviation of the output from the ideal. TUE includes INL, offset, gain error, and internal reference error.

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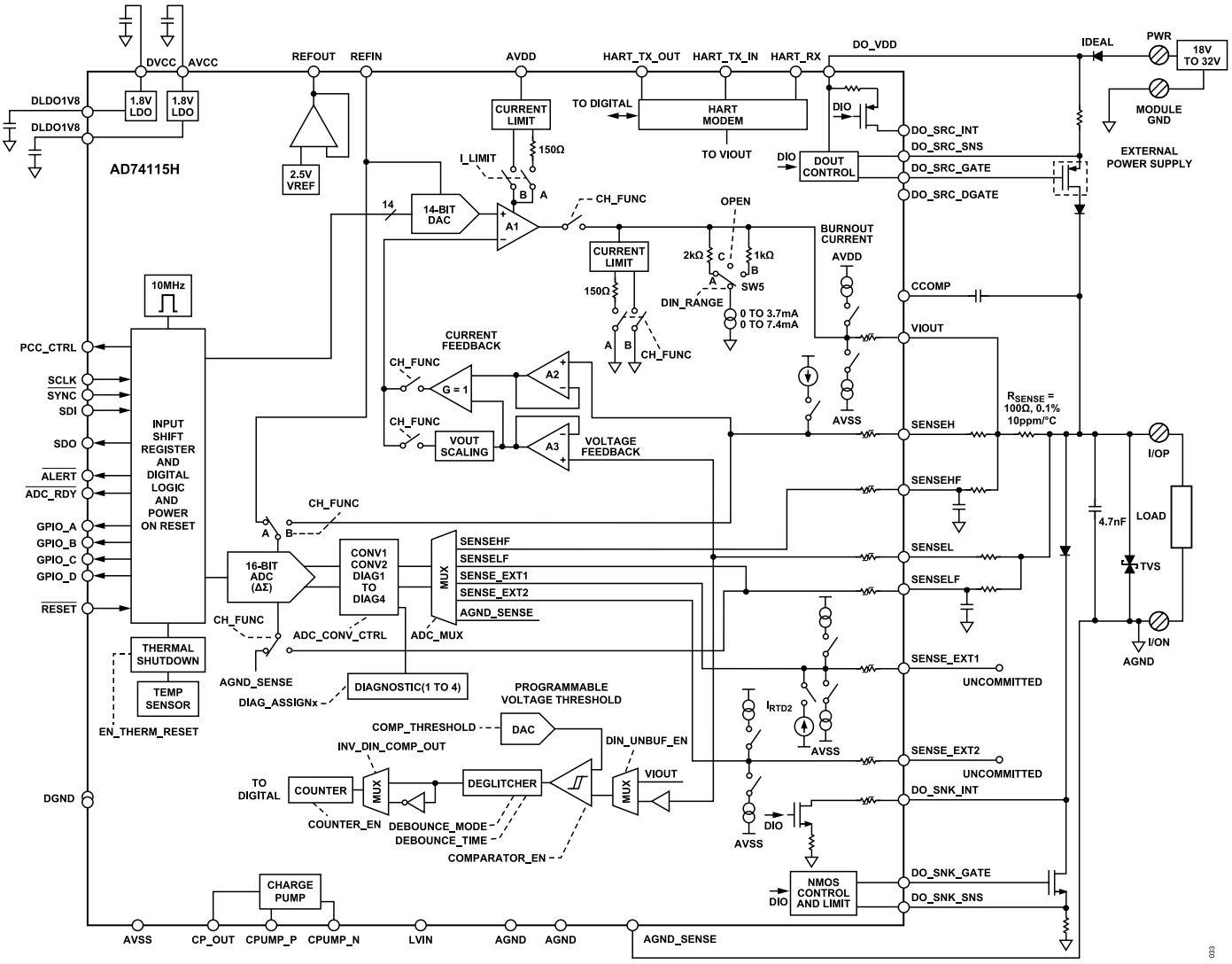

Figure 32. Detailed Functional Block Diagram

The AD74115H is a single-channel, software configurable input and output that is designed to meet the requirements of isolated process control and factory automation applications. The device provides a fully integrated single chip solution for input and output operation. The AD74115H features a 16-bit, Σ-Δ ADC and a 14-bit DAC, and the device is packaged in a 7 mm × 7 mm, 48-lead LFCSP. The AD74115H also includes an integrated HART modem.

The channel is configured by writing to the configuration registers. Users can refine the default configurations of each operation mode via the AD74115H register map. See Figure 32 for a detailed functional block diagram of the AD74115H.

ROBUST ARCHITECTURE

The AD74115H system is robust in noisy environments and can withstand overvoltage scenarios such as miswire and surge events.

On-chip line protectors ensure that the I/OP screw terminal does not provide power to the IC when brought to a higher potential than the AVDD pin.

The recommended external components shown in Figure 32 and Table 36, including the TVS, are selected to withstand surges on the input and output terminals.

With the recommended components, the I/OP and I/ON screw terminals tolerate overvoltages up to dc ± 36 V (limited by the external TVS).

A cyclic redundancy check (CRC) function is built into the SPI to ensure error free communications in noisy environments.

POWER SUPPLIES AND REFERENCE

Four external voltage supply rails are required to power up the AD74115H: V_{AVDD}, which is the positive analog supply, V_{AVSS}, which is the negative analog supply, V_{AVCC}, which is the low voltage

THEORY OF OPERATION

analog supply, and V_{DVCC}, which is the digital supply. See Table 14 for the voltage range of the three external supplies and the associated conditions.

Powering on the AD74115H

When powering up the AD74115H, apply ground connections first. After power-up, the user must wait for the device power-up time (see Table 14) before any transaction to the device can take place.

Upon initial power-up or a device reset of the AD74115H, the output channel is disabled and placed in a high impedance state by default.

Charge Pump

The AD74115H has an internal charge pump that can be enabled to provide AVSS, the negative voltage supply. When only unipolar capability is required, the charge pump can eliminate the requirement for the external AVSS supply voltage. Enable the charge pump using the CPUMP_EN bit. For correct operation, the charge pump requires an external capacitor (CPUMP fly capacitor) between the CPUMP_N pin and CPUMP_P pin. Externally connect the CP_OUT pin to AVSS.

If using the charge pump, take care not to apply an external supply to the AVSS pin.

When the charge pump is enabled, the ±12V bipolar output range is disabled.

Reference

The AD74115H can operate with either an external or an internal reference. The reference input requires 2.5 V for the AD74115H to function correctly. The reference voltage is internally buffered before being applied to the DAC and the ADC. If using the internal reference, the REFIN pin must be tied to the REFOUT pin.

DEVICE FUNCTIONS

The following sections describe the various programmable device functions of the AD74115H with block diagrams and guidelines on how to interpret the ADC results if converting with the default settings. These functions are programmed within the CH_FUNC_SETUP register.

Each device function is configured with default measurement settings. However, users can adjust these settings as required within the register map.

High Impedance

High impedance is the default function upon power-up or after a device reset.

If a channel is held in high impedance for an extended time, such as when the analog input and output functions are not in use, it is recommended to enable a sinking burnout current of 1 µA. Enable the burnout current by programming the following bits in the I_BURNOUT_CONFIG register:

- BRN_VIOUT_EN to 1
- BRN_VIOUT_POL to 0
- BRN_VIOUT_CURR to 100 binary

Interpreting ADC Data

In high impedance mode, the ADC, by default, measures the voltage across the screw terminals (I/OP to I/ON) in a 0 V to 12 V range. Use the following equation to calculate the ADC measurement result:

$$V_{ADC} = (ADC\_CODE/65{,}536) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULT1 register.
Voltage Range is the measurement range of the ADC and is 12 V.

Voltage Output

The voltage output amplifier can generate unipolar or bipolar voltages in the 0 V to +12 V and ±12 V, ranges respectively. Each range has 14 bits of resolution. The voltage on the low-side of the R_{SENSE} is sensed on the SENSEL pin via a 2 kΩ resistor, which closes the feedback loop and maintains stability.

In voltage output mode, the output range is set to 0 V to 12 V by default. To select bipolar mode, use the following sequence:

- Write 0x2000 to the DAC_CODE register to ensure 0 V output.
- Set the VOUT_RANGE bit in the OUTPUT_CONFIG register to 1 for bipolar outputs.
- Select the voltage output use case in the CH_FUNC bits, CH_FUNC_SETUP register.

Figure 33 shows the current, voltage, and measurement paths of the voltage output mode.

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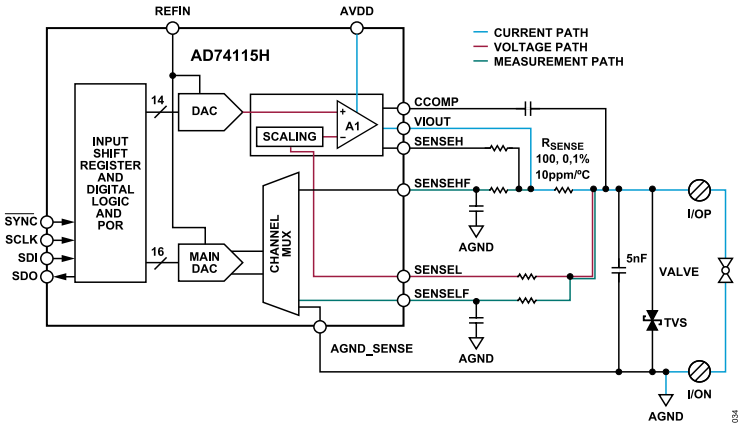

Figure 33. Voltage Output Mode Configuration

Short-Circuit Detection

There are two available short-circuit limits that can be selected by setting the I_LIMIT bit in the OUTPUT_CONFIG registers. See Table 1 for the specified short-circuit current values. If the selected short-circuit limit is reached on a channel, a voltage output short-circuit error is flagged for that channel, and the $\overline{\text{ALERT}}$ pin asserts.

Interpreting ADC Data

In voltage output mode, the ADC, by default, measures the current through the R_{SENSE} in a −25 mA to +25 mA range. Use the ADC measurement result to calculate the current through the R_{SENSE} with the following equation:

$$I_{R_{SENSE}} = \frac{\left(V_{MIN} + \left(\left(\frac{ADC\_CODE}{65,536}\right) \times Voltage\ Range\right)\right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps. A negative current indicates that the current is sourced from the AD74115H. A positive current indicates that the AD74115H is sinking the current.

V_{MIN} is the minimum voltage of the selected ADC range, which is −2.5 V by default.

ADC_CODE is the value of the ADC_RESULT1 register.

Voltage Range is the full span of the ADC range, which is 5 V.

R_{SENSE} is the R_{SENSE} resistor, which is 100 Ω.

THEORY OF OPERATION

Current Output

In current output mode, the DAC provides a current output on the VIOUT pin that is regulated by sensing the differential voltage across R_{SENSE} by using the SENSEL and SENSEH pins.

Figure 34 shows the current, voltage, and measurement paths of the current output mode.

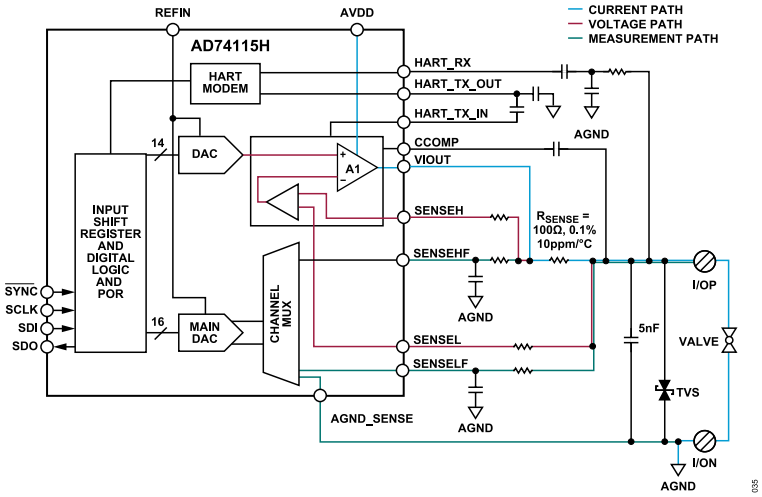

Figure 34. Current Output Mode Configuration

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Open-Circuit Detection

In current output mode, if the headroom voltage falls below the compliance voltage (specified in Table 2), due to an open-loop circuit on the channel, a current output open-circuit error is flagged for that channel, and the $\overline{\text{ALERT}}$ pin asserts. If V_{AVDD} is insufficient to drive the programmed current output, the open-circuit error is flagged.

Interpreting ADC Data

In current output mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/OP to I/ON) in a 0 V to 12 V range. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = (ADC\_CODE/65{,}536) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULT1 register.
Voltage Range is the measurement range of the ADC and is 12 V.

Current Output Mode with HART Compatibility

Current output mode with HART is compatible with HART transmit functionality when users enable the HART compliant slew option via the SLEW_EN bit in the OUTPUT_CONFIG register.

Voltage Input

In voltage input mode, the voltage across the screw terminals (I/OP to I/ON) is measured by the ADC via the SENSELF and the AGND_SENSE pins. It is essential to connect the AGND_SENSE pin as close as possible to the I/ON screw terminal to ensure an accurate voltage measurement. Figure 35 shows the current and measurement paths of the voltage input mode.

In voltage input mode, the voltage can be measured in a ±12 V range. However, there is also an option to measure the I/OP screw terminal voltage using the diagnostics function. The diagnostics function allows the voltage to be measured across the full supply rails.

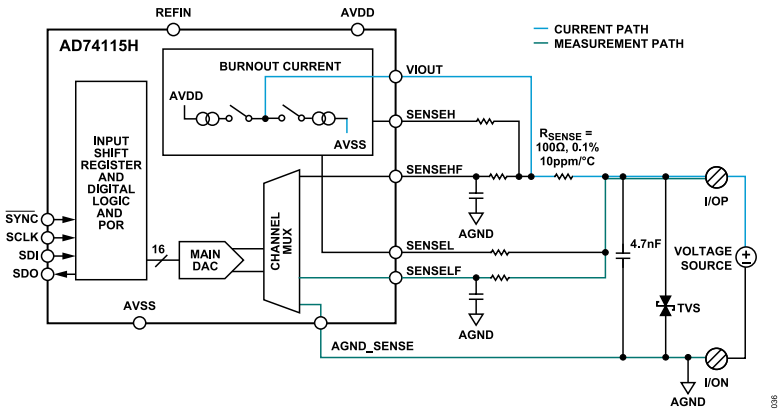

Figure 35. Voltage Input Mode Configuration

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Open-Circuit Detection

Programmable burnout currents can be used to detect an open circuit in voltage input mode (see the Burnout Currents section). Configure the VIOUT pin with the required burnout current by writing to the I_BURNOUT_CONFIG register. If the I/OP screw terminal is floating, the SENSELF pin is pulled to the supply rail, and the ADC result generates a conversion error.

Interpreting ADC Data

In voltage input mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/OP to I/ON) in a 0 V to 12 V range. A different range can be selected using the CONV1_RANGE bits in the ADC_CONFIG register. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = V_{MIN} + (ADC\_CODE/65{,}536) \times Voltage\ Range$$

where:
V_{MIN} is the minimum input voltage of the selected ADC range and is 0 V by default.
V_{ADC} is the measured voltage in volts.
ADC_CODE is value of the ADC_RESULT1 register.
Voltage Range is the measurement range of the ADC and is 12 V.

Thermocouple Measurement

Voltage input mode can measure the voltage of a thermocouple when the thermocouple is connected across the screw terminals (I/OP to I/ON). To accurately measure the thermocouple voltage, select the ±104 mV input range via the ADC_CONFIG register in voltage input mode.

Current Input, Externally Powered

In current input, externally powered mode, the AD74115H provides a current-limited path to ground via the VIOUT pin for an external current source. The 16-bit, Σ-Δ ADC is configured to measure the current through R_{SENSE}. The current is measured by digitizing the voltage across R_{SENSE} via the SENSEHF and the SENSELF pins. Figure 36 shows the current and measurement paths of the current input, externally powered mode.

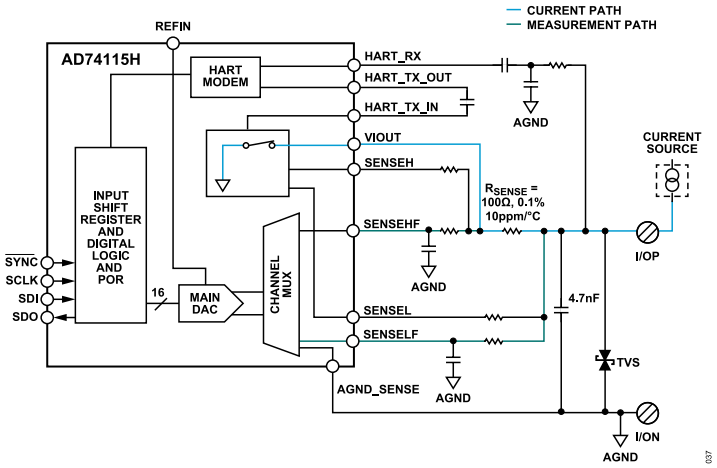

Figure 36. Current Input, Externally Powered Mode Configuration

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Short-Circuit Protection and Detection

The maximum short-circuit limit is 35 mA in current input, externally powered mode to protect the external circuitry and to limit the power dissipated on the AD74115H device.

In current input, externally powered mode, the digital input comparator is enabled by default to detect a short-circuit condition. The digital input comparator is enabled with a threshold voltage of AVDD/2. In normal operation, the voltage on I/OP is typically within 5 V of ground. If the current source attempts to sink more than 35 mA into the AD74115H, the voltage on the SENSEL pin instantly ramps. When the voltage on the I/OP screw terminal is more than the programmed threshold voltage, the comparator trips, setting the ANALOG_IO_SC bit in the ALERT_STATUS register.

Interpreting ADC Data

In current input mode, the ADC, by default, measures the current flowing from the I/OP screw terminal into the AD74115H through the R_{SENSE} in a 25 mA range. Use the ADC measurement current to calculate the current through the R_{SENSE} with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\left(\frac{ADC\_CODE}{65,536}\right) \times Voltage\ Range\right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps.
ADC_CODE is the value of the ADC_RESULT1 register.
Voltage Range is the full span of the ADC range and is 2.5 V.
R_{SENSE} is the sense resistor, which is set to 100 Ω.

Current Input, Externally Powered with HART Mode

This mode is a HART-compatible version of the current input, externally powered mode. The input impedance is set to a minimum of 230 Ω to be compliant with the HART receive impedance.

Current Input, Loop Powered

In current input loop powered mode, the AD74115H provides a current-limited voltage to the I/OP screw terminal. The current is measured by digitizing the voltage across R_{SENSE} via the SENSEHF and the SENSELF pins. Figure 37 shows the current, voltage, and measurement paths of the current input, loop powered mode.

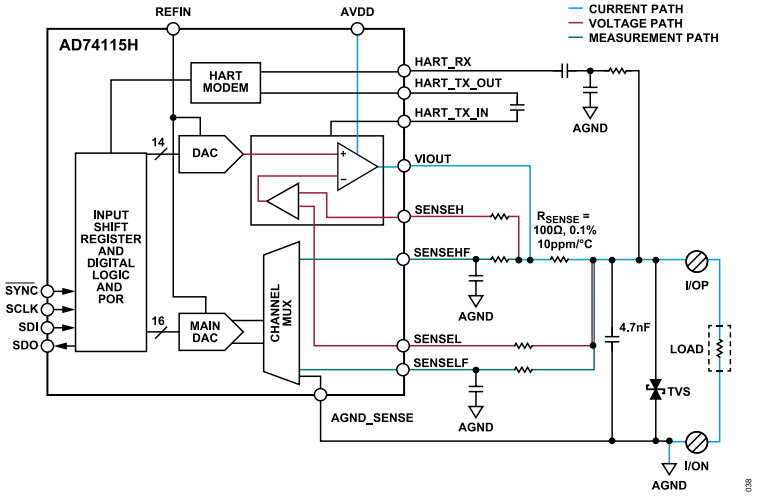

Figure 37. Current Input, Loop Powered Mode Configuration

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Short-Circuit Protection and Detection

The current from the AD74115H is limited by the programmable DAC code.

In current input loop powered mode, the digital input comparator is enabled by default to detect a short circuit.

The digital input comparator is enabled with a threshold voltage of AVDD/2 and with the output inverted. During normal operation, the voltage on I/OP is typically within 5 V of the V_{AVDD}. If the load is short circuited to ground, the voltage on the I/OP is pulled to ground. When the voltage on the I/OP screw terminal falls to less than the programmed threshold level, the comparator trips low, setting the ANALOG_IO_SC bit in the ALERT_STATUS register.

Interpreting ADC Data

In current input loop, powered mode, the ADC, by default, measures the current flowing from the AD74115H into the I/OP screw terminal through the R_{SENSE} in a 25 mA range. Use the ADC measurement result to calculate the current with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\left(\frac{ADC\_CODE}{65,536}\right) \times Voltage\ Range\right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps.

ADC_CODE is the value of the ADC_RESULT1 register.

Voltage Range is the full ADC span of the ADC range and is 2.5 V.

R_{SENSE} is the sense resistor, which has a value of 100 Ω.

Current Input, Loop Powered with HART Compatibility Mode

This mode is a HART-compatible version of the current input, loop powered mode. However, the current source is not programmable; therefore, configuring of the DACs is not needed. A current-limit source of typically 30 mA is enabled when the current input, loop powered with HART mode is selected.

The mode can provide resistive termination in current input, loop powered mode. Input impedance is set to a minimum of 230 Ω to be compliant with the HART receive impedance.

Resistance Measurement (2-Wire RTD)

The resistance measurement configuration biases an external 2-wire RTD with a voltage derived from a 2.5 V bias. The resultant excitation current flows through the 2 kΩ and 100 Ω resistors (shown as R_{PULLUP} in Figure 38). This configuration ensures an accurate ratiometric measurement. The 16-bit, Σ-Δ ADC automatically digitizes the voltage across the RTD. The low excitation current ensures that the power dissipated by the RTD is minimized, reducing self heating. See Figure 38 for an example of the RTD bias circuit.

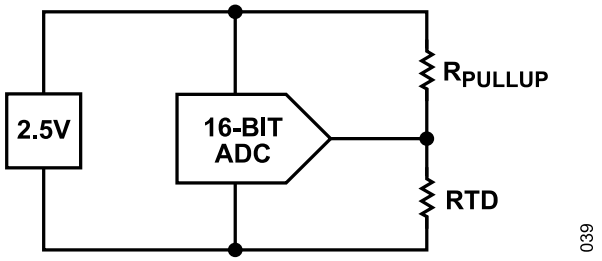

Figure 38. RTD Bias Circuit

It is essential that the AGND_SENSE pin connects to the low-side of the measured RTD. Figure 39 shows the current, voltage, and measurement paths of the resistance measurement configuration.

The resistance measurement mode can be used for 2-wire RTD measurements, but also as a diagnostic of the attached load. Load impedance can be used for load detection techniques or to help to determine the health of the load over time.

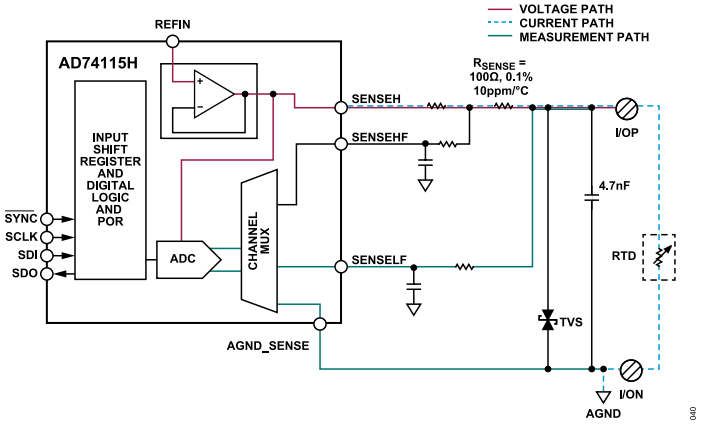

Figure 39. Resistance Measurement Configuration

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Interpreting ADC Data

In resistance measurement mode, the 16-bit, Σ-Δ ADC automatically digitizes the voltage across the RTD in a 2.5 V range.

When a conversion is carried out, the ADC code reflects the ratio between the RTD and the $R_{PULL-UP}$. Use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{(ADC\_CODE \times R_{PULL-UP})}{(65,536 - ADC\_CODE)}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code of the ADC_RESULT1 registers.
$R_{PULL-UP}$ has a value of 2100 Ω.

Do not change the CONV1_MUX bits in the settings of the ADC_CONFIG register if in RTD mode. Changing from the default ADC mux configuration results in a void ADC result.

3-Wire RTD Measurements

3-wire RTD measurements are supported with the AD74115H. Use the CH_FUNC bits in the CH_FUNC_SETUP register to configure the channel in 3-wire or 4-wire RTD mode.

Figure 40 shows a simplified configuration of the 3-wire RTD method. Matched excitation currents, I_1 and I_2 are sourced to two of the RTD leads. The third lead is connected to ground. One of the excitation currents, I_1, generates a voltage across the RTD and lead resistance RL_1. The second excitation current, I_2, generates a drop across RL_2. The resultant voltage across terminals T1 and T2 is equivalent to the voltage drop across the RTD. (It is assumed that the lead resistances are matched, that is, $RL_1 = RL_2 = RL_3$).

The voltage between the T1 and T2 terminals is measured by the ADC using the SENSELF and SENSE_EXT1 pins. The full-scale range of the ADC is determined by the voltage across the reference resistor, R_{REF}, guaranteeing a fully ratiometric measurement.

The excitation currents applied to the RTD terminals can be programed to one of four values between 250 µA to 1 mA in the RTD3W4W_CONFIG register. See Table 7 for the full list of excitation currents. Select the excitation current according to the RTD in use.

Take care that the voltage generated on the SENSEHF pin ($I_1 \times (R_{REF} + R_{RTD})$) is less than V_{AVCC}. The SENSEHF pin voltage provides the positive reference to the ADC and must not exceed the value of V_{AVCC}.

Three measurement ranges are available in 3-wire RTD mode. These ranges are listed in Table 7. The measurement range can be configured in the ADC_CONFIG register using the CONV1_RANGE bits. Select the best range to suit the RTD in use.

When the 3-wire or 4-wire RTD mode is selected, the AD74115H is automatically configured to measure a 3-wire RTD in a Pt100 range. In this case, an excitation current of 1 mA is used, and the ADC measurement range is set to 0 V to 0.625 V.

If a Pt1000 measurement is required, it is recommended to use a 500 µA excitation current with the ADC range set to 0 V to 12 V.

For a lower resistance RTD, for example Cu10, it is recommended to use 1 mA excitation current, and the ADC range set to ±104 mV.

The ADC measurement range can be changed by writing to the CONV1_RANGE bits in the ADC_CONFIG register. The excitation currents can be changed by writing to the RTD_CURRENT bits in the RTD3W4W_CONFIG register.

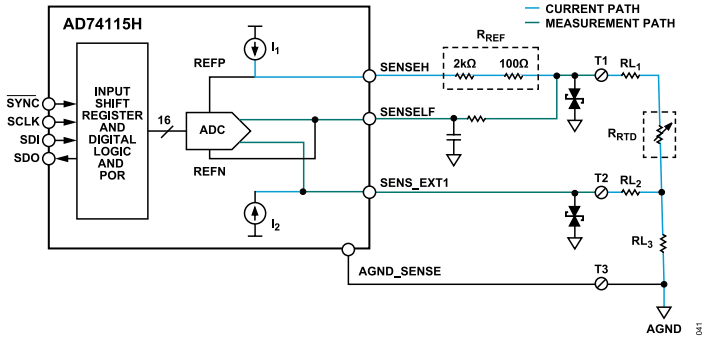

Figure 40. 3-Wire RTD Measurement Configuration

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How to Configure a 3-Wire RTD Measurement for Pt1000 RTD

The following is an example of how to configure a 3-wire RTD measurement for the Pt1000 RTD:

- Select 3-wire or 4-wire resistance measurement in the CH_FUNC_SETUP register.
- Set CONV1_MUX to SENSELF to SENSE_EXT1 and CONV1_RANGE to 0 V to 12 V in the ADC_CONFIG register.
- Set RTD_CURRENT to 500 µA and RTD_MODE_SEL to 3-wire RTD mode in the RTD3W4W_CONFIG register.
- Set CONV1_EN and CONV_SEQ to start continuous conversions in the ADC_CONV_CTRL register.

Open-Circuit Detection

An open-circuit detect feature is available on the leads of the 3-wire RTD. The combination of excitation current and RTD and lead resistances generates voltages on the SENSEH and SENSE_EXT1 pins. If the voltage on either of these pins exceeds the short-circuit detect voltage (shown in Table 7), an open-circuit signal is asserted in the ALERT_STATUS register.

Interpreting ADC Data

In 3-wire RTD mode, configure the 16-bit, Σ-Δ ADC to measure the voltage from SENSELF to SENSE_EXT1. When a conversion is carried out, the ADC code reflects the ratio between R_{RTD} and R_{REF}.

When using unipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \left(\frac{ADC\_CODE+5}{65{,}536 \times ADC\_GAIN} \times R_{REF}\right) + 0.2$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code of the ADC_RESULT1 register.
R_{REF} has a value of 2100 Ω (the combined value of the SENSEH and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the 0 V to 0.625 V range (Pt100), the *ADC_GAIN* is 4.

When using the 0 V to 12 V range (Pt1000), the ADC_GAIN is 1/4.8.

When using bipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \left(\frac{ADC\_CODE - 32{,}763}{32{,}768 \times ADC\_GAIN} \times R_{REF}\right) + 0.2$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code of the ADC_RESULT1 register.
R_{REF} has a value of 2100 Ω (the combined value of the SENSEH and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the ±104 mV range (Cu10), the ADC_GAIN is 24.

4-Wire RTD Measurements

4-wire RTD measurements are supported with the AD74115H. Use the CH_FUNC_SETUP register to configure the channel in 3-wire or 4-wire RTD mode. Configure the RTD_MODE_SEL bit for 4-wire RTD measurements in the RTD3W4W_CONFIG register.

Figure 41 shows a simplified configuration of 4-wire RTD method. An excitation current, I_1 is sourced to a single lead of the RTD via SENSEH. The fourth lead is connected to ground.

There is no current flow in second and third leads of the RTD that are connected to SENSE_EXT2 and SENSE_EXT1, respectively; therefore, these pins are used to sense the voltage directly across the RTD.

The full-scale range of the ADC is determined by the voltage across R_{REF}, guaranteeing a fully ratiometric measurement.

The excitation current applied to the RTD terminal can be programed to one of four values between 250 µA to 1 mA using the RTD_CURRENT bits in the RTD3W4W_CONFIG register. See Table 7 for the full list of excitation currents. Select the excitation current according to the RTD in use. Take care that the voltage generated on the SENSEHF pin ($I_1 \times (R_{REF} + R_{RTD})$) is less than V_{AVCC}. The SENSEHF pin voltage provides the positive reference to the ADC and must not exceed the value of V_{AVCC}.

The measurement range can be configured in the ADC_CONFIG register using the CONV1_RANGE bits. Select the best range to suit the RTD in use.

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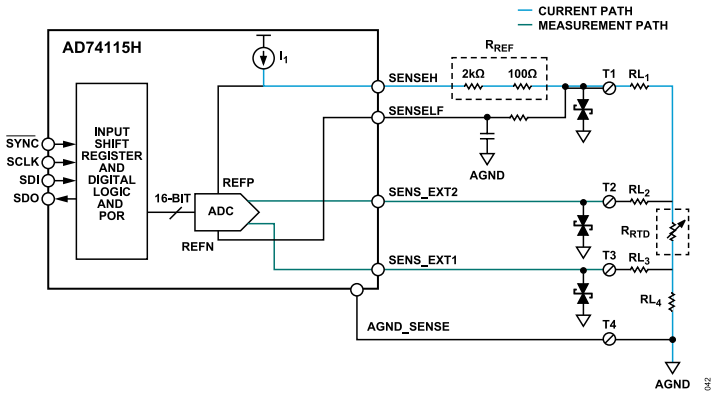

Figure 41. 4-Wire RTD Measurement Configuration

How to Configure a 4-Wire RTD Measurement for Pt100 RTD

The following is an example of how to configure a 4-wire RTD measurement for the Pt100 RTD:

- Select 3-wire or 4-wire resistance measurement in the CH_FUNC_SETUP register.
- Set CONV1_MUX to SENSE_EXT2 to SENSE_EXT1 and CONV1_RANGE to 0 V to 0.625 V in the ADC_CONFIG register.
- Set RTD_CURRENT to 1 mA and RTD_MODE_SEL to 4-wire RTD mode in the RTD3W4W_CONFIG register.
- Set CONV1_EN and CONV_SEQ to start continuous conversions in the ADC_CONV_CTRL register.

Open-Circuit Detection

The combination of excitation current and load resistance generates a voltage on the SENSEH pin. If the voltage generated on the SENSEH pin is greater than the open-circuit detect voltage specified in Table 8, an open-circuit signal is asserted in the ALERT_STATUS register. This signal indicates an open-circuit condition on either T1 or TI 4 (see Figure 41).

The burnout currents can determine if the SENSE_EXT1 or SENSE_EXT2 pins are open circuit (see the Burnout Currents section).

Interpreting ADC Data

In 4-wire RTD mode, configure the 16-bit, Σ-Δ ADC to measure the voltage from SENSE_EXT2 to SENSE_EXT1. When a conversion is carried out, the ADC code reflects the ratio between R_{RTD} and R_{REF}.

When using unipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{ADC\_CODE+5}{65{,}536 \times ADC\_GAIN} \times R_{REF}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code of the ADC_RESULT1 register.
R_{REF} has a value of 2100 Ω (the combined value of the SENSEH and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the 0 V to 0.625 V range (Pt100), the ADC_GAIN is 4.

When using the 0 V to 12 V range (Pt1000), the ADC_GAIN is 1/4.8.

When using bipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{ADC\_CODE - 32{,}763}{32{,}768 \times ADC\_GAIN} \times R_{REF}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code of the ADC_RESULT1 register.
R_{REF} has a value of 2100 Ω (the combined value of the SENSEH and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the ±104 mV range (Cu10), the ADC_GAIN is 24.

Digital Input Logic

The digital input circuit can convert high voltage digital inputs from the I/OP screw terminal to low voltage logic signals on the GPIO_B pin or on the SPI.

An externally powered sensor provides a high voltage digital input on the I/OP screw terminal. The unfiltered screw terminal voltage on the SENSEL pin can be routed to the on-chip comparator. Use the DIN_UNBUF_EN bit in the DIN_CONFIG2 register to bypass the input buffer if high speed digital input data rates are required. See Table 9 for buffered and unbuffered data rates.

The digital input comparator compares the voltage of the input signal to a programmable threshold (see the Digital Input Threshold Setting section for additional information). To debounce the comparator output, see the Debounce Function section.

Monitor the comparator output by reading from the DIN_COMP_OUT register or on the GPIO_A pin. The GPIO_A

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pin is configured via the GPIO_CONFIGx register to drive out the debounced digital input signal.

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements while the digital input logic mode is enabled.

Figure 42 shows the current, voltage, and output paths of the digital input logic mode.

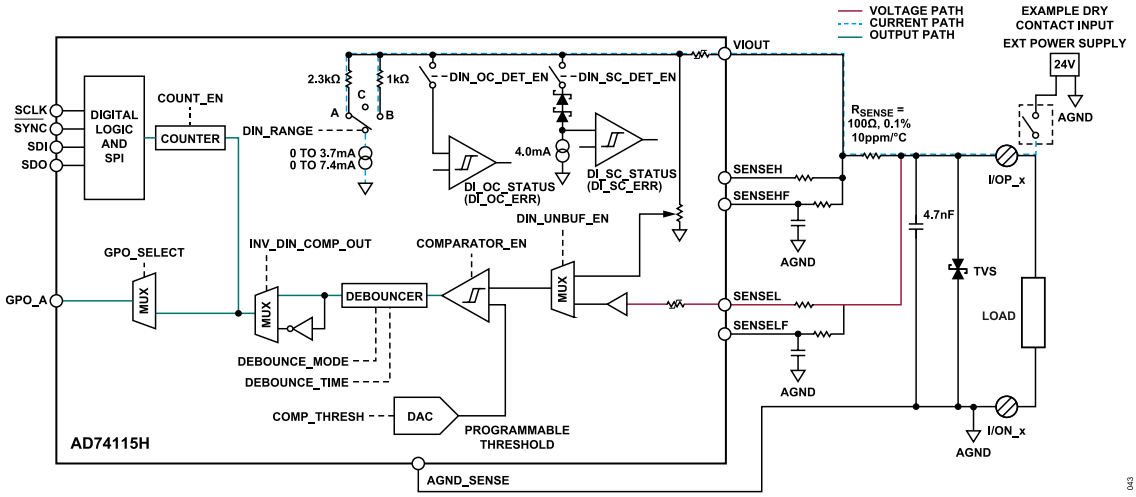

Figure 42. Digital Input Logic Mode Configuration

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Digital Input Threshold Setting

The digital input thresholds are set by an internal DAC. The reference to this DAC is driven by either the V_{AVDD} or the reference voltage, V_{REFIN}. This reference is configured by writing to the DIN_THRESH_MODE bit within the DIN_CONFIG2 register.

The specific threshold levels are programmed using the COMP_THRESH bits in the DIN_CONFIG2 register. There are seven bits available to configure the threshold, and the maximum programmable code is Decimal 98.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to AVDD:

$$V_{THRESH\ (AVDD)} = V_{AVDD} \times \left(\frac{Code - 48}{50}\right)$$

where:
$V_{THRESH\ (AVDD)}$ is the comparator threshold expressed in volts.
V_{AVDD} is the AVDD supply value in volts.
Code is the decimal code loaded to the COMP_THRESH bits.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to V_{REFIN}.

$V_{THRESH\ (FIXED\ VOLTAGE)} = V_{REFIN} \times (Code - 38)/5$

where:
$V_{THRESH\ (FIXED\ VOLTAGE)}$ is the comparator threshold expressed in volts.
V_{REFIN} is the reference voltage.
Code is the decimal code loaded to the COMP_THRESH bits.

Digital Input Current Sink

The AD74115H includes a programmable current sink. The current sink is programmed via the DIN_RANGE bit and the DIN_SINK bits within the DIN_CONFIG1 register. This current sink programmability enables compatibility with Type I, Type II, and Type III of the IEC 61131-2.

Program the current sink and the threshold voltages to enable compatibility with Type I and Type III of the IEC 61131-2.

For Type I and Type III, it is recommended to program the bits in the DIN_CONFIG1 and DIN_CONFIG2 registers as follows:

- DIN_RANGE bit: 0x0
- DIN_SINK bits: 0x14
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits results in a typical current sink of 2.4 mA and a rising voltage trip point of typically 8.5 V.

For Type II, it is recommended to program the DIN_CONFIG1 and DIN_CONFIG2 registers as follows:

- DIN_RANGE bit: 0x1
- DIN_SINK bits: 0x1D
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits result in a typical current sink of 6.96 mA and a rising voltage trip point of 8 V.

Open-Circuit and Short-Circuit Detection

The AD74115H has open-circuit and short-circuit detection capabilities and can be configured to be compatible with IEC 61131-3D.

To use the open-circuit and short-circuit detection functions, enable the current sink by using the DIN_RANGE bit. Set the current using the DIN_SINK bits.

To enable the open-circuit diagnostic, use the DIN_OC_DET_EN bit. An open circuit is detected if the input current is less than 0.35 mA.

To enable the short-circuit diagnostic, use the DIN_SC_DET_EN bit. When the DIN_SC_DET_EN bit is set, an additional 4 mA of current sink is enabled. A short-circuit fault is triggered if the 4 mA sink limit is exceeded.

Once an open-circuit or short-circuit fault is triggered, the appropriate bit is set in the ALERT_STATUS register, and the $\overline{\text{ALERT}}$ pin is asserted.

For Type 3D diagnostics, it is recommended to program the DIN_CONFIG1 and DIN_CONFIG2 registers bits as follows:

- DIN_RANGE bit: 0x0
- DIN_SINK bits: 0xF
- DIN_OC_DET_EN bit: 0x1
- DIN_SC_DET_EN bit: 0x1
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits results in a typical current sink of 1.6 mA and a rising voltage trip point of typically 8.5 V. An open-circuit detection is triggered when sinking currents are less than 220 µA. A short-circuit detection is triggered when sinking currents are greater than typically 6.2 mA.

Digital Input Inverter

The debounced comparator signal can pass directly to the DIN_COMP_OUT register. Alternatively, the signal can be inverted before being sent to the DIN_COMP_OUT register. To enable this inverter, set the INV_DIN_COMP_OUT bit in the DIN_CONFIG1 register.

Digital Input Counter

A counter is available in the digital input modes, and the counter allows the user to count the debounced digital input edges. The

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counter can be programmed to count the positive edges or the negative edges, which depend on whether the digital input inverter is used. Enable the digital input counter and configure the inverter in the DIN_CONFIG1 register. The count value is accessed in the DIN_COUNTER register.

The counter is reset to 0 when the device is reset. When the counter reaches full scale, it rolls over to 0. The counter freezes if the COUNT_EN bit is set to 0.

Digital Input Data Rates

When the AD74115H is configured in digital input mode, the voltage on the SENSEL pin is buffered and monitored by the digital input comparator. Table 9 shows the specified data rate.

To enable higher data rates, a high speed, unbuffered option is available to allow the comparator to monitor high speed signals. For unbuffered operation, the voltage on the VIOUT pin is monitored by the digital input comparator. Refer to Table 9 for the specified data rate for high speed mode. Enable the unbuffered mode by setting the DIN_UNBUF_EN bit in the DIN_CONFIG2 register.

If using unbuffered mode while sourcing or sinking current to the load via the VIOUT pin, consider the voltage drop across R_{SENSE} (100 Ω) and the VIOUT line protector (15 Ω) when setting the threshold voltage.

Debounce Function

The digital input comparator outputs are sampled at regular intervals and passed to a user-programmable debounce operation.

The comparator outputs can be debounced for a user-programmable amount of time via the 5-bit DEBOUNCE_TIME bits within the DIN_CONFIG1 register. Set these bits to 0x00 to bypass the debouncer. Table 21 shows the available programmable debounce times.

The debounce circuit has the following two modes of operation: Debounce Mode 0 and Debounce Mode 1. Both modes are programmed via the DEBOUNCE_MODE bit in the DIN_CONFIG1 register.

Table 21. Digital Input Programmable Debounce Times

DEBOUNCE_TIME Code (Hex)	Debounce Time (ms)
00	Bypass
01	0.0130
02	0.0187
03	0.0244
04	0.0325
05	0.0423
06	0.0561
07	0.0756
08	0.1008
09	0.1301
0A	0.1805
0B	0.2406
0C	0.3203
0D	0.4203
0E	0.5602
0F	0.7504
10	1.0008
11	1.3008
12	1.8008
13	2.4008
14	3.2008
15	4.2008
16	5.6008
17	7.5007
18	10.0007
19	13.0007
1A	18.0006
1B	24.0006
1C	32.0005
1D	42.0004
1E	56.0003
1F	75.0000

Debounce Mode 0 (Default)

In this mode, the sampled comparator outputs are counted. A high sample occurrence is counted in one direction (either up or down), whereas a low sample occurrence is counted in the opposite direction. The DIN_COMP_OUT register changes state when the programmed counter target is reached.

Figure 43 shows an example of Debounce Mode 0 in operation. The debounce time is set to 100 µs in the DIN_CONFIG1 register. A clock with an approximate period of 800 ns sample counts the comparator signal. After the comparator signal changes state from the current debounced signal, the debounce function counter begins to count the duration of the signal at the new state. The count direction changes if the comparator signal reverts back to the original state. After the counter reaches the target count, the DIN_COMP_OUT register is updated with the state of the comparator signal.

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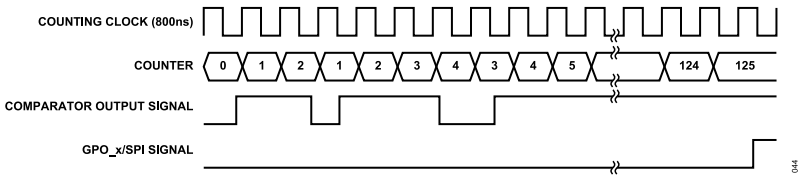

Figure 43. Digital Input Debounce Mode 0 Timing Example

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Debounce Mode 1

In this mode, a counter counts the sampled comparator outputs. After a change of state occurs on the sampled comparator output, the counter increments until the programmed debounce time is reached, at which point the DIN_COMP_OUT register changes state, and the counter resets. If the sampled comparator output returns to the current DIN_COMP_OUT register value, the counter resets.

Figure 44 shows an example of Debounce Mode 1 in operation. Like Debounce Mode 0, the debounce time is set to 100 µs. In Debounce Mode 1, the counter value is reset each time the comparator signal returns to the original state. The comparator output must be at the new state for the full duration of the debounce time to update the DIN_COMP_OUT signal.

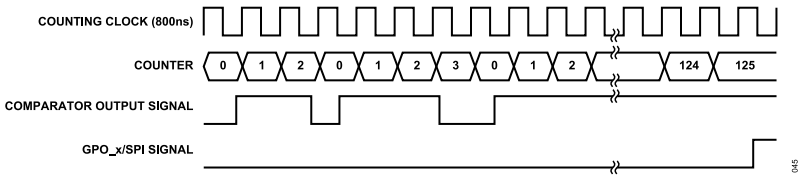

Figure 44. Digital Input Debounce Mode 1 Timing Example

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Digital Input, Loop Powered

Like the current output mode function (see the Current Output (IOUT) and IOUT with HART section), the digital input, loop powered function configures the output stage to provide a high-side current output that can power an external sensor. Program the DAC_CODE register to provide the required current source limit.

The I/OP screw terminal voltage can be monitored by the digital input function. The unfiltered voltage on the SENSEL pin can be routed to the on-chip comparator. Use the DIN_UNBUF_EN bit in the DIN_CONFIG2 register to bypass the input buffer if high speed digital input data rates are required. See Table 9 for buffered and unbuffered data rates.

This comparator compares the voltage on the selected pin to a programmable threshold that can either be a fixed voltage or a voltage proportional to the V_{AVDD}. See the Digital Input Threshold Setting section for more information on the programmable threshold voltages.

The output of the comparators can be debounced (see the Debounce Function section), passed directly, or inverted to the SPI and/or to the GPIO_A pin.

The digital input comparator outputs are monitored by reading from the DIN_COMP_OUT register. The comparator outputs can also be monitored with the GPIO_A pin. The GPIO_A pin is configured via the GPIO_CONFIGx register to drive out the debounced comparator output signal.

Figure 45 shows the current, voltage, and output paths of the digital input, loop powered mode configuration.

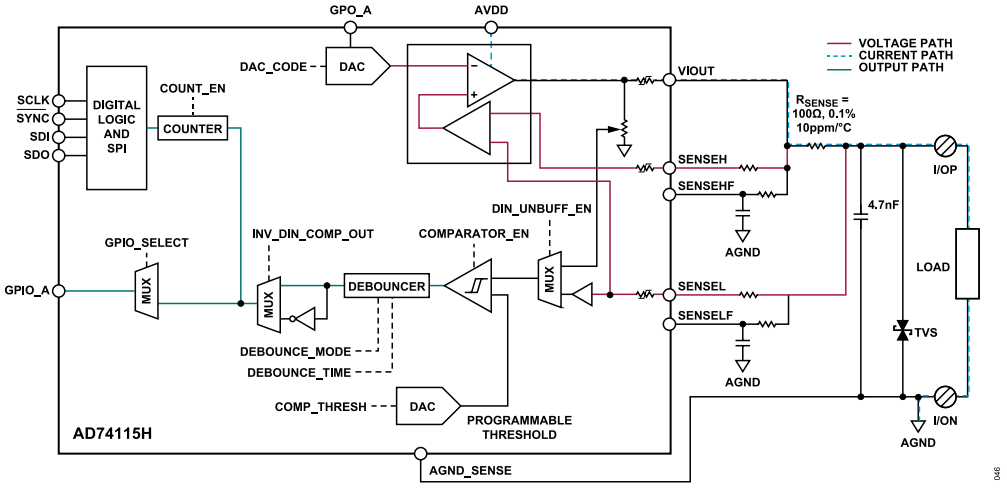

Figure 45. Digital Input, Loop Powered Configuration Mode

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Interpreting ADC Data

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements when the digital input, loop powered mode is enabled. In digital input, loop powered mode, the ADC, by default, measures the voltage across the I/OP to I/ON screw terminals in a 0 V to 12 V range. Use the ADC measurement result to calculate this voltage by using the following equation:

V_{ADC} = (*ADC_CODE*/65,536) × *Voltage Range*

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULT1 register.
Voltage Range is 12 V, the measurement range of the ADC.

Digital Output

The AD74115H supports sourcing and sinking digital outputs. An internal digital output function is available for sourcing or sinking up to 100 mA continuous current. For currents higher than 100 mA, use the external digital output function. A push-pull feature is also available that combines both the source and sink capabilities to provide high speed, high voltage switching.

When the digital output functionality is enabled, the recommended configuration of the CH_FUNC_SETUP register is to set it to high impedance.

Sourcing and Sinking Currents Greater Than 100 mA

The external sourcing digital output operates with an external, P-channel field effect transistor (PFET), and the sinking digital output operates with external N-channel FET (NFET). Push-pull mode uses both PFET and NFET. Choose the FET types to suit the application requirements. Determine the absolute current value by the R_{SET} and short-circuit voltage values. Short-circuit voltages are indicated in the Table 11.

Configure the digital output using the DO_EXT_CONFIG register:

- Select source, sink, or push-pull capability by using the DO_EXT_MODE bits.
- Select the source of the data for the digital output circuit using the DO_EXT_SRC_SEL bit. The digital output data can be provided by the SPI (via the DO_DATA_EXT bit) or by the GPIO_B pin for direct hardware control of the circuits.
- Configure the short-circuit timers using the DO_EXT_T1 and DO_EXT_T2 bits. See the Short-Circuit Protection section for more information on short-circuit functionality. Note that T1 short-circuit limits are not available in push-pull mode

Once the configuration settings are applied, provide stimulus to turn on the selected external FET. For SPI control, a new write is required to the DO_EXT_CONFIG register, to set the DO_DATA_EXT bit. Setting the DO_DATA_EXT to 1 turns on the selected external FET. In push-pull mode, set the bit to 0 to drive a low on the output and to 1 to drive a high on the output.

For GPIO control, configure the GPIO_x pin to control the digital output circuit by writing 0x0004 to the GPIO_CONFIGx register. Drive the GPIO_x pin high to turn on the FET. In push-pull mode, set the GPIO_x pin low for a low on the output and high for a high on the output.

If changing from one digital output function to another, first disable the digital output function before changing to the new mode (set DO_EXT_MODE to digital output external disable).

Figure 46 shows the current and voltage paths of the sourcing digital output mode with the external FET. Figure 47 shows the current and voltage paths of the sinking digital output mode with the external FETs.

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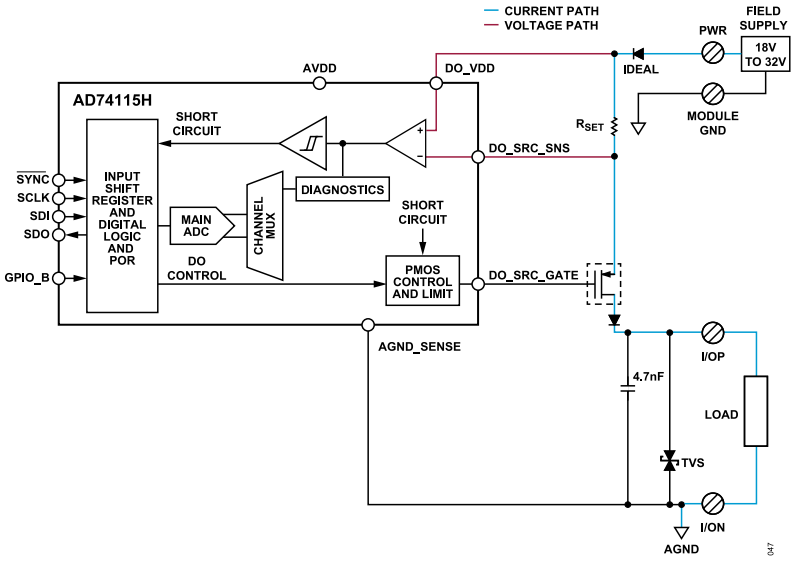

Figure 46. Digital Outputs Sourcing with External FET

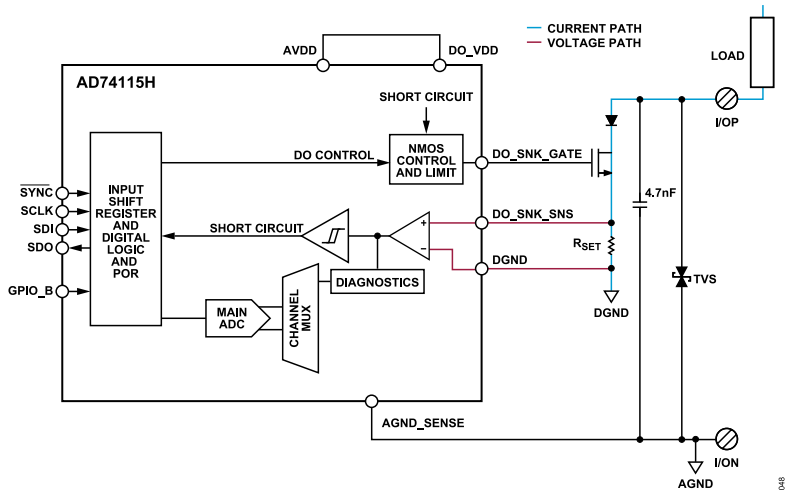

Figure 47. Digital Output Sinking with External FET

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Smart Diode

In current sourcing applications, a blocking diode is typically placed in series with the output FETs to ensure that the digital output path is protected against reverse overvoltage conditions (when the I/OP screw terminal voltage is greater than the DO_VDD voltage, V_{DO_VDD}). This typical configuration is shown in Figure 46.

Significant power can be dissipated in this diode when the digital output circuit is sourcing high currents (for example, a 500 mA current source and a diode drop of 0.5 V generates 250 mW of power).

The AD74115H has a smart diode feature when using the external digital output function. An additional FET is connected, along with a resistor and protection Zener, as shown in Figure 48. The gate of the FET is controlled by the DO_SRC_DGATE pin. When the FET is disabled, the body diode of the FET conducts. When the FET is enabled, the power dissipated is calculated by $P = I^2R$, where I is the sourced current, and R is the R_{ON} of the FET. Typically, the power dissipation in this scenario is <50 mW.

To enable the smart diode option, set DO_EXT_MODE to an external source with a smart diode in the DO_EXT_CONFIG register.

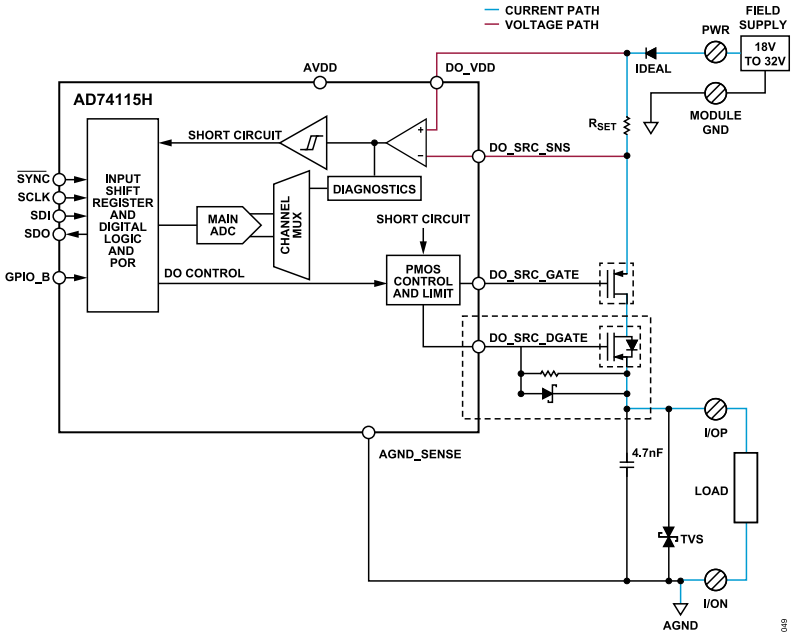

Figure 48. Smart Diode Configuration for Current Sourcing with an External FET

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Sourcing and Sinking Currents up to 100 mA

Internal FETs are available to source or sink up to 100 mA continuous current. A 200 mA start-up current is also accommodated. Using the internal FETs to provide the digital output current eliminates the need for external FETs. Push-pull mode uses both the sourcing and sinking internal FETs. Configure the digital output using the DO_INT_CONFIG register:

- Select source, sink, or push-pull capability using the DO_INT_MODE bits.
- Select the source of the data for the digital output circuit using the DO_INT_SRC_SEL bit. The digital output data can be provided by SPI (via the DO_DATA_INT bit) or by the GPIO_C pin for faster output rates.
- Configure the short-circuit timers using the DO_INT_T1 and DO_INT_T2 bits. See the Short-Circuit Detection section for more information on short-circuit functionality. Note that T1 short-circuit limits are not available in push-pull mode.

Once the configuration settings are applied, a new write is required to the DO_INT_CONFIG register, to set the DO_DATA_INT bit. Setting the DO_DATA_INT to 1 turns on the selected FET. In push-pull mode, set the bit to 0 to drive a low on the output and to 1 to drive a high on the output.

For GPIO control, configure the GPIO_x pinto control the digital output circuit by writing 0x0004 to the GPIO_CONFIGx register. Drive the GPIO_x pin high to turn on the FET. In push-pull mode, set the pin low for a low on the output and high for a high on the output.

If changing from one digital output function to another, first disable the digital output function before changing to the new mode (set DO_INT_MODE to digital output internal disable).

The power and isolation companion chip, ADP1034, can provide the power required to operate the AD74115H in digital output mode (using the internal FETs) sourcing continuous currents up to 100 mA. The ADP1034 also accommodates the 200 mA start-up current. In this case, the AVDD pin can be externally connected to the DO_VDD pin, eliminating the need for an additional DO_VDD supply source.

Figure 49 shows the current and voltage paths of the digital output sourcing mode with the internal FET.

Figure 50 shows the current and voltage paths of the digital output sinking mode with the internal FET.

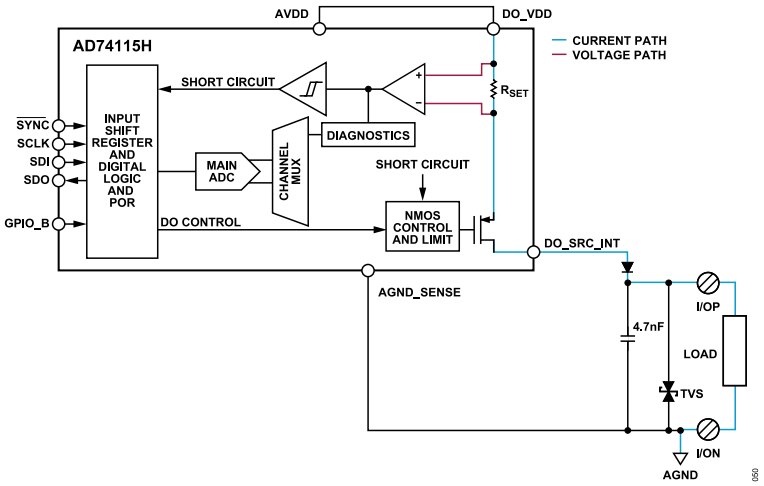

Figure 49. Digital Output Sourcing Mode with the Internal FET

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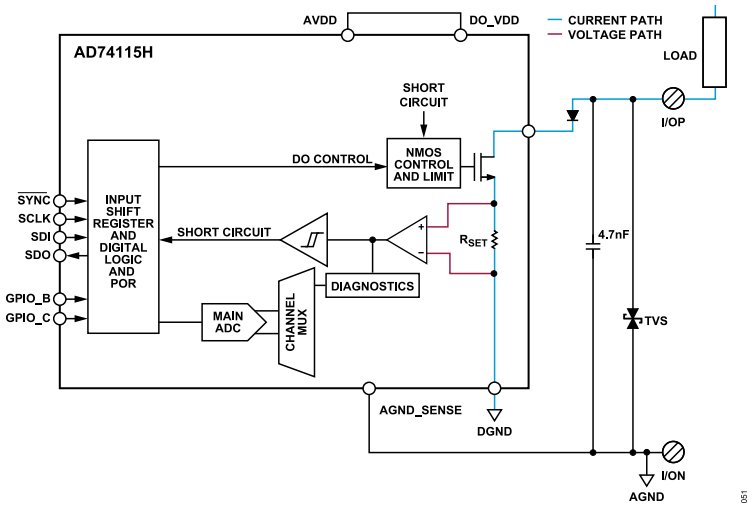

Figure 50. Digital Output Sinking Mode with the Internal FET

Thermal Shutdown

When the internal digital output is enabled, a thermal shutdown function is automatically enabled to protect the AD74115H in short-circuit scenarios.

If the output drivers reach the disable temperature specified in Table 11, the digital output is disabled. The DO_THERM_RESET bit is set in the ALERT_STATUS register to indicate that thermal shutdown of the digital output circuit has occurred.

Once the die temperature reaches the specified reenabled temperature in Table 11, the digital output circuit attempts to turn back on. If the high power dissipation condition persists, the die quickly reaches the disabled temperature again. Take care to manage the power dissipation to prevent multiple disable and reenable cycles on the internal digital output.

Short-Circuit Protection

When using the external digital output, short-circuit protection is achieved using a current-limit setting resistor, R_{SET}. A short-circuit event is triggered when the voltage developed across the resistor reaches the short-circuit voltage specified in Table 11. In the event of a short circuit, the DO_EXT_SC bit is set in the ALERT_STATUS register, which in turn asserts the $\overline{\text{ALERT}}$ pin.

When using the internal digital output, a short circuit is triggered when the current reaches the short-circuit current limit specified in Table 11. In the event of a short circuit, the DO_INT_SC bit is set in the ALERT_STATUS register, which in turn asserts the $\overline{\text{ALERT}}$ pin.

There is programmability around how the short-circuit behavior operates. The two configurable short-circuit timeout times are T1 and T2.

To support charging of large current loads on initial power-on of the digital output load, a higher short-circuit current limit can be enabled for a programmable amount of time, T1. T1 starts counting once the digital output FET is turned on using the DO_DATA_INT or DO_DATA_EXT bit (for internal FETs or external FETs, respectively), even if no short-circuit event was triggered. If a short-circuit event occurs, the digital output FET remains on, clamped at the higher short-circuit current for the remainder of the programmed duration of T1. The short-circuit alert is not triggered during this time.

A second short-circuit limit is deployed once the T1 time elapses, is a lower current limit, and is active for a programmable duration of time, T2. The T2 counter only starts counting if T1 expires and a short circuit is detected. The FET remains on during a short-circuit event, but the current is limited to the lower short-circuit current for the programmed duration of T2.

The T2 counter is an up and down counter: when in short circuit, the time increments. If the short-circuit condition goes away, the time count decrements.

T1 and T2 can be programmed in the DO_EXT_CONFIG register for external FETs or DO_INT_CONFIG register for internal FETs. If the higher short-circuit current limit is not required, T1 can be disabled. See Table 11 for the specified short-circuit values and T1 and T2 durations for both internal and external modes of operation.

If the short circuit continues to persist after the T2 time expires, the FET automatically disables. Once disabled, the relevant digital output timeout bit is set in the ALERT_STATUS register. The digital output is disabled, which is reflected in the DO_EXT_CONFIG register or the DO_INT_CONFIG register for the external digital output or the internal digital output, respectively.

Figure 51 illustrates the operation of the two programmable timeout times along with the short-circuit current limits.

To reenable the digital output circuit after a timeout event:

- Set the DO_DATA_INT or DO_DATA_EXT bit to 0

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- Choose a mode in the DO_INT_MODE or DO_EXT_MODE bits in the relevant configuration register to power on the digital output circuit
- Set the DO_DATA_INT or DO_DATA_EXT bit back to 1 to enable the FET.

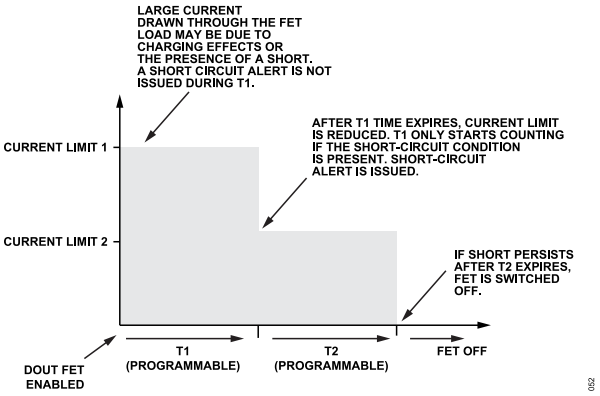

Figure 51. Digital Output Programmable Short-Circuit Control

Current Sensing Diagnostic

A digital output, current sense diagnostic is available to monitor the current in the digital output circuit.

Select the current sense diagnostics by programming the DIAG_ASSIGN register.

When using external FETs, the diagnostic (Diagnostic 0 for the sinking current and Diagnostic 1 for the sourcing current) measures the voltage dropped across the external R_{SET} resistor. Consider the resistance of the selected R_{SET} when calculating the current being sourced or sinked by the digital output circuit. Note that if Diagnostic 1 is required to measure sourcing current in the external digital output circuit, and Diagnostic 0 must also be enabled in the ADC_CONV_CTRL register to guarantee measurement accuracy. Any diagnostic setting of choice can be selected on Diagnostic 0. Consider the additional enabled diagnostics when calculating conversion times.

When using internal FETs, the diagnostic (Diagnostic 2 for the sinking current, and Diagnostic 3 for the sourcing current) measures the current being sourced or sinked by the digital output circuit. Use the equations in Table 29 to determine the current from the returned ADC code, which is read in the ADC_DIAG_RESULTx register. Note that, if Diagnostic 3 is required to measure sourcing current in the internal digital output circuit, Diagnostic 2 must also be enabled in the ADC_CONV_CTRL register to guarantee measurement accuracy. Any diagnostic setting of choice can be selected on Diagnostic 3. Consider the additional enabled diagnostics when calculating conversion times.

HART

The AD74115H has an integrated HART modem. The following sections describe the HART features.

HART Modem

The AD74115H includes an integrated HART modem that can transmit and receive signals to and from the I/OP screw terminal. The HART modem can be used for HART communications in current output and current input modes of operation.

Figure 52 shows the interface, transmit, and receive paths for the HART modem on the AD74115H. HART transmit signals are coupled onto the I/OP screw terminal by injecting the signal from the HART_TX_OUT pin to the HART_TX_IN pin. An external capacitor ensures that there is no dc contribution from the HART modem to output signal.

HART receive signals are coupled directly from the I/OP screw terminal to the HART modem via the HART_RX pin. Refer to Table 36 for the recommended external components required for HART operation.

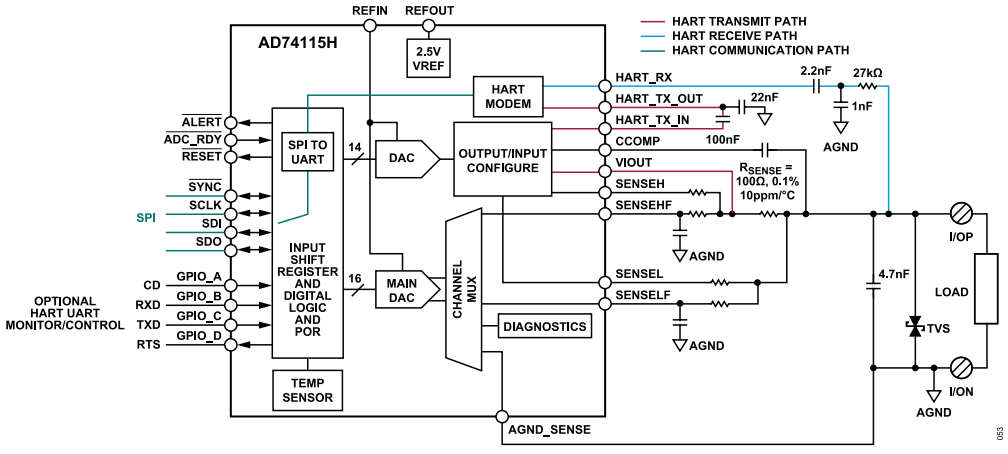

Figure 52. HART Configuration

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Communicating with the HART Modem

Communication with the modem is via the SPI. An internal SPI to universal asynchronous receiver transmitter (UART) implementation handles the transactions on the SPI and converts these transactions to UART commands to and from the modem. The necessary status bits are provided via the SPI to communicate with an existing software stack.

The SPI manages the HART transactions and the software configurable input and output transactions.

It is also possible to configure the GPIO_x pins to either monitor or control the HART modem UART interface by programming the GPIO_SELECT bits in the GPIO_CONFIGx registers.

Transmit and Receive FIFOs

The AD74115H is equipped with a HART transmit first in, first output (FIFO) and HART receive FIFO. Up to 32 bytes of data can be stored in each of the transmit and receive FIFOs.

The transmit FIFO is loaded using the HART_TX register. Data can be read from the receive FIFO via the HART_RX register. An alert is issued if the number of bytes loaded to the transmit FIFO falls below the programmable threshold value. Similarly, an alert is issued if the number of bytes loaded to the receive FIFO goes above the programmable threshold value. These receive and transmit threshold values can be programmed via the TFTRIG and RFTRIG bits in the HART_FCR register.

The number of bytes currently stored in the transmit and receive FIFOs is recorded in the HART_TFC and HART_RFC registers, respectively.

HART Alerts

The HART_ALERT_STATUS register contains all the alert bits associated with HART communications. If any bit is asserted in the HART_ALERT_STATUS register, the HART_ALERT bit is asserted in the ALERT_STATUS register, which allows for an interrupt to be generated on the $\overline{\text{ALERT}}$ pin. The HART alert bits can be masked via the HART_ALERT_MASK register. If an alert bit is masked, it does not generate an interrupt on the $\overline{\text{ALERT}}$ pin when asserted, but the alert is still seen in the HART_ALERT_STATUS register.

Configuring the AD74115H for HART Communications

To initiate HART communications with the AD74115H, take the following steps:

- Configure the channel in the appropriate function (current output with HART; current input, loop powered with HART; or current input externally powered with HART).
- Wait 200 µs before proceeding with another step.
- Enable the HART slew option in the OUTPUT_CONFIG register if the current output with HART is selected.
- Power up the HART modem in the HART_CONFIG register. Other HART configuration options are available in the HART_CONFIG register and can be configured as required. Note that a duplex mode of operation is available to allow for loopback testing of the modem to confirm that data can be transferred and received by the AD74115H.
- Load the HART transmit FIFO with data required for transmission via the HART_TX register.
- Ensure that the HART alerts are cleared in the HART_ALERT_STATUS register.
- Set the RTS bit in the HART_MCR register to start HART transmissions.
- Monitor the HART_ALERT_STATUS register for status alerts on the progress of the HART communication.
- Read the receive FIFO by using the HART_RX register. Note that, the receive bytes of data are stored in the receive FIFO.

GETTING STARTED

Power up the AD74115H as recommended in Powering on the AD74115H section. After initial power-up, the $\overline{\text{ALERT}}$ pin is pulled low as a result of various bits, such as the RESET_OCCURRED bit being set in the ALERT_STATUS register. It is recommended to clear the ALERT_STATUS register before continuing to use the AD74115H. Write 1 to clear each bit in the ALERT_STATUS register.

Using Channel Functions

The channel function is selected using the CH_FUNC_SETUP register. Once a channel function is selected, the contents of a number of registers are updated with predefined values, which allows the user to configure the device with a minimal set of commands. The updated settings include configuration of the channel conversion on the ADC, Conversion 1. Table 22 outlines the default settings of the bits for any given channel function. In addition to the default settings described in Table 22, these bit fields are set to the following values, irrespective of the CH_FUNC_SETUP selection:

- RTD_MODE_SEL in the RTD3W4W_CONFIG register is set to 0 (selects 3-wire RTD)
- RTD_CURRENT in the RTD3W4W_CONFIG register is set to 11 binary (selects 1 mA)
- DIN_SINK in the DIN_CONFIG1 register is set to 0 (ISINK off)
- DIN_THRESH_MODE in the DIN_CONFIG2 register is set to 0 (threshold relative to AVDD)

After configuring the channel function, users can configure the DAC_CODE registers, as required.

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Table 22. Register Defaults Based on Channel Function Selection

CH_FUNC Bits (Programmed via the CH_FUNC_SETUP Register)	Defaults of the ADC_CONFIG Register		Defaults of the DIN_CONFIG1 Register	Defaults of the DIN_CONFIG2 Register
	CONV1_MUX Bits	CONV1_RANGE Bits	COMPARATOR_EN Bit	COMP_THRESH Bits
0000: High Impedance	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	0: disabled	0: −0.96 × AVDD
0001: Voltage Output	01: SENSEHF to SENSELF	010: −2.5 V to +2.5 V	0: disabled	0: −0.96 × AVDD
0010: Current Output	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	0: disabled	0: −0.96 × AVDD
0011: Voltage Input	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	0: disabled	0: −0.96 × AVDD
0100: Current Input, Externally Powered	01: SENSEHF to SENSELF	011: −2.5 V to 0 V	1: enabled	0x49: AVDD/2
0101: Current Input, Loop Powered	01: SENSEHF to SENSELF	100: 0 V to 2.5 V	1: enabled	0x49: AVDD/2
0110: 2-Wire Resistance Measurement	00: SENSELF to AGND_SENSE	100: 0 V to 2.5 V	0: disabled	0: −0.96 × AVDD
0111: 3- or 4-wire RTD Measurement	11: SENSELF to SENSE_EXT1	101: 0 V to 0.625 V	0: disabled	0: −0.96 × AVDD
1000: Digital Input Logic	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	1: enabled	0x49: AVDD/2
1001: Digital Input, Loop Powered	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	1: enabled	0x49: AVDD/2
1010: Current Output with HART	00: SENSELF to AGND_SENSE	000: 0 V to 12 V	0: disabled	0: −0.96 × AVDD
1011: Current Input, Externally Powered with HART	01: SENSEHF to SENSELF	011: −2.5 V to 0 V	1: enabled	0x49: AVDD/2
1100: Current Input, Loop Powered with HART	01: SENSEHF to SENSELF	100: 0 V to 2.5 V	1: enabled	0x49: AVDD/2

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Switching Channel Functions

Take care when switching from one channel function to another. All functions must be selected for a minimum of 200 µs before changing to another function.

The DAC_CODE register is not reset by changing channel functions. Before changing channel functions, it is recommended to set the DAC code to 0x0000 via the DAC_CODE register. Set the channel function to high impedance via the CH_FUNC_SETUP register before transitioning to the new channel function.

For ±12 V voltage output, the DAC_CODE can be updated to 0x2000 before the voltage output is enabled to ensure that the output stage powers up to 0 V. Refer to the Voltage Output section.

After the new channel function is configured, it is recommended to wait 200 µs before updating the DAC code.

ADC FUNCTIONALITY

The AD74115H provides a single, 16-bit Σ-Δ ADC that can be sequenced to measure up to two channel measurements and up to four diagnostics measurements for a single conversion sequence or for continuous conversions. The two channel measurements allow for various voltage and current monitoring options on the I/OP screw terminal and the auxiliary high voltage SENSE_EXT1 and SENSE_EXT2 pins.

Conversion 1 is targeted at supporting the measurements required for each of the AD74115H use cases. Table 23 shows the measurements available for Conversion 1. When any mode of operation is selected in the CH_FUNC_SETUP register, Conversion 1 is configured to a default measurement. These default measurements are described in the Using Channel Functions section.

Conversion 2 can be used for additional diagnostics measurements on the channel or to monitor other external nodes. Table 24 shows the measurements available for Conversion 2.

Each conversion has an individual conversion rate and voltage range control that can be configured in the ADC_CONFIG register.

The ADC also provides diagnostic information on user-selectable inputs such as supplies, internal die temperature, reference, and regulators. See the Diagnostics section for more information on the diagnostics measurements.

After the measurements are configured in the ADC_CONFIG register, enable the relevant ADC measurements via the ADC_CONV_CTRL register.

Select either single conversion or continuous conversion mode by setting the appropriate value to the CONV_SEQ bits in the ADC_CONV_CTRL register.

In single conversion mode, the ADC sequencer starts conversions on Conversion 1 and Conversion 2 followed by the enabled diagnostics. After each enabled input is converted once, the ADC enters idle mode, and conversions are stopped.

In continuous conversion mode, the ADC channel sequencer continuously converts the enabled channel conversions and each enabled diagnostic until a command is written to stop the conversions. Set the stop command by setting the CONV_SEQ bits in the ADC_CONV_CTRL register to idle mode or power-down mode. The command stops conversions at the end of the current sequence.

If the measurement configuration requires a change, continuous conversions must be stopped before making the changes. Restart the continuous conversions after making the appropriate changes.

After a sequence is complete, all data results are transferred to the relevant ADC_RESULT1, ADC_RESULT2, and ADC_DIAG_RESULTn registers and the $\overline{\text{ADC\_RDY}}$ pin is asserted.

Table 23. Selection Options for ADC Conversion 1

CONV1_MUX Settings in the ADC_CONFIG Register	Measurement Selection	Description
00	SENSELF to AGND_SENSE	Voltage measurement across the I/OP and I/ON screw terminals
01	SENSEHF to SENSELF	Voltage measurement across the R_{SENSE} resistor
10	SENSE_EXT2 to SENSE_EXT1	Voltage measurement across SENSE_EXT2 and SENSE_EXT1 for 4-wire RTD measurement
11	SENSELF to SENSE_EXT1	Voltage measurement across SENSE_EXT1 and SENSELF for 3-wire RTD measurement

Table 24. Selection Options for ADC Conversion 2

CONV2_MUX Settings in the ADC_CONFIG Register	Measurement Selection	Description
00	SENSE_EXT1 to AGND_SENSE	Enables single-ended monitor of SENSE_EXT1 pin
01	SENSE_EXT2 to AGND_SENSE	Enables single-ended monitor of SENSE_EXT2 pin
10	SENSE_EXT2 to SENSE_EXT1	Enables differential measurements
11	AGND to AGND	Diagnostic

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Auxiliary Sense Pins

The SENSE_EXT1 and SENSE_EXT2 pins are uncommitted high voltage sense pins that can be measured with the ADC. These pins can be used for a number of functions.

The SENSE_EXT1 and SENSE_EXT2 pins can be used for single-ended or differential voltage measurements using ADC Conversion 2. An appropriate antialiasing filter can be added to the pin being measured. See Table 36 for example components. Use the ADC result to calculate the voltage measured on the relevant sense pin by using the following equation:

$$V_{ADC} = V_{MIN} + (ADC\_CODE/65{,}536) \times Voltage\ Range$$

where:
V_{MIN} is the minimum input voltage of the selected ADC range.
V_{ADC} is the measured voltage in volts.
ADC_CODE is value of the ADC_RESULT2 register.
Voltage Range is the selected measurement range of the ADC.

SENSE_EXT1 is required for 3-wire RTD measurements. See the 3-Wire RTD Measurements section for more detail. SENSE_EXT1 and SENSE_EXT2 are required for 4-wire RTD measurements. See the 4-Wire RTD Measurements section for more details.

If either SENSE_EXT1 or SENSE_EXT2 pins are unused for an extended time, it is recommended to enable a sinking burnout current of 1 µA. Enable the burnout current on SENSE_EXT1 by programming the following bits in the I_BURNOUT_CONFIG register:

- BRN_SENEXT1_EN to 1
- BRN_SENEXT1_POL to 0
- BRN_SENEXT1_CURR to 100 binary

Enable the burnout current on SENSE_EXT2 by programming the following bits in the I_BURNOUT_CONFIG register:

- BRN_SENEXT2_EN to 1
- BRN_SENEXT2_POL to 0
- BRN_SENEXT2_CURR to 100 binary

ADC Transfer Function

Table 25 shows the ideal input voltage for zero-scale, midscale, and full-scale codes for each of the available voltage ranges when measuring voltages with the on-board ADC.

Currents through the external R_{SENSE} resistor are determined by measuring the voltage across R_{SENSE}. Set the CONV1_MUX bits to measure between SENSEHF and SENSELF. Table 26 shows the ideal input currents for zero-scale, midscale, and full-scale codes using each available voltage range (to calculate current, measured voltage is divided by the R_{SENSE} value, 100 Ω.)

If the voltage measured by the ADC is either more than full scale or less than zero scale, an ADC_ERR bit is set in the ALERT_STATUS registers, asserting the $\overline{ALERT}$ pin. In this case, the ADC output reads 0xFFFF or 0x0000, respectively. The ADC_ERR bit can be masked via the ALERT_MASK register (optional) if these alerts are not required.

Table 25. Ideal Output Code to Input Voltage Relationship

	Input Voltage for Selected ADC Codes[1]		
Input Voltage Range	**0x0**	**0x8000**	**0xFFFF**
0 V to +12 V	0 V	+6 V	12 V – 1 LSB
±12 V	−12 V	0 V	12 V – 1 LSB
±2.5 V	−2.5 V	0 V	2.5 V – 1 LSB
0 V to +2.5 V	0 V	+1.25 V	2.5 V – 1 LSB
−2.5 V to 0 V	0 V	−1.25 V	−2.5 V – 1 LSB
±104.16 mV	−104.16 mV	0 V	104.16 mV – 1 LSB
0 V to +0.625 V	0 V	+0.3125 V	0.625 V – 1 LSB

[1] 1 LSB = (Full Scale – Zero Scale)/65,536.

Table 26. Ideal Output Code to Input Current Relationship

	Input Current for Selected ADC Codes[1]			
Input Voltage Range	**0x0**	**0x8000**	**0xFFFF**	**Sourcing or Sinking**
±2.5 V	−25 mA (Sinking)	0 mA	25 mA – 1 LSB (sourcing)	Sink and source
0 V to +2.5 V	0 V	12.5 mA	25 mA – 1 LSB	Sourcing
−2.5 V to 0 V	0 V	12.5 mA	25 mA – 1 LSB	Sinking

[1] 1 LSB = (Full Scale – Zero Scale)/65,536.

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Saving Power When Using the ADC

Each of the high voltage sense pins available for measurement by the ADC (SENSEHF, SENSELF, SENSE_EXT1, and SENSE_EXT2) has a high voltage buffer that is powered up by default. The typical current drawn from each of these buffers is specified in Table 14.

If any of the sense pins are not required for measurement by the ADC, the high voltage buffer associated with that pin can be put in standby mode to save total power consumption by the AD74115H. Configure the AD74115H into the desired channel function and put any of the high voltage sense pin buffers in standby. Buffers are put into standby by setting the appropriate bit in the PWR_OPTIM_CONFIG register. Wait for the appropriate power-up time, specified in Table 14, when taking the buffers out of standby mode.

For optimal performance, power up the buffers before starting the conversion sequence.

Do not update the PWR_OPTIM_CONFIG settings while an ADC conversion sequence is taking place.

ADC Conversion Rates

The available ADC conversion rates on the AD74115H are 10 SPS, 20 SPS, 1.2 kSPS, 4.8 kSPS, and 9.6 kSPS. In addition, 50 Hz and 60 Hz rejection is provided on the 10 SPS and 20 SPS conversion rates.

Configure each of the channel conversion rates via the ADC_CONFIG register. The conversion rate of the diagnostics inputs is set via the ADC_CONV_CTRL register. One conversion rate selection applies to all diagnostic inputs.

The time it takes for a sequence of conversions to complete is dependent on several factors, such as the number of selected inputs, the selected conversion rates, and whether single or continuous mode conversions are enabled. Conversions are clocked by an on-chip oscillator. Table 27 outlines the various components required to estimate a complete conversion time for any given sequence.

For single conversions, consider the following time components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers, if previously powered down.
- The initial pipeline delay before the first conversion.
- The conversion time for each ADC conversion.

Figure 53 shows the timing breakdown of a single conversion example. In this example, the ADC and high voltage buffers are in a power-down state before a single conversion on the channel is enabled, and continuous conversions are initiated with a 4.8 kSPS conversion rate.

The time to the first complete conversion (the $\overline{\text{SYNC}}$ pin falling edge to the $\overline{\text{ADC\_RDY}}$ pin falling edge) is 384.32 µs and is calculated by adding the SPI transfer time, the ADC and high voltage buffer power-up time, the pipeline delay time, and the conversion rate on the channel at 4.8 kSPS (208.33 µs). The time between conversions (the $\overline{\text{ADC\_RDY}}$ pin falling edge to the $\overline{\text{ADC\_RDY}}$ pin falling edge) is 208.33 µs.

For multiple conversions, consider the following components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers, if previously powered down.
- An initial pipeline delay before the first conversion.
- The conversion time required for each ADC conversion.
- The channel switch time for each time the selected ADC channel is switched.

Figure 54 shows an example of the timing breakdown for a multichannel conversion. In this example, Conversion 1, Conversion 2, Diagnostic 1, and Diagnostic 2 are all enabled. Continuous conversions are initiated with a 20 SPS conversion rate. In this example, the ADC is in idle mode, and the high voltage buffers are powered up.

The time it takes for the first complete conversion ($\overline{\text{SYNC}}$ falling edge to $\overline{\text{ADC\_RDY}}$ falling edge), is 200.149 ms and is calculated by adding the SPI transfer time, the pipeline delay time, and the conversion time on Conversion 1 at 20 SPS, followed by adding the channel switch time and conversion time for the remaining three conversions.

The time between all subsequent conversion sequences (the $\overline{\text{ADC\_RDY}}$ pin falling edge to the $\overline{\text{ADC\_RDY}}$ pin falling edge) is 200.0976 ms and is calculated by adding the channel switch time with the conversion time for the four selected ADC inputs.

Table 27. Conversion Times Components

Conversion Rate	ADC and/or Buffer Power-Up Time (µs)	SPI Transfer Time (µs), 42 ns SCLK	Start-Up Pipeline Delay (µs)	Single ADC Conversion Time	Channel Switch Time, Multiple Enabled Conversions (µs)
9.6 kSPS	100	1.99	55	104.17 µs	24.4
4.8 kSPS	100	1.99	81	208.33 µs	24.4
1.2 kSPS	100	1.99	81	833.33 µs	24.4
20 SPS	100	1.99	87	50 ms	33.6

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Table 27. Conversion Times Components

Conversion Rate	ADC and/or Buffer Power-Up Time (µs)	SPI Transfer Time (µs), 42 ns SCLK	Start-Up Pipeline Delay (µs)	Single ADC Conversion Time	Channel Switch Time, Multiple Enabled Conversions (µs)
10 SPS	100	1.99	5000	100 ms	5024

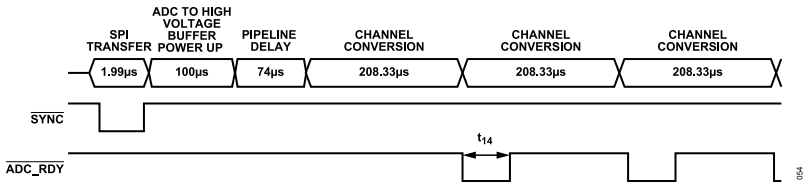

Figure 53. Single Measurement, Continuous Conversions Timing Diagram

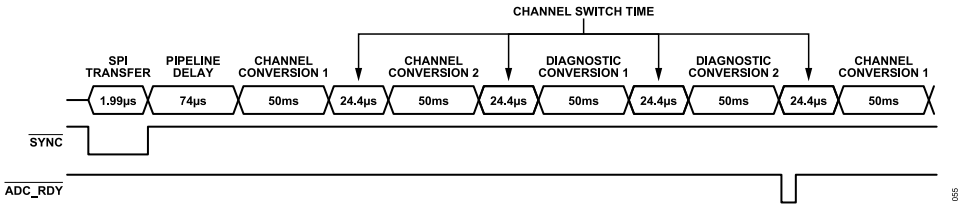

Figure 54. Multiple Measurements, Continuous Conversions Timing Diagram

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$\overline{\text{ADC\_RDY}}$ Functionality

The $\overline{\text{ADC\_RDY}}$ pin asserts low at the end of a sequence of conversions for either single conversion or continuous conversion mode.

The $\overline{\text{ADC\_RDY}}$ pin deasserts in any of the following scenarios:

- After a 1 is written to the ADC_DATA_RDY status bit in the LIVE_STATUS register
- After 24 µs in continuous mode
- After writing to the ADC_CONV_CTRL register

See Figure 55 and Figure 56 for timing diagrams of the $\overline{\text{ADC\_RDY}}$ pin in single and continuous conversion modes.

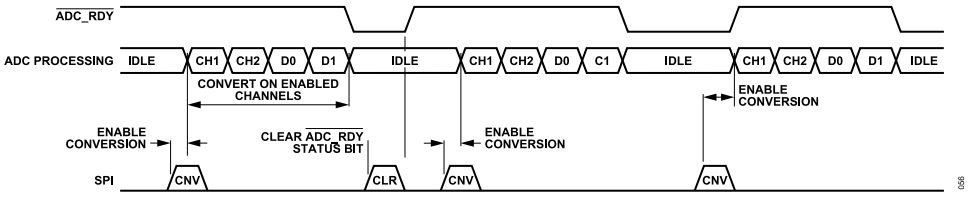

Figure 55. $\overline{\text{ADC\_RDY}}$ Functionality in Single Conversion Mode

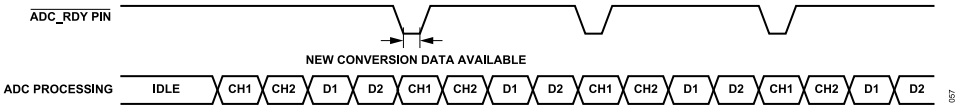

Figure 56. $\overline{\text{ADC\_RDY}}$ Functionality in Continuous Conversion Mode

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ADC Noise

Table 28 shows the peak-to-peak noise of the AD74115H for each of the output data rates and voltage ranges. These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel.

Table 28. Peak-to-Peak Noise in LSBs per Voltage Range and Output Data Rate (Inputs Shorted)

Output Data Rate	+12 V Range (LSBs)	±12 V Range (LSBs)	+2.5 V Range (LSBs)	±2.5 V Range (LSBs)	+0.625 V Range (LSBs)	±104 mV Range (LSBs)
10 SPS	0.1	0.07	0.16	0.08	0.3	0.7
20 SPS	0.2	0.1	0.2	0.1	0.5	1.0
1.2 kSPS	1.1	0.5	1.4	0.7	3.0	8.9
4.8 kSPS	2.7	1.4	3.6	1.8	8.5	18.1
9.6 kSPS	6.0	3.0	7.2	3.6	17.9	33.3

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Diagnostics

The AD74115H has a diagnostic function that allows the ADC to measure various on-chip voltages. These diagnostic voltages are scaled to be measurable within the ADC range.

The diagnostics inputs are independent of the two available channel measurements of the AD74115H. The DIAG_ASSIGN register assigns the voltage measurements to each diagnostic input. Select a diagnostic input to be measured by the ADC by enabling that input in the ADC_CONV_CTRL register. Users can also select the conversion rate via the ADC_CONV_CTRL register. The following three conversion rates are available for selection within the ADC_CONV_CTRL register: 9.6 kSPS, 4.8 kSPS, and 20 SPS. In addition, 50 Hz and 60 Hz rejection is provided on the 20 SPS conversion rate.

Table 29 shows a full list of available diagnostics, and the equations required to calculate the diagnostic value.

In the equations listed in Table 29, DIAG_CODE is the ADC result code read from the ADC_DIAG_RESULTn registers, and the voltage range is the ADC measurement range and is 2.5 V.

Table 29. User-Selectable Diagnostics[1]

Diagnostic	Formula to Interpret ADC Result	Measurement Range
V_{AGND}	$V_{AGND} = \frac{DIAG\_CODE}{65,536} \times 2.5$	0 V to 2.5 V
Temperature Sensor (Internal Die Temperature Measurement)/°C	$Temperature = \left(\frac{DIAG\_CODE - 2034}{8.95}\right) - 40$	See Table 17 for recommended maximum junction temperature
Voltage on AVDD Pin (V_{AVDD})	$V_{AVDD} = \frac{DIAG\_CODE}{65,536} \times 50$	0 V to 50 V
Voltage on DLDO1V8 Pin ($V_{DLDO1V8}$)	$V_{DLDO1V8} = \frac{DIAG\_CODE}{65,536} \times 7.5$	0 V to 7.5 V
Voltage on AVSS Pin (V_{AVSS})	$V_{AVSS} = \left(\frac{DIAG\_CODE}{65,536} \times 31.017\right) - 20$	−20 V to +11 V
Voltage on REFOUT Pin (V_{REFOUT})	$V_{REFOUT} = \frac{DIAG\_CODE}{65,536} \times 3.125$	0 V to 3.125 V
Voltage on AVCC Pin (V_{AVCC})	$V_{ALDO5V} = \frac{DIAG\_CODE}{65,536} \times 17.5$	0 V to 17.5 V
Voltage on ALDO1V8 Pin ($V_{ALDO1V8}$)	$V_{ALDO1V8} = \frac{DIAG\_CODE}{65,536} \times 5.825$	0 V to 5.825 V
Voltage on DVCC Pin (V_{DVCC})	$V_{DVCC} = \frac{DIAG\_CODE}{65,536} \times 8.25$	0 V to 8.25 V
Voltage on SENSEL Pin (V_{SENSEL})		
DIN_THRESH_MODE Bit = 0	$V_{SENSEL} = \left(\frac{DIAG\_CODE}{65,536} \times 60\right) - AVDD$	−AVDD to +60 V − AVDD
DIN_THRESH_MODE Bit = 1	$V_{SENSEL} = \left(\frac{DIAG\_CODE}{65,536} \times 50\right) - 20$	−20 V to +30 V
Voltage on LVIN Pin (V_{LVIN})	$V_{LVIN} = \frac{DIAG\_CODE}{65,536} \times 2.5$	0 V to 2.5 V
Voltage on SENSE_EXT1 Pin (V_{SENSE_EXT1})	$V_{SENSE\_EXT1} = \left(\frac{DIAG\_CODE}{65,536} \times 50\right) - 20$	−20 V to +30 V
Voltage on SENSE_EXT2 Pin (V_{SENSE_EXT2})	$V_{SENSE\_EXT2} = \left(\frac{DIAG\_CODE}{65,536} \times 50\right) - 20$	−20 V to +30 V
Voltage on DO_VDD Pin (V_{DO_VDD})	$V_{DO\_VDD} = \frac{DIAG\_CODE}{65,536} \times 49.2$	0 V to 49.2 V
Voltage Across R_{SET} in External Digital Output Sourcing Mode	$V_{RSET} = \frac{DIAG\_CODE}{65,536} \times 0.3125$	0 V to 0.3125 V (equivalent to 2.08 A when using recommended 0.15 Ω external resistor)
Voltage Across R_{SET} in External Digital Output Sinking Mode	$V_{RSET} = \frac{DIAG\_CODE}{65,536} \times 2.5$	0 V to 2.5 V (equivalent to 16 A when using recommended 0.15 Ω external resistor)
Current Flowing Through R_{SET} in Internal Digital Output Sourcing Mode	$I_{RSET} = \left(\frac{DIAG\_CODE}{65,536} \times 0.3125\right) / 1.38$	0 mA to 226 mA
Current Flowing Through R_{SET} in Internal Digital Output Sinking Mode	$I_{RSET} = \left(\frac{DIAG\_CODE}{65,536} \times 2.5\right) / 1.38$	0 mA to 1.8 A

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DAC FUNCTIONALITY

The AD74115H contains a 14-bit DAC. The DAC core is a 14-bit string DAC. The architecture structure consists of a string of resistors, each with a value of R. The digital input code that is loaded to the DAC_CODE register determines which node on the string the voltage is tapped off from and fed into the output amplifier. This architecture is inherently monotonic and linear.

There are two sources for the code loaded to the DAC. The typical option is to load a code to the DAC from the DAC_CODE register. The second option is to enable slewing to control the rate at which the DAC code is loaded to the DAC.

The code loaded to the DAC from either of the two sources is also loaded to the DAC_ACTIVE register. The DAC_ACTIVE register contains the current code loaded to the DAC, irrespective of the code source.

DAC Transfer Function

Table 30 shows the input code to ideal analog output relationship for each of the available output ranges.

Table 30. Ideal DAC Input Code to Output Relationship

DAC Code				Analog Output		
MSBs		LSBs		±12 V	0 V to 12 V	0 mA to 25 mA
0000	0000	0000	0000	−12 V	0 V	0 mA
0000	0000	0000	0001	24 × (1/16,384) − 12	12 × (1/16,384)	25 mA × (1/16,384)
0010	0000	0000	0000	0 V	6 V	12.5 mA
0011	1111	1111	1110	24 × (16,382/16,384) − 12	12 V × (16,382/16,384)	25 mA × (16,382/16,384)
0011	1111	1111	1111	24 × (16,383/16,384) − 12	12 V × (16,383/16,384)	25 mA × (16,383/16,384)

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Digital Linear Slew Rate Control

The digital linear slew rate control feature of the AD74115H controls the rate at which the output transitions to the new value. This slew rate control feature is available for both the current and voltage outputs.

When the slew rate control feature is disabled, the output value transitions at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the digital slew rate control feature via the OUTPUT_CONFIG register.

After the digital slew rate control feature is enabled, the output steps digitally at a rate defined by the user in the OUTPUT_CONFIG register. The SLEW_LIN_STEP bits dictate the number of codes per increment, and the SLEW_LIN_RATE bits dictate the rate at which the codes are updated. Table 31 shows the typical programmable slew rates for a zero-scale to full-scale (or full-scale to zero-scale) DAC update that is available on the AD74115H.

The DAC_ACTIVE register can monitor the progress of slewing to a target DAC code. This register contains the code that is currently loaded to the DAC.

If the digital slewing is disabled before the end code in the DAC_CODE register is reached, the value remains at the DAC_ACTIVE value, and does not ramp to the end code.

HART Compliant Slew

An enhanced slew option is available to allow compatibility with the HART analog rate of change requirements. Set the SLEW_EN bit in the OUTPUT_CONFIG register to enable this slew option.

Table 31. Programmable Slew Times for a Zero-Scale to Full-Scale Code Update

	Step Size (% of Full-Scale DAC Voltage), Programmable via SLEW_LIN_STEP Bits[1]			
Update Slew Rate, Programmable via SLEW_LIN_RATE Bits (kHz)	**0.8%**	**1.5%**	**6.1%**	**22.2%**
4	31.3 ms	16.7 ms	4.1 ms	1.1 ms
64	2.0 ms	1.0 ms	256 µs	70.4 µs
150	833 µs	444 µs	109 µs	30.0 µs
240	521 µs	277 µs	68.3 µs	18.8 µs

[1] These are theoretical values. The final slew rate is limited by the C_{LOAD} value.

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Driving Inductive Loads

It is recommended to use the digital slew rate control when driving inductive loads greater than approximately 4 mH. Controlling the output slew rate minimizes ringing when stepping the output current by minimizing the current rate of change (di/dt). See the I_{OUT} typical performance of the settling time with an inductive load with and without the slew rate enabled in the Figure 11.

RESET FUNCTION

After the AD74115H is reset, all registers are reset to the default state, and the calibration memory is refreshed. The device is configured in high impedance mode. A reset can be initiated in several ways.

The hardware reset is initiated by pulsing the $\overline{\text{RESET}}$ pin low. The $\overline{\text{RESET}}$ pulse width must comply with the specifications in Table 15.

A software reset is initiated by writing the 0x15FA code (Software Reset Key 1) followed by the 0xAF51 code (Software Reset Key 2) to the CMD_KEY register.

A reset can also be initiated via the thermal reset function, which is described in the Thermal Alert and Thermal Reset section.

If the $V_{DLDO1V8}$ or the V_{DVCC} drop below the specified power supply monitors threshold highlighted in Table 14 the internal power-on reset function resets the AD74115H. The device does not come out of reset until the $V_{DLDO1V8}$ and the V_{DVCC} rise above these voltage levels.

After a reset cycle completes, the RESET_OCCURRED bit is set in the ALERT_STATUS register. If an SPI transfer is attempted before the reset cycle is complete (see Table 14 for typical reset time), the CAL_MEM_ERR bit in the SUPPLY_ALERT_STATUS register is also set to indicate that the calibration memory is not fully refreshed. After the reset time elapses, clear these bits in the ALERT_STATUS register before continuing to use the device.

FAULTS AND ALERTS

The AD74115H is equipped with several fault monitors to detect an error condition.

If an alert or fault condition occurs, the $\overline{\text{ALERT}}$ pin asserts. To determine the source of the alert condition, read the ALERT_STATUS register. This register contains a latched bit for each alert condition.

After the error condition is removed, clear the activated flag by writing 1 to the location of the corresponding bits in the ALERT_STATUS register (write 0xFFFF to the ALERT_STATUS register to clear all alert bits). Alerts asserted in SUPPLY_ALERT_STATUS or HART_ALERT_STATUS must be cleared before the ALERT_STATUS register.

The LIVE_STATUS register is a live representation of the error conditions. The bits in this register are not latched and clear automatically when the error condition is no longer present.

The ALERT_MASK register prevents error conditions from activating the $\overline{\text{ALERT}}$ pin.

Channel Faults

The AD74115H is equipped with multiple open-circuit and short-circuit faults in the various functions as described in the Device Functions section. Manage faults as these faults appear and reset the channel, if necessary, to avoid overheating the device.

Power Supply Monitors

The AD74115H includes six power supply monitors to detect a supply failure. If any of the supplies fall to less than the defined threshold detailed in Table 14, the corresponding bit is set in the ALERT_STATUS register.

Thermal Alert and Thermal Reset

If the AD74115H die temperature reaches the alert temperature described in Table 14, a high temperature error bit (TEMP_ALERT) is set in the ALERT_STATUS register to alert the user of the increasing die temperature.

The device can also be configured to reset at higher die temperatures. To reset the device at higher temperatures, enable the thermal reset function by setting the EN_THERM_RST bit in the THERM_RST register. After this bit is set, the device goes through a full reset after the die temperature reaches the reset temperature described in Table 14.

Burnout Currents

Burnout currents are used to verify the integrity of an attached sensor and to ensure that it has not gone open circuit before taking a measurement from it. The AD74115H can be enabled to provide a user programmable, current source that can be programmed to a fixed value between 50 nA and 10 µA. Burnout currents are available on the VIOUT (to monitor the I/OP screw terminal), SENSE_EXT1, and SENSE_EXT2 pins and can be programmed to source or sink current.

The burnout current sources are disabled on power up. Program the burnout current using the bits in the I_BURNOUT_CONFIG register. The full list of available current settings can be found in Table 14.

The current source can be enabled at all times or alternatively enabled when needed for diagnostic purposes. When a burnout current source is enabled, the selected current is switched onto the selected pin, and it flows in the external load.

FET LEAKAGE COMPENSATION

A software configurable input and output solution can include a precision analog input and output capability along with a high current, digital output capability on a single screw terminal. In this case, the external FET used in the digital output function may

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contribute off-leakage to the screw terminal when not in use. This leakage can affect the accuracy of the analog functions, especially to RTD measurements.

The AD74115H has a FET leakage compensation feature that provides an alternative path to the FET leakage to prevent it from flowing in the I/OP screw terminal.

To enable this feature, configure the FET_LKG_COMP register. Set the FET_SRC_LKG_COMP_EN bit for sourcing digital output and set the FET_SNK_LKG_COMP_EN bit for sinking digital output.

For sourcing the digital output, connect the DO_SRC_INT pin to the drain of the FET as shown in Figure 57. Similarly, for sinking the digital output, connect the DO_SNK_INT pin to the drain of the sinking FET as shown in Figure 58.

The FET leakage compensation feature can be used if the specified leakage of the chosen external FET is expected to contribute error to the precision analog measurements like the current input or 3-wire and 4-wire RTD measurements. This feature is not recommended for use in 2-wire RTD mode.

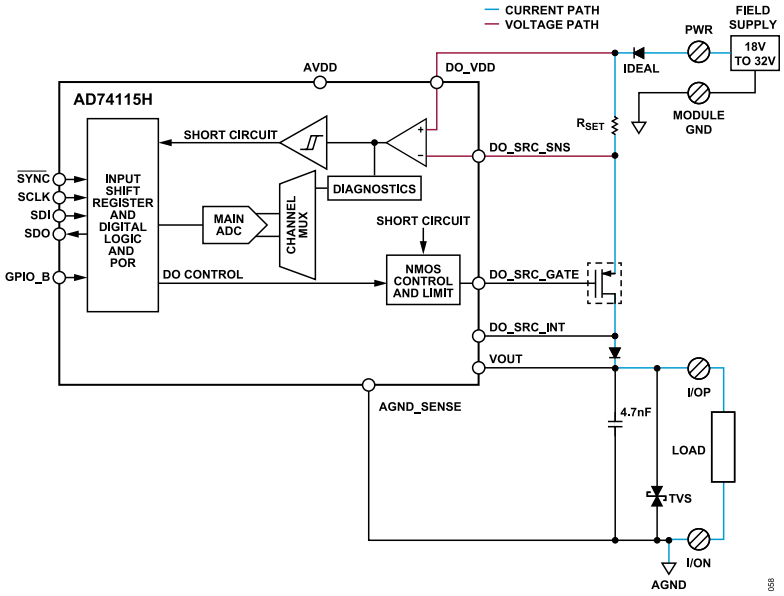

Figure 57. Configuration for Digital Output Sourcing with FET Leakage Compensation

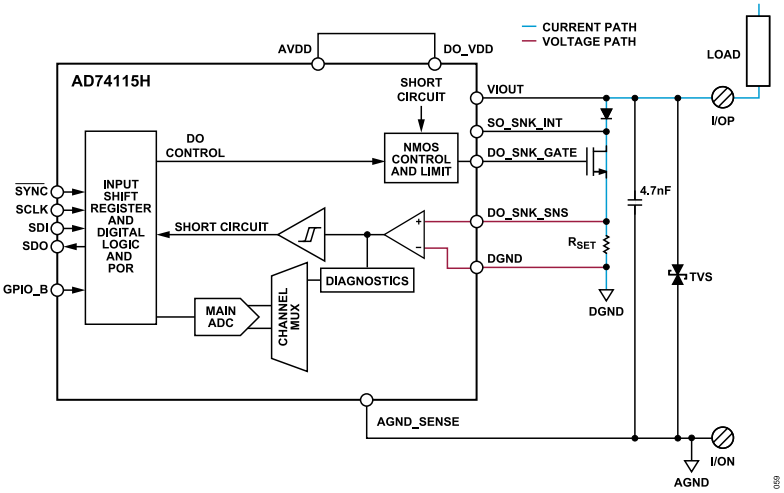

Figure 58. Configuration for Digital Output Sinking with FET Leakage Compensation

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GPIO_x PINS

The AD74115H has four GPIO pins. Each GPIO_x pin can be configured in several ways:

- In high impedance
- As a logic high or low output
- As a logic input

In addition, GPIO_A can be used to monitor the digital input comparator, GPIO_B can be used to control the external digital output circuits, and GPIO_C can be used to control the internal digital output circuits.

Finally, the GPIO_x pins can be configured to monitor or control the UART pins to the HART modem.

By default, a weak pull-down is enabled on the GPIO_x pins. Disable the weak pull-down if configuring any of the GPIO_x pins as logic inputs or outputs. To disable the pull-down, set the GP_WK_PD_EN bit to 0 in the relevant GPIO_CONFIGx register.

The GPIO_x configuration can be set via the GPIO_SELECT bits within the GPIO_CONFIGx registers. When configuring the GPIO_x pins as logic outputs, the data of the pins can be written to the GPO_DATA bit in the GPIO_CONFIGx registers.

SPI

The AD74115H is controlled over a versatile 4-wire SPI with an 8-bit CRC that operates at clock speeds of up to 24 MHz (refer the t_1 parameter in Table 15) and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

SPI Write

The input shift register is 32 bits wide, and data is loaded into the device MSB first under the control of SCLK. Data is clocked in on the falling edge of SCLK. Table 32 shows the structure of an SPI write frame.

Table 32. Writing to a Register

MSB		LSB
[D31:D24]	[D23:D8]	[D7:D0]
Register address	Data	CRC

SPI Read

Two SPI frames are required to read a register location. In the first frame, the address of the register to be read is written to the READ_SELECT register. Table 33 shows the structure of the first SPI frame.

Table 33. First Frame of a Readback Sequence

MSB		LSB
[D31:D24]	[D23:D8]	[D7:D0]
0x64	Readback address	CRC

The second SPI frame consists of either a no operation (NOP) command or a write to any other register. The data is shifted out, MSB first, on the SDO pin.

- The MSB (Bit 31) is always set to 1 to allow the SPI main to detect if the SDO line is stuck low. This MSB is timed off the falling $\overline{SYNC}$ edge. All other bits are clocked out on the SCLK rising edge.
- The contents of the selected register are available in Bits[D23:D8].
- Bits[D30:D24] provide status information on the SDO pin. The contents of these bits is determined by setting the SPI_RD_RET_INFO bit in the READ_SELECT register. Table 34 and Table 35 show the content available for each SPI_RD_RET_INFO setting.
- An 8-bit CRC is returned in Bits[D7:D0].

Figure 59 shows the timing diagram of the two-stage readback.

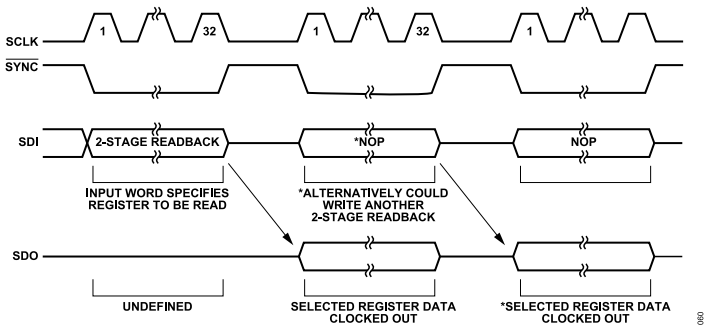


Figure 59. 2-Stage Readback Timing Diagram

THEORY OF OPERATION

Table 34. SDO Contents for a Read Operation When the SPI_RD_RET_INFO Bit = 0

MSB			LSB
D31	**[D30:D24]**	**[D23:D8]**	**[D7:D0]**
1	READBACK_ADDR[6:0]	Read data	CRC

Table 35. SDO Contents for a Read Operation When the SPI_RD_RET_INFO Bit = 1

MSB									LSB
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**[D23:D8]**	**[D7:D0]**
1	0	ALERT	ADC_DATA_RDY	HART_ALERT	0	0	DIN_COMP_OUT	Read data	CRC

THEORY OF OPERATION

Auto Readback

Auto readback allows the user to read from the same register during every SPI transaction. To enable auto readback, set the AUTO_RD_EN bit in the READ_SELECT register. If auto readback is enabled, the contents of the address written to the READBACK_ADDR bits are output on the SDO lines during each SPI transfer.

Burst Read Mode

The AD74115H incorporates a burst read mode that allows sequential reading of multiple registers on the SDO pin as long as there are sufficient SCLKs.

To read back data from multiple registers, the $\overline{\text{SYNC}}$ line must be kept low after the second frame of a 2-stage readback (see the SPI Read section). The AD74115H increments through the register addresses clocking out the 32-bit contents until the $\overline{\text{SYNC}}$ pin is returned high. An SPI_ERR error is reported if the transaction does not end with 32 + (n × 24) SCLK rising edges, where n is the number of transactions.

Here is an example of how to complete a repeated burst read of the two ADC result registers:

1. Enable auto readback (to allow the SDO to return the register address in each SPI transaction).
2. Set the READBACK_ADDR bits in the READ_SELECT register to 0x44 to read the first of the ADC results registers.
3. Provide a NOP command. The contents of the ADC_RESULT1 register are clocked out on the SDO pin, along with the CRC
4. Keep the $\overline{\text{SYNC}}$ pin low to provide an additional 24 clocks to allow for the 16 bits of data from the ADC_RESULT2 register to be clocked out along with the CRC.
5. Return $\overline{\text{SYNC}}$ high.
6. To continue reading from these registers, repeat from Step 3.

Figure 60 shows the contents on the SDO line when burst reading the ADC results registers. The data appearing on the SDO includes 7 bits of the register address (when the SPI_RD_RET_INFO is set to 0), the 16-bit data of ADC_RESULT1, and the 8-bit CRC. When the $\overline{\text{SYNC}}$ pin is kept low and the clocks are applied, the data from the next sequential address (ADC_RESULT2) is clocked out.

A register can be removed from the burst read sequence by deselecting it in the BURST_READ_SEL register.

If a burst read is started at the HART_RX register and the $\overline{\text{SYNC}}$ pin is kept low for multiple reads, the HART_RX register is read continuously. The register address is not incremented in this instance.

Writes to the register map are not supported in streaming mode.

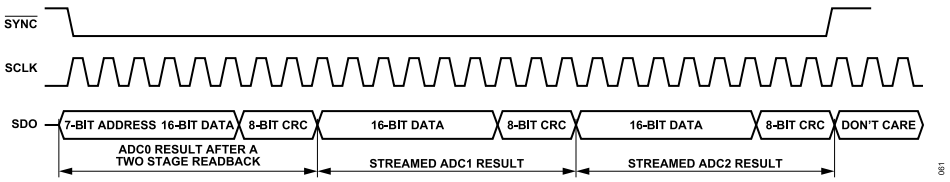


Figure 60. Burst Read Mode SDO Contents

THEORY OF OPERATION

SPI CRC

To ensure that data is received correctly in noisy environments, the AD74115H has a CRC implemented in the SPI. This CRC is based on an 8-bit CRC. The device controlling the AD74115H generates an 8-bit frame check sequence using the following polynomial:

$C(x) = x^8 + x^2 + x^1 + 1$

This frame check sequence is added to the end of the data-word, and the 32-bit data-word is sent to the AD74115H before taking the $\overline{\text{SYNC}}$ pin high.

A frame 32 bits wide containing the 24 data bits and 8 CRC bits must be supplied by the user. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the SPI_ERR status bit in the ALERT_STATUS register is asserted, and the $\overline{\text{ALERT}}$ pin goes low.

An 8-bit CRC is also provided with the data read during a register readback that can be used by the host microcontroller to verify that there are no SPI errors during the read transaction.

Clear the SPI_ERR bit in the ALERT_STATUS register by setting it to 1. Once the alert bit clears, the $\overline{\text{ALERT}}$ pin is deasserted (assuming that there are no other active alerts). The SPI CRC error can be masked by writing to the relevant bit in the ALERT_MASK register.

SPI SCLK Count Feature

An SCLK count feature is built into the SPI diagnostics. Only SPI frames with exactly 32 SCLK falling edges are accepted by the SPI as a valid write. In burst read mode, the number of SCLK rising edges must equal 32 + (n × 24), where n is the number of transactions.

SPI frames of lengths other than the valid cases previously listed are ignored, and the SPI_ERR bit asserts in the ALERT_STATUS register. Mask the SPI_ERR bit via the ALERT_MASK register.

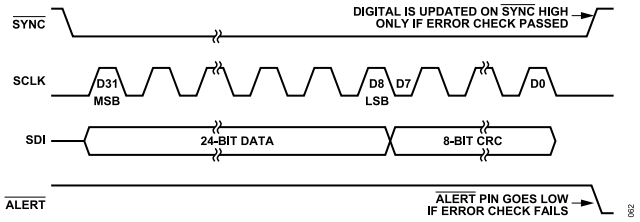


Figure 61. CRC Timing

APPLICATIONS INFORMATION

POWER AND ISOLATION

The AD74115H is designed to operate with a companion power and isolation chip. The ADP1034 provides programmable power control (PPC) to the analog supply (AVDD) so that V_{AVDD} can be software controlled. The ADP1034 also provides fixed power supply voltages to the following AD74115H supply pins: AVSS, AVCC, and DVCC.

The ADP1034 is controlled by the AD74115H via the PPC_CTRL pin using an OWSI. The host controller issues commands to adjust the AVDD supply voltage to the PPC_TX register. In turn, the AD74115H passes the required V_{AVDD} changes to the ADP1034 using the OWSI. Once the ADP1034 receives a command to modify V_{AVDD}, it updates the V_{AVDD} accordingly.

Choose the PPC_TX register code based on the following equation:

$$PPC\_CODE = 252 \times \left(\frac{V_{AVDD}}{V_{AVDD\_MAX}}\right) - 1$$

where:
PPC_CODE is the code that must be programmed to the PPC_TX register for the desired V_{AVDD} value.
V_{AVDD} is the desired A_{VDD} supply voltage.
V_{AVDD_MAX} is the maximum voltage that can be generated by the ADP1034 with the selected feedback resistors. Refer to the ADP1034 data sheet for more information.

The AVDD supply from the ADP1034 can be dynamically changed as the load requirement and selected use case changes. Any changes must be done in a coordinated manner. If the voltage on the I/OP screw terminal is expected to increase due to a change in conditions, V_{AVDD} must be adjusted first. If the voltage on the I/OP screw terminal is expected to decrease due to the change in conditions, V_{AVDD} must be adjusted after the change in load, current, or selected use case.

The diagnostics function can confirm that the voltage is set on the AVDD pin. Select AVDD in one of the available diagnostics in the DIAG_ASSIGN register. Enable an ADC conversion using the ADC_CONFIG register and read the diagnostics result using the relevant ADC_DIAG_RESULTx register.

The ADP1034 provides digital isolation to the AD74115H SPI pins (SCLK, $\overline{SYNC}$, SDO, and SDI). Isolation is available for two other digital output pins and one digital input pin. The block diagram in Figure 63 shows that the $\overline{RESET}$, $\overline{ADC\_RDY}$, and $\overline{ALERT}$ pins are isolated using the ADP1034.

Refer to the ADP1034 data sheet for more information.

One-Wire Serial Interface

Programmable power control is implemented via an OWSI between the AD74115H and the ADP1034.

The AD74115H acts as the OWSI main, using the PPC_CTRL pin. An OWSI transaction requires a number of elements, as shown in Figure 62. OWSI timing specifications are listed in Table 16. The OWSI frame is broken into bit periods. Each start event, data bit, and acknowledge (ACK) bit occurs within a bit period, and each timing specification is defined from the start of that bit period.

A start sequence is defined by two successive rising edge pulses. Once the start command is transmitted, 16 data bits follow to make up the address, data, and CRC bits. Finally, an acknowledge sequence is required from the OWSI subordinate. The acknowledge is comprised of two bits: an ACK bit and a parity bit.

The AD74115H pulls the OWSI bus high at the start of the ACK and parity bit periods. The OWSI bus is sampled by the AD74115H for a fixed time during the ACK and parity bits during which the OWSI subordinate can drive the bus low. Refer to Figure 3 for a detailed view of the OWSI timing and to Table 16 for the appropriate timing specifications.

During a successful transaction, the OWSI subordinate remains high during the ACK bit and drives the bus low during the parity bit.

If the transaction is not successful, the OWSI subordinate drives the bus low during the ACK bit and remains high during the parity bit.

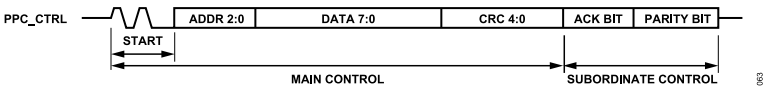


Figure 62. OWSI Write with Acknowledge

APPLICATIONS INFORMATION

OWSI CRC

To ensure that data is received correctly in noisy environments, the AD74115H has a CRC implemented in the OWSI. This CRC is based on a 5-bit CRC. The AD74115H generates a 5-bit frame check sequence using the following polynomial:

$C(x) = x^5 + x^2 + 1$

This 5-bit frame check sequence is added to the end of the 11-bit data-word, and the full 16-bit word is sent to the subordinate device before expecting an acknowledge sequence. If the corresponding CRC check on the subordinate device is valid, the subordinate responds with an acknowledge sequence.

If the CRC check on the subordinate device is not valid, the no acknowledge (NOACK) sequence is issued and the PPC_TX_ACK_ERR bit is asserted in the PPC_ACTIVE register. The PPC_ERR bit is also asserted in the ALERT_STATUS register.

If the CRC check fails, the data is ignored, the PPC_ERR status bit in the ALERT_STATUS register is asserted, and the $\overline{\text{ALERT}}$ pin goes low. The PPC_TX_ACK_ERR is also asserted in the PPC_ACTIVE register.

Clear the PPC_ERR bit (ALERT_STATUS register) by writing a 1, which returns the $\overline{\text{ALERT}}$ pin high (assuming that there are no other active alerts). The PPC_ERR error bit can be masked by writing to the relevant bit in the ALERT_MASK register.

SYSTEM LEVEL BLOCK DIAGRAM

Figure 63 shows the connectivity between the AD74115H and the ADP1034. Figure 63 shows a fully isolated solution for a single-channel software configurable input and output. The V_{AVDD}, V_{AVCC}, V_{DVCC}, and V_{AVSS} supply voltages for the AD74115H are provided by the ADP1034. The AVDD supply voltage can be dynamically controlled from the host controller using the programmable power control function. Refer to the Power and Isolation section for more information on the programmable power control feature using the ADP1034.

The output power available from the ADP1034 is dependent on the input supply voltage to the VINP pin of the ADP1034. The total power required to be delivered to the AD74115H and to the end load must be considered when choosing the system supply voltage. Refer to the ADP1034 for more information on power delivery.

The connectivity shown in Figure 63 allows the AD74115H to operate in bipolar mode with all of the modes of operation of the device that can be delivered on two screw terminals, including HART communications. An external field supply is only required if digital output currents greater than 100 mA are required with this configuration. The SENSE_EXT1 and SENSE_EXT2 pins on the AD74115H can also be connected to additional screw terminals for 3-wire and 4-wire measurements, if required.

APPLICATIONS INFORMATION

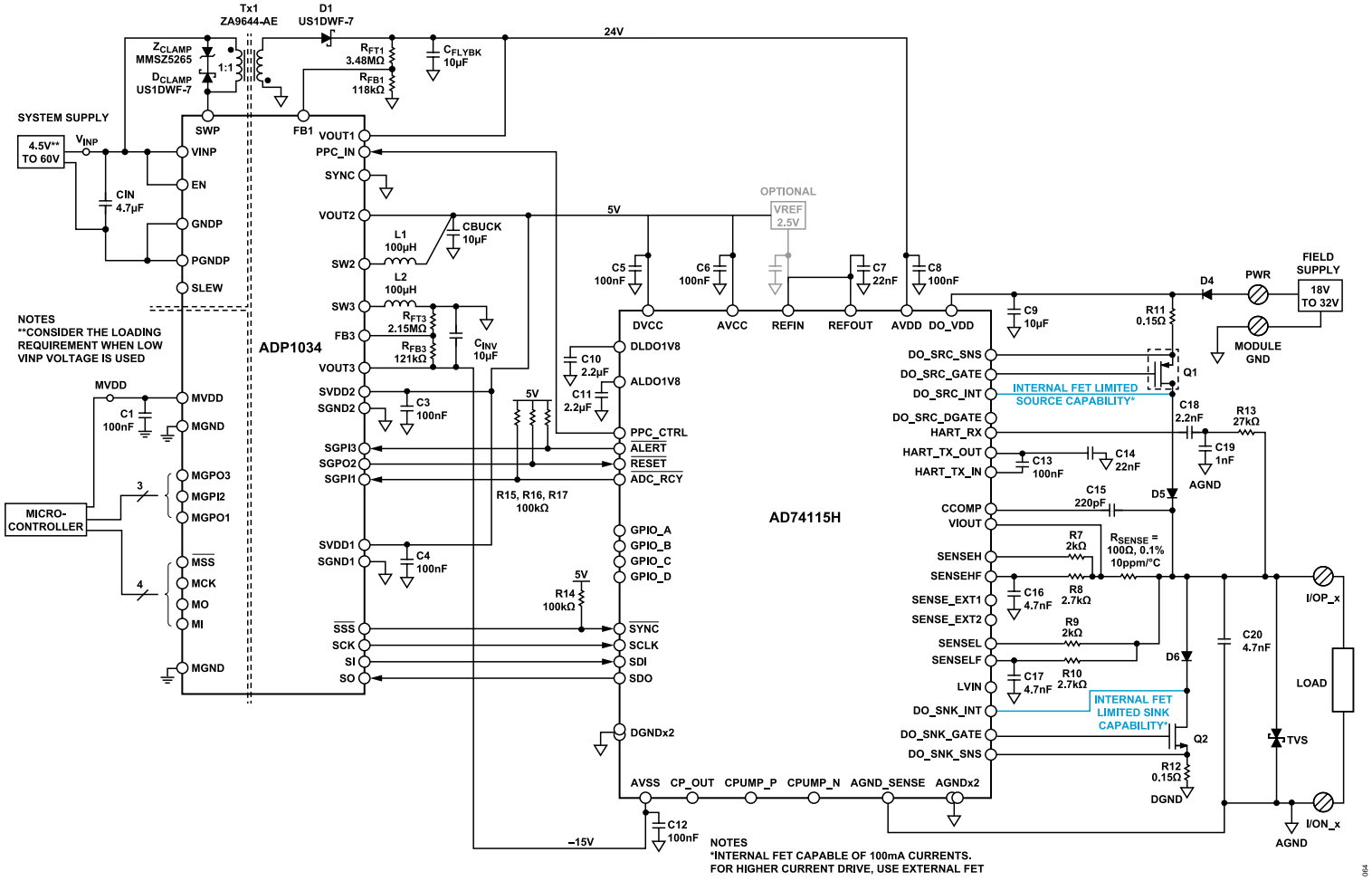


Figure 63. AD74115H and ADP1034 System Level Diagram

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

Table 36 lists the external components that are recommended to operate the AD74115H.

Table 36. External Components

Component	Value			Voltage Rating (V)	Suggested Component[1]	Notes/Comments
	Min	Typical	Max			
Decoupling						
AVDD Decoupling		10 µF		50	Generic	
		0.1 µF		50	Generic	
AVSS Decoupling		10 µF		50[2]	Generic	
		100 nF		50[1]	Generic	
AVCC Decoupling		10 µF		16	Generic	
		100 nF			Generic	
DVCC Decoupling		10 µF		16	Generic	
		0.1 µF		16	Generic	
DO_VDD		10 µF		100	Generic	
ALDO1V8 Decoupling	1 µF	2.2 µF		6.3	GRM21BR70J225MA01	
DLDO1V8 Decoupling	1 µF	2.2 µF		6.3	GRM21BR70J225MA01	
REFOUT Decoupling		22.0 nF	50 nF	6.3	Generic	
Charge Pump						When using the charge pump, connect CP_OUT to AVSS.
Fly Capacitor		330 nF		10	GRM188R71A334KA61	Connect this capacitor between the CPUMP_P and CPUMP_N pins.
Analog Input and Output						
CCOMP Pin Compensation		220 pF		100	Generic	This pin is recommended for a total C_{LOAD} > 14 nF and tied between the CCOMP pin and the I/OP screw terminal.
SENSEHF Filter Capacitor[3]		4.7 nF		100	Generic	
SENSEHF Filter Resistor[3]		2.7 kΩ		Generic	Generic	1% accuracy.
SENSELF Filter Capacitor[3]		4.7 nF		100	Generic	
SENSELF Filter Resistor[3]		2.7 kΩ		Generic	Generic	1% accuracy.
SENSEH Precision		2 kΩ		Generic	Generic	The SENSEH resistor accuracy directly affects RTD specifications.
SENSEL		2 kΩ		Generic	Generic	1% accuracy.
R_{SENSE}		100 Ω		Generic	Generic	R_{SENSE} accuracy directly affects current output, current input, and RTD accuracy.
Screw Terminal						
Load Capacitor		4.7 nF		100	Generic	
36 V TVS				36	SMBJ36CA	
HART						See Figure 52 for implementation.
HART Coupling Capacitor		100 nF		6.3	Generic	This capacitor is tied between HART_TX_IN and HART_TX_OUT.
HART_TX_OUT Capacitor		22 nF		6.3	Generic	This ceramic capacitor is tied between HART_TX_OUT and ground.
HART_RX Band-Pass Filter		27 kΩ		Generic	Generic	
		1 nF		100	Generic	
		2.2 nF		100	Generic	

APPLICATIONS INFORMATION

Table 36. External Components

Component	Value			Voltage Rating (V)	Suggested Component[1]	Notes/Comments
	Min	Typical	Max			
Digital Output						
External FETs				Generic	Generic	
PFET for Sourcing Only				100	Si7113ADN	Suitable for sourcing designs.
NFET for Sinking Only				100	SiA416DJ	Suitable for sinking designs.
External Sense Resistor		0.15 Ω		Generic	Generic	Choose the R_{SENSE} value based on the desired current resolution and range.
Smart Diode FET				100	Si7113ADN	
Smart Diode 5 V Zener				Generic	Generic	
Smart Diode Resistor		10 kΩ		Generic	Generic	
Blocking Diode		1 A		Generic	MSE1PB	
High Voltage Auxiliary Inputs						
SENSE_EXT1						
36 V TVS				Generic	SMBJ36CA	
Filter Resistor[3, 4]		2.7 kΩ		Generic	Generic	Optional.
Filter Capacitor[3, 4]		4.7 nF		100	Generic	Optional.
SENSE_EXT2						
36 V TVS				Generic	SMBJ36CA	
Filter Resistor[3, 4]		2.7 kΩ		Generic	Generic	Optional.
Filter Capacitor[3, 4]		4.7 nF		Generic	Generic	Optional.

1 Use recommended components or ones that are similar.

2 Voltage rating can be reduced if charge pump is used instead of the external supply.

3 Antialiasing filter values provide a compromise in performance for all use cases and conditions. These values can be adjusted to optimize for specific design conditions.

4 Not recommended for 3-wire and 4-wire resistance measurements.

BOARD DESIGN AND LAYOUT CONSIDERATIONS

This section outlines the critical board design and layout considerations for the AD74115H.

To guarantee stability for the SENSEL pin, limit the capacitance to ground between the SENSEL pin and the required 2 kΩ resistor to <10 pF.

To guarantee stability for the SENSEH pin, limit the capacitance to ground between the SENSEH pin and the required 2 kΩ resistor to <10 pF.

To guarantee stability for the CCOMP pin, limit the capacitance to ground between the CCOMP pin and the C_{COMP} capacitor (if required) to <10 pF.

For correct operation of the programmable power control interface, limit the capacitance to ground on the PPC_CTRL pin to 30 pF.

To optimize thermal performance, design the AD74115H boards with a minimum of four layers and with multiple thermal vias connecting the paddle to the bottom layer of the board. See the JEDEC JESD-51 specifications for more details. Users are recommended to thermally connect the exposed pad of the AD74115H to the thermal vias.

When grounding the AD74115H pins, it is recommended to connect the AGND pins and DGND pins to a single ground plane. The I/ON screw terminal must also be tied to this ground plane.

Track the SENSEH, SENSEHF, SENSEL, and SENSELF pins directly to the pad of the R_{SENSE} resistor.

Track the DO_SRC_SNS and DO_SNK_SNS pins directly to the pad of the external R_{SET} resistors.

The AGND_SENSE pin senses the voltage at the I/ON screw terminal and provides this voltage as an input to the ADC. It is not recommended to directly connect the AGND_SENSE pin to ground. Instead, users must route a single trace from the AGND_SENSE pin to the I/ON screw terminal. This connection can be done by connecting the AGND_SENSE pin to the I/ON screw terminal on the AD74115H board.

REGISTER MAP

Table 37 summarizes the register map for the AD74115H with information on how to read and write to and from the registers. R indicates read only access, R/W indicates read and write access, R/W1C indicates read, write, or clear, and W indicates write only access.

Table 37. Register Summary

Address	Name	Description	Reset	Access
0x00	NOP	NOP Register	0x0000	R
0x01	CH_FUNC_SETUP	Function Setup Register	0x0000	R/W
0x02	ADC_CONFIG	ADC Configuration Register	0x2400	R/W
0x03	PWR_OPTIM_CONFIG	Power Optimization Configuration Register	0x001F	R/W
0x04	DIN_CONFIG1	Digital Input Configuration Register 1	0x000B	R/W
0x05	DIN_CONFIG2	Digital Input Configuration Register 2	0x0000	R/W
0x06	OUTPUT_CONFIG	Output Configuration Register	0x0000	R/W
0x07	RTD3W4W_CONFIG	3-Wire and 4-Wire RTD Configuration Register	0x0001	R/W
0x08	DO_INT_CONFIG	Digital Output with Internal FET Configuration Register	0x2E00	R/W
0x09	DO_EXT_CONFIG	Digital Output with External FET Configuration Register	0x2E00	R/W
0x0A	I_BURNOUT_CONFIG	Burnout Currents Configuration Register	0x0000	R/W
0x0B	DAC_CODE	DAC Code Register	0x0000	R/W
0x0D	DAC_ACTIVE	DAC Active Code Register	0x0000	R
0x35 to 0x38	GPIO_CONFIGx	GPIO_x Configuration Register	0x0008	R/W
0x39	FET_LKG_COMP	FET Leakage Compensation Register	0x0000	R/W
0x3A	CHARGE_PUMP	Charge Pump Configuration Register	0x0000	R/W
0x3B	ADC_CONV_CTRL	ADC Conversion Control Register	0x0000	R/W
0x3C	DIAG_ASSIGN	Diagnostics Select Register	0x0000	R/W
0x40	DIN_COMP_OUT	Digital Output Level Register	0x0000	R
0x41	ALERT_STATUS	Alert Status Register	0x0001	R/W
0x42	LIVE_STATUS	Live Status Register	0x0000	R/W
0x44	ADC_RESULT1	ADC Conversion 1 Result Register	0x0000	R
0x46	ADC_RESULT2	ADC Conversion 2 Result Register	0x0000	R
0x53 to 0x56	ADC_DIAG_RESULTx	Diagnostic Results Registers	0x0000	R
0x57	DIN_COUNTER	Digital Input Counter Register	0x0000	R
0x5B	SUPPLY_ALERT_STATUS	Supply Alert Status Register	0x0000	R/W
0x5F	ALERT_MASK	Alert Mask Register for ALERT_STATUS	0x0000	R/W
0x60	SUPPLY_ALERT_MASK	Alert Mask Register for SUPPLY_ALERT_STATUS	0x0000	R/W
0x64	READ_SELECT	Readback Select Register	0x0000	R/W
0x65	BURST_READ_SEL	Select the Registers Read in Burst Mode	0x03FF	R/W
0x66	PPC_TX	PPC Transmit Register	0x00FF	R/W
0x6E	PPC_ACTIVE	PPC Status Register	0x00FF	R
0x77	THERM_RST	Thermal Reset Enable Register	0x0000	R/W
0x78	CMD_KEY	Command Register	0x0000	W
0x79 to 0x7A	SCRATCH	Scratch or Spare Register	0x0000	R/W
0x7B	SILICON_REV	Silicon Revision Register	0x0001	R
0x7C	SILICON_ID0	Silicon ID 0	0x0000	R
0x7D	SILICON_ID1	Silicon ID 1	0x0000	R
0x7E	SILICON_ID2	Silicon ID 2	0x0000	R
0x7F	SILICON_ID3	Silicon ID 3	0x0000	R

Table 38 summarizes the HART register map with information on how to read and write to and from the registers. R indicates read only access, R/W indicates read and write access, and W indicates write only access.

REGISTER MAP

Table 38. HART Register Summary

Address	Name	Description	Reset	Access
0x80	HART_ALERT_STATUS	HART Communications Alert Register	0x0020	R/W
0x81	HART_RX	HART Communications Receive Register	0x0000	R
0x82	HART_TX	HART Communications Transmit Register	0x0000	W
0x83	HART_FCR	FIFO Control Register	0x08C1	R/W
0x84	HART_MCR	HART UART Transmit Control Register	0x0000	R/W
0x85	HART_RFC	Receive FIFO Byte Count Register	0x0000	R
0x86	HART_TFC	Transmit FIFO Byte Count Register	0x0000	R
0x87	HART_ALERT_MASK	HART Communications Alert Mask Register	0x1EFF	R/W
0x88	HART_CONFIG	HART Support Configuration Register	0xC430	R/W
0x89	HART_EVDET_COUNT	HART Event Detected Count Register	0x0000	R

SOFTWARE CONFIGURABLE INPUT AND OUTPUT REGISTERS

Use the following registers to configure the input and output functionality and to take measurements from the AD74115H.

NOP Register

Address: 0x00, Reset: 0x0000, Name: NOP

Read only register. Writing to this register results in a no operation (NOP) command.

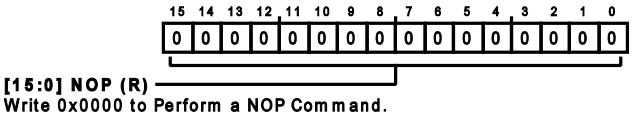


Table 39. Bit Descriptions for NOP

Bits	Bit Name	Description	Reset	Access
[15:0]	NOP	Write 0x0000 to Perform a NOP Command.	0x0	R

Function Setup Register

Address: 0x01, Reset: 0x0000, Name: CH_FUNC_SETUP

Write to this register to select the function. When CH_FUNC_SETUP is programmed, some fields in the ADC_CONFIG, OUTPUT_CONFIG, DIN_CONFIG1, DIN_CONFIG2 and RTD3W4W_CONFIG registers can change.

When changing the function, the high impedance function must be programmed first, before programming the new function.

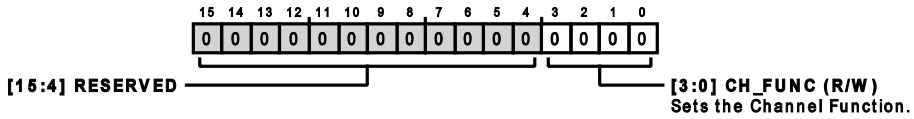


Table 40. Bit Descriptions for CH_FUNC_SETUP

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	CH_FUNC	Sets the Channel Function. The default state on initial power-up or reset is high impedance. Values other than those listed as follows select the high impedance function. 0000: high impedance. The ADC is functional in this mode. 0001: voltage output. Force voltage, measure current. 0010: current output. Force current, measure voltage.	0x0	R/W

REGISTER MAP

Table 40. Bit Descriptions for CH_FUNC_SETUP

Bits	Bit Name	Description	Reset	Access
		0011: voltage input. Measures the voltage between the I/OP and I/ON screw terminals. 0100: current input, externally powered. 0101: current input, loop powered. 0110: 2-wire resistance measurement. 0111: 3-wire or 4-wire resistance measurement. 1000: digital input logic. 1001: digital input, loop powered. 1010: current output with HART. 1011: current input, externally powered with HART. 1100: current input, loop powered with HART.		

ADC Configuration Register

Address: 0x02, Reset: 0x2400, Name: ADC_CONFIG

This register selects the ADC configuration for the input and output channel. Disable ADC conversions before making any changes to the ADC_CONFIG register.

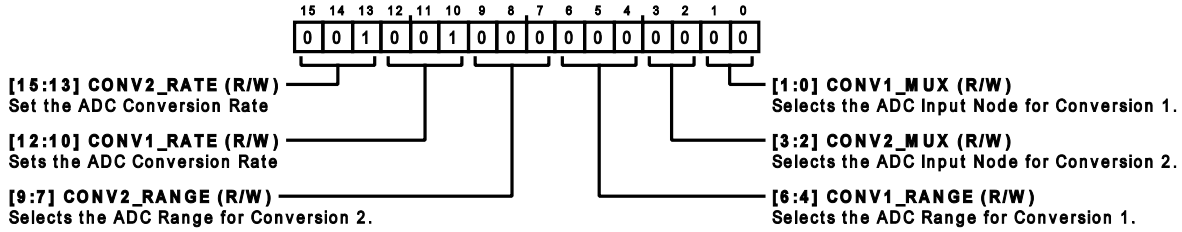


Table 41. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
[15:13]	CONV2_RATE	Set the ADC Conversion Rate. Values other than those listed in this table select the 20 SPS rate. 000: 10 SPS. Provides 50 Hz and 60 Hz noise rejection. 001: 20 SPS. Provides 50 Hz and 60 Hz noise rejection. 010: 1.2 kSPS. 011: 4.8 kSPS. 100: 9.6 kSPS.	0x1	R/W
[12:10]	CONV1_RATE	Sets the ADC Conversion Rate. Values other than those listed in this table select the 20 SPS rate. 000: 10 SPS. Provides 50 Hz and 60 Hz noise rejection. 001: 20 SPS. Provides 50 Hz and 60 Hz noise rejection. 010: 1.2 kSPS. 011: 4.8 kSPS. 100: 9.6 kSPS.	0x1	R/W
[9:7]	CONV2_RANGE	Selects the ADC Range for Conversion 2. Values outside of those listed in this table select the 0 V to 12 V range. 000: 0 V to 12 V. 001: −12 V to +12 V. 010: −2.5V to +2.5 V. 011: −2.5V to 0 V. 100: 0 V to 2.5 V. 101: 0 V to 0.625 V. 110: −104 mV to +104 mV.	0x0	R/W

REGISTER MAP

Table 41. Bit Descriptions for ADC_CONFIG

Bits	Bit Name	Description	Reset	Access
[6:4]	CONV1_RANGE	Selects the ADC Range for Conversion 1. Values outside of those listed in this table select the 0 V to 12 V range. Note that these bits can change when the CH_FUNC_SETUP register is programmed. 000: 0 V to 12 V. 001: −12 V to +12 V. 010: −2.5V to +2.5 V. 011: −2.5V to 0 V. 100: 0 V to 2.5 V. 101: 0 V to 0.625 V. 110: −104 mV to +104 mV.	0x0	R/W
[3:2]	CONV2_MUX	Selects the ADC Input Node for Conversion 2. 00: SENSE_EXT1 to AGND_SENSE. 01: SENSE_EXT2 to AGND_SENSE. 10: SENSE_EXT2 to SENSE_EXT1. 11: AGND to AGND.	0x0	R/W
[1:0]	CONV1_MUX	Selects the ADC Input Node for Conversion 1. These bits can change when the CH_FUNC_SETUP register is programmed. 00: SENSELF to AGND_SENSE. 01: SENSEHF to SENSELF. 10: SENSE_EXT2 to SENSE_EXT1. 11: SENSELF to SENSE_EXT1.	0x0	R/W

Power Optimization Configuration Register

Address: 0x03, Reset: 0x001F, Name: PWR_OPTIM_CONFIG

This register contains some settings to allow for power optimization of the channel.

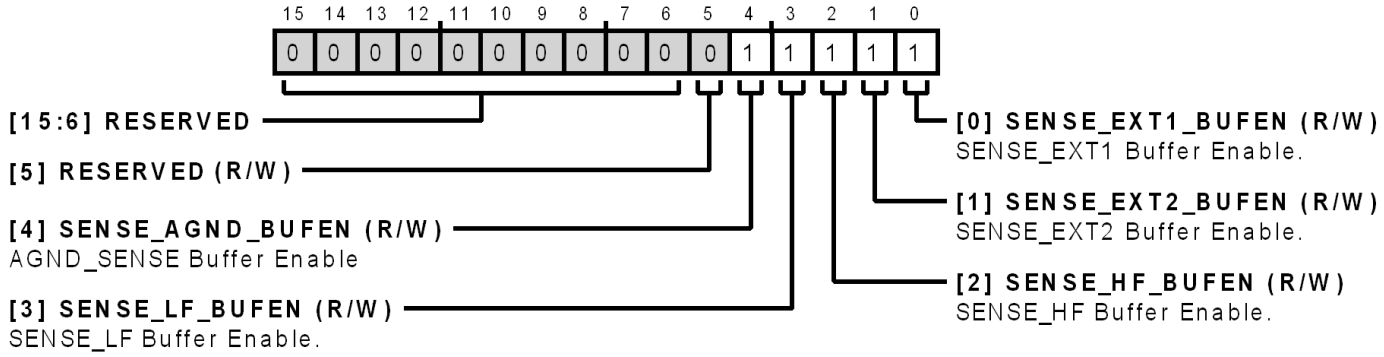


Table 42. Bit Descriptions for PWR_OPTIM_CONFIG

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
4	SENSE_AGND_BUFEN	AGND_SENSE Buffer Enable. 0: the sense AGND buffer is in low power mode. 1: the sense AGND buffer is in full power mode.	0x1	R/W
3	SENSE_LF_BUFEN	SENSE_LF Buffer Enable. 0: the SENSE_LF buffer is in low power mode. 1: the SENSE_LF buffer is in full power mode.	0x1	R/W

REGISTER MAP

Table 42. Bit Descriptions for PWR_OPTIM_CONFIG

Bits	Bit Name	Description	Reset	Access
2	SENSE_HF_BUFEN	SENSE_HF Buffer Enable. 0: the SENSE_HF buffer is in low power mode. 1: the SENSE_HF buffer is in full power mode.	0x1	R/W
1	SENSE_EXT2_BUFEN	SENSE_EXT2 Buffer Enable. 0: the SENSE_EXT2 buffer is in low power mode. 1: the SENSE_EXT2 buffer is in full power mode.	0x1	R/W
0	SENSE_EXT1_BUFEN	SENSE_EXT1 Buffer Enable. 0: the SENSE_EXT1 buffer is in low power mode. 1: the SENSE_EXT1 buffer is in full power mode.	0x1	R/W

Digital Input Configuration Register 1

Address: 0x04, Reset: 0x000B, Name: DIN_CONFIG1

This register (along with DIN_CONFIG2) is used to configure the digital input function of the channel.

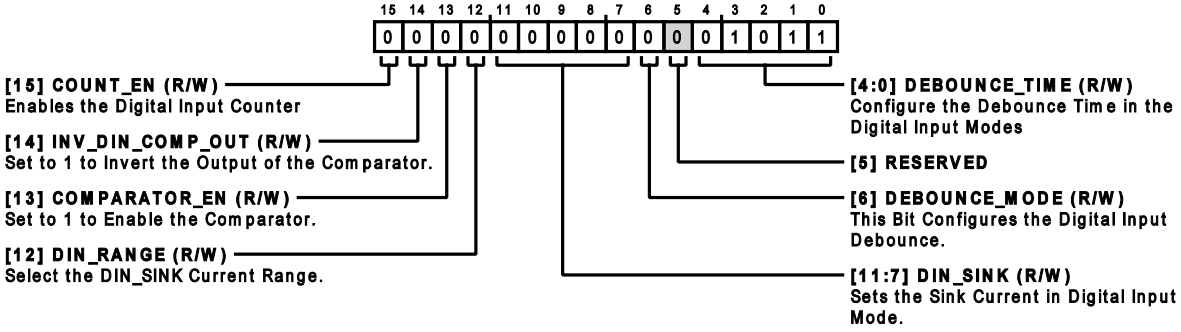


Table 43. Bit Descriptions for DIN_CONFIG1

Bits	Bit Name	Description	Reset	Access
15	COUNT_EN	Enables the Digital Input Counter. If INV_DIN_COMP_OUT is 0, the positive edges of the debounced inputs are counted. If INV_DIN_COMP_OUT is 1, the negative edges of debounced inputs are counted. The count is reflected in the DIN_COUNTER register.	0x0	R/W
14	INV_DIN_COMP_OUT	Set to 1 to Invert the Output of the Comparator.	0x0	R/W
13	COMPARATOR_EN	Set to 1 to Enable the Comparator. This bit can change when the CH_FUNC_SETUP register is programmed.	0x0	R/W
12	DIN_RANGE	Select the DIN_SINK Current Range. 0: Range 0. Range from 0 mA to 3.7 mA in steps of 120 µA and ~2 kΩ of series resistance. 1: Range 1. Range from 0 mA to 7.4 mA in steps of 240 µA and ~1 kΩ of series resistance.	0x0	R/W
[11:7]	DIN_SINK	Sets the Sink Current in Digital Input Mode. Configure these bits to program the current sink as defined by the DIN_RANGE bit. Set DIN_SINK to 0x0 to switch off the current sink. Note that these bits are set to 0 when the corresponding CH_FUNC_SETUP register is written, irrespective of the function.	0x0	R/W
6	DEBOUNCE_MODE	This Bit Configures the Digital Input Debounce. 0: Debounce Mode 0. Integrator method is used. A counter increments when the signal is asserted and decrements when the signal is deasserted. 1: Debounce Mode 1. A simple counter increments while a signal is asserted and resets when the signal deasserts.	0x0	R/W
5	RESERVED	Reserved.	0x0	R
[4:0]	DEBOUNCE_TIME	Configure the Debounce Time in the Digital Input Modes. Reset value: 240 µs. Set the bits to 0x0 to bypass the debounce circuit.	0xB	R/W

REGISTER MAP

Digital Input Configuration Register 2

Address: 0x05, Reset: 0x0000, Name: DIN_CONFIG2

This register (along with DIN_CONFIG1) is used to configure the digital input function of the channel.

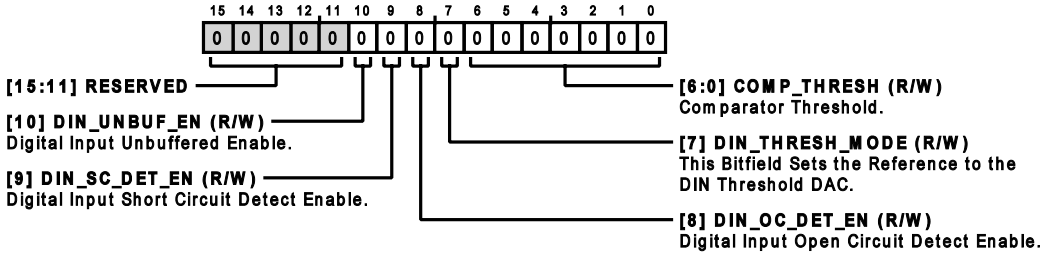


Table 44. Bit Descriptions for DIN_CONFIG2

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	DIN_UNBUF_EN	Digital Input Unbuffered Enable.	0x0	R/W
9	DIN_SC_DET_EN	Digital Input Short Circuit Detect Enable (when configured for IEC 61131 Type 3D diagnostics, as described in the Digital Input Logic section).	0x0	R/W
8	DIN_OC_DET_EN	Digital Input Open Circuit Detect Enable (when configured for IEC 61131 Type 3D diagnostics, as described in the Digital Input Logic section).	0x0	R/W
7	DIN_THRESH_MODE	This Bitfield Sets the Reference to the DIN Threshold DAC. 0: the threshold scales with AVDD. The threshold range is from −0.96 × AVDD to AVDD. 1: fixed threshold. Threshold is from −19 V to +30 V.	0x0	R/W
[6:0]	COMP_THRESH	Comparator Threshold. DIN comparator threshold.	0x0	R/W

Output Configuration Register

Address: 0x06, Reset: 0x0000, Name: OUTPUT_CONFIG

This register configures the output settings of the channel.

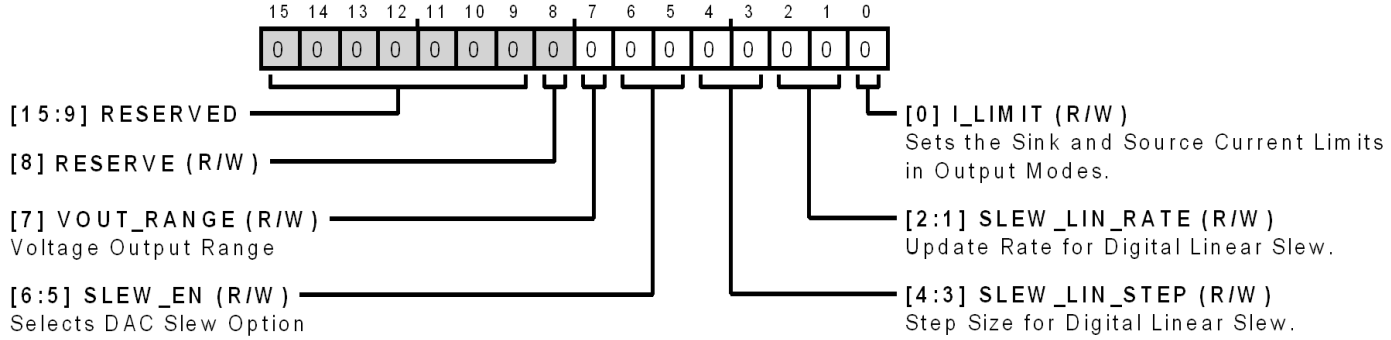


Table 45. Bit Descriptions for OUTPUT_CONFIG

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
7	VOUT_RANGE	Voltage Output Range. 0: 0 to 12 V. 1: −12 V to +12 V.	0x0	R/W
[6:5]	SLEW_EN	Selects DAC Slew Option.	0x0	R/W

REGISTER MAP

Table 45. Bit Descriptions for OUTPUT_CONFIG

Bits	Bit Name	Description	Reset	Access
		00: slewing disabled. Slewing stops immediately when disabled, there are no further updates to the DAC code. 01: enable linear slew on the DAC output. 10: enable HART compliant slewing on the DAC output.		
[4:3]	SLEW_LIN_STEP	Step Size for Digital Linear Slew. 00: voltage step size of 0.8% of full-scale DAC voltage. 01: voltage step size of 1.5% of full-scale DAC voltage. 10: voltage step size of 6.1% of full-scale DAC voltage. 11: voltage step size of 22.2% of full-scale DAC voltage.	0x0	R/W
[2:1]	SLEW_LIN_RATE	Update Rate for Digital Linear Slew. 00: update at a rate of 4 kHz. 01: update at a rate of 64 kHz. 10: update at a rate of 150 kHz. 11: update at a rate of 240 kHz.	0x0	R/W
0	I_LIMIT	Sets the Sink and Source Current Limits in Output Modes. These are typical current limits. 0: Current-Limit 0. V_{OUT}: 32 mA source or sink. I_{OUT}: 4 mA sink. 1: Current-Limit 1. V_{OUT}: 16 mA source or sink. I_{OUT}: 1 mA sink.	0x0	R/W

3-Wire and 4-Wire RTD Configuration Register

Address: 0x07, Reset: 0x0001, Name: RTD3W4W_CONFIG

This register configures the 3-wire and 4-wire RTD measurements.

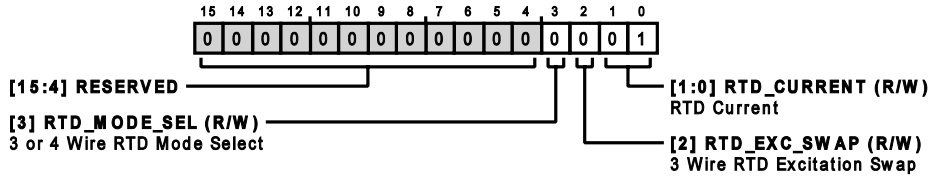


Table 46. Bit Descriptions for RTD3W4W_CONFIG

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	RTD_MODE_SEL	3-Wire or 4-Wire RTD Mode Select. 0: 3-Wire RTD Mode. 1: 4-Wire RTD Mode.	0x0	R/W
2	RTD_EXC_SWAP	3-Wire RTD Excitation Swap. This field is only used for 3-wire RTD.	0x0	R/W
[1:0]	RTD_CURRENT	RTD Current. Values other than those listed as follows select a current of 250 µA. 00: 250 µA. 01: 500 µA. 10: 750 µA. 11: 1 mA.	0x1	R/W

Digital Output with Internal FET Configuration Register

Address: 0x08, Reset: 0x2E00, Name: DO_INT_CONFIG

This register configures the settings for the internal digital output function. When the digital output functionality is enabled, the recommended configuration of the CH_FUNC_SETUP register is to set it to high impedance.

REGISTER MAP

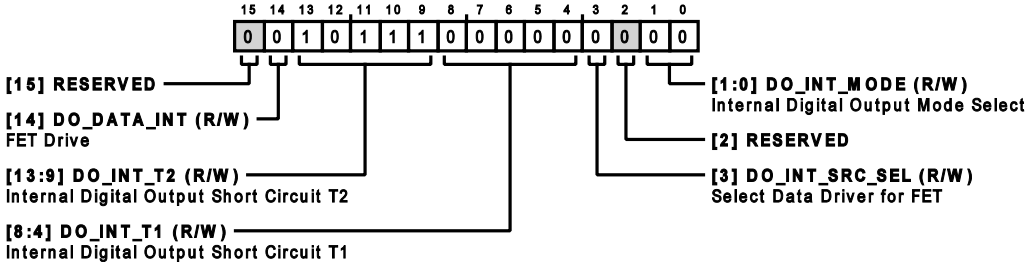


Table 47. Bit Descriptions for DO_INT_CONFIG

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	DO_DATA_INT	FET Drive. 0: source or sink mode, switch off the FET. Push-pull mode: sink current. 1: source or sink mode, switch on the FET. Push-pull mode: source current.	0x0	R/W
[13:9]	DO_INT_T2	Internal Digital Output Short-Circuit T2. Set these bits to program the T2 short-circuit duration. If a short-circuit event duration exceeds this time, the DO_EXT_TIMEOUT alert bit is asserted in the ALERT_STATUS register. Setting this register to 0 results in the minimum timer count and activation of the T2 timer when a short-circuit is detected. 00: T2 18.699 µs. 01: T2 18.699 µs. 02: T2 24.39 µs. 03: T2 32.52 µs. 04: T2 42.276 µs. 05: T2 56.097 µs. 06: T2 75.609 µs. 07: T2 100.812 µs. 08: T2 130.08 µs. 09: T2 180.486 µs. 10: T2 240.648 µs. 11: T2 320.322 µs. 12: T2 420.321 µs. 13: T2 560.157 µs. 14: T2 750.399 µs. 15: T2 1.000803 ms. 16: T2 1.3008 ms. 17: T2 1.800795 ms. 18: T2 2.400789 ms. 19: T2 3.200781 ms. 20: T2 4.200771 ms. 21: T2 5.600757 ms. 22: T2 7.500738 ms. 23: T2 10.000713 ms. 24: T2 13.000683 ms. 25: T2 18.000633 ms. 26: T2 24.000573 ms. 27: T2 32.000493 ms. 28: T2 42.000393 ms. 29: T2 56.000253 ms. 30: T2 100.000626 ms.	0x17	R/W

REGISTER MAP

Table 47. Bit Descriptions for DO_INT_CONFIG

Bits	Bit Name	Description	Reset	Access
		31: T2 infinity.		
[8:4]	DO_INT_T1	Internal Digital Output Short-Circuit T1. Set these bits to program the T1 short-circuit duration. Setting this register to 0 results in the timer being disabled and immediate activation of the T2 timer when a short-circuit is detected. Note T1 is not available in push-pull mode of operation. 00: T1 bypass. 01: T1 18.699 µs. 02: T1 24.39 µs. 03: T1 32.52 µs. 04: T1 42.276 µs. 05: T1 56.097 µs. 06: T1 75.609 µs. 07: T1 100.812 µs. 08: T1 130.08 µs. 09: T1 180.486 µs. 10: T1 240.648 µs. 11: T1 320.322 µs. 12: T1 420.321 µs. 13: T1 560.157 µs. 14: T1 750.399 µs. 15: T1 1.000803 ms. 16: T1 1.3008 ms. 17: T1 1.800795 ms. 18: T1 2.400789 ms. 19: T1 3.200781 ms. 20: T1 4.200771 ms. 21: T1 5.600757 ms. 22: T1 7.500738 ms. 23: T1 10.000713 ms. 24: T1 13.000683 ms. 25: T1 18.000633 ms. 26: T1 24.000573 ms. 27: T1 32.000493 ms. 28: T1 42.000393 ms. 29: T1 56.000253 ms. 30: T1 75.000063 ms. 31: T1 100.000626 ms.	0x0	R/W
3	DO_INT_SRC_SEL	Select Data Driver for FET. 1: the GPIO_x pin is configured to drive the FET. Note that when this bit is set, configure the GPIO_CONFIG2 register as an input to the digital output circuit. 0: direct software control of the FET. When under software control, the FET is controlled via DO_DATA_INT.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	DO_INT_MODE	Internal Digital Output Mode Select. Note that, if the DO_INT_TIMEOUT bit in the ALERT_STATUS register is set, the digital output function disables. The DO_INT_MODE automatically configure to select digital output internal disable mode. When switching between digital output modes, ensure that the digital output internal disable mode is the intermediate step. 00: digital output internal disable. 01: digital output internal source. 10:digital output internal sink. 11: digital output internal push-pull. DO_INT_SRC_SEL determines the data source. A 0 from data source enables the FET sinking current, and a 1 from the data source enables the FET sourcing current.	0x0	R/W

REGISTER MAP

Digital Output with External FET Configuration Register

Address: 0x09, Reset: 0x2E00, Name: DO_EXT_CONFIG

This register configures the settings for the external digital output function. When the digital output functionality is enabled, the recommended configuration of the CH_FUNC_SETUP register is to set it to high impedance.

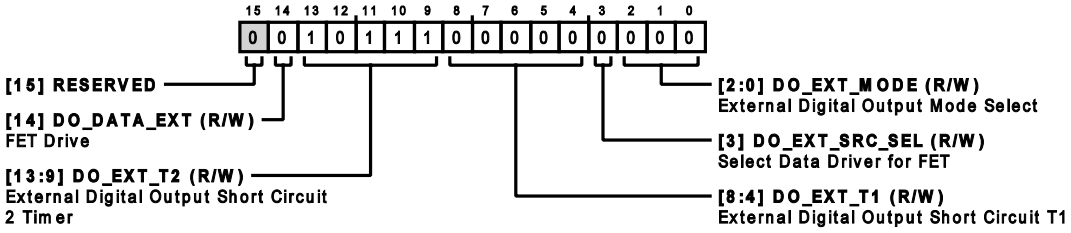


Table 48. Bit Descriptions for DO_EXT_CONFIG

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	DO_DATA_EXT	FET Drive. 0: switch off the FET. 1: switch on the FET.	0x0	R/W
[13:9]	DO_EXT_T2	External Digital Output Short-Circuit 2 Timer. Set these bits to program the T2 short-circuit duration. If a short-circuit event duration exceeds this time, the DO_EXT_TIMEOUT alert bit is asserted in the ALERT_STATUS register. Setting this register to 0 results in the minimum timer count and activation of the T2 timer when a short circuit is detected. Take care when setting T2 to infinity because this can cause thermal damage to the selected external FET. 00: T2 100.812 µs. 01: T2 100.812 µs. 02: T2 100.812 µs. 03: T2 100.812 µs. 04: T2 100.812 µs. 05: T2 100.812 µs. 06: T2 100.812 µs. 07: T2 100.812 µs. 08: T2 130.08 µs. 09: T2 180.486 µs. 10: T2 240.648 µs. 11: T2 320.322 µs. 12: T2 420.321 µs. 13: T2 560.157 µs. 14: T2 750.399 µs. 15: T2 1.000803 ms. 16: T2 1.3008 ms. 17: T2 1.800795 ms. 18: T2 2.400789 ms. 19: T2 3.200781 ms. 20: T2 4.200771 ms. 21: T2 5.600757 ms. 22: T2 7.500738 ms. 23: T2 10.000713 ms. 24: T2 13.000683 ms.	0x17	R/W

REGISTER MAP

Table 48. Bit Descriptions for DO_EXT_CONFIG

Bits	Bit Name	Description	Reset	Access
		25: T2 18.000633 ms. 26: T2 24.000573 ms. 27: T2 32.000493 ms. 28: T2 42.000393 ms. 29: T2 56.000253 ms. 30: T2 100.000626 ms. 31: T2 infinity.		
[8:4]	DO_EXT_T1	External Digital Output Short-Circuit T1. Set these bits to program the T1 short-circuit duration. Setting this register to 0 results in the timer being disabled and immediate activation of the T2 timer when a short circuit is detected. Note T1 is not available in push-pull mode of operation. 00: T1 bypass. 01: T1 100.812 µs. 02: T1 100.812 µs. 03: T1 100.812 µs. 04: T1 100.812 µs. 05: T1 100.812 µs. 06: T1 100.812 µs. 07: T1 100.812 µs. 08: T1 130.08 µs. 09: T1 180.486 µs. 10: T1 240.648 µs. 11: T1 320.322 µs. 12: T1 420.321 µs. 13: T1 560.157 µs. 14: T1 750.399 µs. 15: T1 1.000803 ms. 16: T1 1.3008 ms. 17: T1 1.800795 ms. 18: T1 2.400789 ms. 19: T1 3.200781 ms. 20: T1 4.200771 ms. 21: T1 5.600757 ms. 22: T1 7.500738 ms. 23: T1 10.000713 ms. 24: T1 13.000683 ms. 25: T1 18.000633 ms. 26: T1 24.000573 ms. 27: T1 32.000493 ms. 28: T1 42.000393 ms. 29: T1 56.000253 ms. 30: T1 75.000063 ms. 31: T1 100.000626 ms.	0x0	R/W
3	DO_EXT_SRC_SEL	Select Data Driver for FET. 1: the GPIO_x pin is configured to drive the FET. Note that when this bit is set, configure the GPIO_CONFIG1 register as an input to the digital output circuit. 0: direct software control of the FET. When under software control, the FET is controlled via DO_DATA_EXT.	0x0	R/W
[2:0]	DO_EXT_MODE	External Digital Output Mode Select. Note that, if the DO_EXT_TIMEOUT bit in the ALERT_STATUS register is set, the digital output function disables. The DO_EXT_MODE automatically configures to select digital	0x0	R/W

REGISTER MAP

Table 48. Bit Descriptions for DO_EXT_CONFIG

Bits	Bit Name	Description	Reset	Access
		output external disable mode. When switching between digital output modes, ensure that the digital output external disable mode is the intermediate step. 000: digital output external disable. 001: external source. 010: external sink. 011: external push-pull. DO_EXT_SRC_SEL determines the data source. A 0 from the data source enables the FET sinking, and a 1 from the data source enables the FET sourcing. 100: external source with smart diode.		

Burnout Currents Configuration Register

Address: 0x0A, Reset: 0x0000, Name: I_BURNOUT_CONFIG

This register configures the burnout currents for the VIOUT, SENSE_EXT1, and SENSE_EXT2 pins.

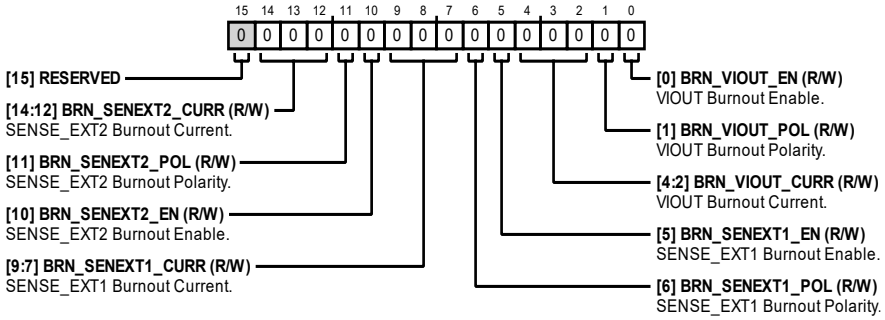


Table 49. Bit Descriptions for I_BURNOUT_CONFIG

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
[14:12]	BRN_SENEXT2_CURR	SENSE_EXT2 Burnout Current. 000: burnout current disabled. 001: 50 nA. 011: 500 nA. 100: 1 µA. 110: 10 µA. Others: reserved	0x0	R/W
11	BRN_SENEXT2_POL	SENSE_EXT2 Burnout Polarity. 0: sinking current. 1: sourcing current.	0x0	R/W
10	BRN_SENEXT2_EN	SENSE_EXT2 Burnout Enable.	0x0	R/W
[9:7]	BRN_SENEXT1_CURR	SENSE_EXT1 Burnout Current. 000: burnout current disabled. 001: 50 nA. 011: 500 nA. 100: 1 µA. 110: 10 µA. Others: reserved	0x0	R/W
6	BRN_SENEXT1_POL	SENSE_EXT1 Burnout Polarity. 0: sinking current. 1: sourcing current.	0x0	R/W

REGISTER MAP

Table 49. Bit Descriptions for I_BURNOUT_CONFIG

Bits	Bit Name	Description	Reset	Access
5	BRN_SENEXT1_EN	SENSE_EXT1 Burnout Enable.	0x0	R/W
[4:2]	BRN_VIOUT_CURR	VIOUT Burnout Current. 000: burnout current disabled. 100: 1 µA. 110: 10 µA. Others: reserved.	0x0	R/W
1	BRN_VIOUT_POL	VIOUT Burnout Polarity. 0: sinking current. 1: sourcing current.	0x0	R/W
0	BRN_VIOUT_EN	VIOUT Burnout Enable.	0x0	R/W

DAC Code Register

Address: 0x0B, Reset: 0x0000, Name: DAC_CODE

This register is used to set the DAC code for the output functions. The DAC_CODE register is not reset by changing channel functions.

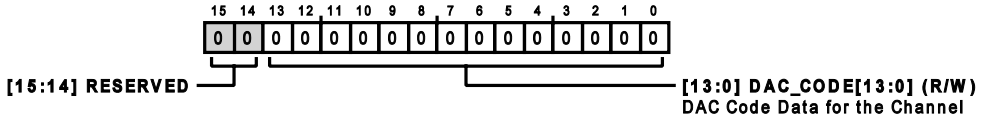


Table 50. Bit Descriptions for DAC_CODE

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
[13:0]	DAC_CODE[13:0]	DAC Code Data for the Channel.	0x0	R/W

DAC Active Code Register

Address: 0x0D, Reset: 0x0000, Name: DAC_ACTIVE

This register displays the current value of the code loaded to the DAC. If slewing is enabled, this register reflects the current slew step.

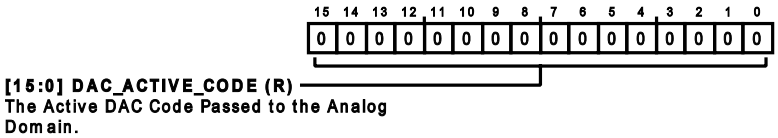


Table 51. Bit Descriptions for DAC_ACTIVE

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_ACTIVE_CODE	The Active DAC Code Passed to the Analog Domain. Current code loaded to the DAC.	0x0	R

GPIO_A Configuration Register

Address: 0x35, Reset: 0x0008, Name: GPIO_CONFIG0

The four GPIO_x registers configure the four GPIO_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP_WK_PD_EN bit.

REGISTER MAP

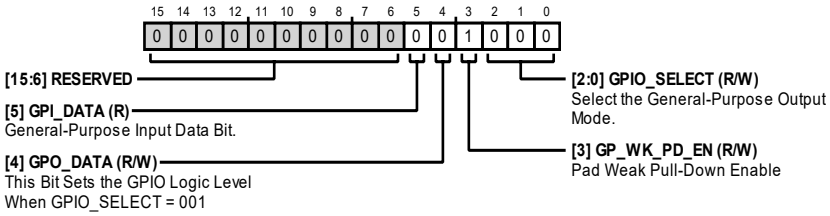


Table 52. Bit Descriptions for GPIO_CONFIG0

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GPI_DATA	General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.	0x0	R
4	GPO_DATA	This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001. 0: drive a logic low on GPIO_x pin. 1: drive a logic high on GPIO_x pin.	0x0	R/W
3	GP_WK_PD_EN	Pad Weak Pull-Down Enable. 0: disable weak pull-down. 1: enable weak pull-down.	0x1	R/W
[2:0]	GPIO_SELECT	Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option. 000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled. 001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled. 010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA. 011: configured as an input. The GPIO_x output driver is configured in high impedance state. 100: configured to monitor the output of the digital input comparator. 101: GPIO_A is configured as an output to monitor the CD signal of the HART modem interface. When this mode is selected on all four GPIO_x pins, the pins can interface with the internal HART modem UART interface. The internal SPI to UART interface is disabled. 110: GPIO_A outputs the CD output. All four GPIO_x pins can be configured to monitor the HART UART signals. The GPIO input pad buffer is disabled. 111: configured to output the EOM status bit in the HART_ALERT_STATUS register.	0x0	R/W

GPIO_B Configuration Register

Address: 0x36, Reset: 0x0008, Name: GPIO_CONFIG1

The four GPIO_x registers configure the four GPIO_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP_WK_PD_EN bit.

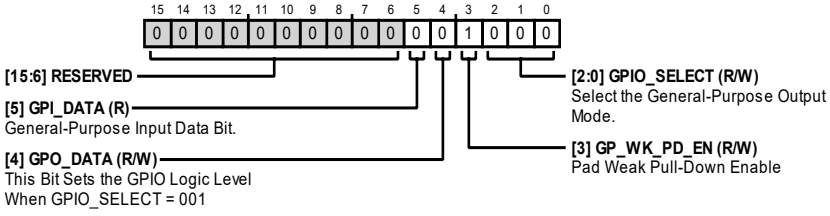


Table 53. Bit Descriptions for GPIO_CONFIG1

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GPI_DATA	General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.	0x0	R
4	GPO_DATA	This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001. 0: drive a logic low on GPIO_x pin.	0x0	R/W

REGISTER MAP

Table 53. Bit Descriptions for GPIO_CONFIG1

Bits	Bit Name	Description	Reset	Access
		1: drive a logic high on GPIO_x pin.		
3	GP_WK_PD_EN	Pad Weak Pull-Down Enable. 0: disable weak pull-down. 1: enable weak pull-down.	0x1	R/W
[2:0]	GPIO_SELECT	Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option. 000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled. 001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO input buffer is disabled. 010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA. 011: configured as an input. GPIO_x output driver is configured in high impedance state. 100: configured to drive the external digital output FET. 101: GPIO_B is configured as an output to monitor the RXD signal of the HART modem interface. When this mode is selected on all four GPIO pins, the pins can be used to interface with the internal HART modem UART interface. The internal SPI to UART interface is disabled. 110: GPIO_B is configured to output the RXD signal. All four GPIO_x pins can be configured to monitor the HART UART signals. The GPIO_x input pad buffer is disabled. 111: configured to output Hart SOM status bit in the HART_ALERT_STATUS register.	0x0	R/W

GPIO_C Configuration Register

Address: 0x37, Reset: 0x0008, Name: GPIO_CONFIG2

The four GPIO_x registers configure the four GPIO_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP_WK_PD_EN bit.

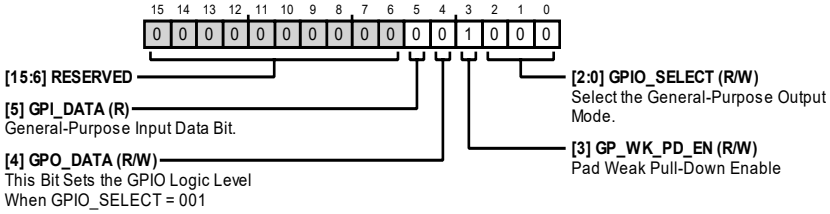


Table 54. Bit Descriptions for GPIO_CONFIG2

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GPI_DATA	General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.	0x0	R
4	GPO_DATA	This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001. 0: drive a logic low on GPIO_x pin. 1: drive a logic high on GPIO_x pin.	0x0	R/W
3	GP_WK_PD_EN	Pad Weak Pull-Down Enable. 0: disable weak pull-down. 1: enable weak pull-down.	0x1	R/W
[2:0]	GPIO_SELECT	Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option. 000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled. 001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled. 010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA. 011: configured as an input. GPIO_x output driver is configured in high impedance state.	0x0	R/W

REGISTER MAP

Table 54. Bit Descriptions for GPIO_CONFIG2

Bits	Bit Name	Description	Reset	Access
		100: configured to drive internal digital output FET. 101: GPIO_C is configured as an input to control the TXD signal of the HART modem interface. When this mode is selected on all four GPIO_x pins, the pins can interface with the internal HART modem UART interface. The internal SPI to UART interface is disabled. 110: GPIO_C is configured to output the TXD signal. All four GPIO_x pins can monitor the HART UART signals. The GPIO_x input pad buffer is disabled. 111: configured to output the TX_COMPLETE status bit in the HART_ALERT_STATUS register.		

GPIO_D Configuration Register

Address: 0x38, Reset: 0x0008, Name: GPIO_CONFIG3

The four GPIO_x registers configure the four GPIO_x pins. A weak pull-down is enabled on each pin, by default, which can be disabled using the GP_WK_PD_EN bit.

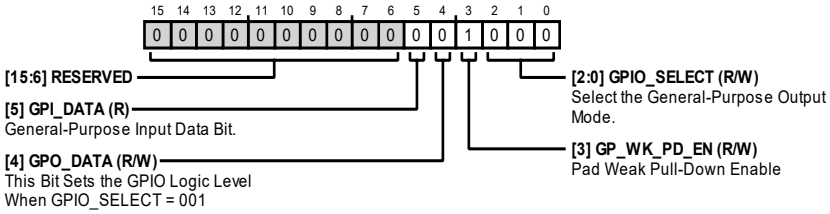


Table 55. Bit Descriptions for GPIO_CONFIG3

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GPI_DATA	General-Purpose Input Data Bit. This bit reflects the current state of the corresponding pin.	0x0	R
4	GPO_DATA	This Bit Sets the GPIO Logic Level When GPIO_SELECT = 001. 0: drive a logic low on GPIO_x pin. 1: drive a logic high on GPIO_x pin.	0x0	R/W
3	GP_WK_PD_EN	Pad Weak Pull-Down Enable. 0: disable weak pull-down. 1: enable weak pull-down.	0x1	R/W
[2:0]	GPIO_SELECT	Select the General-Purpose Output Mode. Values outside of those listed as follows select the high impedance option. 000: high impedance. The GPIO_x output driver is off. The GPIO_x pad input buffer is disabled. 001: configured as an output. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is disabled. 010: configured as an output and input. The output level is set by the GPO_DATA bit. The GPIO_x input buffer is enabled so that the output data can also be read via GPI_DATA. 011: configured as an input. GPIO_x output driver is configured in high impedance state. 100: the GPIO_x output driver is off. The GPIO_x pad input buffer is disabled. 101: GPIO_D is configured as an input to control the RTS signal of the HART modem interface. When this mode is selected on all four GPIO_x pins, the pins can interface with the internal HART modem UART interface. The internal SPI to UART interface is disabled. 110: GPIO_D is configured to output the RTS signal. All four GPIO_x pins can monitor the HART UART signals. The GPIO_x input pad buffer is disabled. 111: configured to output the CD status bit in the HART_ALERT_STATUS register.	0x0	R/W

FET Leakage Compensation Register

Address: 0x39, Reset: 0x0000, Name: FET_LKG_COMP

REGISTER MAP

This register enables compensation for leakage in the external digital output FETs. This feature can be enabled during precision analog input and output measurements. Only use this register when the DO_INT_MODE is programmed to digital output internal disable, and the DO_EXT_MODE is programmed to digital output external disable.

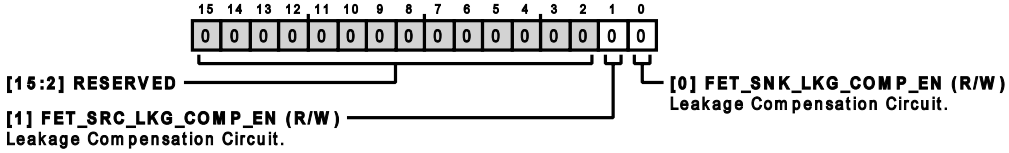


Table 56. Bit Descriptions for FET_LKG_COMP

Bits	Bit Name	Description	Reset	Access
[15:2]	RESERVED	Reserved.	0x0	R
1	FET_SRC_LKG_COMP_EN	Leakage Compensation Circuit. Enables the source FET leakage compensation circuit. 0: leakage compensation circuit off. 1: leakage compensation circuit on.	0x0	R/W
0	FET_SNK_LKG_COMP_EN	Leakage Compensation Circuit. Enable the sink FET leakage compensation circuit. 0: leakage compensation circuit off. 1: leakage compensation circuit on.	0x0	R/W

Charge Pump Configuration Register

Address: 0x3A, Reset: 0x0000, Name: CHARGE_PUMP

The internal charge pump is enabled in this register when the unipolar capability is required.

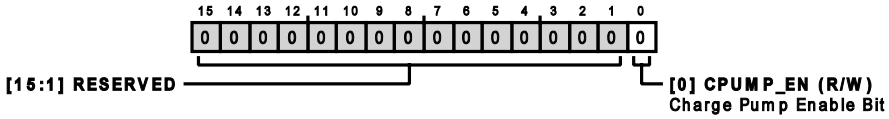


Table 57. Bit Descriptions for CHARGE_PUMP

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CPUMP_EN	Charge Pump Enable Bit. 0: disable charge pump. 1: enable charge pump.	0x0	R/W

ADC Conversion Control Register

Address: 0x3B, Reset: 0x0000, Name: ADC_CONV_CTRL

This register controls the ADC conversions that must be performed.

Disable ADC conversions before making any changes to the ADC_CONV_CTRL register.

If enabling a sequence of conversions, ensure that any previous sequence has completed. Ensure that the ADC_BUSY bit in the LIVE_STATUS register is 0 before enabling the next sequence.

REGISTER MAP

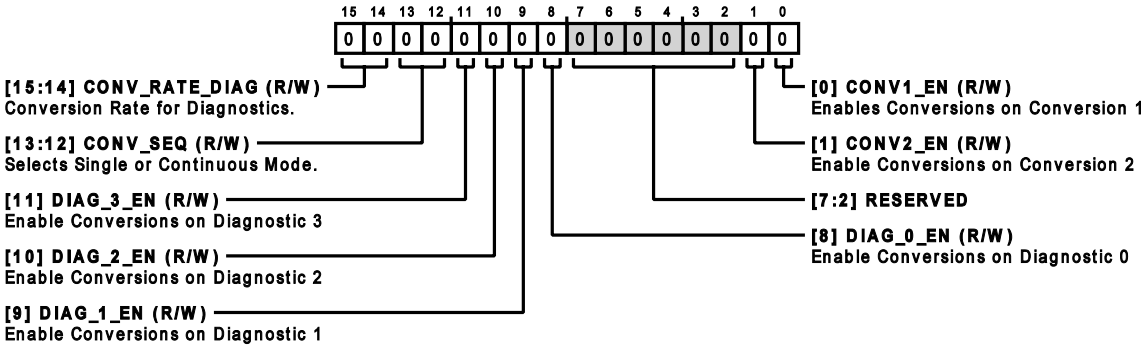


Table 58. Bit Descriptions for ADC_CONV_CTRL

Bits	Bit Name	Description	Reset	Access
[15:14]	CONV_RATE_DIAG	Conversion Rate for Diagnostics. A value outside of those listed as follows select a rate of 20 SPS. 00: sampling rate of 20 SPS and provides 50 Hz and 60 Hz noise rejection. 01: sampling rate of 4.8 kSPS. 10: sampling rate of 9.6 kSPS.	0x0	R/W
[13:12]	CONV_SEQ	Selects Single or Continuous Mode. 00: put ADC in standby mode. If converting continuously, stop conversions at the end of the current sequence and leave the ADC powered up. 01: start single sequence conversion. Perform a single conversion on each enabled channel and diagnostic. Once complete, ADC moves to the idle state. 10: start continuous conversions. Sequences continuously through the enabled channels and diagnostics. Once conversions are stopped, the sequencer waits until the end of the current sequence before moving to idle or ADC power down. 11: stop continuous conversions or power down the ADC. The ADC is powered down and takes 100 µs to power up if subsequent conversions are requested.	0x0	R/W
11	DIAG_3_EN	Enable Conversions on Diagnostic 3.	0x0	R/W
10	DIAG_2_EN	Enable Conversions on Diagnostic 2.	0x0	R/W
9	DIAG_1_EN	Enable Conversions on Diagnostic 1.	0x0	R/W
8	DIAG_0_EN	Enable Conversions on Diagnostic 0.	0x0	R/W
[7:2]	RESERVED	Reserved.	0x0	R
1	CONV2_EN	Enable Conversions on Conversion 2.	0x0	R/W
0	CONV1_EN	Enables Conversions on Conversion 1.	0x0	R/W

Diagnostics Select Register

Address: 0x3C, Reset: 0x0000, Name: DIAG_ASSIGN

This register assigns diagnostics to the four available diagnostics inputs.

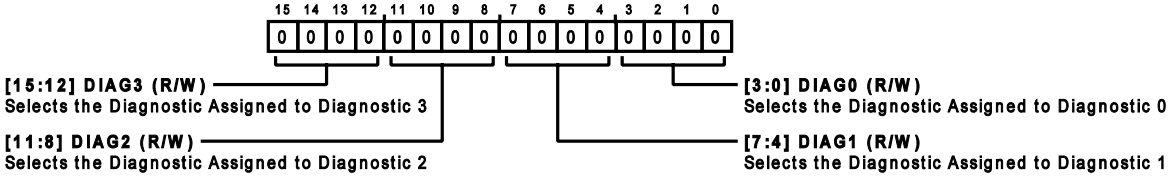


Table 59. Bit Descriptions for DIAG_ASSIGN

Bits	Bit Name	Description	Reset	Access
[15:12]	DIAG3	Selects the Diagnostic Assigned to Diagnostic 3.	0x0	R/W

REGISTER MAP

Table 59. Bit Descriptions for DIAG_ASSIGN

Bits	Bit Name	Description	Reset	Access
		0000: assign AGND to Diagnostic 3. 0001: assign the temperature sensor to Diagnostic 3. 0010: assign DVCC to Diagnostic 3. 0011: assign AVCC to Diagnostic 3. 0100: assign ALDO1V8 to Diagnostic 3. 0101: assign DLDO1V8 to Diagnostic 3. 0110: assign REFOUT to Diagnostic 3. 0111: assign AVDD to Diagnostic 3. 1000: assign AVSS to Diagnostic 3. 1001: assign LVIN to Diagnostic 3. 1010: assign SENSEL to Diagnostic 3. 1011: assign SENSE_EXT1 to Diagnostic 3. 1100: assign SENSE_EXT2 to Diagnostic 3. 1101: assign DO_VDD to Diagnostic 3. 1110: assign AGND to Diagnostic 3. 1111: measure sourcing current from the internal digital output.		
[11:8]	DIAG2	Selects the Diagnostic Assigned to Diagnostic 2. 0000: assign AGND to Diagnostic 2. 0001: assign the temperature sensor to Diagnostic 2. 0010: assign DVCC to Diagnostic 2. 0011: assign AVCC to Diagnostic 2. 0100: assign ALDO1V8 to Diagnostic 2. 0101: assign DLDO1V8 to Diagnostic 2. 0110: assign REFOUT to Diagnostic 2. 0111: assign AVDD to Diagnostic 2. 1000: assign AVSS to Diagnostic 2. 1001: assign LVIN to Diagnostic 2. 1010: assign SENSEL to Diagnostic 2. 1011: assign SENSE_EXT1 to Diagnostic 2. 1100: assign SENSE_EXT2 to Diagnostic 2. 1101: assign DO_VDD to Diagnostic 2. 1110: assign AGND to Diagnostic 2. 1111: measure sinking current from the internal digital output.	0x0	R/W
[7:4]	DIAG1	Selects the Diagnostic Assigned to Diagnostic 1. 0000: assign AGND to Diagnostic 1. 0001: assign the temperature sensor to Diagnostic 1. 0010: assign DVCC to Diagnostic 1. 0011: assign AVCC to Diagnostic 1. 0100: assign ALDO1V8 to Diagnostic 1. 0101: assign DLDO1V8 to Diagnostic 1. 0110: assign REFOUT to Diagnostic 1. 0111: assign AVDD to Diagnostic 1. 1000: assign AVSS to Diagnostic 1. 1001: assign LVIN to Diagnostic 1. 1010: assign SENSEL to Diagnostic 1. 1011: assign SENSE_EXT1 to Diagnostic 1. 1100: assign SENSE_EXT2 to Diagnostic 1. 1101: assign DO_VDD to Diagnostic 1. 1110: assign AGND to Diagnostic 1.	0x0	R/W

REGISTER MAP

Table 59. Bit Descriptions for DIAG_ASSIGN

Bits	Bit Name	Description	Reset	Access
		1111: measure sourcing current from the external digital output.		
[3:0]	DIAG0	Selects the Diagnostic Assigned to Diagnostic 0. 0000: assign AGND to Diagnostic 0. 0001: assign the temperature sensor to Diagnostic 0. 0010: assign DVCC to Diagnostic 0. 0011: assign AVCC to Diagnostic 0. 0100: assign ALDO1V8 to Diagnostic 0. 0101: assign DLDO1V8 to Diagnostic 0. 0110: assign REFOUT to Diagnostic 0. 0111: assign AVDD to Diagnostic 0. 1000: assign AVSS to Diagnostic 0. 1001: assign LVIN to Diagnostic 0. 1010: assign SENSEL to Diagnostic 0. 1011: assign SENSE_EXT1 to Diagnostic 0. 1100: assign SENSE_EXT2 to Diagnostic 0. 1101: assign DO_VDD to Diagnostic 0. 1110: assign AGND to Diagnostic 0. 1111: measure sinking current from the external digital output.	0x0	R/W

Digital Output Level Register

Address: 0x40, Reset: 0x0000, Name: DIN_COMP_OUT

This register reflects the debounced output of the digital input comparator.

The I/OP screw terminal voltage is compared to a programmed threshold voltage. The output of this comparison is fed into a programmable debounce circuit.

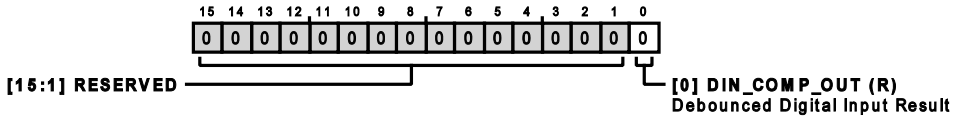


Table 60. Bit Descriptions for DIN_COMP_OUT

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	DIN_COMP_OUT	Debounced Digital Input Result.	0x0	R

Alert Status Register

Address: 0x41, Reset: 0x0001, Name: ALERT_STATUS

This register contains the alert status of the alert status bits. Once the alert condition has been removed, write 1 to clear any of the bits in this register.

REGISTER MAP

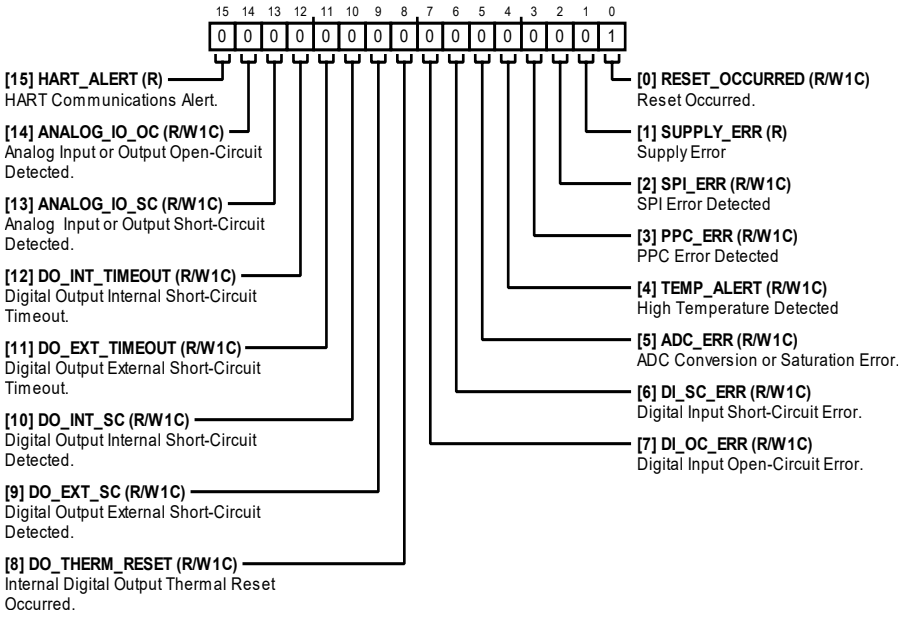


Table 61. Bit Descriptions for ALERT_STATUS

Bits	Bit Name	Description	Reset	Access
15	HART_ALERT	HART Communications Alert. This bit is set if any of the bits in the HART_ALERT_STATUS register are set (excluding CD and FRM_MON_STATE) and the corresponding field in HART_ALERT_MASK is 0. This bit clears when all of fields (excluding CD and FRM_MON_STATE) in HART_ALERT_STATUS are 0 or masked. Read the HART_ALERT_STATUS register to determine the source of this error.	0x0	R
14	ANALOG_IO_OC	Analog Input or Output Open-Circuit Detected. This bit is asserted if an open circuit is detected in any of the analog input or output functions.	0x0	R/W1C
13	ANALOG_IO_SC	Analog Input or Output Short-Circuit Detected. This bit is asserted if a short circuit is detected in any of the analog input or output functions.	0x0	R/W1C
12	DO_INT_TIMEOUT	Digital Output Internal Short-Circuit Timeout. Digital output internal is disabled.	0x0	R/W1C
11	DO_EXT_TIMEOUT	Digital Output External Short-Circuit Timeout. Digital output external is disabled.	0x0	R/W1C
10	DO_INT_SC	Digital Output Internal Short-Circuit Detected. Note that this interrupt does not assert while the digital output FET is in the T1 period of operation.	0x0	R/W1C
9	DO_EXT_SC	Digital Output External Short-Circuit Detected. Note that this interrupt does not assert while the digital output FET is in the T1 period of operation.	0x0	R/W1C
8	DO_THERM_RESET	Internal Digital Output Thermal Reset Occurred.	0x0	R/W1C
7	DI_OC_ERR	Digital Input Open-Circuit Error.	0x0	R/W1C
6	DI_SC_ERR	Digital Input Short-Circuit Error.	0x0	R/W1C
5	ADC_ERR	ADC Conversion or Saturation Error.	0x0	R/W1C
4	TEMP_ALERT	High Temperature Detected. This bit asserts if the die temperature reaches 115°C.	0x0	R/W1C
3	PPC_ERR	PPC Error Detected. This bit is asserted if a programmable power control command results in either the PPC_TX_BUSY_ERR or the PPC_TX_ACK_ERR asserting in the PPC_ACTIVE register.	0x0	R/W1C
2	SPI_ERR	SPI Error Detected. This bit is asserted if an SPI transaction does not contain the correct number of SCLKs or if a CRC error is detected.	0x0	R/W1C
1	SUPPLY_ERR	Supply Error. Read the SUPPLY_ALERT_STATUS register to determine the source of this error. This bit is set if any of the fields in the SUPPLY_ALERT_STATUS register are set and the corresponding fields in SUPPLY_ALERT_MASK are 0. This bit clears when all bit fields in SUPPLY_ALERT_STATUS are 0 or masked.	0x0	R
0	RESET_OCCURRED	Reset Occurred. This bit is asserted after a reset event that asserts the $\overline{\text{ALERT}}$ pin. Write a 1 to this bit to clear the flag. Note that a mask bit is not provided for this bit.	0x1	R/W1C

REGISTER MAP

Live Status Register

Address: 0x42, Reset: 0x0000, Name: LIVE_STATUS

This register contains the live status of some of the status bits. The bits are not latched and directly reflect the status bits.

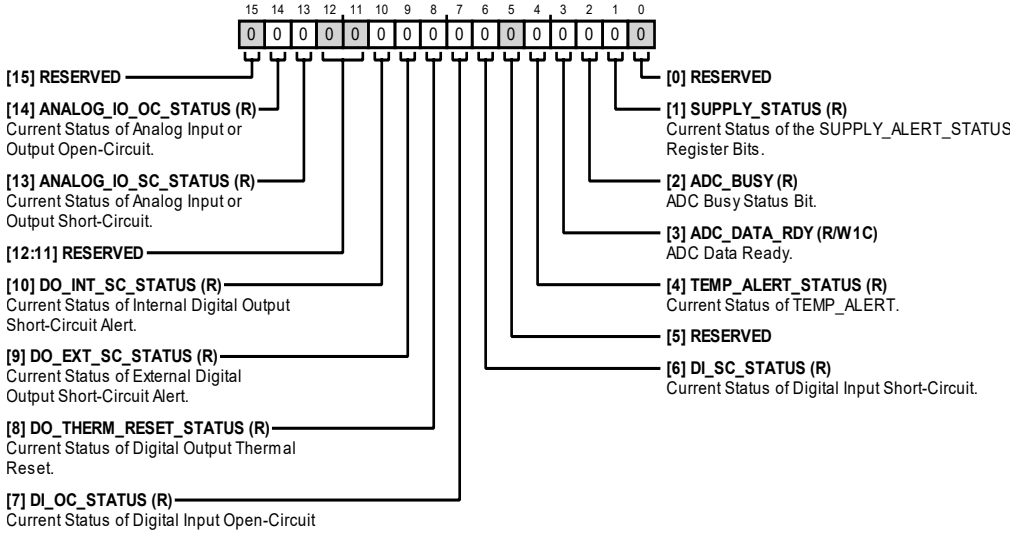


Table 62. Bit Descriptions for LIVE_STATUS

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	ANALOG_IO_OC_STATUS	Current Status of Analog Input or Output Open-Circuit.	0x0	R
13	ANALOG_IO_SC_STATUS	Current Status of Analog Input or Output Short-Circuit.	0x0	R
[12:11]	RESERVED	Reserved.	0x0	R
10	DO_INT_SC_STATUS	Current Status of Internal Digital Output Short-Circuit Alert. Note: This interrupt does not assert during the T1 short-circuit time.	0x0	R
9	DO_EXT_SC_STATUS	Current Status of External Digital Output Short-Circuit Alert. Note: This interrupt does not assert during the T1 short-circuit time.	0x0	R
8	DO_THERM_RESET_STATUS	Current Status of Digital Output Thermal Reset.	0x0	R
7	DI_OC_STATUS	Current Status of Digital Input Open-Circuit.	0x0	R
6	DI_SC_STATUS	Current Status of Digital Input Short-Circuit.	0x0	R
5	RESERVED	Reserved.	0x0	R
4	TEMP_ALERT_STATUS	Current Status of TEMP_ALERT. If the die temperature is at or above typically 115°C, this bit is asserted.	0x0	R
3	ADC_DATA_RDY	ADC Data Ready. In continuous conversion mode, the $\overline{\text{ADC\_RDY}}$ pin returns high after 24 µs, but the ADC_DATA_RDY status bit stays asserted until a user writes 1 to clear the bit.	0x0	R/W1C
2	ADC_BUSY	ADC Busy Status Bit. This bit resets to 1 as the ADC is initially in a power-up state.	0x0	R
1	SUPPLY_STATUS	Current Status of the SUPPLY_ALERT_STATUS Register Bits.	0x0	R
0	RESERVED	Reserved.	0x0	R

ADC Conversion 1 Result Register

Address: 0x44, Reset: 0x0000, Name: ADC_RESULT1

This register contains the 16 bits of the ADC conversion result.

REGISTER MAP

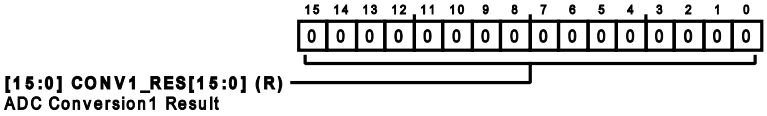


Table 63. Bit Descriptions for ADC_RESULT1

Bits	Bit Name	Description	Reset	Access
[15:0]	CONV1_RES[15:0]	ADC Conversion1 Result.	0x0	R

ADC Conversion 2 Result Register

Address: 0x46, Reset: 0x0000, Name: ADC_RESULT2

This register contains the 16 bits of the ADC conversion result.

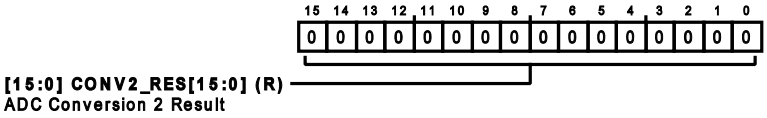


Table 64. Bit Descriptions for ADC_RESULT2

Bits	Bit Name	Description	Reset	Access
[15:0]	CONV2_RES[15:0]	ADC Conversion 2 Result.	0x0	R

Diagnostic Results Registers

Address: 0x53 to 0x56, Reset: 0x0000, Name: ADC_DIAG_RESULTx

These four registers contain the 16-bit diagnostic conversion results.

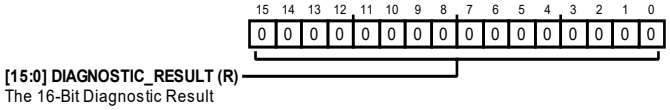


Table 65. Bit Descriptions for ADC_DIAG_RESULTx

Bits	Bit Name	Description	Reset	Access
[15:0]	DIAGNOSTIC_RESULT	The 16-Bit Diagnostic Result.	0x0	R

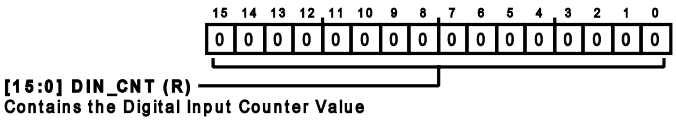
Digital Input Counter Register

Address: 0x57, Reset: 0x0000, Name: DIN_COUNTER

This register reflects the digital input counter value when the COUNT_EN bit in DIN_CONFIG1 register is set. This count is allowed to roll over from full scale back to 0; therefore, read this register often enough to avoid unexpected roll-over.

Note that, when the enable signal is low, the count is frozen.

The INV_DIN_COMP_OUT bit inverts the deglitched output allowing the counter increment edge to be modified.



REGISTER MAP

Table 66. Bit Descriptions for DIN_COUNTER

Bits	Bit Name	Description	Reset	Access
[15:0]	DIN_CNT	Contains the Digital Input Counter Value. This counter is enabled when the COUNT_EN bit within the DIN_CONFIG1 register is set. When the enable signal is low, the count is frozen. This count is allowed to roll over by design, as in normal operation, and its update rate must be slow. Read the counter often enough to avoid unexpected roll over. The INV_DIN_COMP_OUT bit inverts the deglitched output allowing the counter increment edge to be modified.	0x0	R

Supply Alert Status Register

Address: 0x5B, Reset: 0x0000, Name: SUPPLY_ALERT_STATUS

This register contains the supply alert status bits. Once the alert condition has been removed, write 1 to clear the bits in this register.

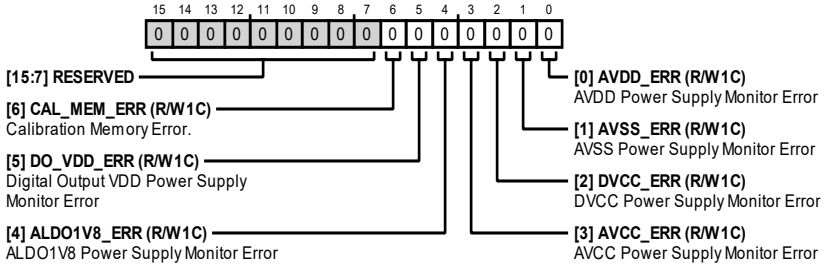


Table 67. Bit Descriptions for SUPPLY_ALERT_STATUS

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	CAL_MEM_ERR	Calibration Memory Error. This flag asserts when a calibration memory CRC error or an uncorrectable error correcting code (ECC) error is detected on calibration memory upload, or when there is an attempted SPI access to a register when the memory refresh has not completed. (Do not address this device until the one time programmable (OTP) memory is uploaded.) If this bit is asserted, it is recommended to reset the device and check the supplies.	0x0	R/W1C
5	DO_VDD_ERR	Digital Output VDD Power Supply Monitor Error. This bit is asserted when digital output VDD falls below 9.3 V.	0x0	R/W1C
4	ALDO1V8_ERR	ALDO1V8 Power Supply Monitor Error. This bit is asserted when ALDO1V8 falls below 1.4 V.	0x0	R/W1C
3	AVCC_ERR	AVCC Power Supply Monitor Error. This bit is asserted when AVCC falls below 4.1 V.	0x0	R/W1C
2	DVCC_ERR	DVCC Power Supply Monitor Error. This bit is asserted when DVCC falls below 1.9 V.	0x0	R/W1C
1	AVSS_ERR	AVSS Power Supply Monitor Error. This bit is asserted when AVSS goes above –1.6V.	0x0	R/W1C
0	AVDD_ERR	AVDD Power Supply Monitor Error. This bit is asserted when AVDD falls below 5.5 V.	0x0	R/W1C

Alert Mask Register for ALERT_STATUS

Address: 0x5F, Reset: 0x0000, Name: ALERT_MASK

This register is used to mask specific status bits from activating the $\overline{\text{ALERT}}$ pin. The position of mask bits in this register line up the corresponding status bits in the ALERT_STATUS register. To mask a specific alert condition, set the corresponding mask bit to 1.

Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT_STATUS register.

REGISTER MAP

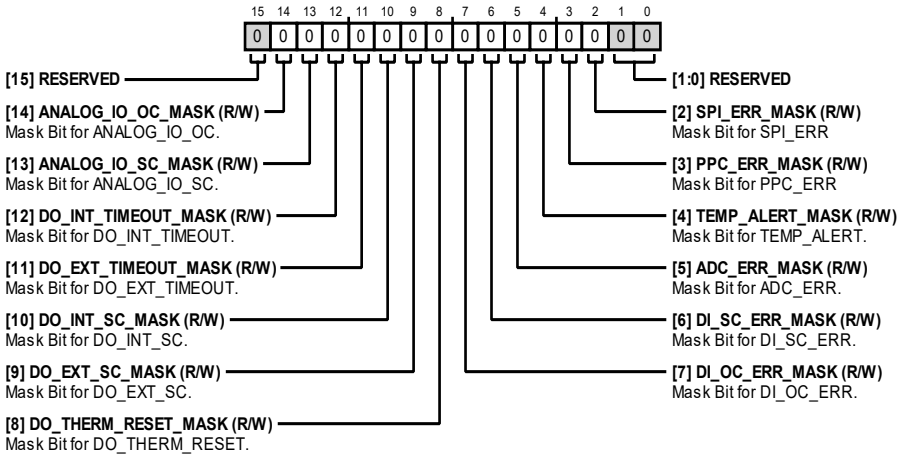


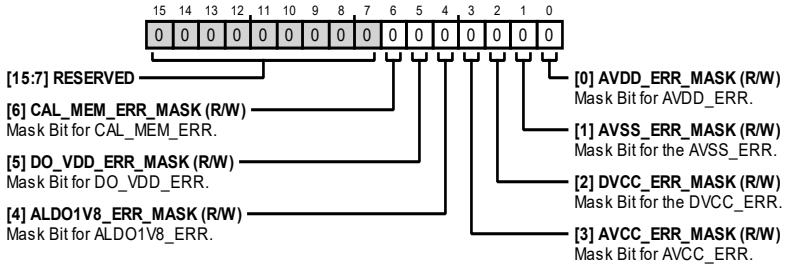
Table 68. Bit Descriptions for ALERT_MASK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved.	0x0	R
14	ANALOG_IO_OC_MASK	Mask Bit for ANALOG_IO_OC.	0x0	R/W
13	ANALOG_IO_SC_MASK	Mask Bit for ANALOG_IO_SC.	0x0	R/W
12	DO_INT_TIMEOUT_MASK	Mask Bit for DO_INT_TIMEOUT.	0x0	R/W
11	DO_EXT_TIMEOUT_MASK	Mask Bit for DO_EXT_TIMEOUT.	0x0	R/W
10	DO_INT_SC_MASK	Mask Bit for DO_INT_SC.	0x0	R/W
9	DO_EXT_SC_MASK	Mask Bit for DO_EXT_SC.	0x0	R/W
8	DO_THERM_RESET_MASK	Mask Bit for DO_THERM_RESET.	0x0	R/W
7	DI_OC_ERR_MASK	Mask Bit for DI_OC_ERR.	0x0	R/W
6	DI_SC_ERR_MASK	Mask Bit for DI_SC_ERR.	0x0	R/W
5	ADC_ERR_MASK	Mask Bit for ADC_ERR.	0x0	R/W
4	TEMP_ALERT_MASK	Mask Bit for TEMP_ALERT.	0x0	R/W
3	PPC_ERR_MASK	Mask Bit for PPC_ERR.	0x0	R/W
2	SPI_ERR_MASK	Mask Bit for SPI_ERR.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Alert Mask Register for SUPPLY_ALERT_STATUS

Address: 0x60, Reset: 0x0000, Name: SUPPLY_ALERT_MASK

This register is used to mask specific SUPPLY_ALERT_STATUS bits from activating the $\overline{\text{ALERT}}$ pin. The position of mask bits in this register line up the corresponding status bits in the SUPPLY_ALERT_STATUS register. To mask a particular alert, set the corresponding mask bit to 1. Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT_STATUS register.



REGISTER MAP

Table 69. Bit Descriptions for SUPPLY_ALERT_MASK

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	CAL_MEM_ERR_MASK	Mask Bit for CAL_MEM_ERR.	0x0	R/W
5	DO_VDD_ERR_MASK	Mask Bit for DO_VDD_ERR.	0x0	R/W
4	ALDO1V8_ERR_MASK	Mask Bit for ALDO1V8_ERR.	0x0	R/W
3	AVCC_ERR_MASK	Mask Bit for AVCC_ERR.	0x0	R/W
2	DVCC_ERR_MASK	Mask Bit for the DVCC_ERR.	0x0	R/W
1	AVSS_ERR_MASK	Mask Bit for the AVSS_ERR.	0x0	R/W
0	AVDD_ERR_MASK	Mask Bit for AVDD_ERR.	0x0	R/W

Readback Select Register

Address: 0x64, Reset: 0x0000, Name: READ_SELECT

This register selects the address of the register required to be read back and determines the contents of the SPI readback frame.

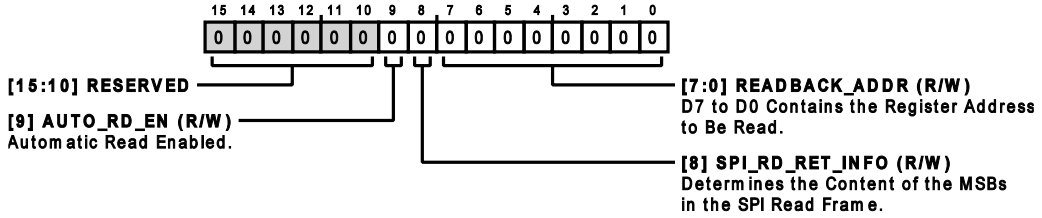


Table 70. Bit Descriptions for READ_SELECT

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R
9	AUTO_RD_EN	Automatic Read Enabled. When this bit is set to 1, read data is returned on the SDO on every SPI access. The location read is determined by READBACK_ADDR.	0x0	R/W
8	SPI_RD_RET_INFO	Determines the Content of the MSBs in the SPI Read Frame. When this bit is set to 0, READBACK_ADDR[6:0] is returned in Bits[30:24] of any subsequent SPI read. When this bit is set to 1, the $\overline{\text{ADC\_RDY}}$ and $\overline{\text{ALERT}}$ flags and the four DIN outputs are returned in Bits[30:24] of any subsequent SPI read.	0x0	R/W
[7:0]	READBACK_ADDR	D7 to D0 Contains the Register Address to Be Read.	0x0	R/W

Select the Registers Read in Burst Mode

Address: 0x65, Reset: 0x03FF, Name: BURST_READ_SEL

This register can be used to select which registers are returned on a burst read that includes any of the ALERT_STATUS, LIVE_STATUS, ADC_RESULTx, ADC_DIAG_RESULTx, and DIN_COUNTER registers.

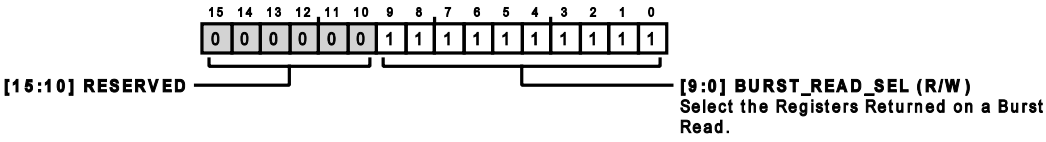


Table 71. Bit Descriptions for BURST_READ_SEL

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved.	0x0	R

REGISTER MAP

Table 71. Bit Descriptions for BURST_READ_SEL

Bits	Bit Name	Description	Reset	Access
[9:0]	BURST_READ_SEL	Select the Registers Returned on a Burst Read. If a bit corresponding to a register is 0, that register is skipped during the burst read. Bit 0: enable burst read of the ALERT_STATUS register. Bit 1: enable burst read of the LIVE_STATUS register. Bit 2: enable burst read of the ADC_RESULT1 register. Bit 3: enable burst read of the ADC_RESULT2 register. Bit 4: enable burst read of the ADC_DIAG_RESULT0 register. Bit 5: enable burst read of the ADC_DIAG_RESULT1 register. Bit 6: enable burst read of the ADC_DIAG_RESULT2 register. Bit 7: enable burst read of the ADC_DIAG_RESULT3 register. Bit 8: enable burst read of the DIN_COUNTER register. Bit 9: enable burst read of the SUPPLY_ALERT_STATUS register. Read data for all registers outside of those previously listed always return on a burst read if the burst read includes the register. Note that the starting address location of a burst read is always returned even if its corresponding BURST_READ_SEL bit is 0. Burst reads can start at DIN_COMP_OUT to include this as the first register in a burst read. However, DIN_COMP_OUT does not have a corresponding BURST_READ_SEL bit.	0x3FF	R/W

PPC Transmit Register

Address: 0x66, Reset: 0x00FF, Name: PPC_TX

Programmable power control voltage configuration register. This register allows the power supply voltage generated by the ADP1034 to be configured via the OWSI to adjust the AD74115H power supply, AVDD.

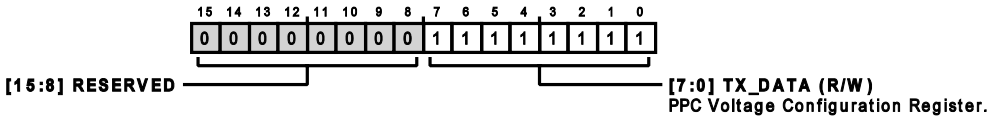


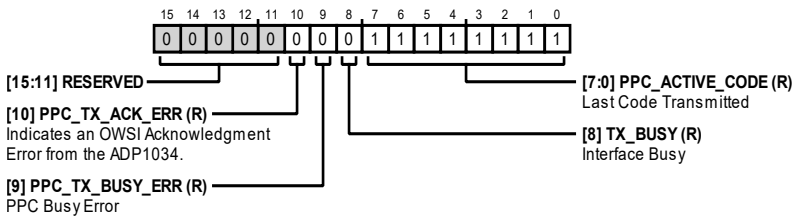
Table 72. Bit Descriptions for PPC_TX

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	TX_DATA	PPC Voltage Configuration Register. These bits reset to the maximum power supply voltage that matches the ADP1034 configuration. Note that once these bits are updated, further writes are blocked until the transmission completes.	0xFF	R/W

PPC Status Register

Address: 0x6E, Reset: 0x00FF, Name: PPC_ACTIVE

This read only register provides status information on the OWSI transactions.



REGISTER MAP

Table 73. Bit Descriptions for PPC_ACTIVE

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	PPC_TX_ACK_ERR	Indicates an OWSI Acknowledgment Error from the ADP1034. This bit is set if a second attempt to write to the ADP1034 is not acknowledged. When the ADP1034 does not acknowledge an initial data transfer, the OWSI controller attempts a second OWSI transfer to the PPC. If this second transfer is not successful, this bit asserts. This flag is cleared when the PPC_ERR bit is programmed to 1 in the ALERT_STATUS register.	0x0	R
9	PPC_TX_BUSY_ERR	PPC Busy Error. This bit indicates that a write to the PPC_TX register was blocked because the TX_BUSY bit is set. This flag is cleared when PPC_ERR is programmed to 1 in the ALERT_STATUS register.	0x0	R
8	TX_BUSY	Interface Busy. Indicates that TX_DATA is in the process or waiting to be transmitted. Do not attempt a write to TX_DATA while this bit is set. This bit deasserts once TX_DATA is transmitted.	0x0	R
[7:0]	PPC_ACTIVE_CODE	Last Code Transmitted. These bits reflect the last successfully transmitted data to the ADP1034.	0xFF	R

Thermal Reset Enable Register

Address: 0x77, Reset: 0x0000, Name: THERM_RST

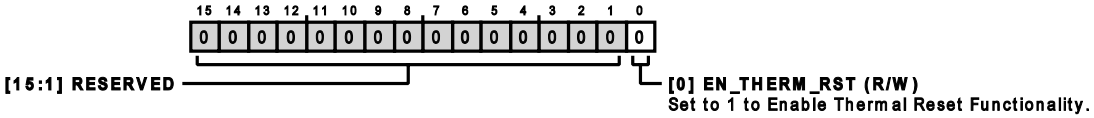


Table 74. Bit Descriptions for THERM_RST

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EN_THERM_RST	Set to 1 to Enable Thermal Reset Functionality. If the die temperature reaches typically 140°C, a thermal reset event triggers a digital reset, which is detected via a change in the $\overline{\text{ALERT}}$ pin and the RESET_OCCURRED flag.	0x0	R/W

Command Register

Address: 0x78, Reset: 0x0000, Name: CMD_KEY

This register is used to issue specific commands to the device.

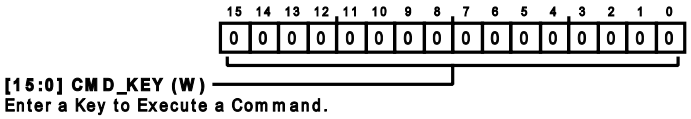


Table 75. Bit Descriptions for CMD_KEY

Bits	Bit Name	Description	Reset	Access
[15:0]	CMD_KEY	Enter a Key to Execute a Command. 0x15FA: Software Reset Key 1. To trigger a software reset, write to this key followed by Software Reset Key 2. The SPI writes must be back to back. 0xAF51: Software Reset Key 2. To trigger a software reset, write to Software Reset Key 1 followed by this key. The SPI writes must be back to back. 0x3F5C: Fuse Upload Key. When this key is entered, the fuses are uploaded and refreshed. The CAL_MEM_ERR bit asserts if there is an SPI access while the fuses are being uploaded. Therefore, it is possible to determine when the fuse upload has completed by repeatedly reading and clearing the CAL_MEM_ERR bit until it does not assert on an SPI access. Note that the oscillator trim bits are passed from the shadow register to the active register (connected to oscillator) upon completion of the ECC in the user mode. In test mode, oscillator trim bits pass	0x0	W

REGISTER MAP

Table 75. Bit Descriptions for CMD_KEY

Bits	Bit Name	Description	Reset	Access
		directly to the active register during fuse reading. Therefore, it is recommended to upload fuses in user mode only to avoid errant trim bits being passed to the oscillator.		

Scratch or Spare Register

Address: 0x79 to 0x7A (Increments of 1), Reset: 0x0000, Name: SCRATCHx

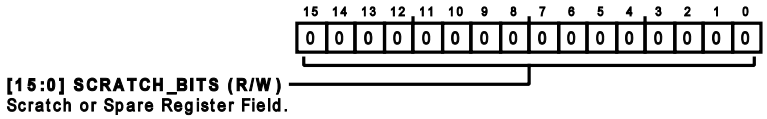


Table 76. Bit Descriptions for SCRATCHx

Bits	Bit Name	Description	Reset	Access
[15:0]	SCRATCH_BITS	Scratch or Spare Register Field.	0x0	R/W

Silicon Revision Register

Address: 0x7B, Reset: 0x0001, Name: SILICON_REV

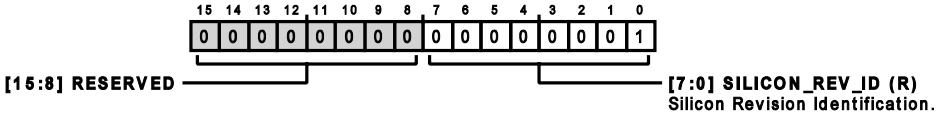


Table 77. Bit Descriptions for SILICON_REV

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SILICON_REV_ID	Silicon Revision Identification.	0x1	R

Silicon ID 0 Register

Address: 0x7C, Reset: 0x0000, Name: SILICON_ID0

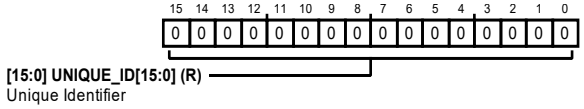
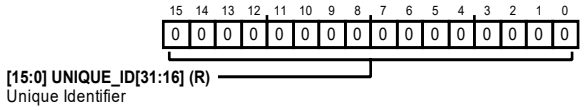


Table 78. Bit Descriptions for SILICON_ID0

Bits	Bit Name	Description	Reset	Access
[15:0]	UNIQUE_ID[15:0]	Unique Identifier	0x0	R

Silicon ID 1 Register

Address: 0x7D, Reset: 0x0000, Name: SILICON_ID1



REGISTER MAP

Table 79. Bit Descriptions for SILICON_ID1

Bits	Bit Name	Description	Reset	Access
[15:0]	UNIQUE_ID[31:16]	Unique Identifier	0x0	R

Silicon ID 2 Register

Address: 0x7E, Reset: 0x0000, Name: SILICON_ID2

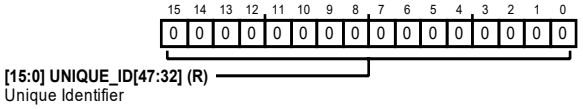


Table 80. Bit Descriptions for SILICON_ID2

Bits	Bit Name	Description	Reset	Access
[15:0]	UNIQUE_ID[47:32]	Unique Identifier	0x0	R

Silicon ID 3 Register

Address: 0x7F, Reset: 0x0000, Name: SILICON_ID3

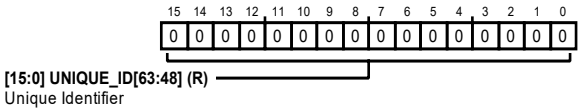


Table 81. Bit Descriptions for SILICON_ID3

Bits	Bit Name	Description	Reset	Access
[15:0]	UNIQUE_ID[63:48]	Unique Identifier	0x0	R

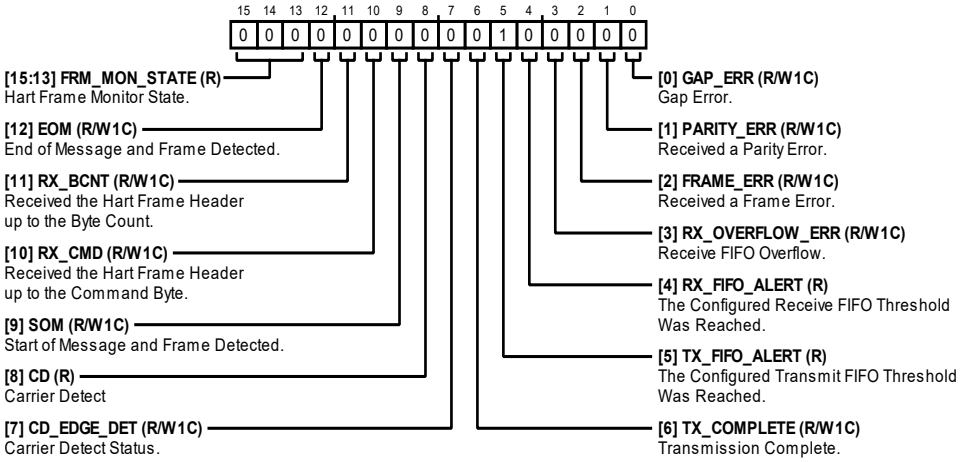
HART MODEM REGISTERS

The following registers (Address 0x80 to Address 0x89) are HART modem configuration registers.

HART Communications Alert Register

Address: 0x80, Reset: 0x0020, Name: HART_ALERT_STATUS

This register contains the alert status of the HART alert status bits. Once the alert condition is removed, write 1 to clear any of the bits in this register.



REGISTER MAP

Table 82. Bit Descriptions for HART_ALERT_STATUS

Bits	Bit Name	Description	Reset	Access
[15:13]	FRM_MON_STATE	HART Frame Monitor State. This field indicates the current state of the frame monitor. 000: HM_PREAM, receiving preamble bytes. 001: HM_ADDR, receiving address bytes. 010: HM_EXP, receiving expansion bytes. 011: HM_CMD, receiving the command byte. 100: HM_FRM_SIZE, receiving the frame size byte. 101: HM_FRM_DATA, receiving payload data. 110: HM_CHK_BYTE, receiving the check byte.	0x0	R
12	EOM	End of Message and Frame Detected. This bit asserts when all of a frame is received up to and including the check byte. If there was a gap error in the received frame, the EOM bit does not assert. A parity error or frame error in one of the received bytes does not prevent this bit from asserting, except if the error was in the byte count byte.	0x0	R/W1C
11	RX_BCNT	Received the HART Frame Header up to the Byte Count. The receive FIFO contains the header of a frame. This bit asserts when the frame header up to the byte count is received. A gap error in the received bytes prevents this bit from asserting. A parity error or frame error in the byte count byte also prevents this bit from asserting. A parity error or frame error in any other received byte does not prevent this bit from asserting.	0x0	R/W1C
10	RX_CMD	Received the HART Frame Header up to the Command Byte. The receive FIFO contains the header of a frame. This bit asserts when the frame header up to the command byte is received. A gap error in the received bytes prevents this bit from asserting. A parity error or frame error in one of the received bytes does not prevent this bit from asserting.	0x0	R/W1C
9	SOM	Start of Message and Frame Detected. The receive FIFO contains the header of a frame. This bit asserts when at least two preamble bytes and a delimiter are received, and there were no errors in the received bytes.	0x0	R/W1C
8	CD	Carrier Detect. This bit directly reflects the CD signal. It does not drive the $\overline{\text{ALERT}}$ pin and therefore does not have a corresponding ALERT_HART_MASK bit.	0x0	R
7	CD_EDGE_DET	Carrier Detect Status. This bit can detect edges on the CD bit. CD_EDGE_SEL is used to determine if a falling, rising, or any edge on the CD asserts this bit. After changing CD_EDGE_SEL, the next selected edge (rising or falling) causes this bit to assert.	0x0	R/W1C
6	TX_COMPLETE	Transmission Complete. This bit asserts when the transmit engine has finished transmitting the last bit of a byte, and there are no more bytes in the transmit FIFO.	0x0	R/W1C
5	TX_FIFO_ALERT	The Configured Transmit FIFO Threshold Was Reached. This bit asserts when the number of bytes in the transmit FIFO is less than or equal to the value configured in the TFTRIG bits of the HART_FCR register. If TFTRIG = 0, this bit indicates when the FIFO is empty. Because the FIFO is empty on power-up and TFTRIG powers up to 8, this bit is 1 on power up. It deassert when greater than the TFTRIG bits are written to the transmit FIFO.	0x1	R
4	RX_FIFO_ALERT	The Configured Receive FIFO Threshold Was Reached.	0x0	R
3	RX_OVERFLOW_ERR	Receive FIFO Overflow. A received byte was not written to the receive FIFO as it was full.	0x0	R/W1C
2	FRAME_ERR	Received a Frame Error. This bit asserts when a frame error is detected in a received character.	0x0	R/W1C
1	PARITY_ERR	Received a Parity Error. This bit asserts when a parity error is detected in a received byte.	0x0	R/W1C
0	GAP_ERR	Gap Error. This bit asserts when there is a gap between characters of 1 character time (9 ms) or more. This gap can assert at the end of frame; however, it is not guaranteed to assert at the end of a frame, that is, there cannot be a gap of 1 character between frames.	0x0	R/W1C

HART Communications Receive Register

Address: 0x81, Reset: 0x0000, Name: HART_RX

The receive FIFO is read via this register.

It is possible to burst read the contents of the receive FIFO over the SPI. If the burst read is started at this register, internally the logic does not increment to the next address. Instead, the logic stays at the address of the HART_RX register and repeatedly returns characters from the receive FIFO.

REGISTER MAP

When the address of this register is written to the READ_SELECT register, the clock to the HART UART logic is automatically enabled. Therefore, when finished using the UART, write any address other than HART_RX to the READ_SELECT register to disable the clock to the UART to save power.

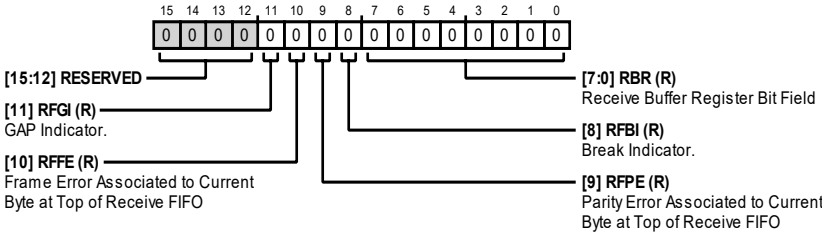


Table 83. Bit Descriptions for HART_RX

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	RFGI	GAP Indicator. RXD was detected high for at least a character time (11 bits) since the last character was received. This indicates that there was a gap before this character. RFGI is not set in the first word of the first frame received after exiting reset. It is asserted at the start of all subsequent frames received if the frames are preceded by a gap.	0x0	R
10	RFFE	Frame Error Associated to Current Byte at Top of Receive FIFO.	0x0	R
9	RFPE	Parity Error Associated to Current Byte at Top of Receive FIFO.	0x0	R
8	RFBI	Break Indicator. RXD was detected low for a character time (11 bits), which indicates a break associated with the byte at top of the receive FIFO.	0x0	R
[7:0]	RBR	Receive Buffer Register Bit Field. Reading these bits returns the character at the top of the receive FIFO and pops the entry from the FIFO.	0x0	R

HART Communications Transmit Register

Address: 0x82, Reset: 0x0000, Name: HART_TX

The transmit FIFO is written via this register.

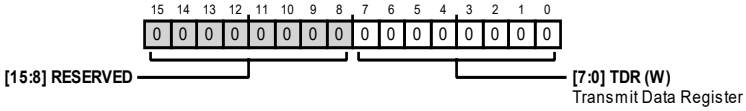


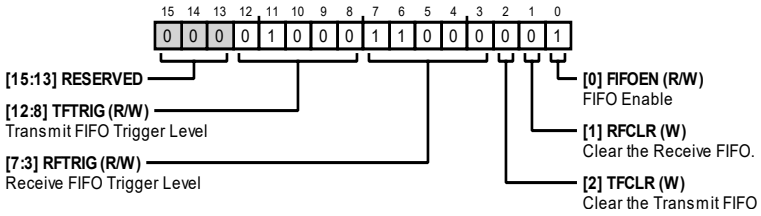
Table 84. Bit Descriptions for HART_TX

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	TDR	Transmit Data Register. Writing to these bits adds a byte to the transmit FIFO.	0x0	W

FIFO Control Register

Address: 0x83, Reset: 0x08C1, Name: HART_FCR

This register is used to configure the transmit and receive FIFOs.



REGISTER MAP

Table 85. Bit Descriptions for HART_FCR

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TFTRIG	Transmit FIFO Trigger Level. Sets the transmit FIFO level to trigger an interrupt. When the transmit FIFO fill level is greater than or equal to the configured level, the TX_FIFO_ALERT bit of the ALERT_HART_STATUS register goes to 1. 1 ≥ 1 byte, 2 ≥ 2 bytes, and so on.	0x8	R/W
[7:3]	RFTRIG	Receive FIFO Trigger Level. Sets the receive FIFO level to trigger an interrupt. When the receive FIFO fill level is greater than or equal to the configured level, the RX_FIFO_ALERT bit of the ALERT_HART_STATUS register goes to 1. 1 ≥ 1 byte, 2 ≥ 2 bytes, and so on.	0x18	R/W
2	TFCLR	Clear the Transmit FIFO. If the UART transmit FIFO is cleared while frame transmission is in progress, the host software must wait until the TX_COMPLETE bit of the HART_ALERT_STATUS register asserts before attempting to transmit another frame. The host software must not write to the transmit FIFO (the TDR bits of the HART_TX register) until TX_COMPLETE asserts. Otherwise, the next frame transmits without a preamble if the TX_PREM_CNT bit of the HART_CONFIG register is nonzero. Alternatively, write 0x0 to the TX_PREM_CNT bits of the HART_CONFIG register and proceed to write the preamble bytes and the next frame to the transmit FIFO. In this case, after writing to the FIFO, check if TX_COMPLETE has asserted. If it has, RTS must be set again to start frame transmission. If TX_COMPLETE has not asserted, frame transmission continues as normal.	0x0	W
1	RFCLR	Clear the Receive FIFO.	0x0	W
0	FIFOEN	FIFO Enable	0x1	R/W

HART UART Transmit Control Register

Address: 0x84, Reset: 0x0000, Name: HART_MCR

This register is used to send the request to send (RTS) signal.

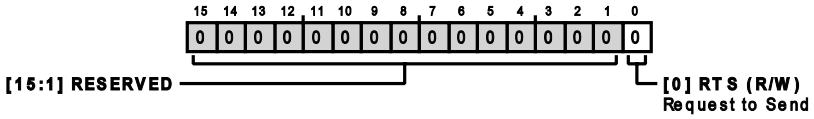


Table 86. Bit Descriptions for HART_MCR

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	RTS	Request to Send.	0x0	R/W

Receive FIFO Byte Count Register

Address: 0x85, Reset: 0x0000, Name: HART_RFC

This register shows the number of bytes contained in the HART receive FIFO.

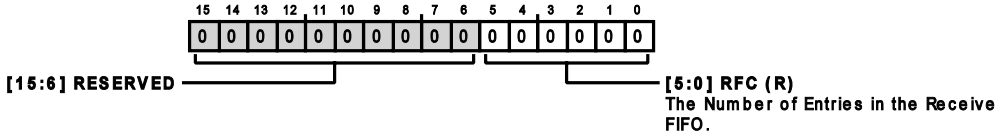


Table 87. Bit Descriptions for HART_RFC

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	RFC	The Number of Entries in the Receive FIFO.	0x0	R

REGISTER MAP

Transmit FIFO Byte Count Register

Address: 0x86, Reset: 0x0000, Name: HART_TFC

This register shows the number of bytes contained in the HART transmit FIFO.

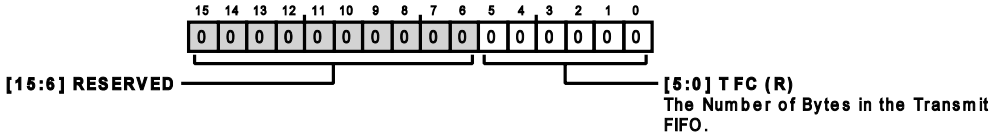


Table 88. Bit Descriptions for HART_TFC

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	TFC	The Number of Bytes in the Transmit FIFO.	0x0	R

HART Communications Alert Mask Register

Address: 0x87, Reset: 0x1EFF, Name: HART_ALERT_MASK

This register is used to mask specific status bits from activating the $\overline{\text{ALERT}}$ pin. The position of the mask bits in this register line up with the corresponding status bits in the HART_ALERT_STATUS register. To mask a specific alert, set the corresponding mask bit to 1.

Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT_STATUS register.

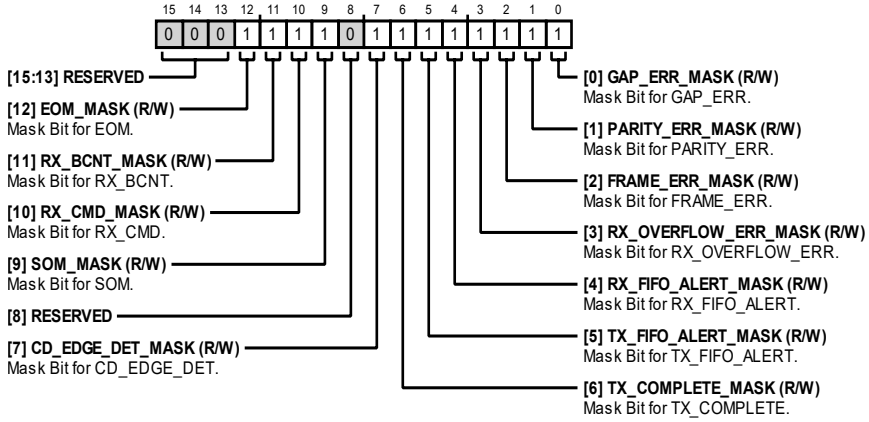


Table 89. Bit Descriptions for HART_ALERT_MASK

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	EOM_MASK	Mask Bit for EOM.	0x1	R/W
11	RX_BCNT_MASK	Mask Bit for RX_BCNT.	0x1	R/W
10	RX_CMD_MASK	Mask Bit for RX_CMD.	0x1	R/W
9	SOM_MASK	Mask Bit for SOM.	0x1	R/W
8	RESERVED	Reserved.	0x0	R
7	CD_EDGE_DET_MASK	Mask Bit for CD_EDGE_DET.	0x1	R/W
6	TX_COMPLETE_MASK	Mask Bit for TX_COMPLETE.	0x1	R/W
5	TX_FIFO_ALERT_MASK	Mask Bit for TX_FIFO_ALERT.	0x1	R/W
4	RX_FIFO_ALERT_MASK	Mask Bit for RX_FIFO_ALERT.	0x1	R/W
3	RX_OVERFLOW_ERR_MASK	Mask Bit for RX_OVERFLOW_ERR.	0x1	R/W
2	FRAME_ERR_MASK	Mask Bit for FRAME_ERR.	0x1	R/W
1	PARITY_ERR_MASK	Mask Bit for PARITY_ERR.	0x1	R/W

REGISTER MAP

Table 89. Bit Descriptions for HART_ALERT_MASK

Bits	Bit Name	Description	Reset	Access
0	GAP_ERR_MASK	Mask Bit for GAP_ERR.	0x1	R/W

HART Support Configuration Register

Address: 0x88, Reset: 0xC430, Name: HART_CONFIG

This register is used to configure the HART settings.

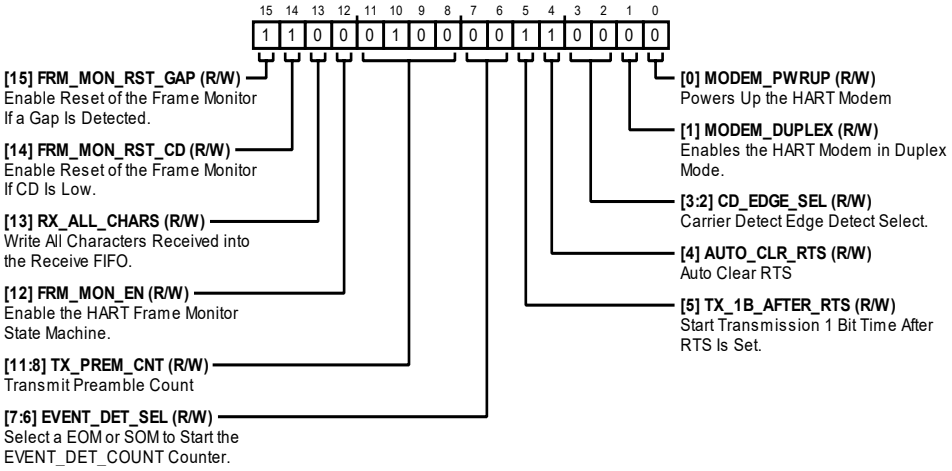


Table 90. Bit Descriptions for HART_CONFIG

Bits	Bit Name	Description	Reset	Access
15	FRM_MON_RST_GAP	Enable Reset of the Frame Monitor If a Gap Is Detected. 0: frame monitor is not reset on detecting a gap. The frame monitor state machine is not reset if a gap is detected. 1: frame monitor is reset on detecting a gap. The frame monitor state machine is reset to the preamble state if a gap is detected.	0x1	R/W
14	FRM_MON_RST_CD	Enable Reset of the Frame Monitor If CD Is Low. 0: frame monitor is not reset on CD low. The frame monitor state machine is not reset when CD goes low. 1: frame monitor is reset on CD low. The frame monitor state machine is reset to the preamble state when CD goes low.	0x1	R/W
13	RX_ALL_CHARS	Write All Characters Received into the Receive FIFO. If 0 and FRM_MON_EN is also set, only valid characters from a frame (as determined by the frame monitor) are written to the receive FIFO. Characters are not written into the receive FIFO until the first byte received after good preamble bytes are received. That is, the delimiter field is the first byte written to the receive FIFO. If 1, all characters received are written to the receive FIFO.	0x0	R/W
12	FRM_MON_EN	Enable the HART Frame Monitor State Machine.	0x0	R/W
[11:8]	TX_PREM_CNT	Transmit Preamble Count. Indicate the number of preamble bytes to transmit at the start of a frame. TX_PREM_CNT × 2 bytes is transmitted. If 0, preamble bytes must be written directly to the transmit FIFO.	0x4	R/W
[7:6]	EVENT_DET_SEL	Select a EOM or SOM to Start the EVENT_DET_COUNT Counter. 00: start the event counter on detecting an EOM on receive. 01: start the event counter on detecting an SOM on receive. 10: start the event counter on detecting transmit complete. 11: start the event counter on detecting an edge on the CD (as configured by CD_EDGE_SEL).	0x0	R/W
5	TX_1B_AFTER_RTS	Start Transmission 1 Bit Time After RTS Is Set. If 1, the frame transmission starts 1 bit time (at 1200 bauds) after RTS is asserted, and there is data in the transmit FIFO. This setting gives the AD5700	0x1	R/W

REGISTER MAP

Table 90. Bit Descriptions for HART_CONFIG

Bits	Bit Name	Description	Reset	Access
		modem 1 bit time to enable the carrier. If 0, the frame transmission starts immediately when data is written to the transmit FIFO, irrespective of the value on RTS.		
4	AUTO_CLR_RTS	Auto Clear RTS. If 1, when frame transmission completes (that is, the last word in the transmit FIFO is transmitted), the RTS signal is automatically deasserted, and the RTS bit of the HART_MCR register goes to 0. If 0, RTS does not go to 0 at the end of frame transmission, and the RTS signal stays asserted. In this case, software must deassert the RTS signal by writing 0 to the RTS bit.	0x1	R/W
[3:2]	CD_EDGE_SEL	Carrier Detect Edge Detect Select. 00: detect a falling edge. 01: detect a rising edge. 10: detect any edge. 11: edges detect disable.	0x0	R/W
1	MODEM_DUPLEX	Enables the HART Modem in Duplex Mode. This enabling allows loop back testing of the modem.	0x0	R/W
0	MODEM_PWRUP	Powers Up the HART Modem.	0x0	R/W

HART Event Detected Count Register

Address: 0x89, Reset: 0x0000, Name: HART_EVDET_COUNT

This register records the time since the last event was detected by the HART modem.

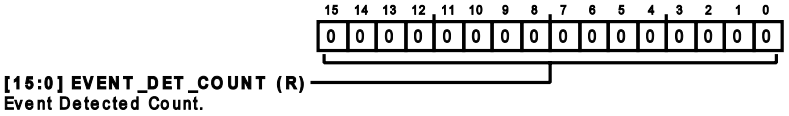


Table 91. Bit Descriptions for HART_EVDET_COUNT

Bits	Bit Name	Description	Reset	Access
[15:0]	EVENT_DET_COUNT	Event Detected Count. Indicates the time since a receive EOM, receive SOM, CD edge, or TX_COMPLETE was detected. The counter increments in steps of 3.255 µs (307.2 kHz). The counter starts incrementing on detecting an EOM, SOM, CD edge (see EVENT_DET_SEL), or TX_COMPLETE. It increments until it reaches 0xFFFF. It stays at 0xFFFF until another event is detected. The maximum duration that the counter can measure is 213 ms. The counter is cleared if FRM_MON_EN is 0. This counter allows the software to more accurately determine when the HART frames start or end.	0x0	R