16-Bit, 6 MSPS, PulSAR Differential ADC

Data Sheet **AD7625**

FEATURES

- Throughput: 6 MSPS
- SNR: 93 dB
- INL: ±0.45 LSB typical, ±1 LSB maximum
- DNL: ±0.3 LSB typical, ±0.5 LSB maximum
- Power dissipation: 135 mW
- 32-lead LFCSP (5 mm × 5 mm)
- SAR architecture
  - No latency/no pipeline delay
- 16-bit resolution with no missing codes
- Zero error: ±1.5 LSB
- Differential input voltage: ±4.096 V
- Serial LVDS interface
  - Self-clocked mode
  - Echoed-clock mode
  - Can use LVDS or CMOS for conversion control (CNV signal)
- Reference options
  - Internal: 4.096 V
  - External (1.2 V) buffered to 4.096 V
  - External: 4.096 V

APPLICATIONS

- High dynamic range telecommunications
- Receivers
- Digital imaging systems
- High speed data acquisition
- Spectrum analysis
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

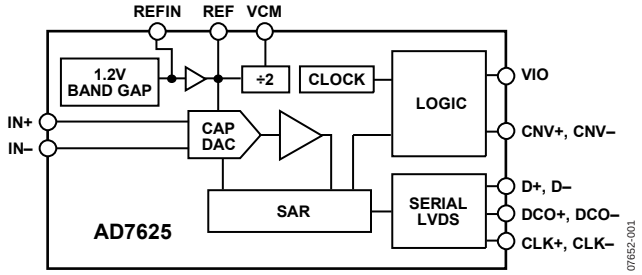

Figure 1.

GENERAL DESCRIPTION

The AD7625 is a 16-bit, 6 MSPS, charge redistribution successive approximation register (SAR) based architecture analog-to-digital converter (ADC). SAR architecture allows unmatched performance both in noise (93 dB SNR) and in linearity (1 LSB). The AD7625 contains a high speed, 16-bit sampling ADC, an internal conversion clock, and an internal buffered reference. On the CNV± rising edge, it samples the voltage difference between the IN+ and IN− pins. The voltages on these pins swing in opposite phase between 0 V and REF. The 4.096 V reference voltage, REF, can be generated internally or applied externally.

All converted results are available on a single LVDS self-clocked or echoed-clock serial interface, reducing external hardware connections.

The AD7625 is housed in a 32-lead, 5 mm × 5 mm LFCSP with operation specified from −40°C to +85°C.

Table 1. Fast PulSAR® ADC Selection

Input Type	Resolution (Bits)	1 MSPS to <2 MSPS	2 MSPS to 3 MSPS	5 MSPS	6 MSPS	10 MSPS
Differential (Ground Sense)	16	AD7653	AD7985			
		AD7667				
		AD7980				
		AD7983				
True Bipolar	16	AD7671				
Differential (Antiphase)	16	AD7677	AD7621		AD7625	AD7626
		AD7623	AD7622	AD7961		
	18	AD7643	AD7641	AD7960		
		AD7982	AD7986			
		AD7984				

Rev. B
Document Feedback

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7/12—Rev. 0 to Rev. A

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1/09—Revision 0: Initial Version

SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.5 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	$V_{IN+} - V_{IN-}$	$-V_{REF}$		$+V_{REF}$	V
Operating Input Voltage	V_{IN+}, V_{IN-} to GND	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range		$V_{REF}/2 - 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V
Common-Mode Rejection Ratio	f_{IN} = 1 MHz		60		dB
Input Current	Midscale input		77		µA
THROUGHPUT					
Complete Cycle				166	ns
Throughput Rate		0.1		6	MSPS
DC ACCURACY					
Integral Linearity Error		−1	±0.45	+1	LSB
No Missing Codes		16			Bits
Differential Linearity Error		−0.5	±0.3	+0.5	LSB
Transition Noise			0.6		LSB
Zero Error	T_{MIN} to T_{MAX}	−4	±1.5	+4	LSB
Zero Error Drift			0.5		ppm/°C
Gain Error	T_{MIN} to T_{MAX}		8	20	LSB
Gain Error Drift			0.4		ppm/°C
Power Supply Sensitivity[1]	VDD1 = 5 V ± 5%		0.4		LSB
	VDD2 = 2.5 V ± 5%		0.2		LSB
AC ACCURACY					
External Reference	f_{IN} = 20 kHz				
Dynamic Range		92.5	93.2		dB
Signal-to-Noise Ratio		92	93		dB
Spurious-Free Dynamic Range			106		dB
Total Harmonic Distortion			−105.5		dB
Signal-to-(Noise + Distortion)		91.5	92		dB
Internal Reference	f_{IN} = 20 kHz				
Dynamic Range		92.5	93.2		dB
Signal-to-Noise Ratio		91.5	92.9		dB
Spurious-Free Dynamic Range			106		dB
Total Harmonic Distortion			−105.5		dB
Signal-to-(Noise + Distortion)		91	92.5		dB
−3 dB Input Bandwidth			100		MHz
Aperture Delay			1.5		ns
Aperture Jitter			0.25		ps rms
INTERNAL REFERENCE					
Output Voltage	REFIN @ 25°C		1.2		V
Temperature Drift	−40°C to +85°C		±15		ppm/°C
REFERENCE BUFFER					
REFIN Input Voltage Range			1.2		V
REF Output Voltage Range		4.076	4.096	4.116	V
Line Regulation	VDD1 ± 5%, VDD2 ± 5%		5		mV
EXTERNAL REFERENCE					
Voltage Range	REF		4.096		V
Current Drain	6 MSPS		590		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCM PIN	@ 25°C				
Output Voltage			REF/2		V
Output Impedance		4	5	6	kΩ
LVDS I/O (ANSI-644)					
Data Format			Serial LVDS twos complement		
Differential Output Voltage, V_{OD}	R_L = 100 Ω	200	350	454	mV
Common-Mode Output Voltage, V_{OCM}[2]	R_L = 100 Ω	850	1250	1375	mV
Differential Input Voltage, V_{ID}		100		650	mV
Common-Mode Input Voltage, V_{ICM}		800		1575	mV
POWER SUPPLIES					
Specified Performance					
VDD1		4.75	5	5.25	V
VDD2		2.37	2.5	2.63	V
VIO		2.37	2.5	2.63	V
Operating Currents					
Static—Not Converting					
VDD1			4.5	7.8	mA
VDD2			17	22.7	mA
VIO	Self-clocked mode and echoed-clock mode		11	13	mA
With Internal Reference	6 MSPS throughput				
VDD1			11	15.4	mA
VDD2			21.5	28.3	mA
VIO	Self-clocked mode and echoed-clock mode		13.5	16	mA
Without Internal Reference	6 MSPS throughput				
VDD1			9	12.1	mA
VDD2			21	26	mA
VIO	Self-clocked mode and echoed-clock mode		13.5	16	mA
Power Dissipation[3]					
Static—Not Converting			95	130	mW
With Internal Reference	6 MSPS throughput		145	190	mW
Without Internal Reference	6 MSPS throughput		135	165	mW
Energy per Conversion	6 MSPS throughput		22		nJ/sample
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

[1] Using an external reference.
[2] The ANSI-644 LVDS specification has a minimum output common mode (V_{OCM}) of 1125 mV.
[3] Power dissipation is for the AD7625 device only. In self-clocked interface mode, 9 mW is dissipated in the 100 Ω terminator. In echoed-clock interface mode, 18 mW is dissipated in two 100 Ω terminators.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 2.5 V; VIO = 2.37 V to 2.63 V; REF = 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions[1]	t_{CYC}	166		10,000	ns
Acquisition Time	t_{ACQ}	40			ns
CNV± High Time	t_{CNVH}	10		40	ns
CNV± to D± (MSB) Delay	t_{MSB}			145	ns
CNV± to Last CLK± (LSB) Delay	t_{CLKL}			110	ns
CLK± Period[2]	t_{CLK}	$(t_{CYC} - t_{MSB} + t_{CLKL})/n$	4	3.33	ns
CLK± Frequency	f_{CLK}		250	300	MHz
CLK± to DCO± Delay (Echoed-Clock Mode)	t_{DCO}	0	4	7	ns
DCO± to D± Delay (Echoed-Clock Mode)	t_D		0	1	ns
CLK± to D± Delay	t_{CLKD}	0	4	7	ns

[1] The maximum time between conversions is 10,000 ns. If CNV± is left idle for a time greater than the maximum value of t_{CYC}, the subsequent conversion result is invalid.
[2] For the minimum CLK period, the window available to read data is $t_{CYC} - t_{MSB} + t_{CLKL}$. Divide this time by the number of bits (n) that are read. In echoed-clock interface mode, n = 16; in self-clocked interface mode, n = 18.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN− to GND[1]	−0.3 V to REF + 0.3 V or ±130 mA
REF[2] to GND	−0.3 V to +6 V
VCM, CAP2 to GND	−0.3 V to +6 V
CAP1, REFIN to GND	−0.3 V to +2.7 V
Supply Voltage	
VDD1	−0.3 V to +6 V
VDD2, VIO	−0.3 V to +3 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Input Current to Any Pin Except Supplies[3]	±10 mA
Operating Temperature Range (Commercial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD	1 kV

[1] See the Analog Inputs section.
[2] Keep CNV+/CNV− low for any external REF voltage > 4.3 V applied to the REF pin.
[3] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_WQ	40	4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

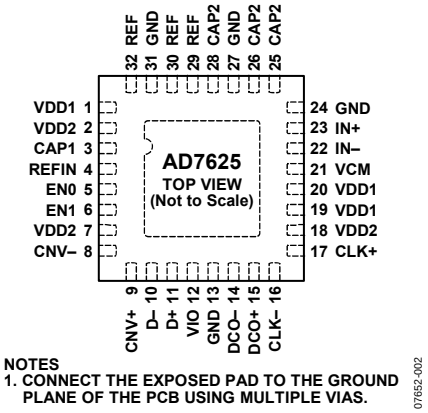


Figure 2.

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VDD1	P	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
2	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor. The 2.5 V supply source should supply this pin first and then be traced to the other VDD2 pins (Pin 7 and Pin 18).
3	CAP1	AO	Connect this pin to a 10 nF capacitor.
4	REFIN	AI/O	Prebuffer Reference Voltage. When using the internal reference, this pin outputs the band gap voltage and is nominally at 1.2 V. It can be overdriven with an external reference voltage such as the ADR280. In either internal or external reference mode, a 10 µF capacitor is required. If using an external 4.096 V reference (connected to REF), this pin is a no connect and does not require any capacitor.
5, 6	EN0, EN1	DI	Enable Pins. The logic levels of these pins set the operation of the device as follows: EN1 = 0, EN0 = 0: Illegal state. EN1 = 0, EN0 = 1: Enable internal buffer, disable internal reference. An external 1.2 V reference connected to the REFIN pin is required. EN1 = 1, EN0 = 0: Disable internal reference and reference buffer. An external 4.096 V reference connected to the REF pin is required. EN1 = 1, EN0 = 1: Enable internal reference and reference buffer.
7	VDD2	P	Digital 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
8, 9	CNV–, CNV+	DI	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV– is grounded; otherwise, CNV+ and CNV– are differential LVDS inputs.
10, 11	D–, D+	DO	LVDS Data Outputs. The conversion data is output serially on these pins.
12	VIO	P	Input/Output Interface Supply. Use a 2.5 V supply and decouple this pin with a 100 nF capacitor.
13	GND	P	Ground. Return path for the 100 nF capacitor connected to Pin 12.
14, 15	DCO–, DCO+	DO	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self-clocked interface mode is selected. In this mode, the 16-bit results on D± are preceded by a 2-bit header (10) to allow synchronization of the data by the digital host with simple logic. When DCO+ is not grounded, the echoed-clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be latched in the digital host on the next rising edge of DCO+.
16, 17	CLK–, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
18	VDD2	P	Analog 2.5 V Supply. Decouple this pin with a 100 nF capacitor.
19, 20	VDD1	P	Analog 5 V Supply. Isolate these pins from Pin 1 with a ferrite bead and decouple them with a 100 nF capacitor.
21	VCM	AO	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
22	IN–	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN–.
24	GND	P	Ground.

Pin No.	Mnemonic	Type[1]	Description
25, 26, 28	CAP2	AO	Connect all three CAP2 pins together and decouple them with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 27 (GND).
27	GND	P	Ground. Return path for the 10 µF capacitor connected to Pin 25, Pin 26, and Pin 28.
29, 30, 32	REF	AI/O	Buffered Reference Voltage. When using the internal reference or the 1.2 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference, such as the ADR434 or the ADR444, the internal reference buffer must be disabled. In either case, connect all three REF pins together and decouple them with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to Pin 31 (GND).
31	GND	P	Ground. Return path for the 10 µF capacitor connected to Pin 29, Pin 30, and Pin 32.
EP	Exposed Pad		The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias. See the Exposed Pad section for more information.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

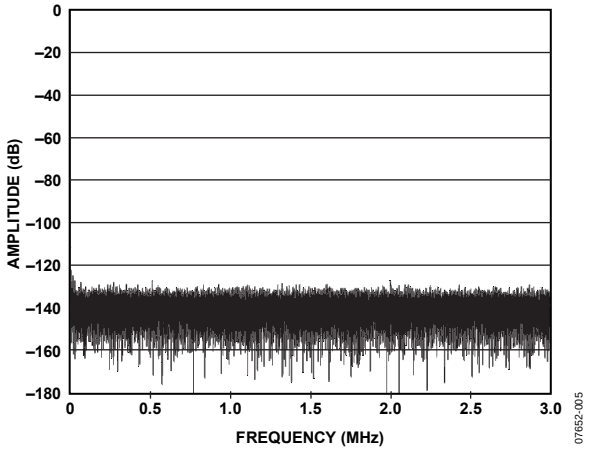


Figure 3. FFT 2 kHz Input Tone, Full View

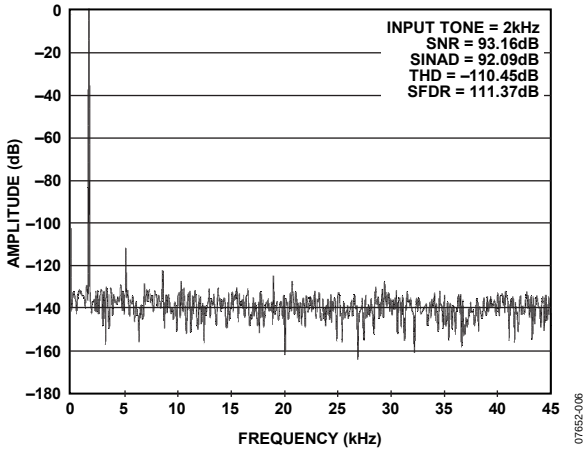


Figure 6. FFT 2 kHz Input Tone, Zoom In on Input Tone and Harmonics

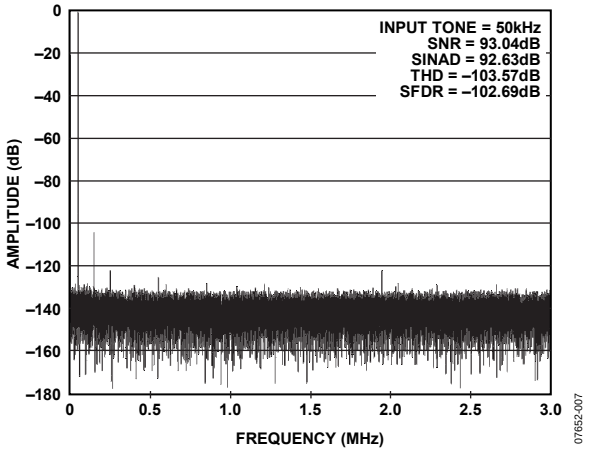


Figure 4. FFT 50 kHz Input Tone

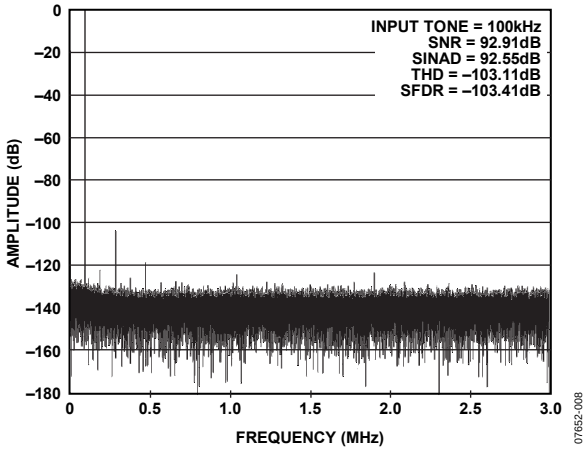


Figure 7. FFT 100 kHz Input Tone

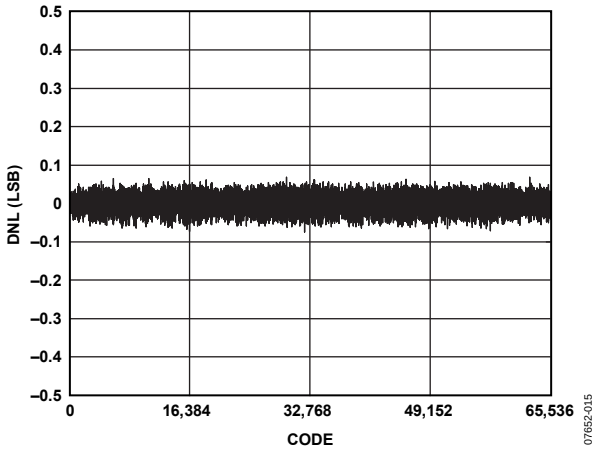


Figure 5. Differential Nonlinearity vs. Code

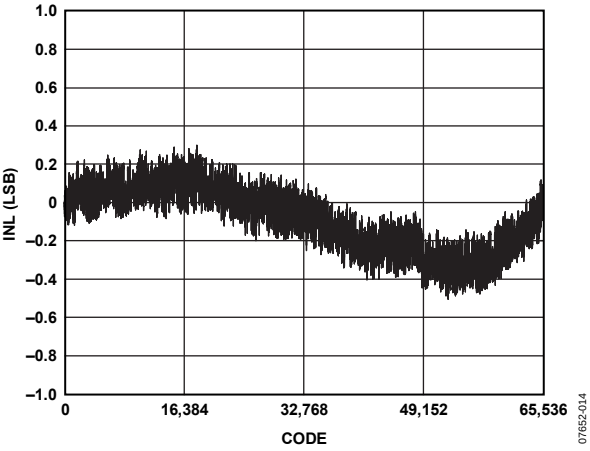


Figure 8. Integral Nonlinearity vs. Code

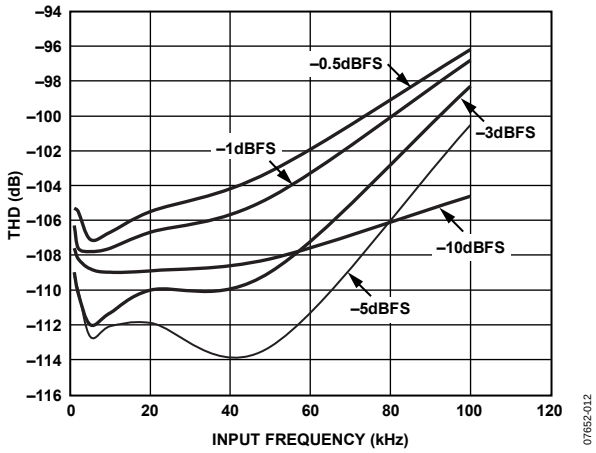


Figure 9. THD at Input Amplitudes of −0.5 dBFS to −10 dBFS vs. Frequency

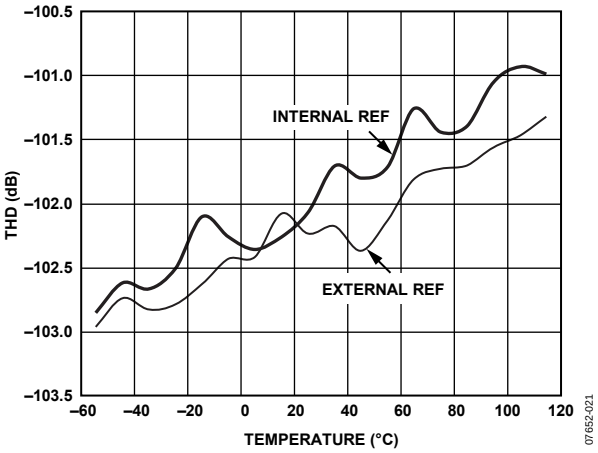


Figure 12. THD vs. Temperature (−0.5 dB, 20 kHz Input Tone)

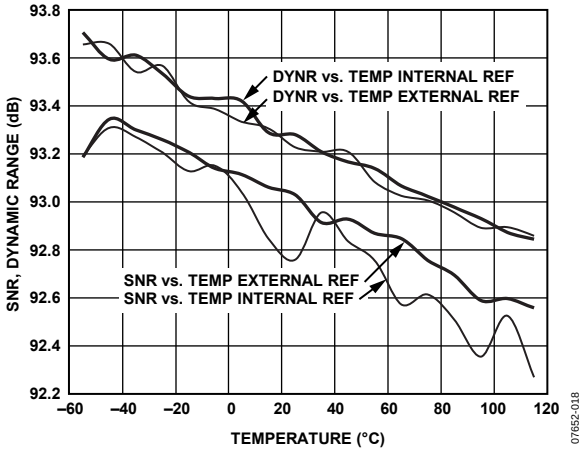


Figure 10. Dynamic Range and SNR vs. Temperature (−0.5 dB, 20 kHz Input Tone)

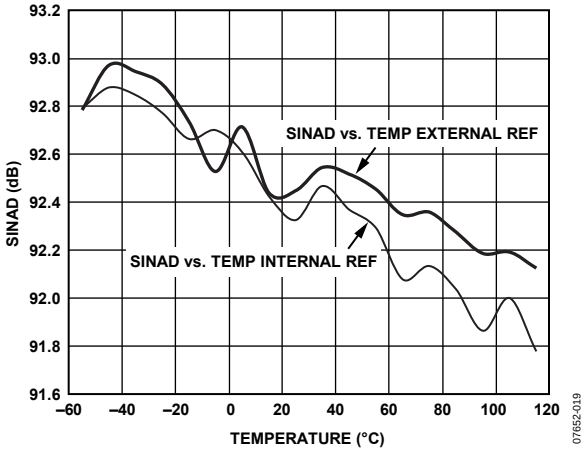


Figure 13. SINAD vs. Temperature (−0.5 dB, 20 kHz Input Tone)

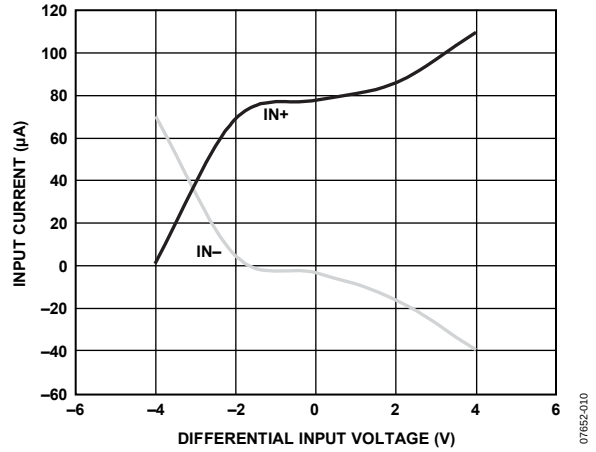


Figure 11. Input Current (IN+, IN−) vs. Differential Input Voltage (6 MSPS)

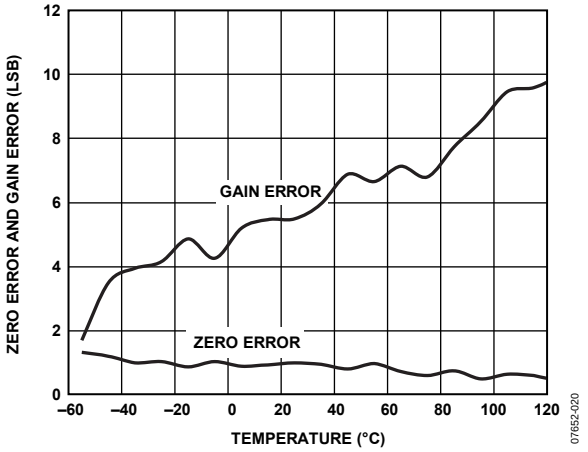


Figure 14. Zero Error and Gain Error vs. Temperature

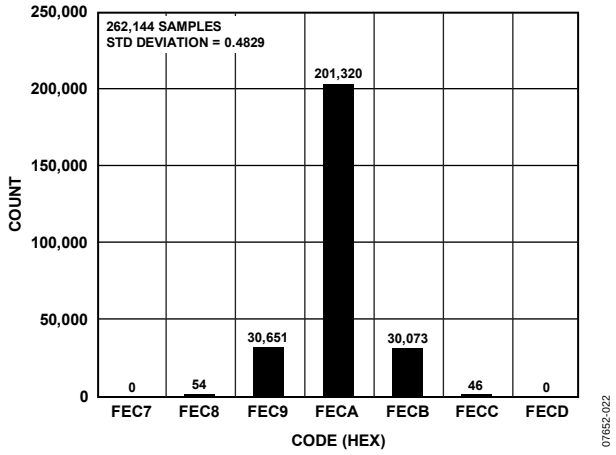


Figure 15. Histogram of 262,144 Conversions of a DC Input at the Code Center (Internal Reference)

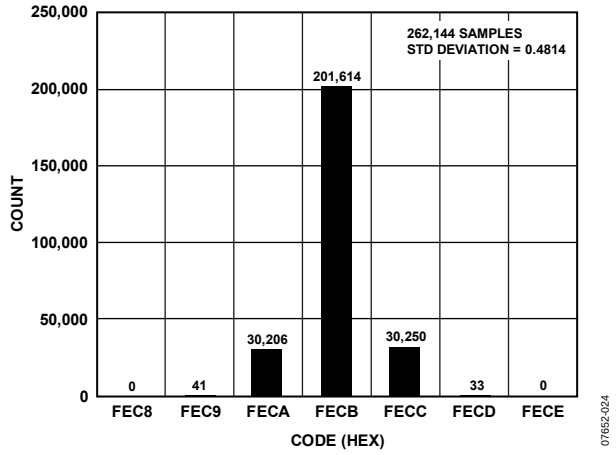


Figure 16. Histogram of 262,144 Conversions of a DC Input at the Code Center (External Reference)

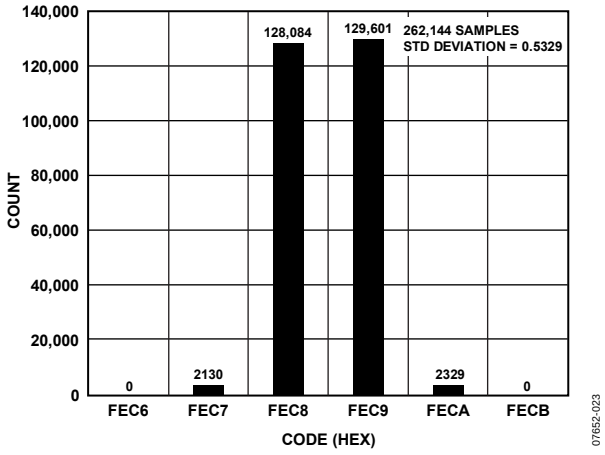


Figure 17. Histogram of 262,144 Conversions of a DC Input at the Code Transition (Internal Reference)

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)

CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of an 80 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} at frequency f_S.

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency f in the ADC output.
Pf_S is the power at frequency f_S in the ADC output.

Differential Nonlinearity (DNL) Error

In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL) Error

Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the rms noise measured for an input typically at −60 dB. The value for dynamic range is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{\text{dB}} - 1.76)/6.02]$$

Gain Error

The first transition (from 100 … 000 to 100 …001) should occur at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Least Significant Bit (LSB)

The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = \frac{V_{IN\ p\text{-}p}}{2^N}$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Reference Voltage Temperature Coefficient

The reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T(25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}\,(Max) - V_{REF}\,(Min)}{V_{REF}\,(25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:
$V_{REF}\,(Max)$ = maximum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}\,(Min)$ = minimum V_{REF} at T_{MIN}, T(25°C), or T_{MAX}.
$V_{REF}\,(25°\text{C})$ = V_{REF} at 25°C.
T_{MAX} = +85°C.
T_{MIN} = −40°C.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Zero Error

Zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

THEORY OF OPERATION

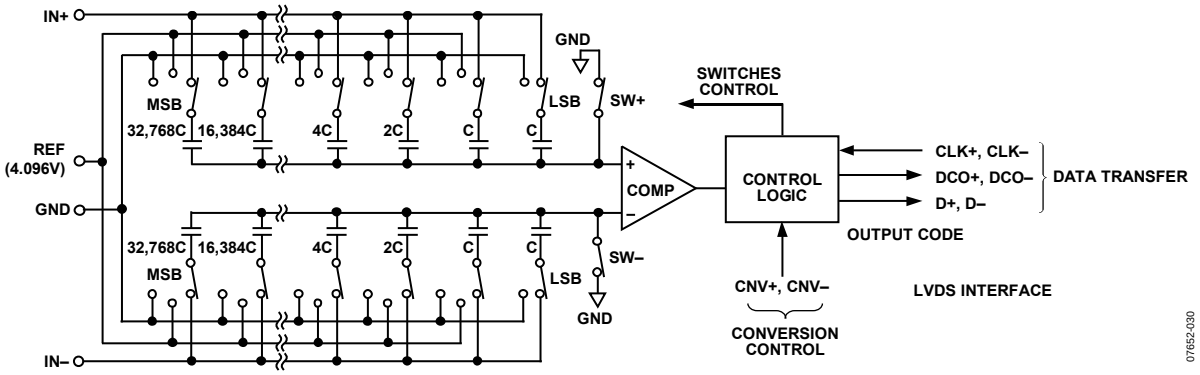


Figure 18. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7625 is a 6 MSPS, high precision, power efficient, 16-bit ADC that uses SAR based architecture to provide performance of 93 dB SNR, ±0.45 LSB INL, and ±0.3 LSB DNL.

The AD7625 is capable of converting 6,000,000 samples per second (6 MSPS). The device typically consumes 135 mW. The AD7625 offers the added functionality of a high performance on-chip reference and on-chip reference buffer.

The AD7625 is specified for use with 5 V and 2.5 V supplies (VDD1, VDD2). The interface from the digital host to the AD7625 uses 2.5 V logic only. The AD7625 uses an LVDS interface to transfer data conversions. The CNV+ and CNV− inputs to the device activate the conversion of the analog input. The CNV+ and CNV− pins can be applied using a CMOS or LVDS source.

The AD7625 is housed in a space-saving, 32-lead, 5 mm × 5 mm LFCSP.

CONVERTER INFORMATION

The AD7625 is a 6 MSPS ADC that uses SAR based architecture incorporating a charge redistribution DAC. Figure 18 shows a simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two comparator inputs.

During the acquisition phase, the terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. In this way, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. A conversion phase is initiated when the acquisition phase is complete and the CNV± input goes logic high. Note that the AD7625 can receive a CMOS (CNV+) or LVDS format (CNV±) signal.

When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and 4.096 V (the reference voltage), the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65,536$). The control logic toggles these switches, MSB first, to bring the comparator back into a balanced condition. At the completion of this process, the control logic generates the ADC output code.

The AD7625 digital interface uses low voltage differential signaling (LVDS) to enable high data transfer rates.

The AD7625 conversion result is available for reading after t_{MSB} (time from the conversion start until MSB is available) has elapsed. The user must apply a burst LVDS CLK± signal to the AD7625 to transfer data to the digital host.

The CLK± signal outputs the ADC conversion result onto the data output D±. The bursting of the CLK± signal is illustrated in Figure 29 and Figure 30 and is characterized as follows: The differential voltage on CLK± should be held to create logic low in the time between t_{CLKL} and t_{MSB}.

The AD7625 has two data read modes. For more information about the echoed-clock and self-clocked interface modes, see the Digital Interface section.

TRANSFER FUNCTIONS

The AD7625 uses a 4.096 V reference. The AD7625 converts the differential voltage of the antiphase analog inputs (IN+ and IN−) into a digital output. The analog inputs, IN+ and IN−, require a 2.048 V common-mode voltage (REF/2).

The 16-bit conversion result is in MSB first, twos complement format.

The ideal transfer functions for the AD7625 are shown in Figure 19 and Table 7.

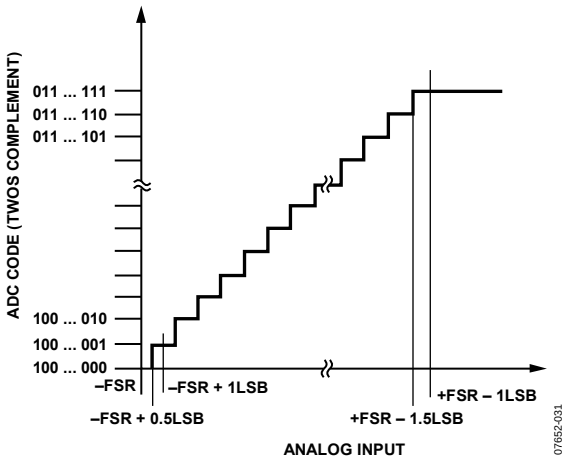


Figure 19. ADC Ideal Transfer Functions (FSR = Full-Scale Range)

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input (IN+ − IN−) REF = 4.096 V	Digital Output Code Twos Complement (Hex)
FSR − 1 LSB	+4.0959375 V	0x1FFF
Midscale + 1 LSB	+62.5 µV	0x0001
Midscale	0 V	0x0000
Midscale − 1 LSB	−62.5 µV	0xFFFF
−FSR + 1 LSB	−4.0959375 V	0x1001
−FSR	−4.096 V	0x1000

ANALOG INPUTS

The analog inputs, IN+ and IN−, applied to the AD7625 must be 180° out of phase with each other. Figure 20 shows an equivalent circuit of the input structure of the AD7625.

The two diodes provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal does not exceed the reference voltage by more than 0.3 V. If the analog input signal exceeds this level, the diodes become forward-biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. However, if the supplies of the input buffer (for example, the supplies of the ADA4899-1 in Figure 24) are different from those of the reference, the analog input signal may eventually exceed the supply rails by more than 0.3 V. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the device.

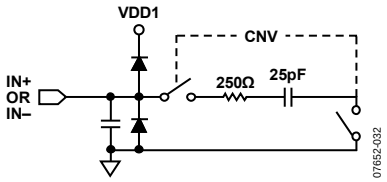


Figure 20. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected. The AD7625 shows some degradation in THD with higher analog input frequencies.

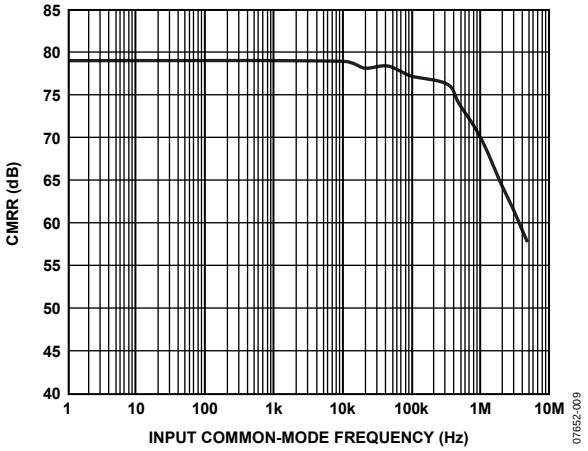
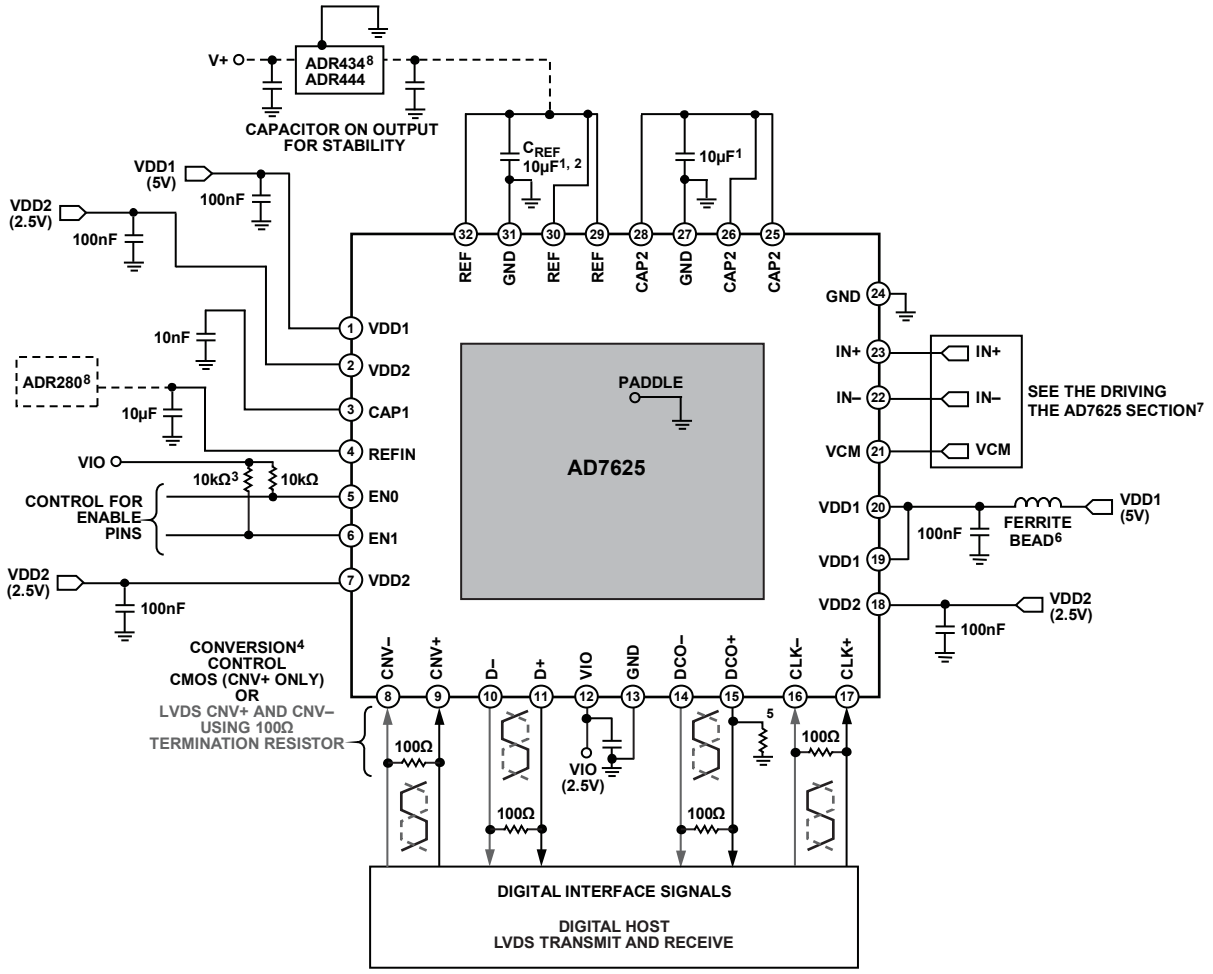


Figure 21. Analog Input CMRR vs. Frequency

TYPICAL CONNECTION DIAGRAM



[1] SEE THE LAYOUT, DECOUPLING, AND GROUNDING SECTION.
[2] C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR WITH LOW ESR AND ESL.
[3] USE PULL-UP OR PULL-DOWN RESISTORS TO CONTROL EN0, EN1 DURING POWER-UP. EN0 AND EN1 INPUTS CAN BE FIXED IN HARDWARE OR CONTROLLED USING A DIGITAL HOST (EN0 = 0 AND EN1 = 0 IS AN ILLEGAL STATE).
[4] OPTION TO USE A CMOS (CNV+) OR LVDS (CNV±) INPUT TO CONTROL CONVERSIONS.
[5] TO ENABLE SELF-CLOCKED MODE, TIE DCO+ TO GND USING A PULL-DOWN RESISTOR.
[6] CONNECT PIN 19 AND PIN 20 TO VDD1 SUPPLY; ISOLATE FROM PIN 1 USING A FERRITE BEAD SIMILAR TO WURTH 74279266.
[7] SEE THE DRIVING THE AD7625 SECTION FOR DETAILS ON AMPLIFIER CONFIGURATIONS.
[8] SEE THE VOLTAGE REFERENCE OPTIONS SECTION FOR DETAILS.

07652-027

Figure 22. Typical Application Diagram

DRIVING THE AD7625

Differential Analog Input Source

Figure 24 shows an ADA4899-1 driving each differential input to the AD7625.

Single-Ended-to-Differential Driver

For applications using unipolar analog signals, a single-ended-to-differential driver, as shown in Figure 23, allows for a differential input into the device. This configuration, when provided with an input signal of 0 V to 4.096 V, produces a differential ±4.096 V with midscale at 2.048 V. The one-pole filter using R = 33 Ω and C = 56 pF provides a corner frequency of 86 MHz. The VCM output of the AD7625 can be buffered and then used to provide the required 2.048 V common-mode voltage.

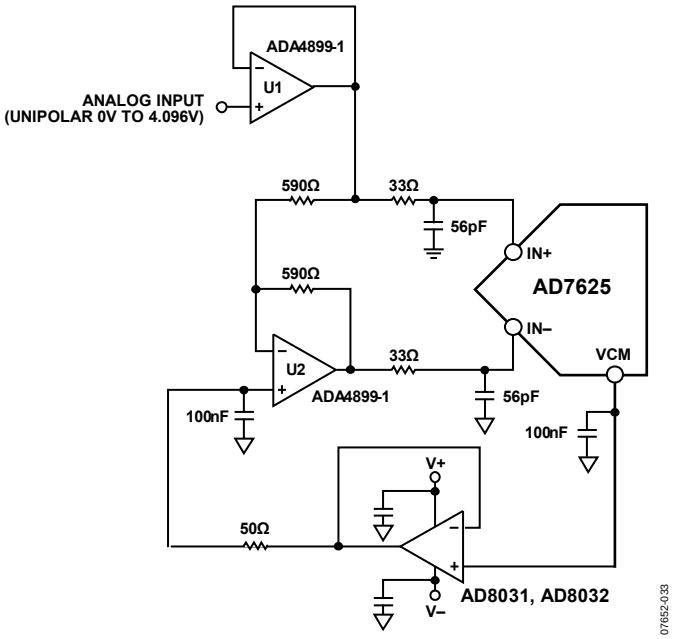
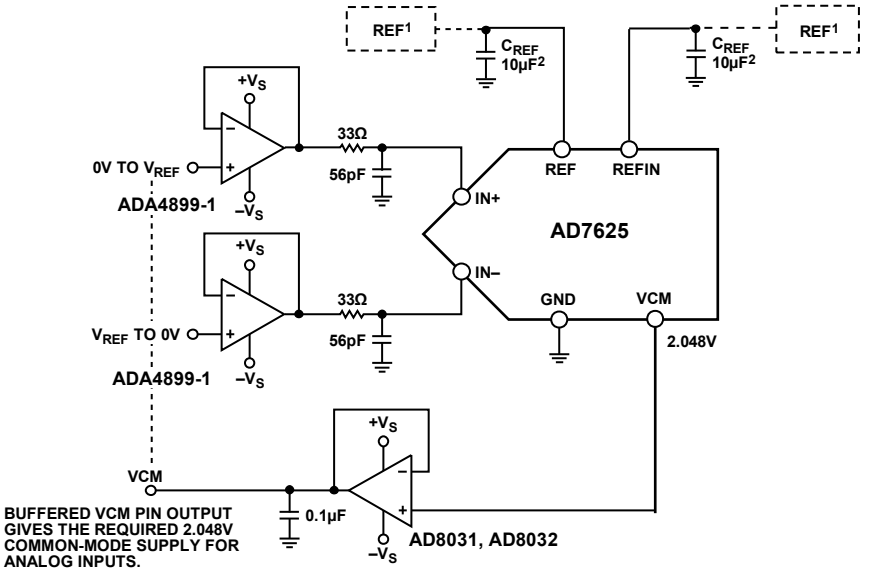


Figure 23. Single-Ended-to-Differential Driver Circuit



[1]SEE THE VOLTAGE REFERENCE OPTIONS SECTION. CONNECTION TO EXTERNAL REFERENCE SIGNALS IS DEPENDENT ON THE EN1 AND EN0 SETTINGS.
[2]C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR WITH LOW ESL AND ESR. THE REF AND REFIN PINS ARE DECOUPLED REGARDLESS OF EN1 AND EN0 SETTINGS.

Figure 24. Driving the AD7625 from a Differential Analog Source

VOLTAGE REFERENCE OPTIONS

The AD7625 allows flexible options for creating and buffering the reference voltage. The AD7625 conversions refer to 4.096 V only. The various options creating this 4.096 V reference are controlled by the EN1 and EN0 pins (see Table 8).

Table 8. Voltage Reference Options[1]

Option	EN1	EN0	Reference Mode
A	1	1	Use internal reference and internal reference buffer (both are enabled).
B	0	1	Use external 1.2 V reference with internal reference buffer enabled. The internal reference is disabled.
C	1	0	Use external 4.096 V reference with an external reference buffer. The internal reference and reference buffer are disabled.

[1] EN1 = 0 and EN0 = 0 is an illegal state.

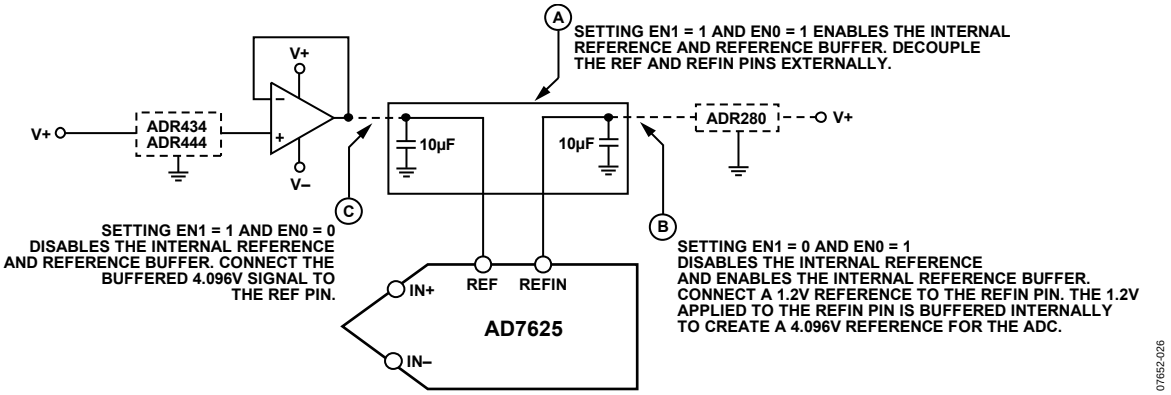


Figure 25. Voltage Reference Options

POWER SUPPLY

The AD7625 uses both 5 V (VDD1) and 2.5 V (VDD2) power supplies, as well as a digital input/output interface supply (VIO). VIO allows a direct interface with 2.5 V logic only. VIO and VDD2 can be taken from the same 2.5 V source; however, it is best practice to isolate the VIO and VDD2 pins using separate traces and also to decouple each pin separately.

The 5 V and 2.5 V supplies required for the AD7625 can be generated using Analog Devices, Inc., low dropout regulators (LDOs) such as the ADP3330-2.5, ADP3330-5, ADP3334, and ADP1708.

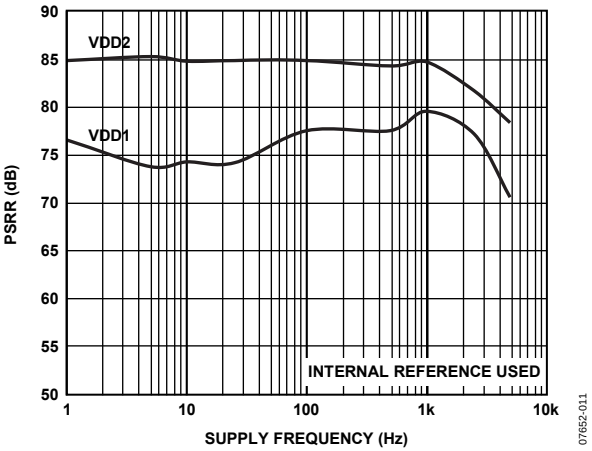


Figure 26. PSRR vs. Supply Frequency (350 mV pp Ripple on VDD2, 600 mV Ripple on VDD1)

Power-Up

When powering up the AD7625 device, first apply the VIO voltage to the device so that the EN1 and EN0 values can be set for the reference option in use. Connect the EN0 and EN1 pins to pull-up/pull-down resistors to ensure that one or both of these pins is set to a nonzero value. EN0 = 0 and EN1 = 0 is an illegal state that must be avoided.

After VIO is established, apply the 2.5 V VDD2 supply to the device followed by the 5 V VDD1 supply and then an external reference (depending on the reference setting being used). Finally, apply the analog inputs to the ADC.

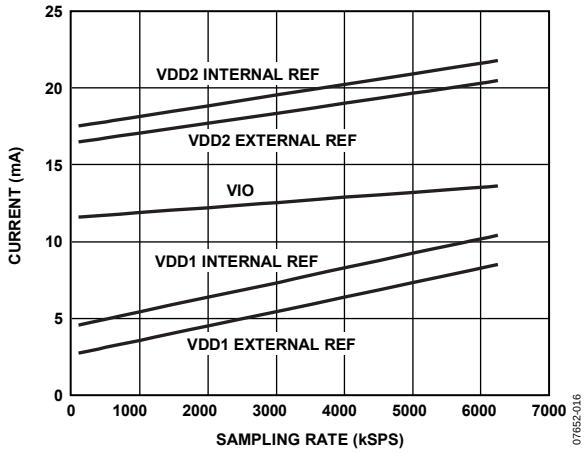


Figure 27. Current Consumption vs. Sampling Rate

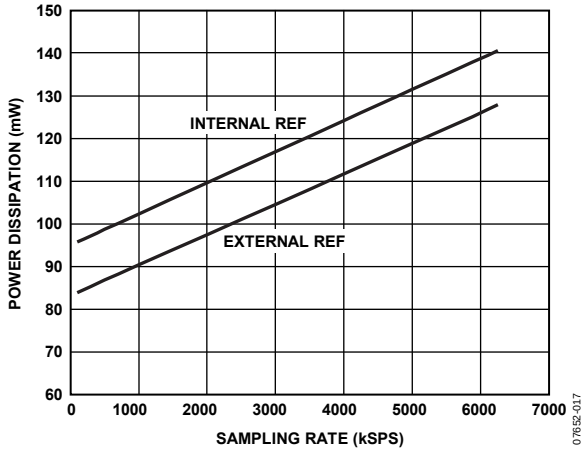


Figure 28. Power Dissipation vs. Sampling Rate

DIGITAL INTERFACE

Conversion Control

All analog-to-digital conversions are controlled by the CNV signal. This signal can be applied in the form of a CNV+/CNV− LVDS signal, or it can be applied in the form of a 2.5 V CMOS logic signal to the CNV+ pin. The conversion is initiated by the rising edge of the CNV signal.

After the AD7625 is powered up, the first conversion result generated is invalid. Subsequent conversion results are valid provided that the time between conversions does not exceed the maximum specification for t_{CYC}.

The two methods for acquiring the digital data output of the AD7625 via the LVDS interface are described in the following sections.

Echoed-Clock Interface Mode

The digital operation of the AD7625 in echoed-clock interface mode is shown in Figure 29. This interface mode, requiring only a shift register on the digital host, can be used with many digital hosts (FPGA, shift register, microprocessor, and so on). It requires three LVDS pairs (D±, CLK±, and DCO±) between each AD7625 and the digital host.

The clock DCO± is a buffered copy of CLK± and is synchronous to the data, D±, which is updated on the falling edge of DCO+ (t_D). By maintaining good propagation delay matching between D± and DCO± through the board and the digital host, DCO± can be used to latch D± with good timing margin for the shift register.

Conversions are initiated by a CNV± pulse. The CNV± pulse must be returned low (≤t_{CNVH} maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK±. Note that t_{MSB} is the maximum time for the MSB of the new conversion result and should be used as the gating device for CLK±. The echoed clock, DCO±, and the data, D±, are driven in phase, with D± being updated on the falling edge of DCO+; the host should use the rising edge of DCO+ to capture D±. The only requirement is that the 16 CLK pulses finish before the time t_{CLKL} elapses for the next conversion phase or the data is lost. From the time t_{CLKL} to t_{MSB}, D± and DCO± are driven to 0s. Set CLK± to idle low between CLK± bursts.

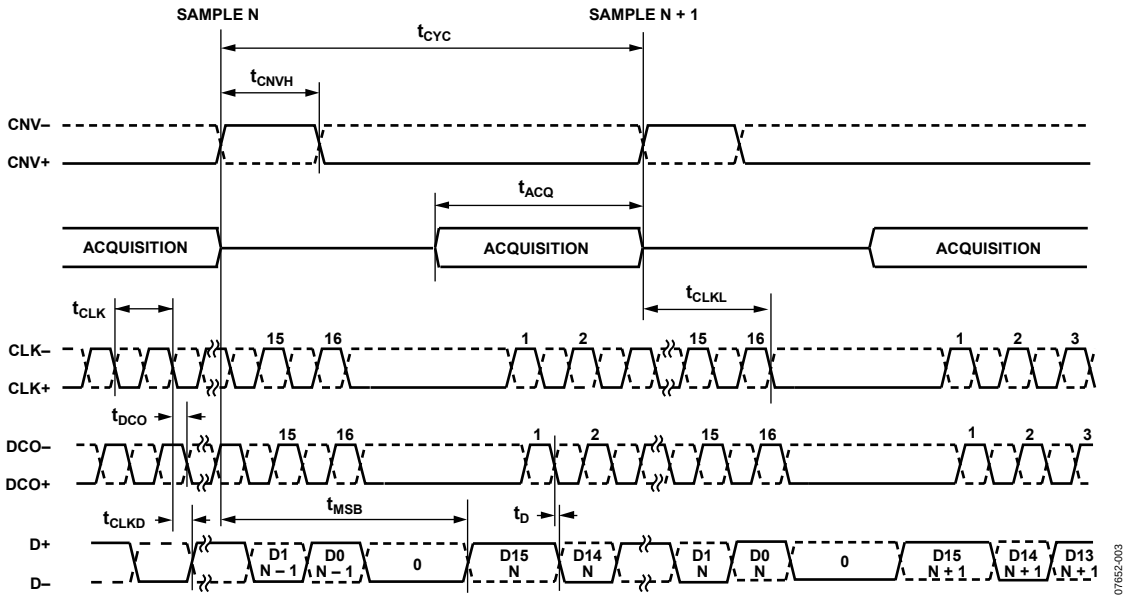


Figure 29. Echoed-Clock Interface Mode Timing Diagram

Self-Clocked Interface Mode

The digital operation of the AD7625 in self-clocked interface mode is shown in Figure 30. This interface mode reduces the number of wires between ADCs and the digital host to two LVDS pairs per AD7625 (CLK± and D±) or to a single pair if sharing a common CLK± using multiple AD7625 devices. Self-clocked interface mode facilitates the design of boards that use multiple AD7625 devices. The digital host can adapt the interfacing scheme to account for differing propagation delays between each AD7625 device and the digital host.

The self-clocked interface mode consists of preceding the results of each ADC word with a 2-bit header on the data, D±. This header is used to synchronize D± of each conversion in the digital host. Synchronization is accomplished by one simple state machine per AD7625 device. For example, if the state machine is running at the same speed as CLK± with three phases, the state machine measures when the Logic 1 of the header occurs.

Conversions are initiated by a CNV± pulse. The CNV± pulse must be returned low ($\leq t_{CNVH}$ maximum) for valid operation. After a conversion begins, it continues until completion. Additional CNV± pulses are ignored during the conversion phase. After the time t_{MSB} elapses, the host should begin to burst the CLK±. Note that t_{MSB} is the maximum time for the first bit of the header and should be used as the gating device for CLK±. CLK± is also used internally on the host to begin the internal synchronization state machine. The next header bit and conversion results are output on subsequent falling edges of CLK±. The only requirement is that the 18 CLK± pulses finish before the time t_{CLKL} elapses for the next conversion phase or the data is lost. Set CLK± to idle high between bursts of 18 CLK± pulses.

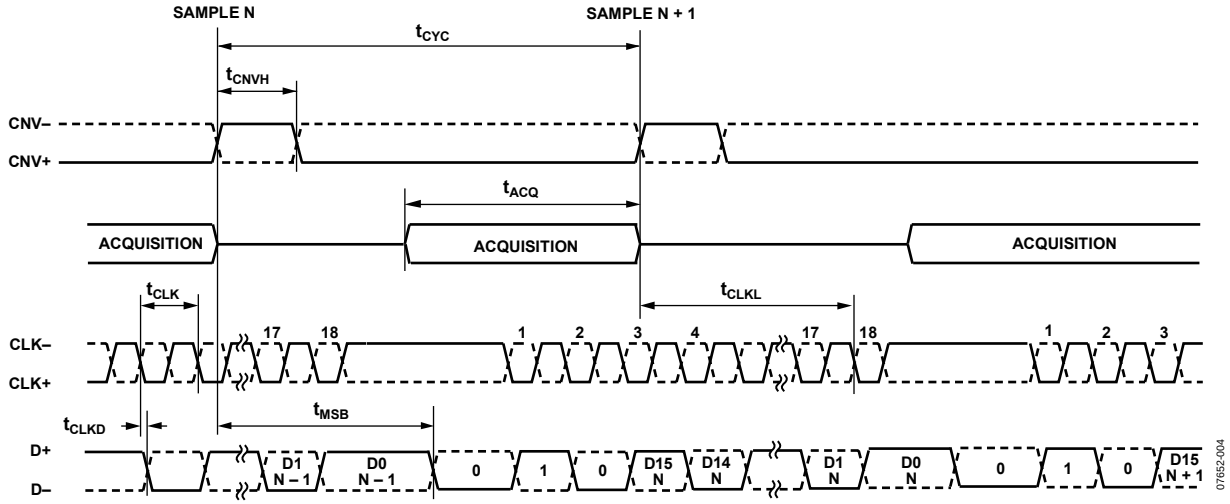


Figure 30. Self-Clocked Interface Mode Timing Diagram

APPLICATIONS INFORMATION

LAYOUT, DECOUPLING, AND GROUNDING

When laying out the printed circuit board (PCB) for the AD7625, follow the practices described in this section to obtain the maximum performance from the converter.

Exposed Pad

The AD7625 has an exposed pad on the underside of the package.

- Solder the pad directly to the PCB.
- Connect the pad to the ground plane of the board using multiple vias, as shown in Figure 31.
- Decouple all supply pins except for Pin 12 (VIO) directly to the pad, minimizing the current return path.
- Pin 13 and Pin 24 can be connected directly to the pad. Use vias to ground at the point where these pins connect to the pad.

VDD1 Supply Routing and Decoupling

The VDD1 supply is connected to Pin 1, Pin 19, and Pin 20. The supply should be decoupled using a 100 nF capacitor at Pin 1. The user can connect this supply trace to Pin 19 and Pin 20. Use a series ferrite bead to connect the VDD1 supply from Pin 1 to Pin 19 and Pin 20. The ferrite bead isolates any high frequency noise or ringing on the VDD1 supply. Decouple the VDD1 supply to Pin 19 and Pin 20 using a 100 nF capacitor to GND. This GND connection can be placed a short distance away from the exposed pad.

VIO Supply Decoupling

Decouple the VIO supply applied to Pin 12 to ground at Pin 13.

Layout and Decoupling of Pin 25 to Pin 32

Connect the outputs of Pin 25, Pin 26, and Pin 28 together and decouple them to Pin 27 using a 10 µF capacitor with low ESR and low ESL.

Reduce the inductance of the path connecting Pin 25, Pin 26, and Pin 28 by widening the PCB traces connecting these pins.

A similar approach should be taken in the connections used for the reference pins of the AD7625. Connect Pin 29, Pin 30, and Pin 32 together using widened PCB traces to reduce inductance. In internal or external reference mode, a 4.096 V reference voltage is output on Pin 29, Pin 30, and Pin 32. Decouple these pins to Pin 31 using a 10 µF capacitor with low ESR and low ESL.

Figure 31 shows an example of the recommended layout for the underside of the AD7625 device. Note the extended signal trace connections and the outline of the capacitors decoupling the signals applied to the REF pins (Pin 29, Pin 30, and Pin 32) and to the CAP2 pins (Pin 25, Pin 26, and Pin 28).

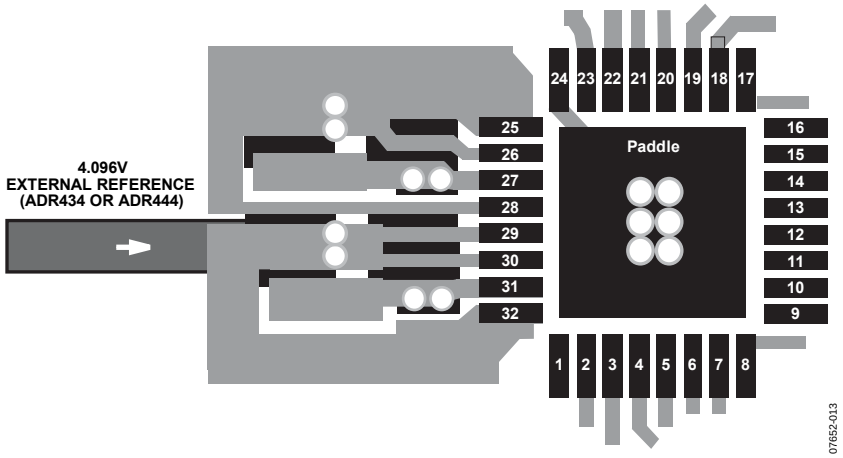
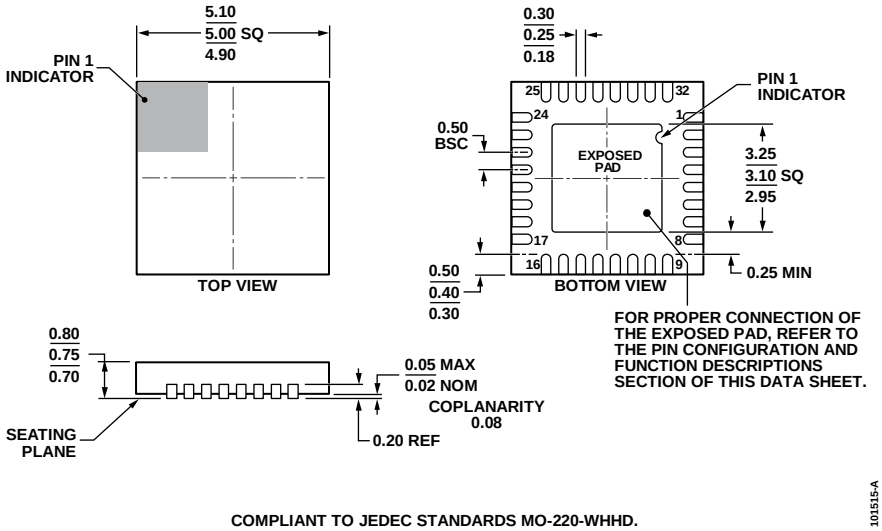


Figure 31. PCB Layout and Decoupling Recommendations for Pin 24 to Pin 32

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 32. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD7625BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
AD7625BCPZRL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-7
EVAL-AD7625FMCZ		Evaluation Board	
EVAL-SDP-CH1Z		Controller Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-SDP-CH1Z board allows the PC to control and communicate with all Analog Devices evaluation boards with model numbers ending with the FMC designator.

NOTES