14-Bit, 250 kSPS PulSAR, Pseudo Differential ADC in MSOP/LFCSP

Data Sheet **AD7942**

FEATURES

- 14-bit resolution with no missing codes
- Throughput: 250 kSPS
- INL: ±0.4 LSB typical, ±1 LSB maximum (±0.0061% of FSR)
- SINAD: 85 dB at 20 kHz
- THD: −100 dB at 20 kHz
- Pseudo differential analog input range
  - 0 V to V_{REF} with V_{REF} up to VDD
- No pipeline delay
- Single-supply 2.3 V to 5.5 V operation with
  - 1.8 V/2.5 V/3 V/5 V logic interface
- Proprietary serial interface
  - SPI-/QSPI-/MICROWIRE-/DSP-compatible[1]
- Daisy-chaining for multiple ADCs and busy indicator
- Power dissipation
  - 1.25 mW at 2.5 V/100 kSPS, 3.6 mW at 5 V/100 kSPS
  - 1.25 µW at 2.5 V/100 SPS
- Standby current: 1 nA
- 10-lead package: MSOP and 3 mm × 3 mm LFCSP
- Pin-for-pin compatible with the 16-bit AD7685

APPLICATIONS

- Battery-powered equipment
- Data acquisition
- Instrumentation
- Medical instruments
- Process controls

APPLICATION DIAGRAM

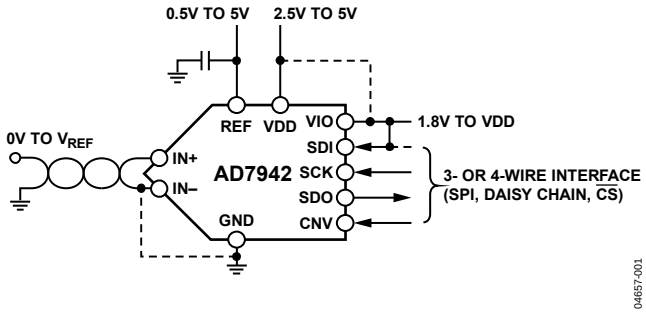


Figure 1.

GENERAL DESCRIPTION

The AD7942 is a 14-bit, charge redistribution, successive approximation PulSAR® ADC that operates from a single power supply, VDD, between 2.3 V to 5.5 V. It contains a low power, high speed, 14-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, it samples an analog input, IN+, between 0 V to V_{REF} with respect to a ground sense, IN−. The reference voltage, V_{REF}, is applied externally and is set up to be the supply voltage. Its power scales linearly with the throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. It is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic using a separate supply (VIO).

The AD7942 is housed in a 10-lead MSOP or a 10-lead LFCSP package yet fits in the same size footprint as the 8-lead MSOP or SOT-23. Operation for the AD7942 is specified from −40°C to +85°C.

[1] Protected by U.S. Patent 6,703,961.

Table 1. MSOP, LFCSP/SOT-23, 14-/16-/18-Bit ADCs

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	≥1000 kSPS	ADC Driver
14-Bit	AD7940	AD7942[1]	AD7946[1]		
16-Bit	AD7680	AD7685[1]	AD7686[1]	AD7980[1]	ADA4941-x
	AD7683	AD7687[1]	AD7688[1]	AD7983[1]	ADA4841-x
	AD7684	AD7694	AD7693[1]		
18-Bit		AD7691[1]	AD7690[1]	AD7982[1]	ADA4941-x
				AD7984[1]	ADA4841-x

[1] Pin-for-pin compatible to the AD7942.

Rev. C
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/14—Rev. B to Rev. C

Changed QFN (LFCSP) Notation to LFCSP ... Throughout
Added Patent Footnote ... 1
Changes to Evaluating the Performance of the AD7942 ... 23
Changes to Ordering Guide ... 24

6/08—Rev. A to Rev. B

Changes to Features Section and General Description Section ... 1
Moved Figure 2 and Figure 3 ... 6
Changes to Table 6 ... 8
Moved Terminology Section ... 12
Changes to Figure 41 ... 22
Changes to Ordering Guide ... 24

12/07—Rev. 0 to Rev. A

Changes to Table 1 ... 1
Changes to General Description Section ... 1
Changes to Table 6 ... 7
Changes to Table 7 ... 8
Changes to Circuit Information Section ... 13
Changes to Table 9 ... 15
Changes to Figure 39 ... 21
Changes to Figure 41 ... 22
Updated Outline Dimensions ... 24
Changes to Ordering Guide ... 24

3/05—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 2.3 V to VDD, V_{REF} = VDD, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		14			Bits
ANALOG INPUT					
Voltage Range	IN+ − IN−	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		VDD + 0.1	V
	IN−	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		65		dB
Leakage Current	T_A = 25°C, acquisition phase		1		nA
Input Impedance		See the Analog Input section			
ACCURACY					
No Missing Codes		14			Bits
Differential Linearity Error		−0.7	±0.3	+0.7	LSB[1]
Integral Linearity Error		−1	±0.4	+1	LSB
Transition Noise	V_{REF} = VDD = 5 V		0.33		LSB
Gain Error[2], T_{MIN} to T_{MAX}			±0.7	±6	LSB
Gain Error Temperature Drift			±1		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}	VDD = 4.5 V to 5.5 V		±0.45	±3	mV
	VDD = 2.3 V to 4.5 V		±0.75	±4.5	mV
Offset Temperature Drift			±2.5		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.1		LSB
THROUGHPUT					
Conversion Rate	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
Transient Response	Full-scale step			1.8	µs
AC ACCURACY					
Signal-to-Noise Ratio (SNR)	f_{IN} = 20 kHz, V_{REF} = 5 V	84.5	85		dB[3]
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		84		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 20 kHz		−100		dB
Total Harmonic Distortion (THD)	f_{IN} = 20 kHz		−100		dB
Signal-to-Noise and Distortion Ratio (SINAD)	f_{IN} = 20 kHz, V_{REF} = 5 V	83	85		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		25		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V		84		dB
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	250 kSPS, V_{REF} = 5 V		50		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			2		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
Data Format			Serial 14 bits straight binary		
Pipeline Delay			Conversion results available immediately after completed conversion		
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[4, 5]	VDD and VIO = 5 V, at 25°C		1	50	nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.25		µW
	VDD = 2.5 V, 100 kSPS throughput		1.25	2	mW
	VDD = 2.5 V, 200 kSPS throughput		2.5	4	mW
	VDD = 5 V, 100 kSPS throughput		3.6	5	mW
	VDD = 5 V, 250 kSPS throughput			12.5	mW
TEMPERATURE RANGE[6]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] LSB means least significant bit. With a 5 V input range, 1 LSB = 305.2 µV.
[2] See the Terminology section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.
[3] All specifications in decibels are referred to a full-scale input, FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4] With all digital inputs forced to VIO or GND as required.
[5] During acquisition phase.
[6] Contact Analog Devices, Inc., sales for an extended temperature range.

TIMING SPECIFICATIONS

VDD = 4.5 V to 5.5 V[1], VIO = 2.3 V to 5.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated, T_A = −40°C to +85°C.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Available Data	t_{CONV}	0.5		2.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	4			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO ≥ 4.5 V		17			ns
VIO ≥ 3 V		18			ns
VIO ≥ 2.7 V		19			ns
VIO ≥ 2.3 V		20			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data-Valid Delay	t_{DSDO}				
VIO ≥ 4.5 V				14	ns
VIO ≥ 3 V				15	ns
VIO ≥ 2.7 V				16	ns
VIO ≥ 2.3 V				17	ns
CNV or SDI Low to SDO D13 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO ≥ 4.5 V				15	ns
VIO ≥ 2.7 V				18	ns
VIO ≥ 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	5			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$				
VIO ≥ 4.5 V				15	ns
VIO ≥ 2.3 V				26	ns

[1] See Figure 2 and Figure 3 for load conditions.

VDD = 2.3 V to 4.5 V[1], VIO = 2.3 V to 4.5 V or VDD + 0.3 V, whichever is the lowest, unless otherwise stated, T_A = −40°C to +85°C.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.7		3.2	µs
Acquisition Time	t_{ACQ}	1.8			µs
Time Between Conversions	t_{CYC}	5			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	25			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO ≥ 3 V		29			ns
VIO ≥ 2.7 V		35			ns
VIO ≥ 2.3 V		40			ns
SCK Low Time	t_{SCKL}	12			ns
SCK High Time	t_{SCKH}	12			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO ≥ 3 V				24	ns
VIO ≥ 2.7 V				30	ns
VIO ≥ 2.3 V				35	ns
CNV or SDI Low to SDO D13 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO ≥ 2.7 V				18	ns
VIO ≥ 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	30			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	8			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	5			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with Busy Indicator)	$t_{DSDOSDI}$			36	ns

[1] See Figure 2 and Figure 3 for load conditions.

Timing Diagrams

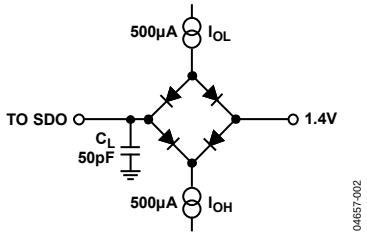


Figure 2. Load Circuit for Digital Interface Timing

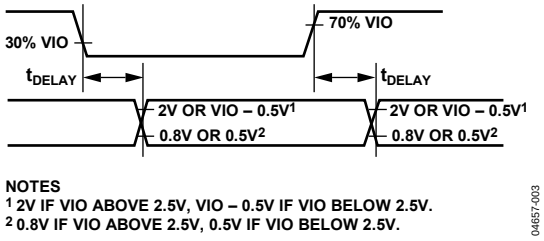


Figure 3. Voltage Reference Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+[1], IN−[1]	GND − 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND − 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD and VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
10-Lead MSOP	200°C/W
10-Lead LFCSP_WD	48.7°C/W
θ_{JC} Thermal Impedance	
10-Lead MSOP	44°C/W
10-Lead LFCSP_WD	2.96°C/W
Lead Temperature	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] See the Analog Input section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

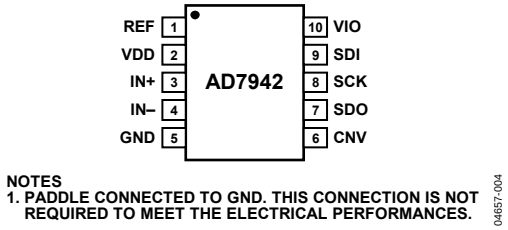


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The V_{REF} range is from 0.5 V to VDD. REF is referred to the GND pin. Decouple REF as closely as possible to a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Analog Input. IN+ is referred to IN−. The voltage range, that is, the difference between IN+ and IN−, is 0 V to V_{REF}.
4	IN−	AI	Analog Input Ground Sense. Connect IN− to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input pin has multiple functions. On its leading edge, CNV initiates the conversions and selects the interface mode of the part: chain mode or $\overline{CS}$ mode. In $\overline{CS}$ mode, CNV enables the SDO pin when low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 14 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low, and if SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).

[1] AI = analog input, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

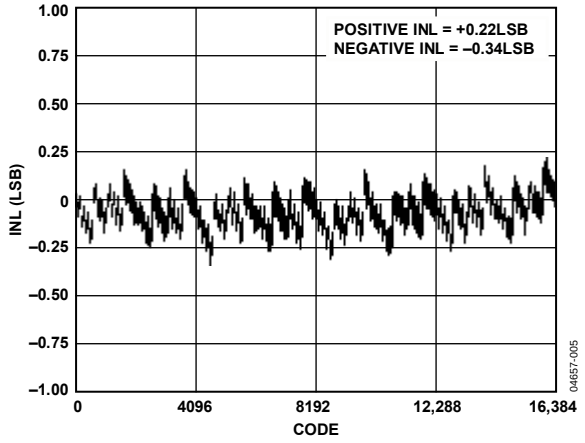


Figure 5. Integral Nonlinearity vs. Code

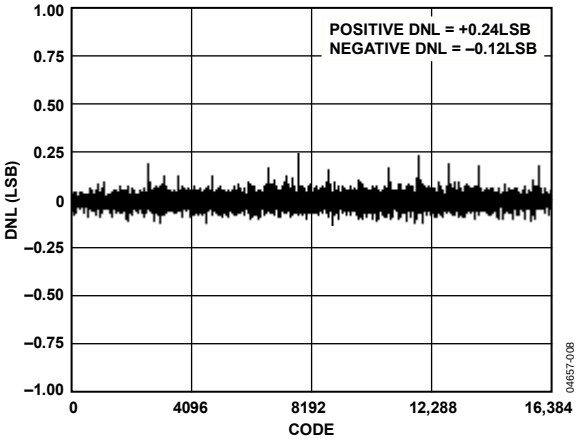


Figure 8. Differential Nonlinearity vs. Code

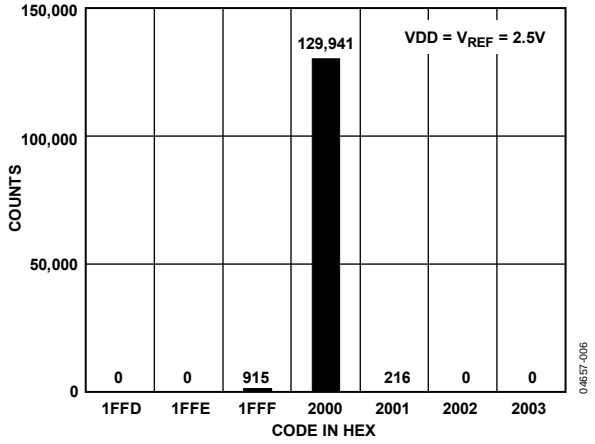


Figure 6. Histogram of a DC Input at the Code Center

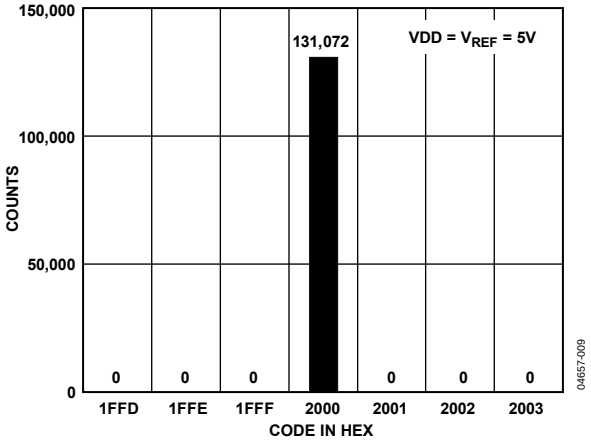


Figure 9. Histogram of a DC Input at the Code Center

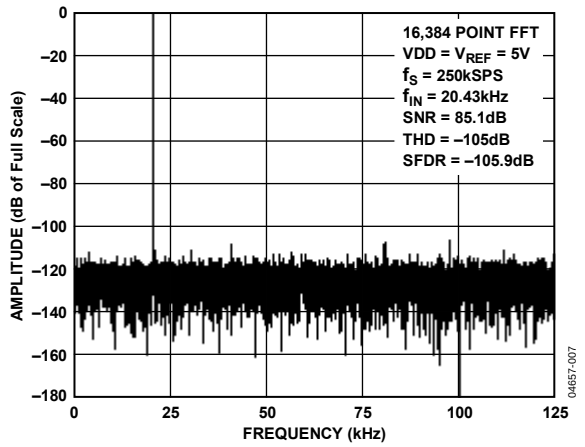


Figure 7. FFT Plot

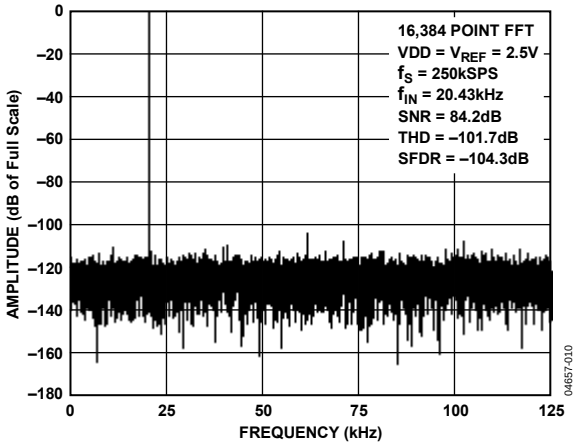


Figure 10. FFT Plot

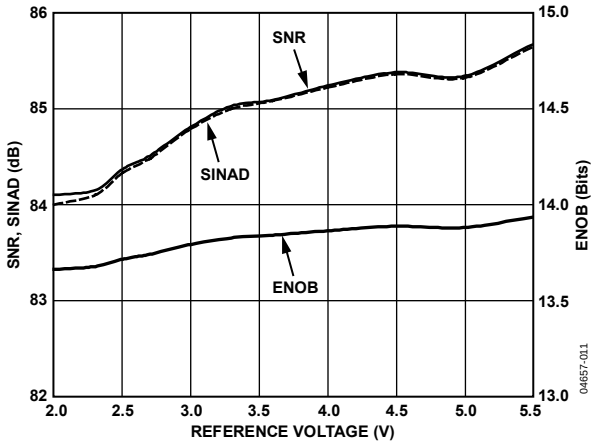


Figure 11. SNR, SINAD, and ENOB vs. Reference Voltage

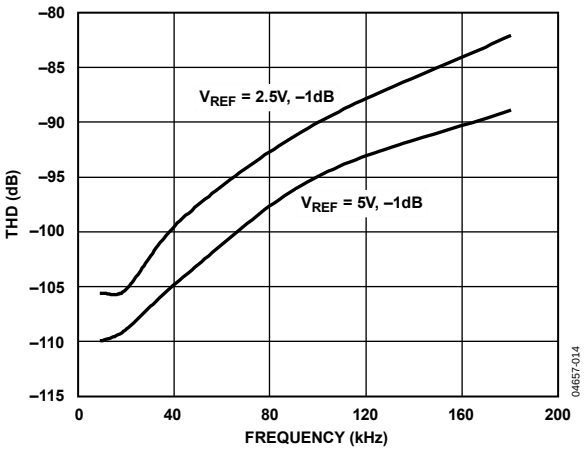


Figure 14. THD vs. Frequency

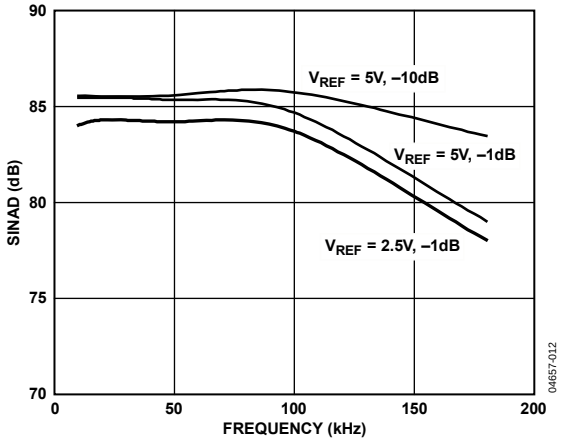


Figure 12. SINAD vs. Frequency

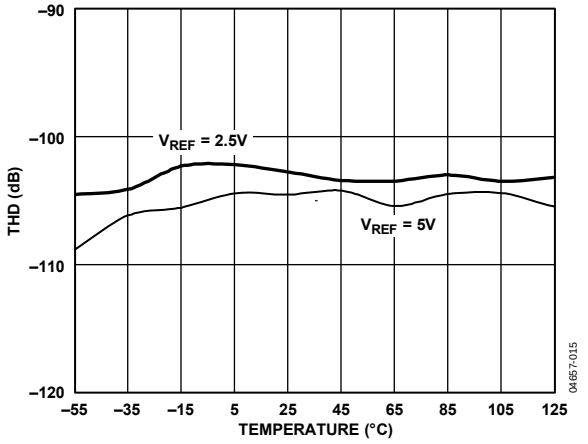


Figure 15. THD vs. Temperature

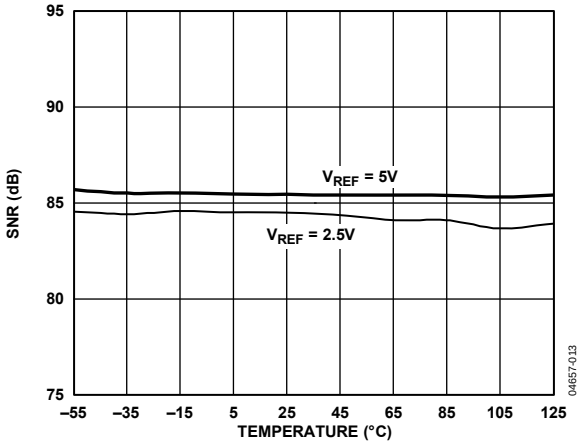


Figure 13. SNR vs. Temperature

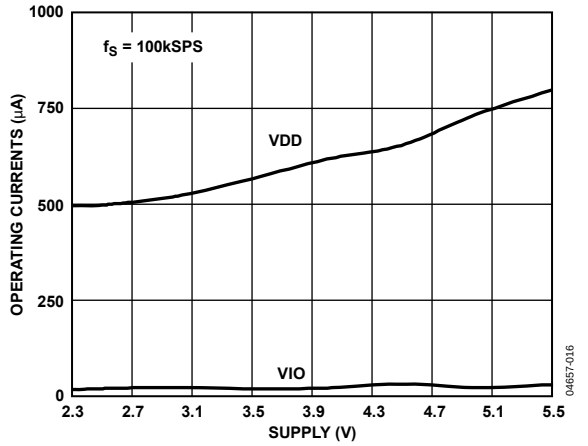


Figure 16. Operating Currents vs. Supply

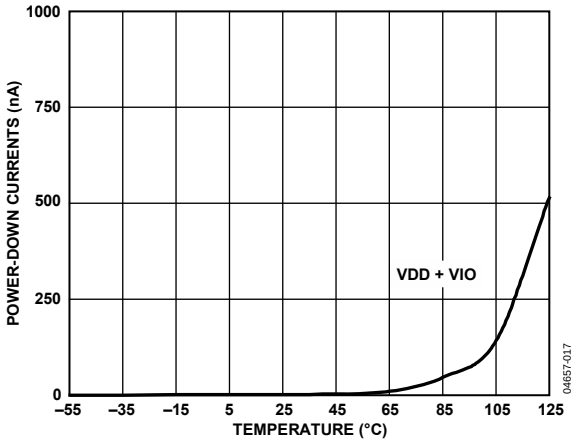


Figure 17. Power-Down Currents vs. Temperature

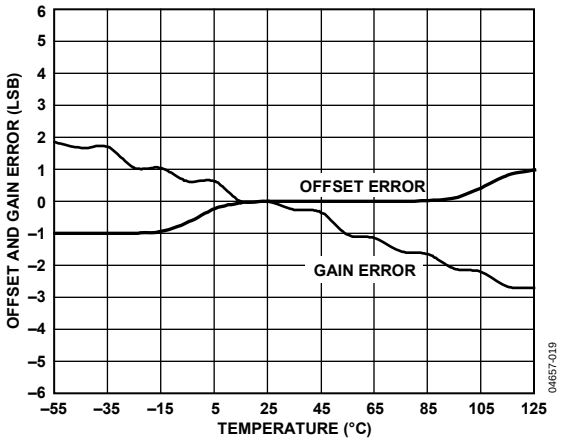


Figure 19. Offset Error and Gain Error vs. Temperature

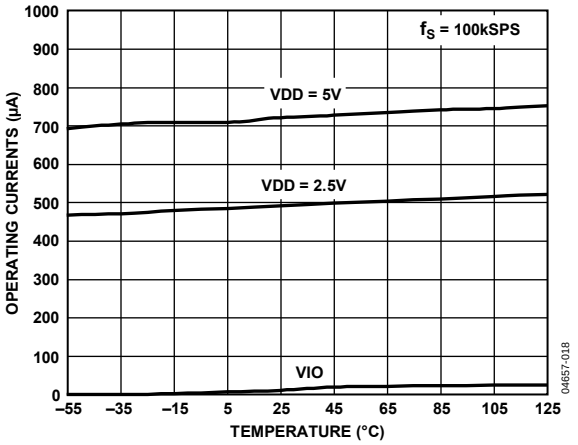


Figure 18. Operating Currents vs. Temperature

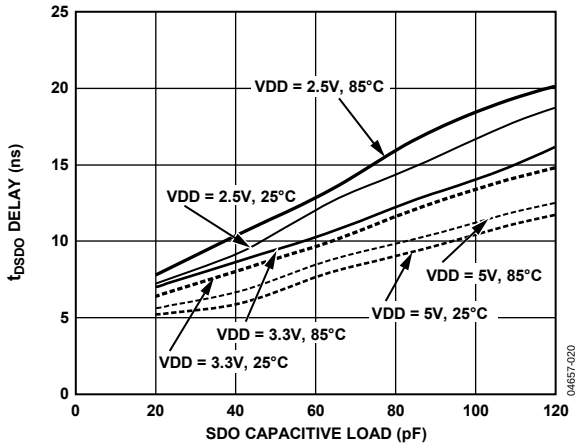


Figure 20. t_{DSDO} Delay vs. SDO Capacitance Load and Supply

TERMINOLOGY

Linearity Error or Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition should occur at a level ½ LSB above analog ground (152.6 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111...10 to 111...11) should occur for an analog voltage 1½ LSB below the nominal full scale (4.999542 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula and is expressed in bits as follows:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise and Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Aperture Delay
Aperture delay is a measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
The time required for the ADC to accurately acquire its input after a full-scale step function was applied.

THEORY OF OPERATION

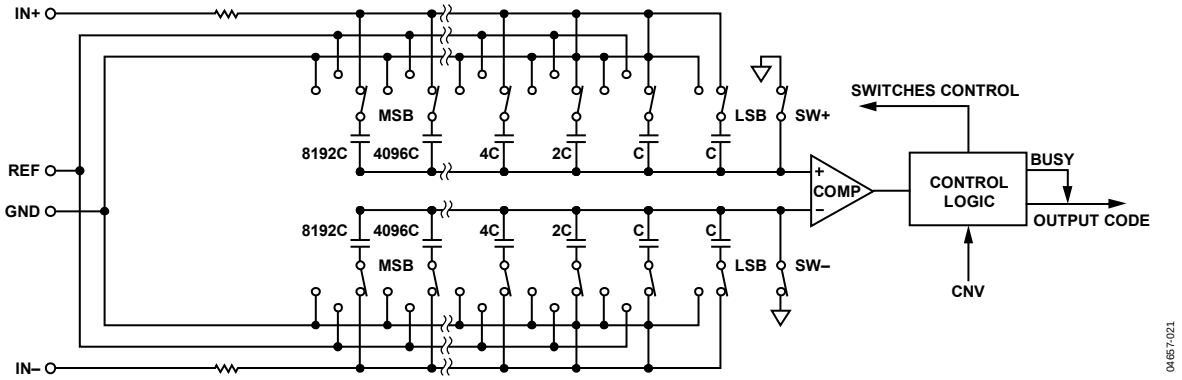


Figure 21. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7942 is a fast, low power, single-supply, precise 14-bit ADC using successive approximation architecture.

The AD7942 is capable of converting 250,000 samples per second (250 kSPS) and powers down between conversions. When operating at 100 SPS, for example, it consumes typically 1.25 µW with a 2.5 V power supply, which is ideal for battery-powered applications.

The AD7942 provides the user with an on-chip track-and-hold and does not exhibit any pipeline delay or latency, making it ideal for multiple, multiplexed channel applications.

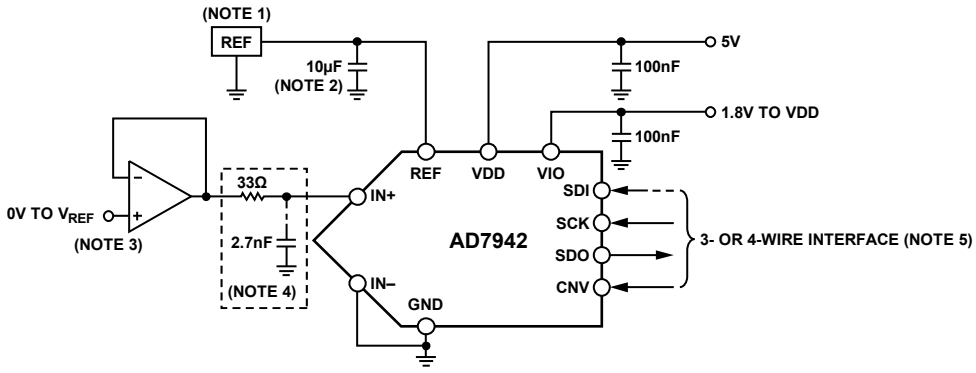
The AD7942 is specified from 2.3 V to 5.5 V and can be interfaced to a 1.8 V, 2.5 V, 3.3 V, or 5 V digital logic. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that is space saving, yet allows flexible configurations. It is pin-for-pin-compatible with the 16-bit ADC AD7685.

CONVERTER OPERATION

The AD7942 is a successive approximation ADC based on a charge redistribution DAC. Figure 21 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 14 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase starts, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the inputs (IN+ and IN−) captured at the end of the acquisition phase, is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/16,384$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7942 has an on-board conversion clock, the serial clock is not required for the conversion process.



NOTE 1: SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
NOTE 2: C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
NOTE 3: SEE DRIVER AMPLIFIER CHOICE SECTION.
NOTE 4: OPTIONAL FILTER. SEE ANALOG INPUT SECTION.
NOTE 5: SEE DIGITAL INTERFACE FOR MOST CONVENIENT INTERFACE MODE.

Figure 22. Typical Application Diagram

Transfer Functions

The ideal transfer characteristic for the AD7942 is shown in Figure 23 and Table 7.

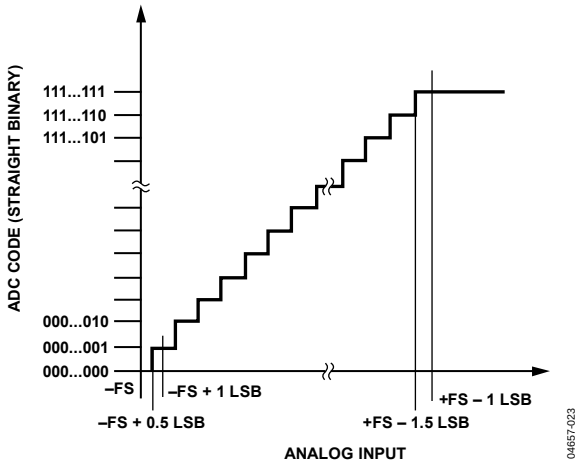


Figure 23. ADC Ideal Transfer Function

Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code Hexadecimal
FSR – 1 LSB	4.999695 V	0x3FFF[1]
Midscale + 1 LSB	2.500305 V	0x2001
Midscale	2.5 V	0x2000
Midscale – 1 LSB	2.499695 V	0x1FFF
–FSR + 1 LSB	305.2 µV	0x0001
–FSR	0 V	0x0000[2]

[1] This is also the code for an overranged analog input ($V_{IN+} - V_{IN-} > V_{REF} - V_{GND}$).
[2] This is also the code for an underranged analog input ($V_{IN+} - V_{IN-} < V_{GND}$).

TYPICAL CONNECTION DIAGRAM

Figure 22 shows an example of the recommended connection diagram for the AD7942 when multiple supplies are available.

Analog Input

Figure 24 shows an equivalent circuit of the input structure of the AD7942.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN–. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to become forward-biased and to start conducting current. However, these diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer (U1) supplies are different from VDD. In such a case, an input buffer with a short-circuit current limitation can be used to protect the part.

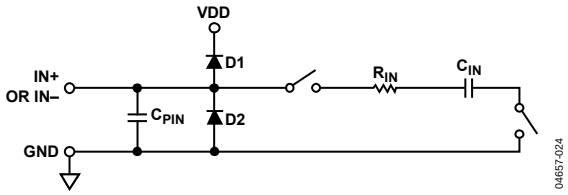


Figure 24. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the differential signal between IN+ and IN–. By using this differential input, small signals common to both inputs are rejected, as shown in Figure 25, which represents the typical CMRR over frequency. For instance, by using IN– to sense a remote signal ground, ground potential differences between the sensor and the local ADC ground are eliminated.

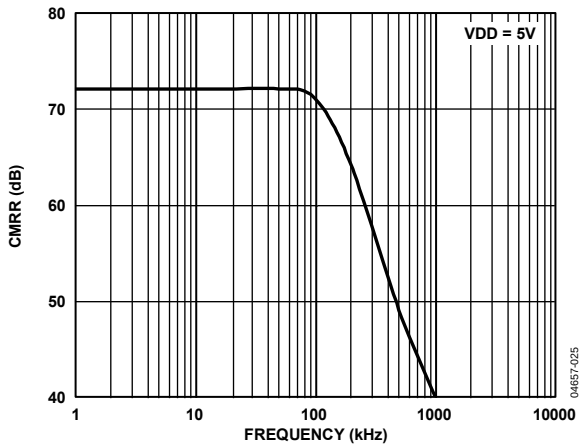


Figure 25. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog input, IN+, can be modeled as a parallel combination of the Capacitor C_{PIN} and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 3 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor. During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7942 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency, as shown in Figure 26.

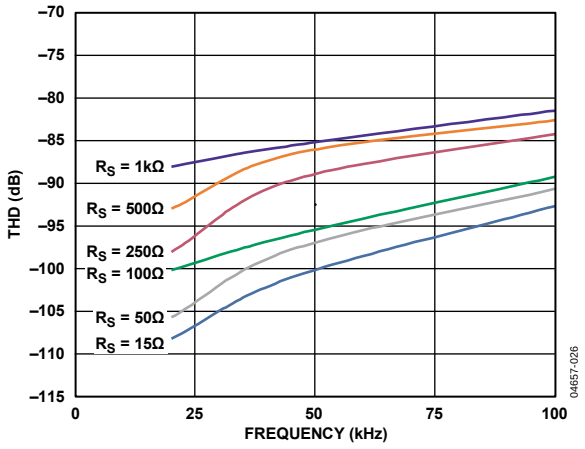


Figure 26. THD vs. Analog Input Frequency and Source Resistance

Driver Amplifier Choice

Although the AD7942 is easy to drive, the driver amplifier needs to meet the following requirements:

- The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7942. Note that the AD7942 produces much less noise than most other 14-bit ADCs and therefore can be driven by a noisier op amp while preserving the same or better system performance. The noise coming from the driver is filtered by the AD7942 analog input circuit, 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used.
- For ac applications, the driver needs to have a THD performance suitable to that of the AD7942. Figure 14 gives the THD vs. frequency that the driver should exceed.
- For multichannel multiplexed applications, the driver amplifier and the AD7942 analog input circuit must be able to settle for a full-scale step of the capacitor array at a 14-bit level (0.006%). In the amplifier data sheet, settling at 0.1% to 0.01% is more commonly specified. This could differ significantly from the settling time at a 14-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4841	Very low noise, small, and low power
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single supply, low power
AD8519	Small, low power, and low frequency
AD8031	High frequency and low power

Voltage Reference Input

The AD7942 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, a reference buffer using the AD8031 or the AD8605), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance, using a low temperature drift ADR43x reference.

If desired, smaller reference decoupling capacitor values ≥ 2.2 µF can be used with a minimal impact on performance, especially on DNL.

Power Supply

The AD7942 is specified over a wide operating range from 2.3 V to 5.5 V. It has, unlike other low voltage converters, a noise low enough to design a low supply (2.5 V) 14-bit resolution system with respectable performance. It uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD can be tied together. The AD7942 is independent of power supply sequencing between VIO and VDD. Additionally, it is insensitive to power supply variations over a wide frequency range, as shown in Figure 27.

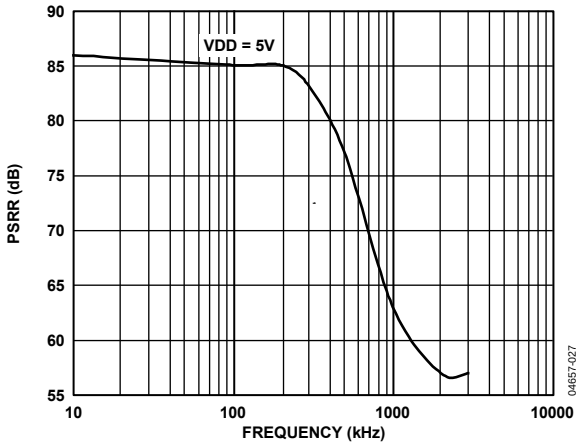


Figure 27. PSRR vs. Frequency

The AD7942 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate, as shown in Figure 28. This makes the part ideal for low sampling rates (even rates of a few hertz) and low battery-powered applications.

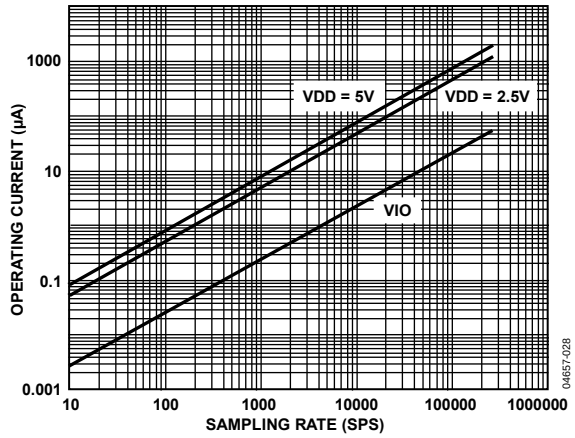
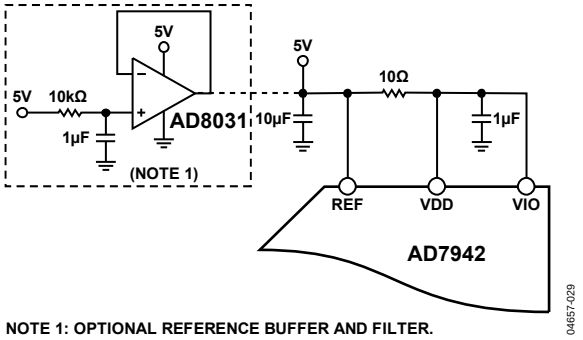


Figure 28. Operating Current vs. Sampling Rate

Supplying the ADC from the Reference

For simplified applications, the AD7942, with its low operating current, can be supplied directly using the reference circuit, as shown in Figure 29. The reference line can be driven by either

- The system power supply directly,
- A reference voltage with enough current output capability, such as the ADR43x, or
- A reference buffer, such as the AD8031, that can also filter the system power supply (see Figure 29).



NOTE 1: OPTIONAL REFERENCE BUFFER AND FILTER.

Figure 29. Example of Application Circuit

DIGITAL INTERFACE

Although the AD7942 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7942 is compatible with SPI, QSPI, digital hosts, and DSPs (for example, Blackfin® ADSP-BF53x or ADSP-219x). A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7942 provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is always selected.

In either mode, the AD7942 offers the flexibility to optionally force a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must time out the maximum conversion time prior to readback.

The busy indicator feature is enabled as follows:

- In the $\overline{CS}$ mode, if CNV or SDI is low when the ADC conversion ends (see Figure 33 and Figure 37).
- In the chain mode, if SCK is high during the CNV rising edge (see Figure 41).

$\overline{CS}$ Mode 3-Wire Without Busy Indicator

This mode is most often used when a single AD7942 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 30 and the corresponding timing diagram is shown in Figure 31.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. When a conversion is initiated, it continues to completion irrespective of the state of CNV. For instance, it is useful to bring CNV low to select other SPI devices, such as analog multiplexers. However, CNV must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator. When the conversion is complete the AD7942 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the 14th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

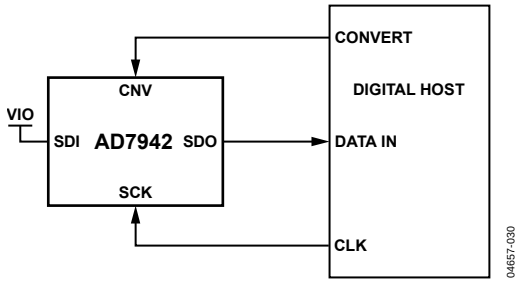


Figure 30. $\overline{CS}$ Mode 3-Wire Without Busy Indicator Connection Diagram (SDI High)

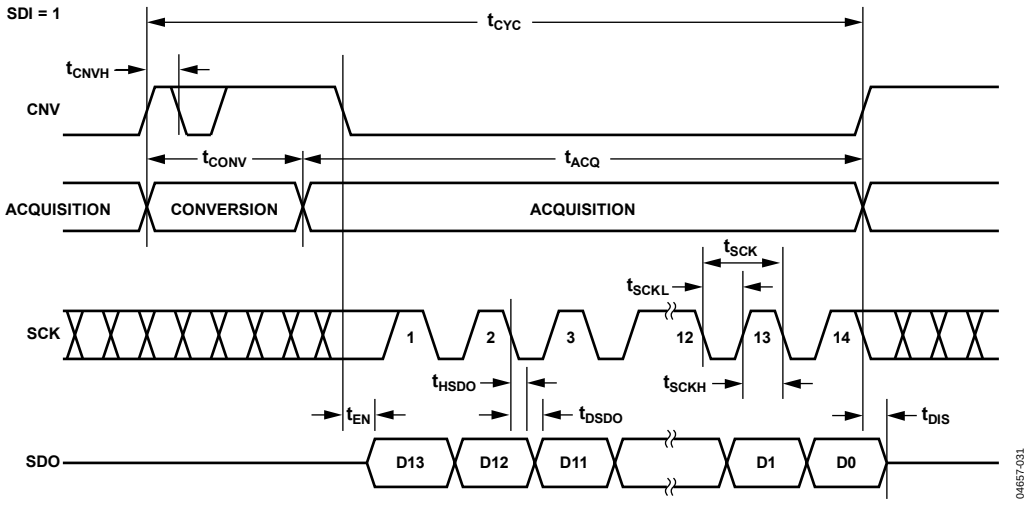


Figure 31. $\overline{CS}$ Mode 3-Wire Without Busy Indicator, Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 3-Wire with Busy Indicator

This mode is most often used when a single AD7942 is connected to an SPI-compatible digital host with an interrupt input. The connection diagram is shown in Figure 32 and the corresponding timing diagram is shown in Figure 33.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers. However, CNV must be returned low before the minimum conversion time and held low until the maximum conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7942 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate provided it has an acceptable hold time. After the optional 15th SCK falling edge or when CNV goes high, whichever is earlier, SDO returns to high impedance.

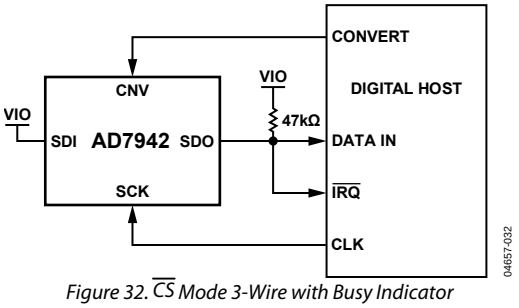


Figure 32. $\overline{CS}$ Mode 3-Wire with Busy Indicator Connection Diagram (SDI High)

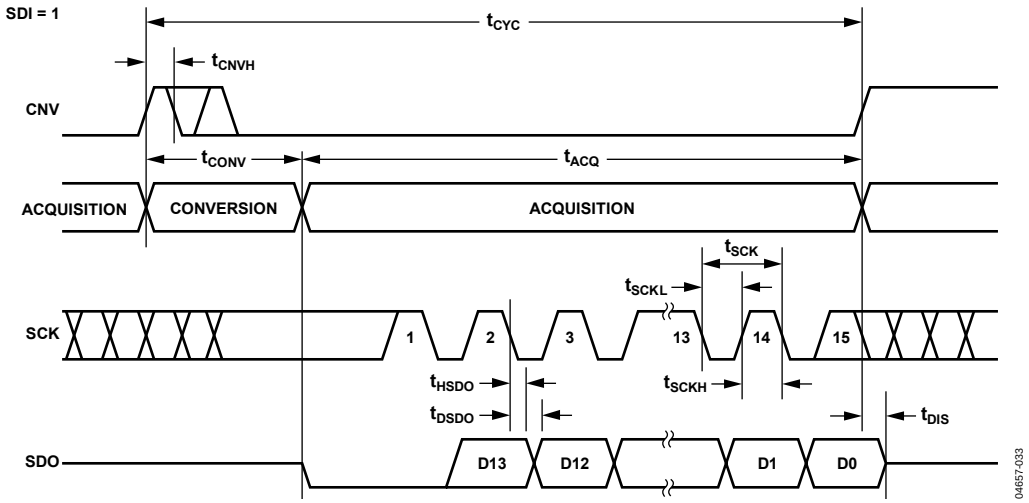


Figure 33. $\overline{CS}$ Mode 3-Wire with Busy Indicator, Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 4-Wire Without Busy Indicator

This mode is most often used when multiple AD7942s are connected to an SPI-compatible digital host. A connection diagram using two AD7942s is shown in Figure 34 and the corresponding timing diagram is given in Figure 35.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers. However, SDI must be returned high before the minimum conversion time elapses and held high until the maximum conversion time is completed to avoid generating the busy signal indicator. When the conversion is complete, the AD7942 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK driving edges. The data is valid on both SCK edges. Although the nondriving edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 14th SCK falling edge or when SDI goes high, whichever is earlier, SDO returns to high impedance and another AD7942 can be read.

If multiple AD7942s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

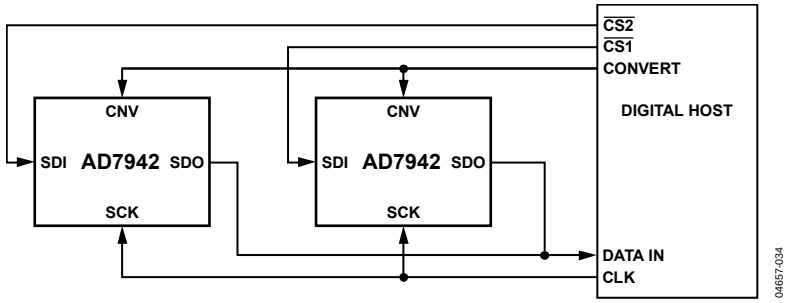


Figure 34. $\overline{CS}$ Mode 4-Wire Without Busy Indicator Connection Diagram

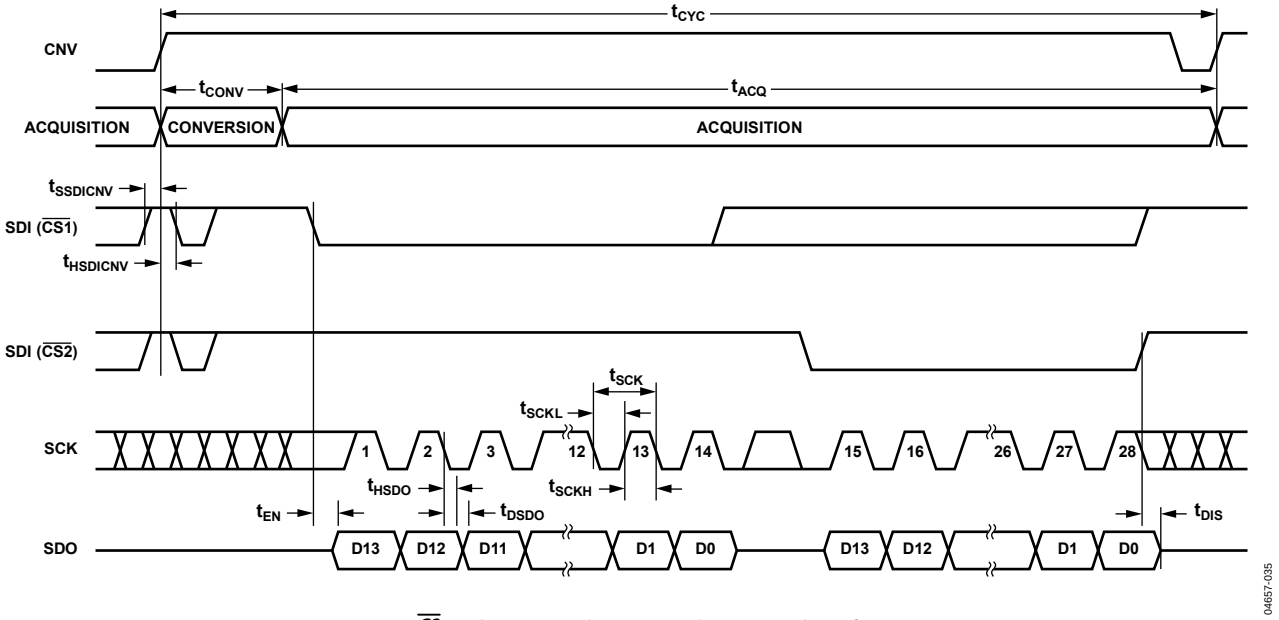


Figure 35. $\overline{CS}$ Mode 4-Wire Without Busy Indicator, Serial Interface Timing

$\overline{CS}$ Mode 4-Wire with Busy Indicator

This mode is most often used when a single AD7942 is connected to an SPI-compatible digital host with an interrupt input and to keep CNV (which is used to sample the analog input) independent of the signal used to select the data reading. This requirement is particularly important in applications where low jitter on CNV is desired. The connection diagram is shown in Figure 36 and the corresponding timing diagram is given in Figure 37.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback (if SDI and CNV are low, SDO is driven low). Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and held low until the maximum conversion time is completed to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low. With a pull-up on the SDO line this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7942 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK driving edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 15th SCK falling edge or SDI going high, whichever is earlier, the SDO returns to high impedance.

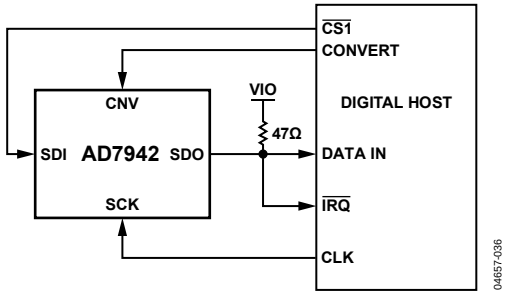


Figure 36. $\overline{CS}$ Mode 4-Wire with Busy Indicator Connection Diagram

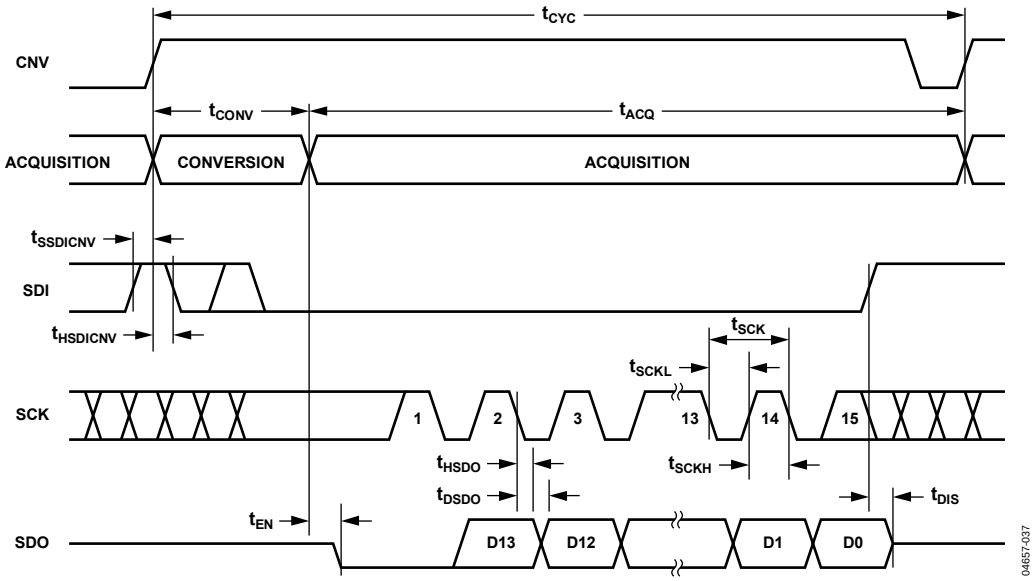


Figure 37. $\overline{CS}$ Mode 4-Wire with Busy Indicator, Serial Interface Timing

Chain Mode Without Busy Indicator

This mode can be used to daisy-chain multiple AD7942s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using two AD7942s is shown in Figure 38 and the corresponding timing diagram is given in Figure 39.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7942 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are then clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first and 14 × N clocks are required to readback the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate and consequently more AD7942s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time. For instance, with a 5 ns digital host setup time and 3 V interface, up to eight AD7942s running at a conversion rate of 220 kSPS can be daisy-chained on a 3-wire port.

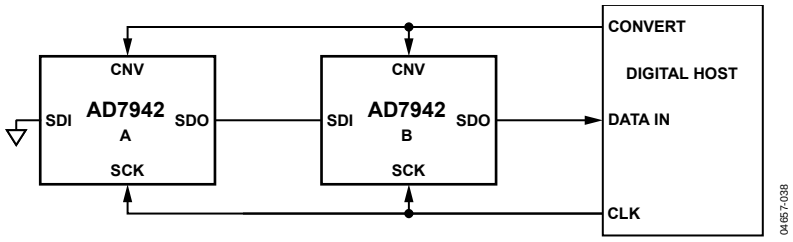


Figure 38. Chain Mode Without Busy Indicator Connection Diagram

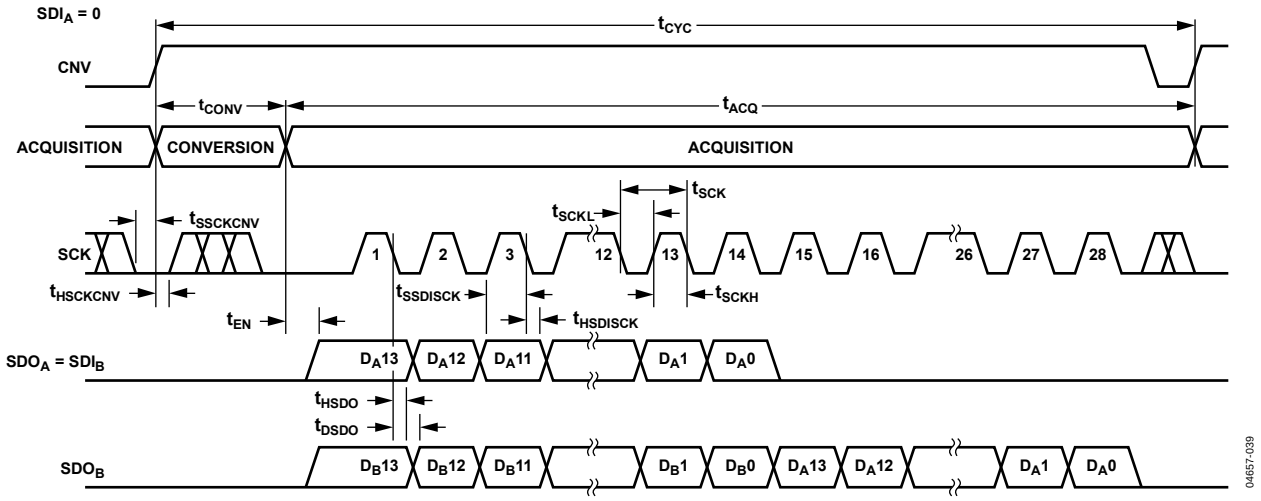


Figure 39. Chain Mode Without Busy Indicator, Serial Interface Timing

Chain Mode with Busy Indicator

This mode can also be used to daisy-chain multiple AD7942s on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register. A connection diagram example using three AD7942s is shown in Figure 40 and the corresponding timing diagram is given in Figure 41.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, SDO in the near end ADC (ADC C in Figure 40) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7942 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are then clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 14 × N + 1 clocks are required to readback the N ADCs. Although the rising edge can be used to capture the data, a digital host also using the SCK falling edge allows a faster reading rate and consequently more AD7942s in the chain, provided the digital host has an acceptable hold time. For instance, with a 5 ns digital host setup time and a 3 V interface, up to eight AD7942s running at a conversion rate of 220 kSPS can be daisy-chained to a single 3-wire port.

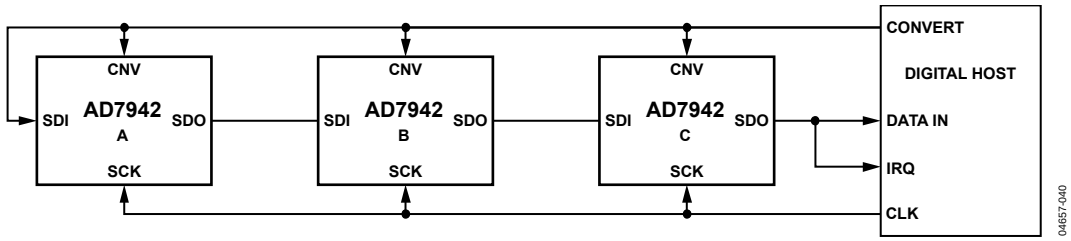


Figure 40. Chain Mode with Busy Indicator Connection Diagram

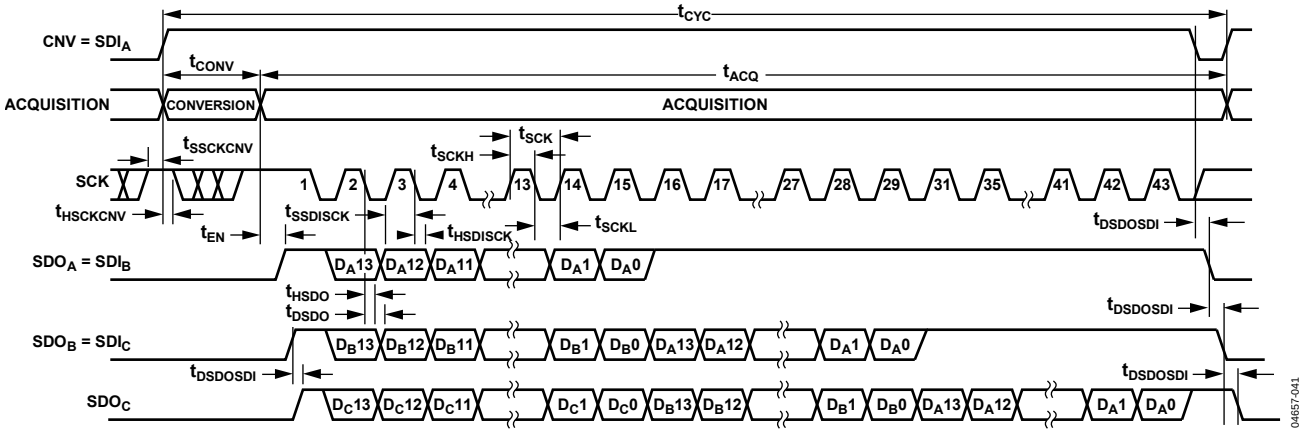


Figure 41. Chain Mode with Busy Indicator, Serial Interface Timing

APPLICATION HINTS

LAYOUT

Design the PCB that houses the AD7942 so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7942, with all its analog signals on the left side and all its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die, unless a ground plane under the AD7942 is used as a shield. Fast switching signals, such as CNV or clocks, should never run near analog signal paths. Avoid crossover of digital and analog signals.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the case of being split, the ground plane should be joined underneath the AD7942.

The AD7942 voltage reference input, REF, has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is accomplished by placing the reference decoupling ceramic capacitor close to, and ideally right up against, the REF and GND pins. Connect these pins with wide, low impedance traces.

Finally, decouple the power supply of the AD7942, VDD and VIO, with ceramic capacitors, typically 100 nF, placed close to the AD7942. Connect the capacitors using short and large traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines. An example of layout following these rules is shown in Figure 42 and Figure 43.

EVALUATING THE PERFORMANCE OF AD7942

Other recommended layouts for the AD7942 are outlined in the evaluation board for the AD7942 (EVAL-AD7942SDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

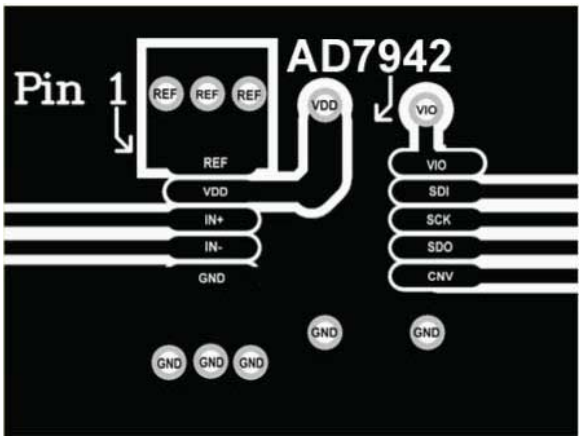


Figure 42. Layout Example (Top Layer)

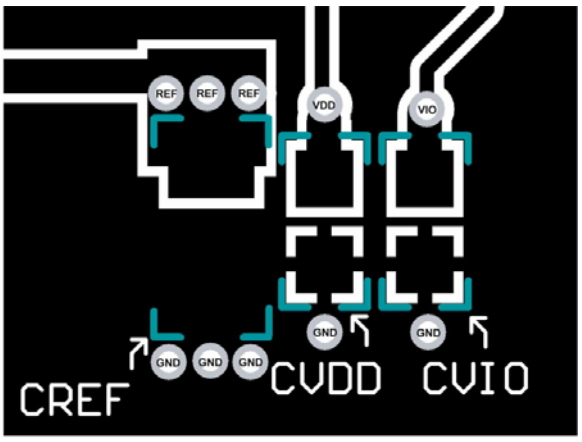


Figure 43. Layout Example (Bottom Layer)