

TABLE OF CONTENTS

Features.....	1	Theory of Operation.....	20
Applications.....	1	AMR Magnetic Field Sensor.....	20
Product Highlights.....	1	Sense Field Axis.....	20
Functional Block Diagram.....	1	Operating Magnetic Field Range.....	22
General Description.....	1	Integrated Signal-Chain Conditioning.....	22
Specifications.....	3	Precision Instrumentation Amplifier.....	22
Magnetic Characteristics.....	3	Flip Coil and Flip Coil Driver.....	23
Magnetic Range Characteristics.....	3	Diagnostic Coil.....	23
General Characteristics.....	5	Applications Information.....	25
Optional Features Specifications.....	7	Typical Application Diagram.....	25
Absolute Maximum Ratings.....	10	Ratiometric Output Configuration.....	26
Thermal Resistance.....	10	Amplifier Synchronization.....	26
Electrostatic Discharge (ESD) Ratings.....	10	Electrical Offset Cancellation.....	27
ESD Caution.....	10	Example Offset Calculation.....	27
Pin Configuration and Function Descriptions.....	11	Nonlinearity Compensation.....	28
Typical Performance Characteristics.....	12	Flip Coil and Measurement Timing.....	28
Terminology.....	18	Flipping Frequency.....	28
B_{SENSE}	18	Flip Coil Filter Configuration.....	28
S_{DEVICE}	18	V_{SET} Voltage.....	28
S_{COEFF1}	18	Output Anti-Alias Filter.....	29
S_{COEFF3}	18	Diagnostic Coil Driver.....	30
S_{ERROR}	18	Temperature Measurement.....	31
S_{DEVICE_T}	18	Design Examples.....	32
S_{ERROR_TC}	18	Circuit Board Layout Recommendations.....	34
Full-Scale Range (FSR).....	18	Recommended PCB Layout.....	34
L_{ERROR}	18	Mechanical Tolerances.....	35
Cross Field (B_{CROSS}).....	18	Outline Dimensions.....	36
Stray Field.....	18	Ordering Guide.....	36
Output Error due to a Cross Field.....	19	Evaluation Boards.....	36

REVISION HISTORY

1/2023—Revision 0: Initial Version

SPECIFICATIONS

MAGNETIC CHARACTERISTICS

Table 1. Magnetic Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
MAXIMUM MAGNETIC FIELD STRENGTH ON SENSE FIELD AXIS	B _{SENSE}	±8	mT	
REFERENCE ERROR				
Position		±50	µm	Reference position is the center of the package top
Angle		±3	Degrees	Reference position for angle $\Phi = 0^\circ$ is parallel to the horizontal line of the package top

MAGNETIC RANGE CHARACTERISTICS

-40°C ≤ T_A ≤ +125°C, supply voltage (V_{DD}) = 4.5 V to 5.5 V, and the V_{OUT} pin has a 1 kΩ resistor load (R_{OUT}) with a 1 nF capacitor load (C_{OUT}) to GND. The output voltage (V_{OUT}) is taken between the R_{OUT} and C_{OUT} components. The V_{OUT} common mode is set to V_{SET}/2, where V_{SET} is the voltage on the VSET pin and is tied to V_{DD}, unless otherwise stated.

Table 2. Magnetic Range ±2 mT

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSITIVITY PARAMETERS						
Ideal Sensitivity ^{1,2}	S _{COEFF1}	T _A = 25°C, V _{DD} = 5 V, G = 80 T _A = 25°C, V _{DD} = 5 V, G = 40 T _A = 25°C, V _{DD} = 5 V, G = 20		199.25 99.75 50		mV/mT mV/mT mV/mT
Nonlinearity Coefficient ³	S _{COEFF3}	T _A = 25°C, V _{DD} = 5 V, G = 80		8.28 × 10 ⁻⁸		mV ³ /mT
Sensitivity Initial Error ²	S _{ERROR}	T _A = 25°C	-1		+1	%S _{COEFF1}
Sensitivity Error over Temperature ²	S _{ERROR_TC}	T _A = -20°C to +85°C T _A = -40°C to +125°C	-0.32 -2.6		+2.93 +2.93	%S _{COEFF1} %S _{COEFF1}
Linearity Error	L _{ERROR}	±2 mT range, full-scale ratio (FSR) = 4 mT	-0.2		+0.2	%FSR
Maximum Cross Field Strength						
Sensitivity Error due to a Cross Field ²	S _{ERROR_BC}	Cross field (B _{CROSS}) = ±0.5 mT B _{CROSS} = sense field (B _{SENSE}) = ±2 mT		0.08 1.2		%S _{COEFF1} %S _{COEFF1}
Sensitivity Lifetime Error ²				0.003		%S _{COEFF1}

¹ Ideal sensitivity, factory trimmed and calculated with the linear best-fit, is measured from the following points: ±2 mT, ±1 mT, and ±0.5 mT.

² Production tested at ±1 mT. Full range guaranteed by design and/or characterization.

³ Ideal coefficient, factory trimmed and calculated with the third-order best-fit, is measured from the following points: ±2 mT, ±1 mT, and ±0.5 mT.

Table 3. Magnetic Range ±4 mT

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSITIVITY PARAMETERS						
Ideal Sensitivity ^{1,2}	S _{COEFF1}	T _A = 25°C, V _{DD} = 5 V, G = 80 T _A = 25°C, V _{DD} = 5 V, G = 40 T _A = 25°C, V _{DD} = 5 V, G = 20		195 97.5 48.75		mV/mT mV/mT mV/mT
Nonlinearity Coefficient ³	S _{COEFF3}	T _A = 25°C, V _{DD} = 5 V, G = 80		8.17 × 10 ⁻⁸		mV ³ /mT
Sensitivity Initial Error ²	S _{ERROR}	T _A = 25°C	-1		+1	%S _{COEFF1}
Sensitivity Error over Temperature ²	S _{ERROR_TC}	T _A = -20°C to +85°C	-0.32		+2.9	%S _{COEFF1}

SPECIFICATIONS

Table 3. Magnetic Range ± 4 mT (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Linearity Error	L _{ERROR}	T _A = -40°C to +125°C	-2.8		+3.3	%S _{COEFF1}
		± 4 mT range, FSR = 8 mT	-0.65		+0.59	%FSR
Sensitivity Error due to a Cross Field ²	S _{ERROR_BC}	B _{CROSS} = ± 0.5 mT		0.08		%S _{COEFF1}
Sensitivity Lifetime Error ²				0.009		%S _{COEFF1}

¹ Ideal sensitivity, factory trimmed and calculated with the linear best-fit, is measured from the following points: ± 4 mT, ± 3 mT, ± 2 mT, ± 1 mT, and ± 0.5 mT.

² Production tested at ± 1 mT. Full range guaranteed by design and/or characterization.

³ Ideal coefficient, factory trimmed and calculated with the third-order best-fit, is measured from the following points ± 4 mT, ± 3 mT, ± 2 mT, ± 1 mT, and ± 0.5 mT.

Table 4. Magnetic Range ± 8 mT

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SENSITIVITY PARAMETERS						
Ideal Sensitivity ^{1,2}	S _{COEFF1}	T _A = 25°C, V _{DD} = 5 V, G = 80		183		mV/mT
		T _A = 25°C, V _{DD} = 5 V, G = 40		91.5		mV/mT
		T _A = 25°C, V _{DD} = 5 V, G = 20		45.75		mV/mT
Nonlinearity Coefficient ³	S _{COEFF3}	T _A = 25°C, V _{DD} = 5 V, G = 80		8.08 x 10 ⁻⁸		mV ³ /mT
Sensitivity Initial Error ²	S _{ERROR}	T _A = 25°C	-2.19		+2.39	%S _{COEFF1}
Sensitivity Error over Temperature ²	S _{ERROR_TC}	T _A = -20°C to +85°C	-0.32		+2.7	%S _{COEFF1}
		T _A = -40°C to +125°C	-3.56		+3.63	%S _{COEFF1}
Linearity Error	L _{ERROR}	± 8 mT range, FSR = 16 mT	-3.42		+3.28	%FSR
Sensitivity Error due to a Cross Field ²	S _{ERROR_BC}	B _{CROSS} = ± 0.5 mT		0.06		%S _{COEFF1}
Sensitivity Lifetime Error ²				0.032		%S _{COEFF1}

¹ Ideal sensitivity, factory trimmed and calculated with the linear best-fit, is measured from the following points: ± 8 mT, ± 7 mT, ± 6 mT, ± 5 mT, ± 4 mT, ± 3 mT, ± 2 mT, ± 1 mT, and ± 0.5 mT.

² Production tested at ± 1 mT. Full range guaranteed by design and/or characterization.

³ Ideal coefficient, factory trimmed and calculated with the third-order best-fit, is measured from the following points: ± 8 mT, ± 7 mT, ± 6 mT, ± 5 mT, ± 4 mT, ± 3 mT, ± 2 mT, ± 1 mT, and ± 0.5 mT.

SPECIFICATIONS

GENERAL CHARACTERISTICS

$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $V_{DD} = 4.5\text{ V to }5.5\text{ V}$, the VOUT pin has a $1\text{ k}\Omega$ resistor load (R_{OUT}) with a 1 nF capacitor load (C_{OUT}) to GND. V_{OUT} is taken between the R_{OUT} and C_{OUT} components. The output voltage common mode is set to $V_{SET}/2$, where V_{SET} is the voltage on the VSET pin and is tied to V_{DD} , unless otherwise stated.

Table 5. General Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OFFSET—OUTPUT REFERRED						
Electrical Offset with Flipping	$V_{OFFSETWFLIP}$	Residual offset with the use of internal flip coil $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $G = 80^1$ $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, input equivalent ²		20 100		μV nT
Electrical Offset Stability		Standard deviation of $V_{OFFSETWFLIP}$ ³ $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $G = 80^1$ $T_A = 25^{\circ}\text{C}$, input equivalent		6.8 34		$\mu\text{V rms}$ nT rms
Electrical Offset without Flipping	V_{OFFSET}	Without the use of the internal flip coil $T_A = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $G = 80^1$	-100	-4	+100	mV
Temperature Offset Coefficient	TC_{OFFSET}	Without the use of the internal flip coil $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$, $G = 80^1$ $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$, input equivalent		-130 ± 650	+650	$\mu\text{V}/^{\circ}\text{C}$ $\text{nT}/^{\circ}\text{C}$
Electrical Offset Drift over Lifetime	V_{OFFSET_LT}	Without the use of the internal flip coil $V_{DD} = 5\text{ V}$, $G = 80$, $T_A = 25^{\circ}\text{C}^1$		-23		μV
Magnetic Offset Hysteresis		Sweep from -8 mT to $+8\text{ mT}$		0.7		μT
OUTPUT						
Bandwidth	f_{-3dB}	-3 dB bandwidth $R_{OUT} = 0\ \Omega$, $C_{OUT} = 150\text{ pF}$, $G = 80$ $R_{OUT} = 0\ \Omega$, $C_{OUT} = 150\text{ pF}$, $G = 40$ or $G = 20$		1.45 2.2		MHz MHz
Noise	V_{NOISE}	Low frequency RMS noise, $0.1\text{ Hz to }10\text{ Hz}$, $V_{DD} = 5\text{ V}$, $G = 80$, $B = 0\text{ mT}^1$ Chopping enabled, SYNC_EN pin pulled to V_{DD} Chopping disabled, SYNC_EN pin pulled to GND Noise density, frequency = 50 kHz , $V_{DD} = 5\text{ V}$, $G = 80$, $B = 0\text{ mT}^1$ Noise density magnetic field equivalent, frequency = 50 kHz , $V_{DD} = 5\text{ V}$, $G = 80$, $B = 0\text{ mT}$		16 350 1.2 6		$\mu\text{V rms}$ $\mu\text{V rms}$ $\mu\text{V}/\sqrt{\text{Hz}}$ $\text{nT}/\sqrt{\text{Hz}}$
Voltage Range		V_{OUT}	0.2		$V_{DD} - 0.2$	V
Internal Series Resistance	R_{SERIES}	Series resistance on the VOUT pin		2		Ω
External Load Capacitance	C_{OUT}	From R_{OUT} to GND, solder close to the package, $R_{OUT} = 0\ \Omega$ in series with VOUT $200\ \Omega < R_{OUT} < 5\text{ k}\Omega$ $R_{OUT} > 5\text{ k}\Omega$		100 1 10	150	pF nF nF
Short-Circuit Current	I_{SC}	Short to GND Short to V_{DD}		-50 70		mA mA
VSET INPUT						
Voltage Range	V_{SET}	Sets the output common mode to $V_{SET}/2$, where V_{SET} is the voltage applied to the VSET pin	0.1		$V_{DD} - 0.1$	V
Input Impedance	R_{IN}			70		$\text{k}\Omega$
DIGITAL INPUTS (A0, A1)						
Input Voltage						
High	V_{IH}		1.5			V
Low	V_{IL}				0.3	V

SPECIFICATIONS

Table 5. General Characteristics (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Drive Current	I_B				25	μA
POWER SUPPLY						
Supply Voltage	V_{DD}		4.5		5.5	V
Quiescent Supply Current	I_{SY}	No load	5	6.5	9	mA
Power-Up Time	t_{PWRUP}	To 98% of desired output level after V_{DD} was reached		15		ms
VREG Output Voltage	V_{REG}	Internally regulated voltage		1.8		V
Power-Supply Rejection Ratio	PSRR	Ratiometric measurement $V_{DD} = 4.5\text{ V to }5.5\text{ V}$, DC bias Frequency = 100 Hz	-81	-82		dB
				-82		dB

¹ Output referred. Divide by 2 if $G = 40$, and divide by 4 if $G = 20$.

² Calculated equivalent magnetic field.

³ The stability of $V_{OFFSETWFLIP}$ is the calculated offset with the flipping functionality. The sensor is flipped 200 times and standard deviation of the 100 offsets calculated.

SPECIFICATIONS

OPTIONAL FEATURES SPECIFICATIONS

Flipping Functionality Specifications

Table 6. Flipping Functionality Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VDD_FLIP			4.5		5.5	V
Supply Voltage	V_{DD_FLIP}					
Average Flip Current	I_{FLIP_AVG}	FLIP_DRV clock period ($t_{CLK_FLIP_DRV}$) = 0.05 sec, $T_A = 25^\circ\text{C}$		308		μA
		$t_{CLK_FLIP_DRV} = 0.05$ sec, $T_A = -40^\circ\text{C}$		400		μA
		$t_{CLK_FLIP_DRV} = 0.05$ sec, $T_A = 125^\circ\text{C}$		226		μA
Peak Flip Current	I_{FLIP_ON}	Peak current for t_{PULSE} supported by C_{FLIP}				
		$T_A = 25^\circ\text{C}$		2.4		A
		$T_A = -40^\circ\text{C}$		3.1		A
		$T_A = 125^\circ\text{C}$		1.8		A
Recommended Input Capacitance	C_{FLIP}			10		μF
Series Resistance	R_{FLIP}			10		Ω
FLIP_DRV						
Input Voltage			1.5			V
High	$FLIP_{HIGH}$					
Low	$FLIP_{LOW}$				0.3	V
Input Drive Current	I_B				25	μA
FLIP_DRV Clock Frequency	$f_{CLK_FLIP_DR}$	$t_{CLK_FLIP_DRV}$ period = $1/f_{CLK_FLIP_DR}$			1000	Hz
Minimum Pulse Width						
High	t_{CYCLE1}		320			μs
Low	t_{CYCLE2}		320			μs
Flip Pulse Delay	t_{DELAY}		2.46	2.5	2.55	μs
Flip Pulse Duration	t_{PULSE}		1.2	1.25	1.3	μs
OUTPUT TIMING						
Invalid Output Time	$t_{INVALID}$	Does not include settling of the amplifier		2.5	2.6	μs
Settling Time	$t_{SETTLING}$	$R_{OUT} = 0 \Omega$, $C_{OUT} = 150 \text{ pF}$, $G = 80$, $B_{SENSED} = 1 \text{ mT}$, 99% settling		0.7		μs

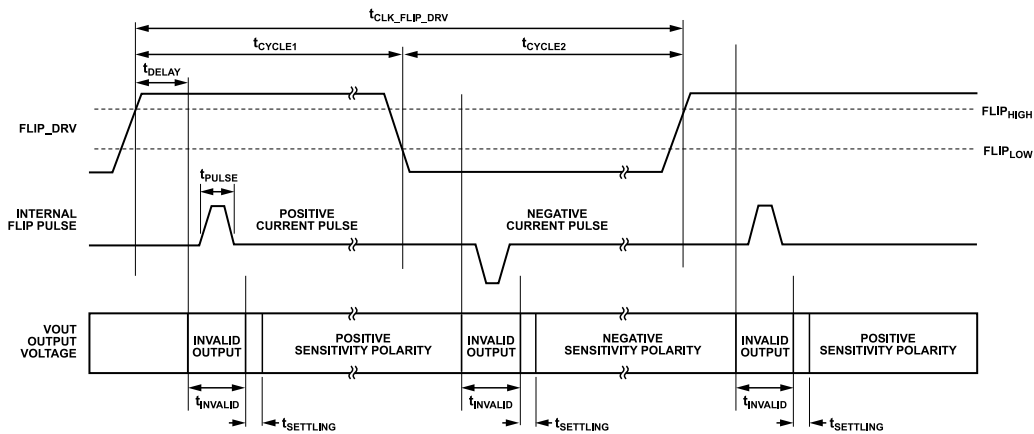


Figure 2. Flip Coil Driver Timing Diagram with Output Voltage Status

SPECIFICATIONS

Diagnostic Coil Specifications

Table 7. Diagnostic Coil Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIAGNOSTIC						
Diagnostic Coil Resistance	R_{DIAG}			12		m Ω
DIAG+ Input Voltage					V_{DD}	V
DIAG+ Input Current	I_{DIAG}				100	mA
Magnetic Field Factor	B_{DIAG}	The magnetic field experienced by the AMR sensor element per unit ($I_{DIAG} = 100$ mA, 1 unit)		22.8		μ T

Temperature Sensor Specifications

Table 8. Temperature Sensor Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE SENSOR						
VTEMP Output Voltage		$V_{DD} = 5$ V, $T_A = 25^\circ\text{C}$	2.25	2.56	2.88	V
VTEMP Temperature Coefficient	TC_{VTEMP}	$V_{DD} = 5$ V		15		mV/ $^\circ\text{C}$
VTEMP Output Voltage Range		$V_{DD} = 5$ V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	1.68		4.45	V
VTEMP Output Error		After initial calibration at $T_A = 25^\circ\text{C}$		± 1.25		$^\circ\text{C}$
		$T_A = 25^\circ\text{C}$ to 85°C		± 3		$^\circ\text{C}$
		$T_A = 25^\circ\text{C}$ to 125°C		73		Ω
VTEMP Output Resistance				73		Ω
VTEMP Load Capacitance	C_{VTEMP}			20		pF

Synchronization and Chopping Specifications

Table 9. Synchronization and Chopping Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYNC_EN						
Input Voltage						
High	V_{IH}		3			V
Low	V_{IL}				1.6	V
Input Drive Current	I_B				25	μ A
Setup Time	t_{SETUP}		60			ns
SYNC						
Input Frequency Range	f_{SYNC}	SYNC_EN = V_{DD} for synchronization feature, $f_{SYNC} = 1/\text{SYNC time } (t_{SYNC})$	400		1600	kHz
Minimum Pulse Width						
High	t_{HIGH}		150			ns
Low	t_{LOW}		150			ns
Input Voltage						
High	V_{IH}		3			V
Low	V_{IL}				1.6	V
Input Drive Current	I_B				25	μ A
Chopping Clock Delay	t_{CONV}			50		ns
Chopping Frequency	f_{CHOP}	Chopping frequency of the amplifier, $f_{CHOP} = 1/\text{chopping time } (t_{CHOP})$				
		SYNC = GND		200		kHz
		400 kHz < f_{SYNC} < 1600 kHz, SYNC_EN = V_{DD}		$f_{SYNC}/4$		kHz
		SYNC = V_{DD}		Chopping disabled		

SPECIFICATIONS

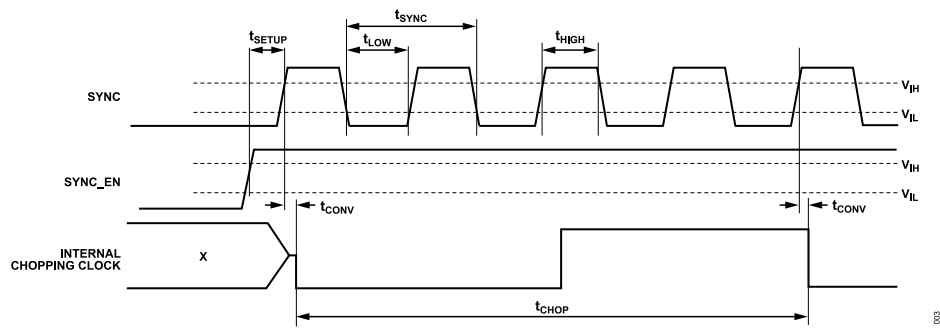


Figure 3. Synchronization Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 10. Absolute Maximum Ratings

Parameter	Rating
V _{DD}	GND – 0.3 V to +6 V
All Input and Output Pins	GND – 0.3 V to V _{DD} + 0.3 V
Temperature	
Operating Junction Range	–40°C to +125°C
Storage Range	–40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-20-21	36	62	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2014

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADAF1080

Table 12. ADAF1080, 20-Lead LFCSP

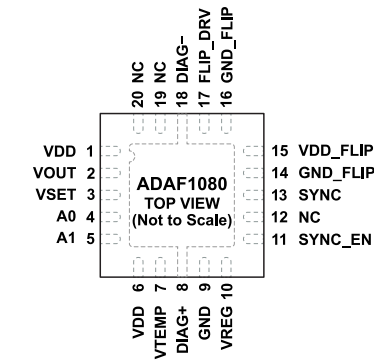
ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
CDM	1250	1

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT, THE NC PIN CAN BE LEFT OPEN OR CONNECTED TO GND.
2. EXPOSED PAD. LEAVE THE EXPOSED PAD OF THE PACKAGE AT A FLOATING VOLTAGE BUT SOLDERED TO THE PCB IN THE APPLICATION. THE EPAD IS USED AS THE DIAGNOSTIC COIL AND IS INTERNALLY CONNECTED BETWEEN THE DIAG+ AND DIAG- PINS.

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Figure 4. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Supply Voltage. The VDD pin must be connected to the other VDD supply voltage pin (Pin 6).
2	VOUT	Output Voltage Proportional to the Magnetic Field Sensed. Output ratiometric to V_{DD} .
3	VSET	VSET Input. The VSET pin sets the common-mode voltage of the OUT pin to $V_{SET}/2$.
4	A0	Gain Setting LSB. When A0 is not in use, it is internally pulled high to V_{DD} .
5	A1	Gain Setting MSB. When A1 is not in use, it is internally pulled high to V_{DD} .
6	VDD	Supply Voltage. Connect a 1 μF capacitor to GND as close to the VDD pin as possible.
7	VTEMP	Temperature Sensor Output. The maximum VTEMP capacitance load (C_{LOAD_VTEMP}) is 20 pF; therefore, do not drive current out of this pin. VTEMP is proportional to the die junction temperature.
8	DIAG+	Positive Input of the Diagnostic Coil. If DIAG+ is not in use, connect it to GND.
9	GND	Ground.
10	VREG	Internally Regulated 1.8 V. Connect a 0.1 μF capacitor only to GND. Do not connect any other load to this regulated supply.
11	SYNC_EN	Sync Enable. Set SYNC_EN high to enable clock synchronization. Set SYNC_EN low to use the internal clock for chopping. If SYNC_EN is not in use, it is internally pulled to GND.
12	NC	No Connect. The NC pin can be left open or connected to GND.
13	SYNC	Digital Input Where an External Clock Can Synchronize the Internal Chopping Amplifier Timing. If SYNC is open, it is internally pulled to GND.
14	GND_FLIP	Ground of the Flip Coil Driver, Attach to System Ground.
15	VDD_FLIP	Supply of the Flip Coil Driver. Place a 10 μF capacitor between VDD_FLIP and GND_FLIP and a 10 Ω resistor in series between VDD_FLIP and VDD as close as possible to the VDD_FLIP pin.
16	GND_FLIP	Ground of the Flip Coil Driver, Attach to System Ground.
17	FLIP_DRV	Drive Signal for the Flip Coil Driver. A rising edge sets a positive sensitivity, and a falling edge sets a negative sensitivity. If FLIP_DRV is not in use, internally pulled it high.
18	DIAG-	Negative Input of the Diagnostic Coil and Measurement Point for the Diagnostic Current. If DIAG- is not in use, this pin can be left open or connected to the EPAD.
19	NC	No Connect. The NC pin can be left open or connected to GND.
20	NC	No Connect. The NC pin can be left open or connected to GND.
	EPAD	Exposed Pad. Leave the exposed pad of the package at a floating voltage but soldered to the PCB in the application. The EPAD is used as the diagnostic coil and is internally connected between the DIAG+ and DIAG- pins.

TYPICAL PERFORMANCE CHARACTERISTICS

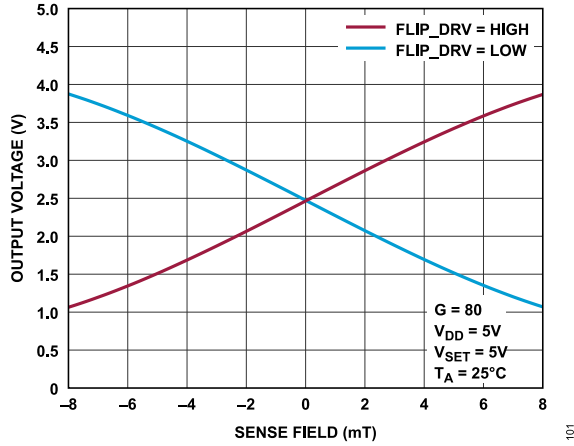


Figure 5. Output Voltage vs. Sense Field, $V_{SET} = V_{DD} = 5\text{ V}$, $G = 80$

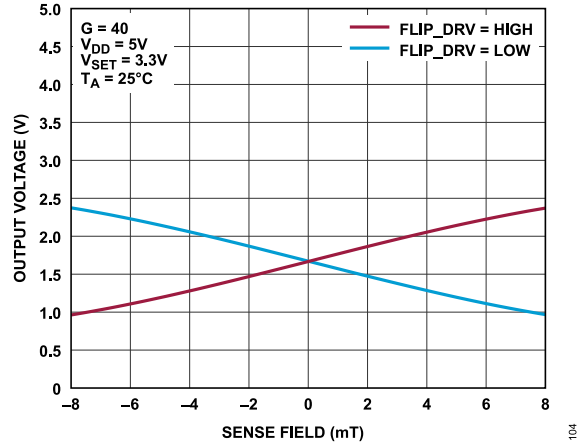


Figure 8. Output Voltage vs. Sense Field, $V_{SET} = 3.3\text{ V}$, $V_{DD} = 5\text{ V}$, $G = 40$

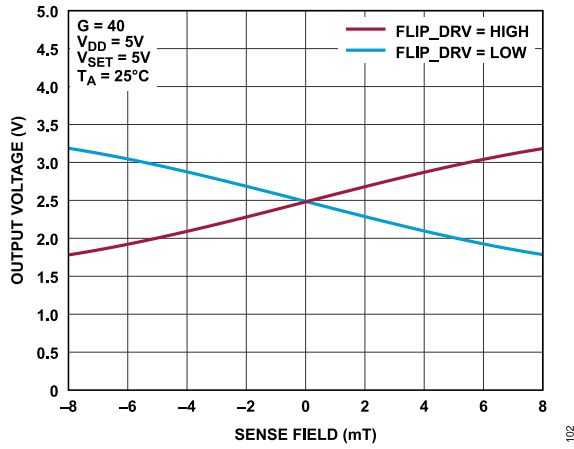


Figure 6. Output Voltage vs. Sense Field, $V_{SET} = V_{DD} = 5\text{ V}$, $G = 40$

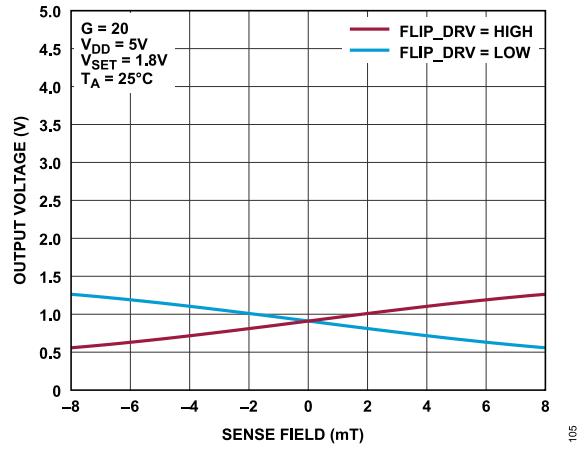


Figure 9. Output Voltage vs. Sense Field, $V_{SET} = 1.8\text{ V}$, $V_{DD} = 5\text{ V}$, $G = 20$

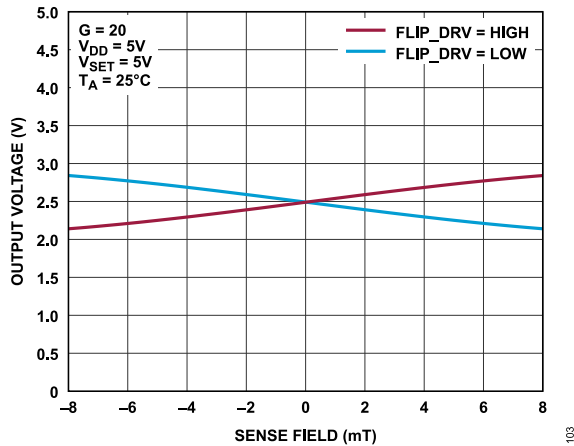


Figure 7. Output Voltage vs. Sense Field, $V_{DD} = V_{SET} = 5\text{ V}$, $G = 20$

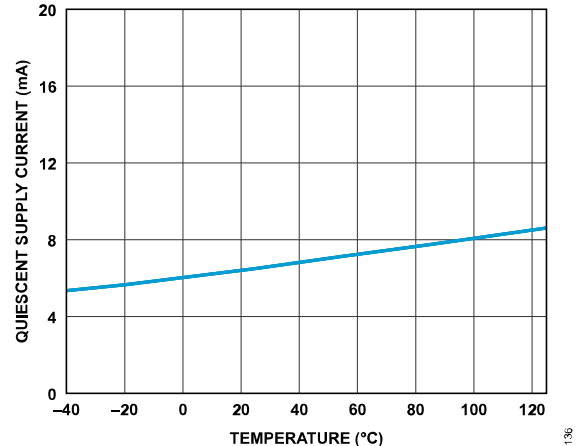


Figure 10. Quiescent Supply Current vs. Temperature for All Gain Values

TYPICAL PERFORMANCE CHARACTERISTICS

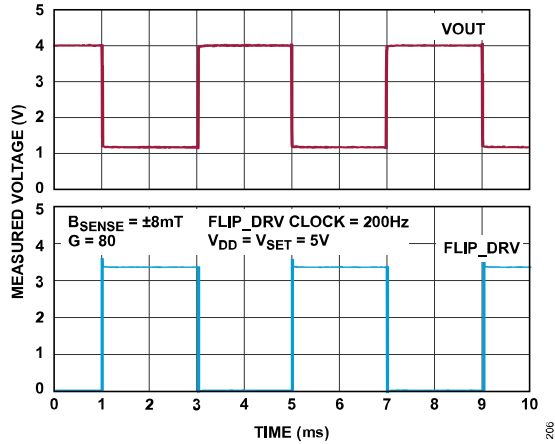


Figure 11. Measured Voltage During Flip Coil Switching for VOUT and FLIP_DRV Signals, $G = 80$, $B_{SENSE} = \pm 8$ mT, FLIP_DRV Clock = 200 Hz

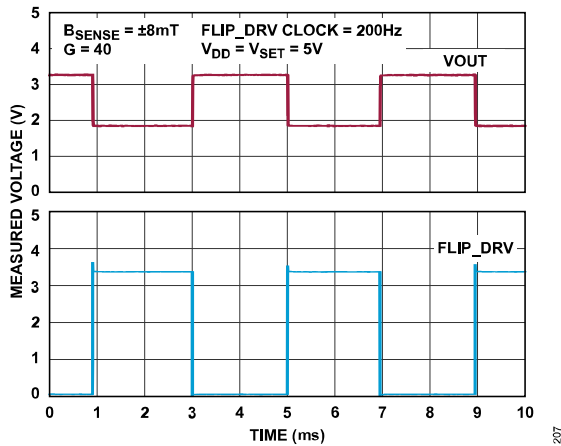


Figure 12. Measured Voltage During Flip Coil Switching for VOUT and FLIP_DRV Signals, $G = 40$, $B_{SENSE} = \pm 8$ mT, FLIP_DRV Clock = 200 Hz

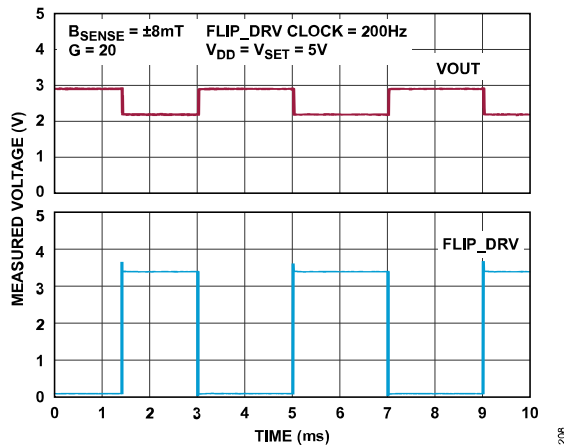


Figure 13. Measured Voltage During Flip Coil Switching for VOUT and FLIP_DRV Signals, $G = 20$, $B_{SENSE} = \pm 8$ mT, FLIP_DRV Clock = 200 Hz

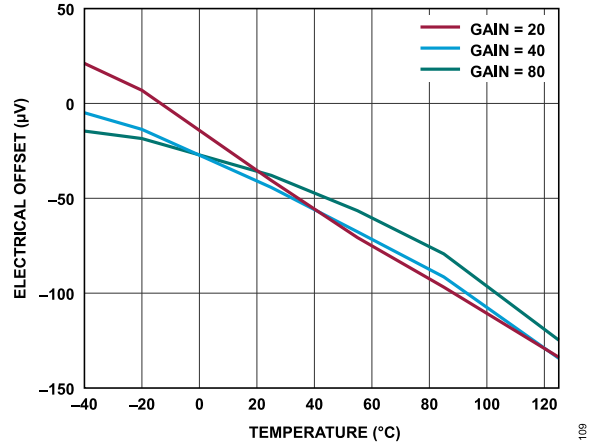


Figure 14. Electrical Offset vs. Temperature Without Offset Correction for All Gain Values, Output Referred

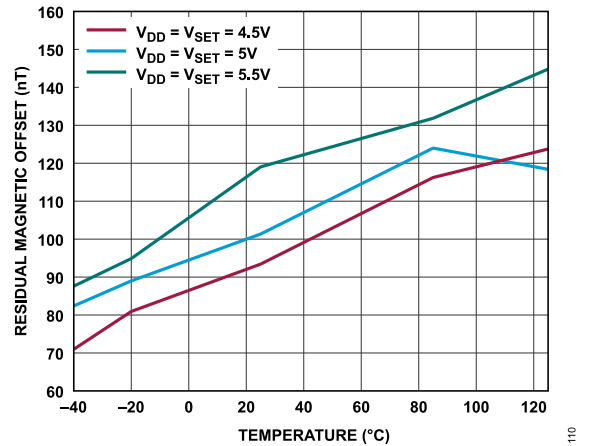


Figure 15. Residual Magnetic Offset vs. Temperature with Offset Correction

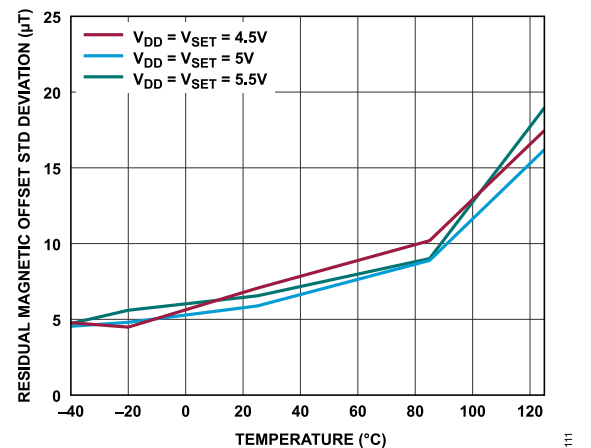


Figure 16. Residual Magnetic Offset STD Deviation vs. Temperature with Offset Correction

TYPICAL PERFORMANCE CHARACTERISTICS

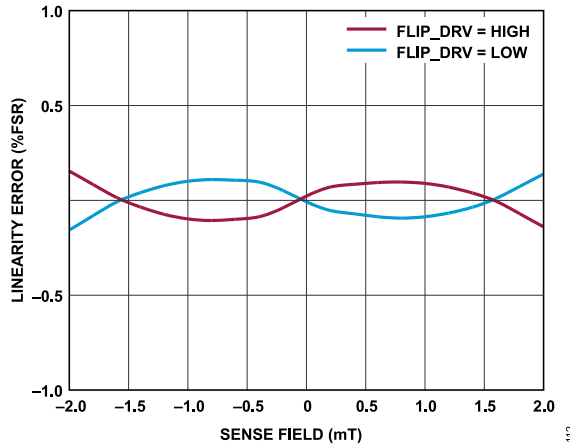


Figure 17. Linearity Error vs. Sense Field over ± 2 mT Range, $V_{DD} = V_{SET} = 5$ V, $G = 80$

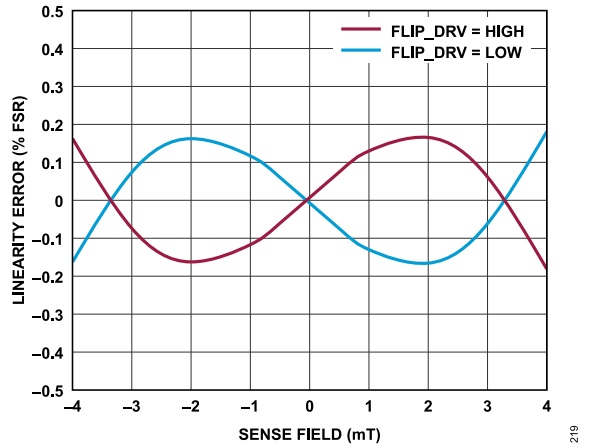


Figure 20. Linearity Error vs. Sense Field over ± 4 mT Range with Compensation, $V_{DD} = V_{SET} = 5$ V, $G = 80$

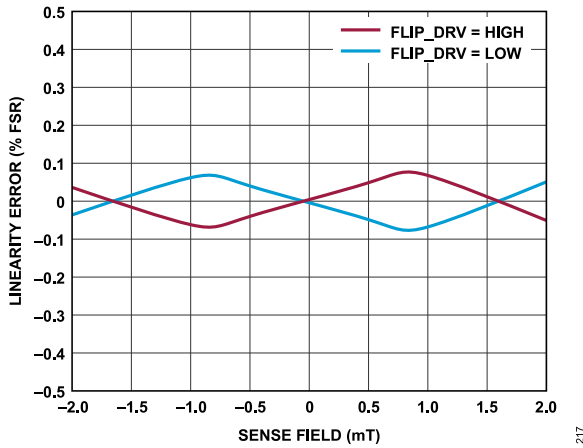


Figure 18. Linearity Error vs. Sense Field over ± 2 mT Range with Compensation, $V_{DD} = V_{SET} = 5$ V, $G = 80$

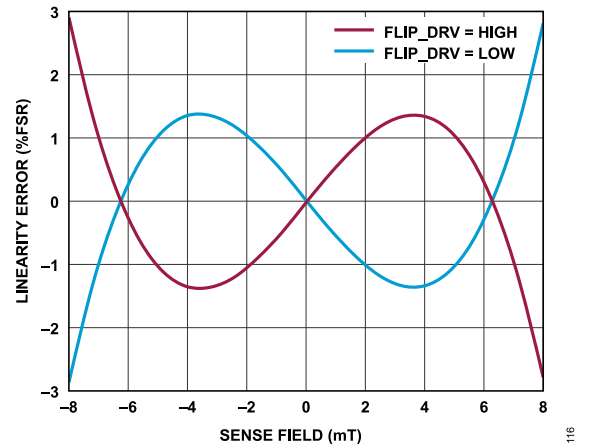


Figure 21. Linearity Error vs. Sense Field over ± 8 mT Range, $V_{DD} = V_{SET} = 5$ V, $G = 80$

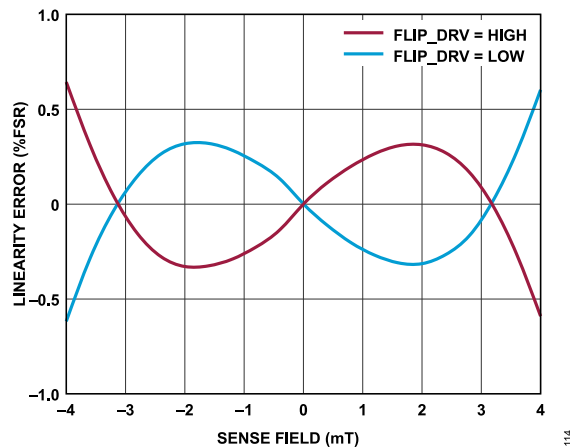


Figure 19. Linearity Error vs. Sense Field over ± 4 mT Range, $V_{DD} = V_{SET} = 5$ V, $G = 80$

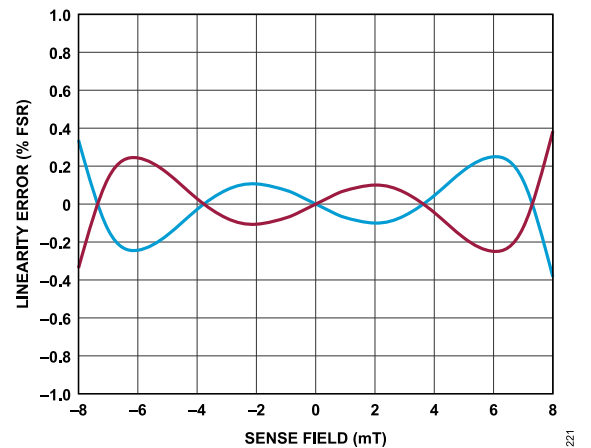


Figure 22. Linearity Error vs. Sense Field over ± 8 mT Range with Compensation, $V_{DD} = V_{SET} = 5$ V, $G = 80$

TYPICAL PERFORMANCE CHARACTERISTICS

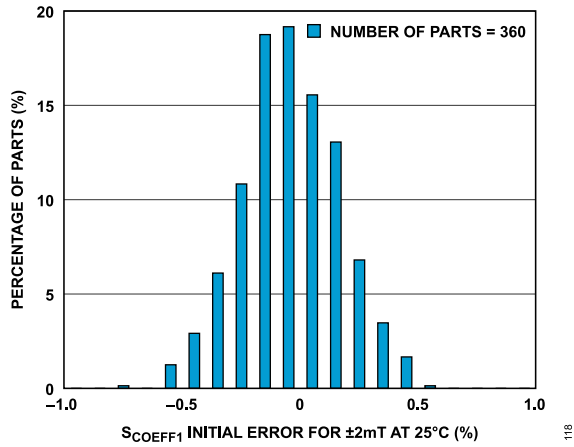


Figure 23. S_{COEFF1} Initial Error for ± 2 mT at 25°C

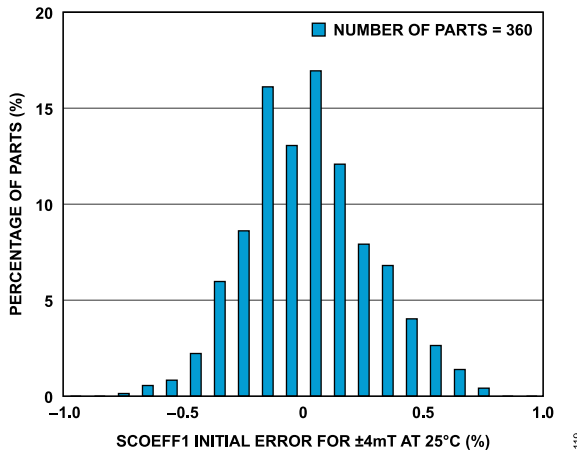


Figure 24. S_{COEFF1} Initial Error for ± 4 mT at 25°C

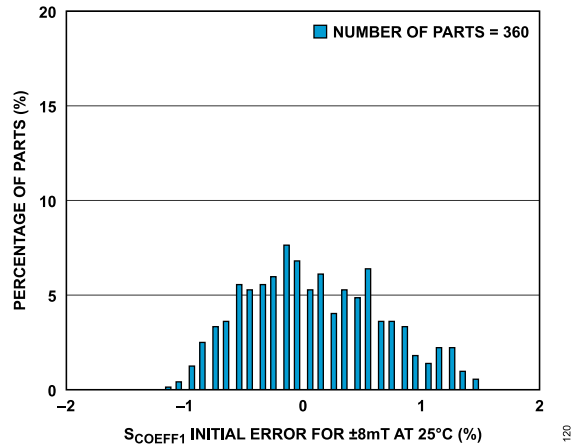


Figure 25. S_{COEFF1} Initial Error for ± 8 mT at 25°C

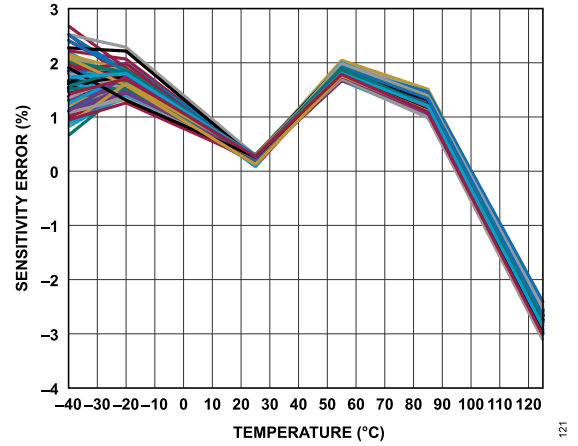


Figure 26. Sensitivity Error vs. Temperature, $B_{SENSE} = 8$ mT, $G = 80$, $V_{SET} = V_{DD} = 5$ V

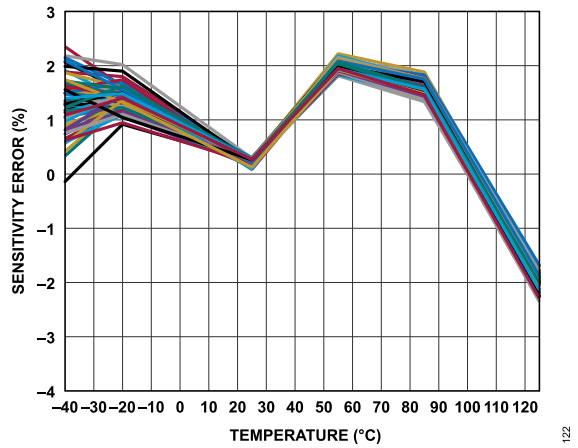


Figure 27. Sensitivity Error vs. Temperature, $B_{SENSE} = 4$ mT, $G = 80$, $V_{SET} = V_{DD} = 5$ V

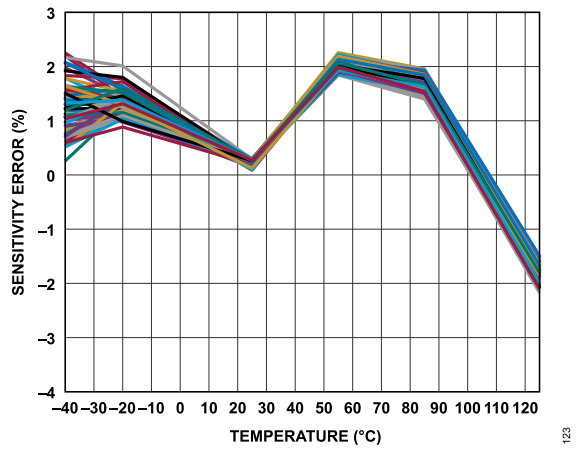


Figure 28. Sensitivity Error vs. Temperature, $B_{SENSE} = 2$ mT, $G = 80$, $V_{SET} = V_{DD} = 5$ V

TYPICAL PERFORMANCE CHARACTERISTICS

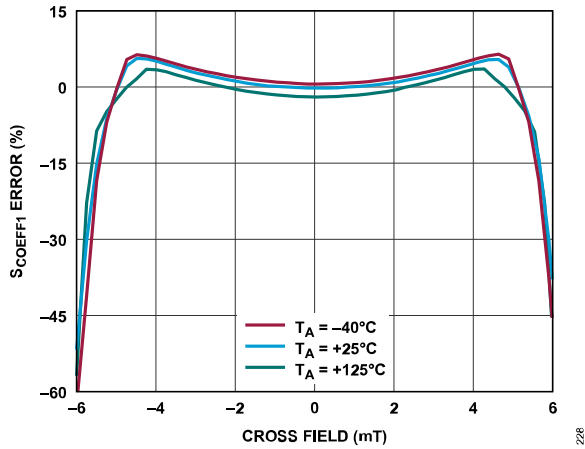


Figure 29. S_{COEFF1} Error vs. Cross Field over Temperature, Maximum Error for Sense Field Sweep of ± 8 mT

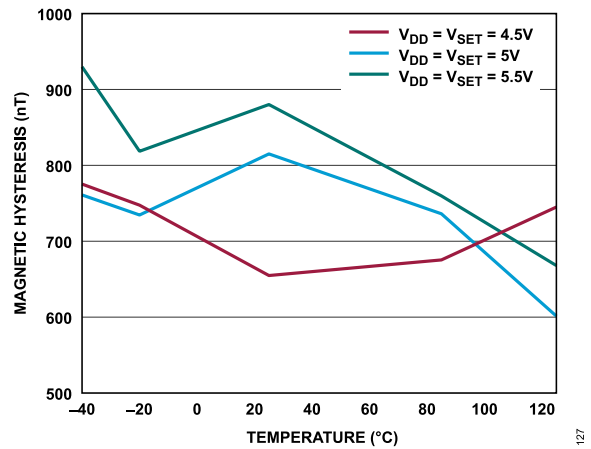


Figure 32. Magnetic Hysteresis vs. Temperature, -8 mT to $+8$ mT Range, No Flipping

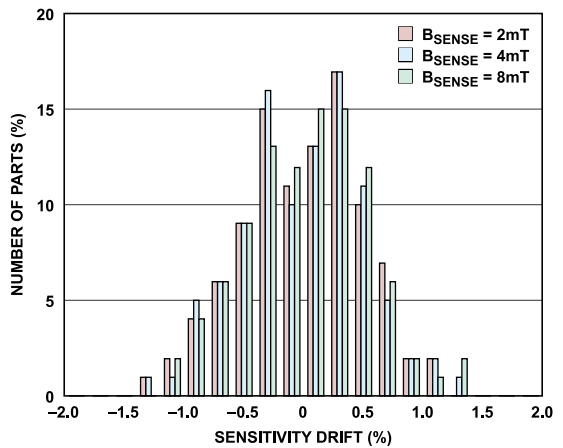


Figure 30. Sensitivity Drift for S_{COEFF1} , High Temperature Over Lifetime (HTOL), Parts Tested Over 1000 Hours, $125^{\circ}\text{C} <$ Junction Temperature $< 135^{\circ}\text{C}$

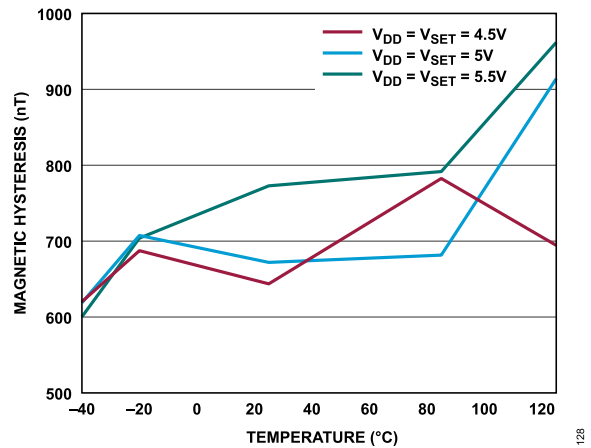


Figure 33. Magnetic Hysteresis vs. Temperature, -8 mT to $+8$ mT Range, With Flipping

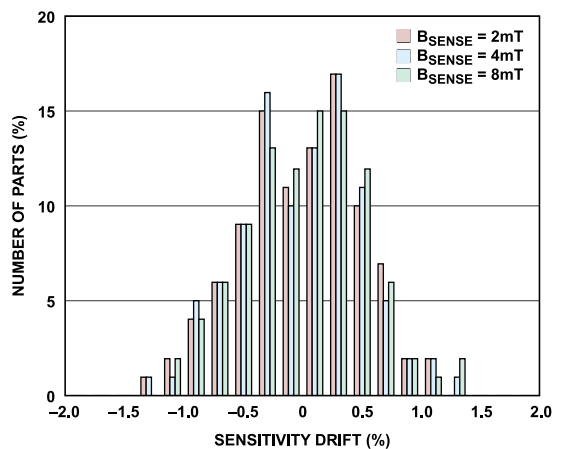


Figure 31. Sensitivity Drift for S_{COEFF1} , Highly Accelerated Stress Test (HAST), Parts Tested Over 96 Hours at 130°C , 85% Relative Humidity, 33.3 psia

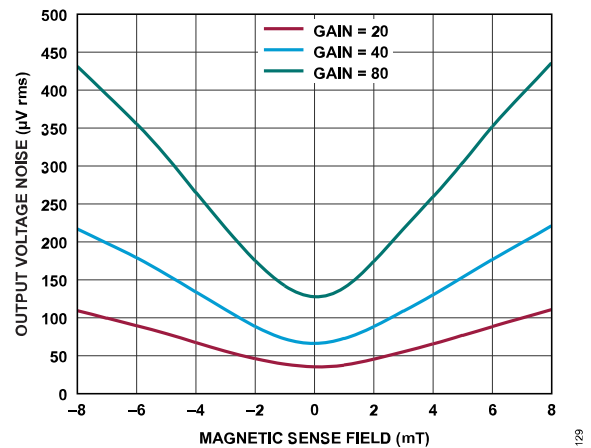


Figure 34. Output Voltage Noise vs. Magnetic Sense Field, $V_{SET} = V_{DD} = 5$ V, $T_A = 25^{\circ}\text{C}$

TYPICAL PERFORMANCE CHARACTERISTICS

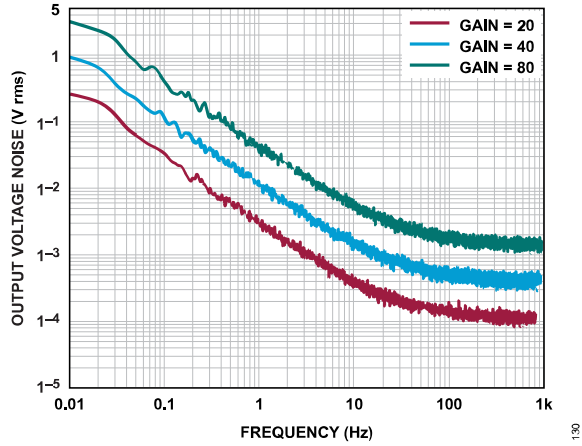


Figure 35. Output Voltage Noise vs. Frequency, Chopping Disabled

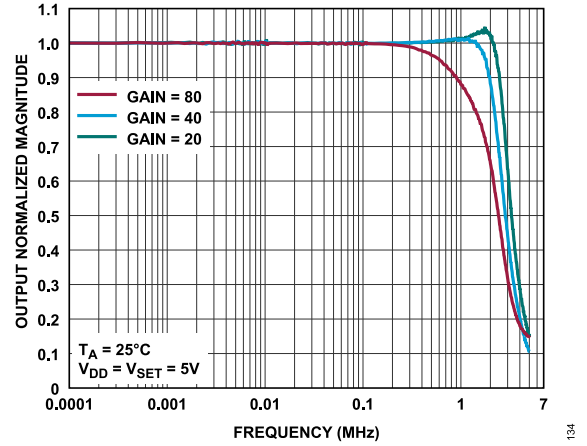


Figure 38. Output Normalized Magnitude vs. Frequency, $V_{SET} = V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

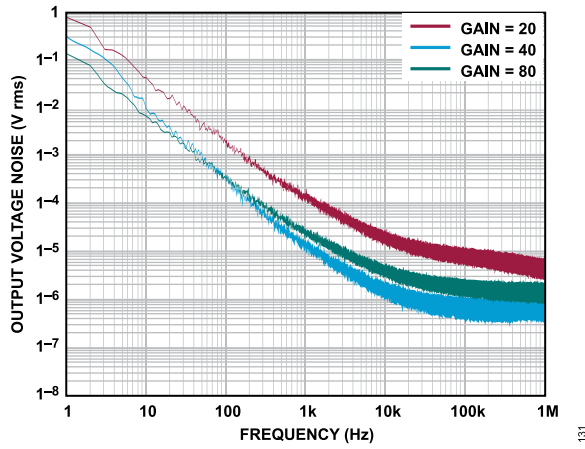


Figure 36. Output Voltage Noise vs. Frequency, Chopping Enabled, All Gain Settings

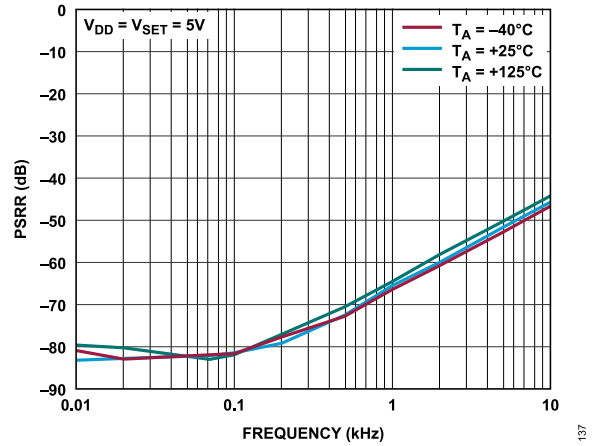


Figure 39. PSRR vs. Frequency, $B_{SENSE} = 0\text{ mT}$

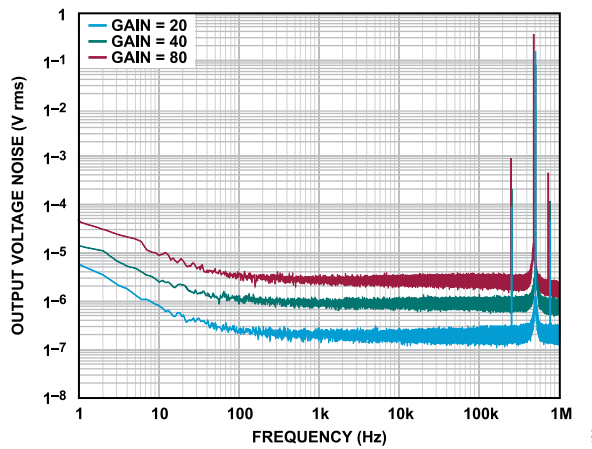


Figure 37. Output Voltage Noise vs. Frequency, External Chopping, $f_{SYNC} = 1.6\text{ MHz}$, All Gain Settings

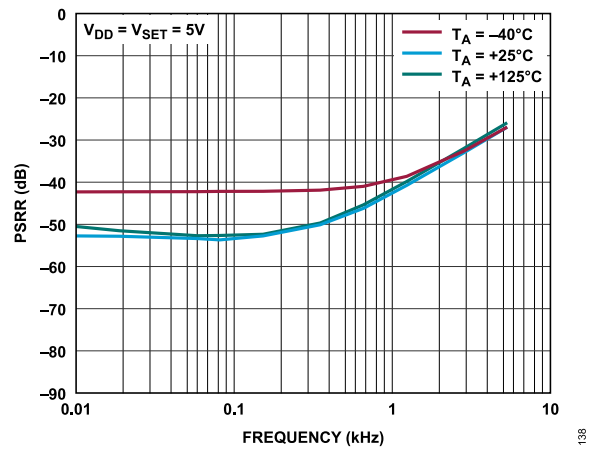


Figure 40. PSRR vs. Frequency, $B_{SENSE} = 8\text{ mT}$

TERMINOLOGY

B_{SENSE}

B_{SENSE} is defined as the magnetic field vector in parallel with the sense field axis of the sensor and in-plane with the package of the sensor. Figure 41 shows the sense field axis relative to the ADAF1080 package.

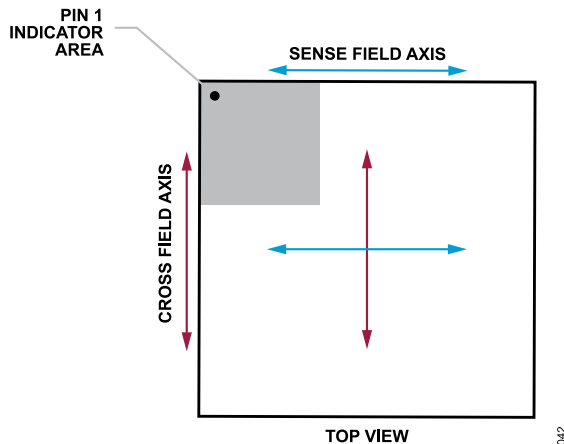


Figure 41. Sense Field Axis and Cross Field Axis

S_{DEVICE}

S_{DEVICE} is the magnetic sensitivity of the device defined as the proportional change of the voltage output of the sensor due to a change in the applied magnetic field on the sense field axis at $T_A = 25^\circ\text{C}$, as shown in Figure 41.

S_{COEFF1}

S_{COEFF1} is the best-fit coefficient for a first-order linear fit of the magnetic sensitivity of the device (S_{DEVICE}) in the sense field axis for each of the three ranges shown in Table 2, Table 3, and Table 4.

$S_{COEFF1} = \text{Linear Best Fit}(B_{SENSE} \text{ vs. } V_{OUT})$

S_{COEFF3}

S_{COEFF3} is the third-order coefficient used to compensate nonlinearity of the output of the ADAF1080.

S_{ERROR}

S_{ERROR} is the sensitivity error defined as the difference between the measured sensitivity of the device (S_{DEVICE}) and the ideal sensitivity (S_{COEFF1}). S_{ERROR} is expressed as a percentage of the ideal sensitivity and is mathematically defined as follows:

$$S_{ERROR} = \frac{(S_{DEVICE} - S_{COEFF1})}{S_{COEFF1}} \times 100$$

S_{DEVICE_T}

S_{DEVICE_T} is the measured sensitivity for the device at the operating temperature.

S_{ERROR_TC}

S_{ERROR_TC} is the sensitivity error over temperature and is defined as difference between the measured sensitivity of a device at the operating temperature against the measured sensitivity at $T_A = 25^\circ\text{C}$, S_{DEVICE} . S_{ERROR_TC} is expressed as a percentage of the ideal sensitivity and is mathematically defined as follows:

$$S_{ERROR_TC} = \frac{(S_{DEVICE_T} - S_{DEVICE})}{S_{COEFF1}} \times 100$$

Full-Scale Range (FSR)

The FSR of a bipolar measurement is defined as the variation of the output voltage when the highest valid positive and negative magnetic fields are applied in the application.

The FSR of a ± 8 mT magnetic field range is the change in output voltage over a 16 mT range.

The FSR of a unipolar measurement is equivalent to the variation of the output voltage between 0 mT and the highest absolute value of the magnetic field range.

The FSR of a 0 mT to 8 mT range is the change in output voltage over an 8 mT range.

L_{ERROR}

L_{ERROR} is the percentage linearity error and is defined as the worst case deviation of V_{OUT} from the expected V_{OUT} based on S_{COEFF1} across the operating magnetic field range. L_{ERROR} does not include offset error, sensitivity error, temperature related errors, or noise. L_{ERROR} is expressed as a percentage of the output voltage FSR and is mathematically defined as follows:

$$L_{ERROR} = \frac{(S_{COEFF1} \times B_{SENSE}) - (S_{DEVICE} \times B_{SENSE})}{FSR} \times 100$$

Cross Field (B_{CROSS})

B_{CROSS} is defined as the magnetic field vector perpendicular to, and in plane with, the sense field axis of the sensor.

The component of the magnetic field vector out of plane of the package is not considered as cross field because it does not affect the sensor, and it can be ignored. Figure 41 outlines this cross field axis relative to the ADAF1080 package.

Stray Field

Stray field is any interferer magnetic field that is measurable on the sense field axis of the ADAF1080 but is not the target magnetic field to be measured. These interferers can be generated by a nearby magnet, a current into a conductor, the influence of a nearby ferromagnetic material, or the magnetic field of the earth. The ADAF1080 cannot differentiate between stray fields and target fields. Therefore, PCB and system board layout and component placement is critical to minimize stray fields and to achieve optimal measurement results as described in the [Recommended PCB Layout](#) section.

TERMINOLOGY**Output Error due to a Cross Field**

S_{ERROC_BC} is the error due to the presence of a cross field. S_{ERROC_BC} is defined as the percentage change of the output voltage in the presence of a cross field compared to the output voltage with no cross field.

$$S_{ERROR_BC} = \frac{V_{OUT}(B_{CROSS}) - V_{OUT}(B_{CROSS} = 0)}{V_{OUT}(B_{CROSS} = 0)} \times 100$$

where:

$V_{OUT}(B_{CROSS})$ is the measured output voltage of the device with a cross field present.

$V_{OUT}(B_{CROSS} = 0)$ is the measured output voltage of the device with no cross field present.

THEORY OF OPERATION

The ADAF1080 provides a completely coreless solution for wide range low-noise and low-hysteresis magnetic field measurements, with reduced package size and current consumption. Unlike traditional Hall-based magnetic field sensors, the ADAF1080 does not require a magnetic core or flux concentrator.

The ADAF1080 includes the following in a single package:

- ▶ An AMR sensor with an electrical-offset cancellation capability provided through an integrated flip coil
- ▶ An integrated, precision, zero-drift instrumentation amplifier and ADC driver for signal conditioning
- ▶ Digital circuitry for additional functionality such as gain control, temperature compensation, electrical-offset cancellation, and clock synchronization

AMR MAGNETIC FIELD SENSOR

The integrated AMR magnetic field sensor is composed of four AMR elements in a Wheatstone bridge configuration. The output voltage of the Wheatstone bridge changes when the elements sense a magnetic field along the sense field axis as shown in Figure 42. The cross field axis of the sensor is the long axis of the AMR elements. The bridge output is then amplified by the integrated signal conditioning circuit (see the [Integrated Signal-Chain Conditioning](#) section). The bridge supply is driven by the internal bridge driver circuit that keeps the bridge supply proportional to V_{DD} .

The transfer function of the ADAF1080 can be described by the following equation:

$$V_{OUT} = (B_{SENSE} \times S_{DEVICE}) \times \frac{V_{DD}}{5} + \frac{V_{SET}}{2} \tag{1}$$

where:

V_{OUT} is the measured output of the ADAF1080 on the VOUT pin.

B_{SENSE} is the magnetic field along the sense field axis.

S_{DEVICE} is the sensitivity of the device due to a magnetic field on the sense field axis.

V_{DD} is the voltage on the VDD pin.

V_{SET} is the voltage on the VSET pin.

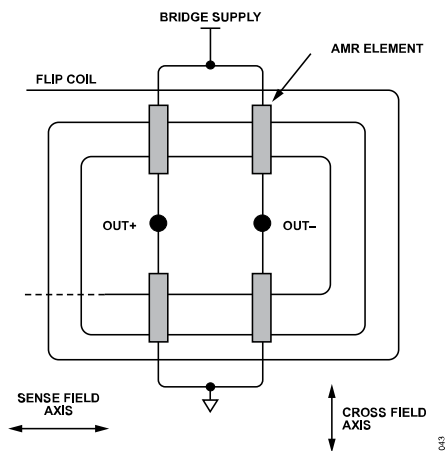


Figure 42. AMR Sensor Bridge and Flip Coil

A short high-current pulse is applied on the flip coil by the flip coil driver circuitry to generate a strong, localized magnetic field at the AMR sensor elements to align the internal magnetic domains of the sensor to set its sensitivity polarity. Changing the polarity of this current pulse reverses the magnetic domains of the sensor along the easy axis, as shown in Figure 43, which can be used for electrical-offset measurement and cancellation (see the [Flip Coil and Flip Coil Driver](#) section). The flip coil can also be used after a saturation event to realign the magnetic domain along the easy axis and to reset the sensitivity polarity.

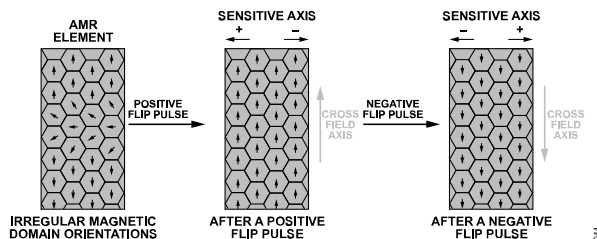


Figure 43. Effect of the Flip Coil to Align the Magnetic Domains of the Sensor

SENSE FIELD AXIS

The integrated AMR sensor in the ADAF1080 produces an analog output that is proportional to the magnetic field strength on a single axis in the plane of the package. This AMR sensor is capable of sensing over a wide magnetic field up to ± 8 mT.

The sense field axis of the ADAF1080 is shown in Figure 44 and is referenced by Pin 1 of the lead frame chip-scale package.

THEORY OF OPERATION

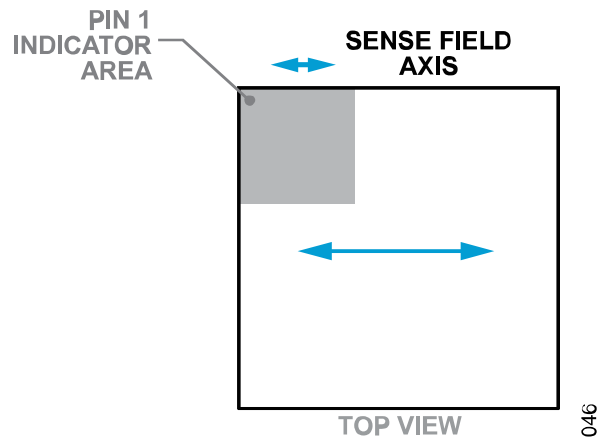


Figure 44. Sense Field Axis of the ADAF1080

Due to its coreless design, the ADAF1080 is also capable of measuring small magnetic fields in the nT range.

THEORY OF OPERATION

OPERATING MAGNETIC FIELD RANGE

The ADAF1080 AMR field sensor is capable of accurately measuring magnetic fields in the ± 8 mT range along the sense field axis.

The ADAF1080 has a defined operating window dependent on the combination of the sense field and the cross field detected by the sensor. The valid operating region for the ADAF1080 over temperature is shown in Figure 45. The lines plotted within Figure 45 define the worst-case limits for a combination of the sense field and the cross field that the sensor can be subjected to while maintaining the sensitivity coefficient in the Specifications section.

Outside this operating region, sensitivity of the sensor reduces from the specified values. If the combination of the sense field and the cross field is too far outside the defined operating region shown in Figure 45, the sensitivity coefficient of the sensor can change significantly, or in extreme cases, become zero. If the sensitivity becomes zero, the output voltage of the ADAF1080 does not change with a changing magnetic field. The diagnostic coil can be used to determine if such an event has occurred as described in the Diagnostic Coil section.

When such an event occurs, the functionality of the sensor can be restored by flipping the sensor by driving the FLIP_DRV pin with a rising or falling edge provided that the combination of the sense field and the cross field is within the operating region. For more information on the flipping functionality, refer to the Flip Coil and Flip Coil Driver section.

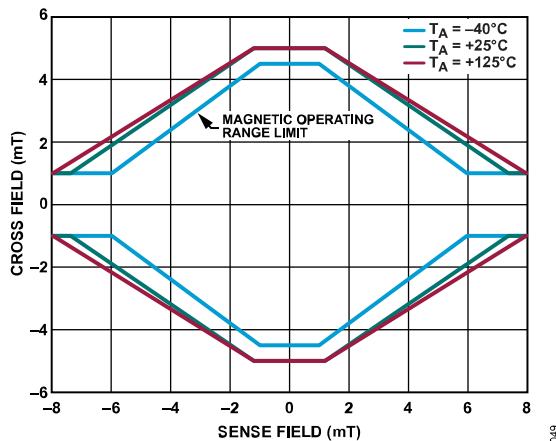


Figure 45. Magnetic Field Operating Region of the ADAF1080

INTEGRATED SIGNAL-CHAIN CONDITIONING

Figure 46 shows the internal sensing signal chain, consisting of the AMR bridge, flip coil, and the supporting functions for signal amplification, control, filtering, and buffering.

The sensor sensitivity of an AMR field sensor is inversely proportional to the temperature. To improve the stability of output sensitivity over temperature, a bridge driver circuit is used to generate a bridge supply voltage that is proportional to temperature. Full factory calibration of the bridge driver circuit enables the ADAF1080

to deliver precision stable magnetic field measurements over the full temperature range.

The precision instrumentation amplifier has programmable gains ($G = 20, 40, \text{ or } 80$) that are set by using the A0 and A1 pins. The amplified output is then biased around a common-mode voltage of $V_{SET}/2$ and buffered to drive the input of an external ADC that can be referenced to the supply voltage to improve PSRR. This biasing of the output around a configurable common-mode voltage leads to optimal use of the input range of the ADC by ensuring that the input voltage of the ADC tracks the reference voltage of the ADC in a ratiometric manner.

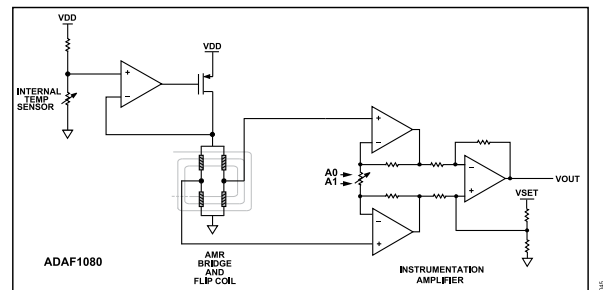


Figure 46. A Detailed Internal Block Diagram of the ADAF1080

PRECISION INSTRUMENTATION AMPLIFIER

The architecture of the integrated instrumentation amplifier consists of a precision, low-noise, zero-drift amplifier that features a proprietary chopping technique. This chopping technique offers a low input-offset voltage (V_{OFFSET}) and input-offset voltage drift (V_{OFFSET_LT} and TC_{OFFSET}). The zero-drift design also features ripple suppression circuitry that removes glitches and other artifacts caused by chopping.

Offset-voltage errors caused by common-mode voltage swings are corrected by the chopping technique, resulting in a high CMRR of the static magnetic field. The amplifier features low-input broadband noise of $15 \text{ nV}/\sqrt{\text{Hz}}$ with a low flicker noise component due to the use of chopping. These features are ideal for amplification of the small AMR bridge signals for high-precision sensing applications.

The gain of the programmable gain instrumentation amplifier (PGIA) is set through the digital pins (A1 and A0). There are three possible gain settings that can be used based on the magnetic field ranges that are used in the application. For example, if the application only needs a magnetic field range of ± 2 mT, using a PGIA gain = 80 delivers the largest output signal. However, if the magnetic field range is ± 8 mT, using a PGIA gain = 20 enables the entire magnetic field range to be measured without potentially overranging an ADC. The gain can be fixed using pull-up and pull-down resistors or controlled dynamically during the application by a microcontroller GPIO. The digital inputs (A0 and A1) are internally pulled up to VDD through a $300 \text{ k}\Omega$ pull-up resistor. Therefore, the default gain is 80 if no external voltage is applied, and the A0 and A1 pins are left no connect. Table 14 outlines the truth table logic for the three gain setting of the ADAF1080.

THEORY OF OPERATION

Table 14. Truth Table Logic Levels for the PGIA

A1	A0	Gain
GND	V _{DD}	20
GND	GND	Do not use
V _{DD}	GND	40
V _{DD}	V _{DD}	80

FLIP COIL AND FLIP COIL DRIVER

The integrated flip coil at the AMR sensors enables the user to set and reset the magnetic domains of the AMR field sensor to align the sense field axis in the positive or negative polarity, as described in the [AMR Magnetic Field Sensor](#) section.

This flip coil can be used to:

- ▶ Change the polarity of the AMR sensor enabling electrical-offset cancellation, including thermal coefficient and lifetime drift
- ▶ Set the sensor to a known state at startup
- ▶ Reset the sensor following a magnetic saturation event

For ease-of-use, the ADAF1080 integrates a flip coil driver. A rising edge on the FLIP_DRV pin generates a positive current pulse through the flip coil, setting a positive sensitive polarity on the sense field axis, and a falling edge generates a negative current pulse through the flip coil, setting a negative sensitive polarity on the sense field axis. In [Figure 47](#), the orientation of the sense field axis is shown with the arrows.

If FLIP_DRV is left floating or connected to V_{DD}, the FLIP_DRV pin automatically generates at startup a positive-current pulse to ensure initialization of the sensor with a positive-sensitivity polarity.

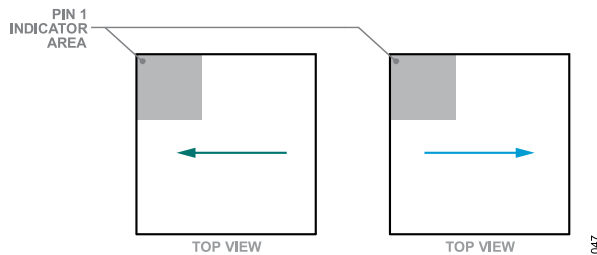


Figure 47. The Polarity of the AMR Sensor Sensitivity (Positive Sensitivity Polarity When FLIP_DRV Set High Shown on the Left, and Negative Sensitivity Polarity when FLIP_DRV Set Low Shown on the Right)

The output of the sensor after a negative flip edge can be defined as the following:

$$V_{OUTFn} = -B_{SENSE} \times S_{DEVICE} + \frac{V_{SET}}{2} + V_{OFFSET} \quad (2)$$

where:

B_{SENSE} is the magnetic field vector on the sense field axis of the ADAF1080.

S_{DEVICE} is the sensitivity of the ADAF1080 due to a magnetic field on the sense field axis.

V_{SET} is the voltage on the VSET pin.

V_{OFFSET} is the output voltage when B_{SENSE} = 0 mT.

After a positive flip edge, the output of the sensor can be defined as the following:

$$V_{OUTFp} = B_{SENSE} \times S_{DEVICE} + \frac{V_{SET}}{2} + V_{OFFSET} \quad (3)$$

[Equation 2](#) shows the sensor response after a negative-current pulse through the flip coil, and [Equation 3](#) shows the sensor response after a positive-current pulse through the flip coil. V_{OFFSET} is the electrical output from the device with zero magnetic field applied as shown in [Figure 48](#)

Using [Equation 2](#) and [Equation 3](#), the user can calculate and remove the electrical offset from the measurement, as described in the [Electrical Offset Cancellation](#) section.

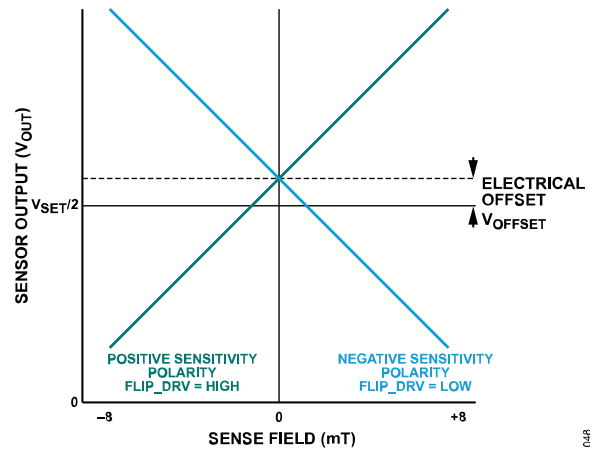


Figure 48. Sensor Response Following a Positive and a Negative Current Pulse Through the Flip Coil

DIAGNOSTIC COIL

The lead frame of the ADAF1080 can be used to provide a conductive path such that a known current can be applied at the AMR magnetic sensor to generate a known magnetic field. The exposed pad of the ADAF1080 package is fused with Pin 8 and Pin 18. This conductive path is referred to as the diagnostic coil (see [Figure 49](#)). The diagnostic coil enables the user to generate a known magnetic field that can verify the sensitivity of the AMR sensor. When a current (I_{DIAG}) is driven through the diagnostic coil, a magnetic field (B_{DIAG}) is sensed by the AMR sensor as shown in the following equation. Ensure that the maximum diagnostic current (I_{DIAG}) does not exceed 100 mA, and that the time duration of the diagnostic coil excitation is limited due to thermal considerations. To calculate the magnetic field detected by the AMR sensor (B_{DIAG}) using the following equation:

$$B_{DIAG} = (22.8 \mu\text{T}/100 \text{ mA}) \times I_{DIAG} \quad (4)$$

THEORY OF OPERATION

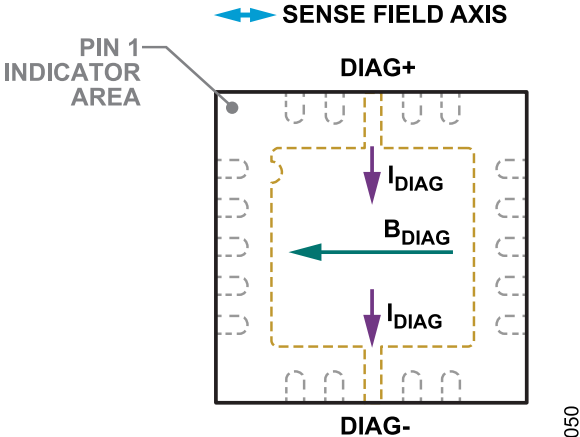


Figure 49. Sense Field Axis

050

APPLICATIONS INFORMATION

The ADAF1080 is an integrated magnetic field sensor and signal conditioning ASIC that can be used with an ADC and microcontroller, digital signal processor (DSP), and/or field-programmable gate array (FPGA) to build a complete ± 8 mT contactless magnetic field sensing solution or a contactless current sensing solution capable of measuring currents in excess of ± 500 A.

TYPICAL APPLICATION DIAGRAM

Figure 50 shows a single ADAF1080 connected to an ADC operating at 3.3 V and a microcontroller showing the required external components.

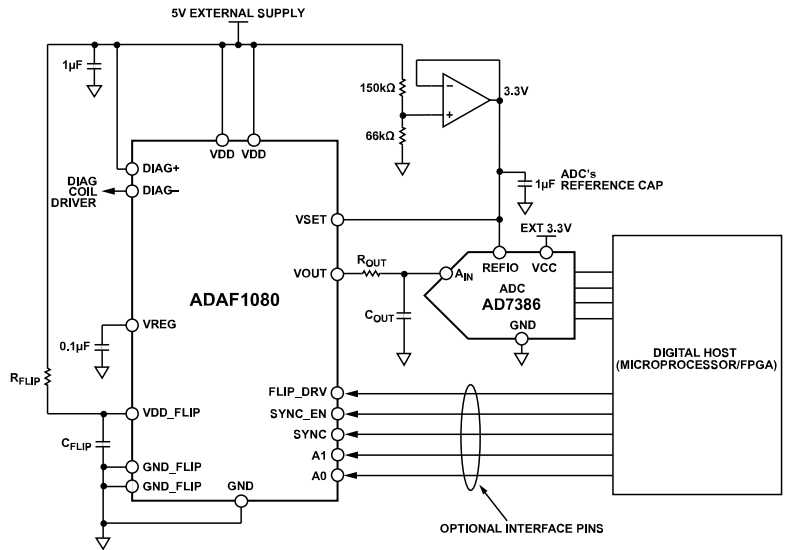


Figure 50. Typical Application Diagram for Magnetic Field Sensing with the ADAF1080 and an ADC Operating at 3.3 V

APPLICATIONS INFORMATION

RATIOMETRIC OUTPUT CONFIGURATION

The typical applications of the ADAF1080 are designed to be ratiometric to the supply voltage to prevent any power supply variations from corrupting the magnetic field measurements. As outlined previously in the [AMR Magnetic Field Sensor](#) section, the output of the ADAF1080 can be described by the following equation:

$$V_{OUT} = B_{SENSE} \times S_{DEVICE} \times \frac{V_{DD}}{5} + \frac{V_{SET}}{2} \tag{5}$$

The typical transfer function of an n-bit ADC can be simplified to the following equation:

$$Digital\ Code = \left(\frac{V_{IN}}{REF_{ADC}} \times 2^n \right) \tag{6}$$

where:

V_{IN} is the voltage applied to the input pin of the ADC.

REF_{ADC} is the reference voltage of the ADC.

n is the number of bits of the ADC.

Therefore, by connecting REF_{ADC} , V_{DD} , and V_{SET} together, as shown in [Figure 51](#), the resulting conversion code is equivalent to the following:

$$Output\ Code = \left(\frac{B_{SENSE} \times S_{DEVICE} \times \frac{V_{DD}}{5} + \frac{V_{DD}}{2}}{V_{DD}} \right) \times 2^n \tag{7}$$

$$= B_{SENSE} \times S_{DEVICE} \times \frac{2^n}{5} + 2^{n-1}$$

$$= B_{SENSE} \times S_{DEVICE} \times \frac{2^n}{5} + Midcode$$

The converted result is independent of the supply voltage and supply voltage variation. Due to the ratiometric configuration, precision measurements can be achieved.

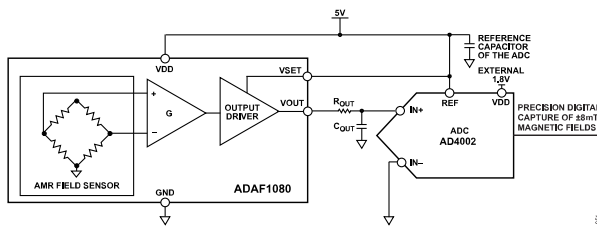


Figure 51. Simplified Schematic of a Ratiometric Configuration

AMPLIFIER SYNCHRONIZATION

The ADAF1080 integrates a precision zero-drift instrumentation amplifier that removes the offset and low frequency noise (1/f) noise of the internal circuitry at low frequencies but adds output ripple at the chopping frequency. This output ripple can be reduced with an output filter designed to get 20 dB attenuation at the chopping frequency.

Applications that require a wide bandwidth, or a fast response and low-phase delay behavior, can synchronize the sampling of the

ADC to the chopping frequency of the ADAF1080 to sample the output after the output ripple settles. This synchronizing of the ADC sampling to the chopping frequency enables the use of a wider bandwidth output filter while keeping the advantages of a zero-drift instrumentation amplifier.

The synchronization functionality can be enabled by driving the SYNC_EN pin to V_{DD} and driving the SYNC pin of the ADAF1080 by the convert input (CNV signal) of the ADC. The ADAF1080 internally generates a chopping clock frequency, $f_{CHOP} = f_{SYNC}/4$. This chopping clock is internally delayed by 50 ns to ensure that the chopping action of the amplifier follows the sampling action of the ADC aligned to the SYNC clock. Therefore, the ADC samples the fully settled ADAF1080 output before the next chopping action that triggers an output settling event. See [Figure 54](#) for the system-level timing diagram.

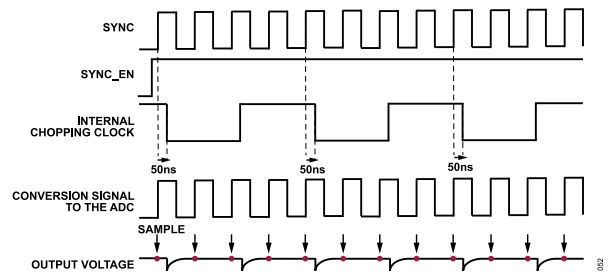


Figure 52. Synchronization of the ADC Sampling and the Chopping of the Amplifier

Applications that use a slower ADC sampling clock can generate a secondary clock from the SYNC clock, as shown in [Figure 53](#).

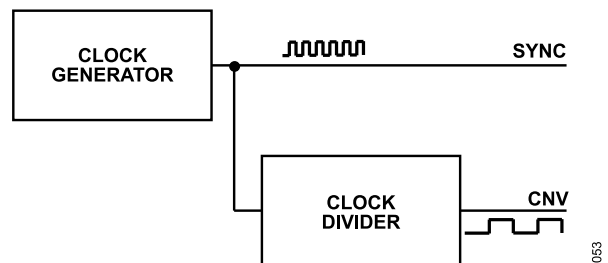


Figure 53. Generate CNV Signal for the ADC from SYNC Clock

In this case, the SYNC_EN transition from low to high can be used to indicate which rising edge of the SYNC signal must be used for the internal chopping signal for the PGIA so that the ADC has the longest settling time before sampling.

When SYNC_EN goes high, the next rising edge of the SYNC clock triggers the falling edge of the internal chopping clock after an internal delay of 50 ns, as shown in [Figure 54](#).

APPLICATIONS INFORMATION

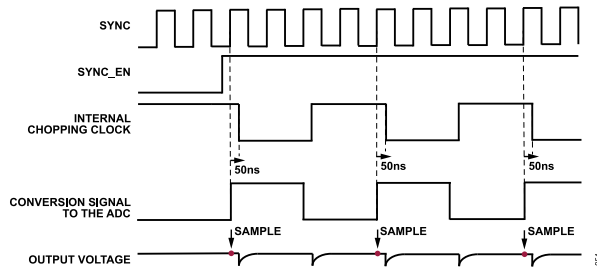


Figure 54. Synchronization of the ADAF1080 and the ADC Sampling for Slow Sampling Rate

Applications that do not require precision performance at low frequencies can disable the chopping functionality of the integrated PGIA by tying the SYNC pin to V_{DD} . When the chopping feature of the PGIA is disabled, the full bandwidth of the PGIA can be used for settling; however, higher flicker noise at lower frequencies is observed. Refer to Figure 37 and Figure 36 for PGIA noise performance with and without chopping.

Table 15 outlines the different modes available for the integrated amplifier.

Table 15. SYNC Pin Functionality

SYNC Pin State	SYNC_EN Pin	Instrumentation Amplifier Chopping Functionality
VDD	Don't care	Chopping disabled
GND	Don't care	Internal 200 kHz chopping
$400 \text{ kHz} < f_{\text{SYNC}} < 1.6 \text{ MHz}$	Low	Internal 200 kHz chopping
$400 \text{ kHz} < f_{\text{SYNC}} < 1.6 \text{ MHz}$	High	$f_{\text{SYNC}}/4$ chopping

If the SYNC and SYNC_EN pins are left floating, two internal 300 k Ω pull-downs ensure that the amplifier is chopping at 200 kHz as a default condition.

ELECTRICAL OFFSET CANCELLATION

The integrated flip coil driver can be used to reverse the sensitivity polarity so that all error sources related to the electrical offset and offset drift of the AMR sensor and signal conditioning circuit can be calibrated out of the sense magnetic field measurement.

For one time offset cancellation, in the presence of constant or low frequency magnetic fields, two measurements can be made with reverse states of the flip coil. The offset can then be calculated directly by the following equation:

$$V_{\text{OFFSET}} = \frac{V_{\text{OUTFn}} + V_{\text{OUTFp}}}{2} - \frac{V_{\text{SET}}}{2} \quad (8)$$

where:

V_{OUTFn} is the output of the ADAF1080 when FLIP_DRV is GND.

V_{OUTFp} is the output of the ADAF1080 when FLIP_DRV is V_{DD} .

V_{SET} is the voltage on the VSET pin.

Once the electrical offset is measured, this offset can be canceled in any further measurements as shown in the following equation:

$$V_{\text{OUT_OC}} = V_{\text{OUT}} - \frac{V_{\text{SET}}}{2} - V_{\text{OFFSET}} \quad (9)$$

where $V_{\text{OUT_OC}}$ is the offset canceled output voltage of the ADAF1080.

For periodic offset cancellation, the flip coil can be reversed at a fixed frequency, and the offset and offset drift can be removed by using the following equation:

$$V_{\text{OUT_OC}} = \frac{V_{\text{OUTFn}} - V_{\text{OUTFp}}}{2} \quad (10)$$

When using the flip coil driver, sampling of the output must take place after the settling time of the sensor (t_{SETTLING}) is complete, as shown in the Flip Coil and Measurement Timing section.

EXAMPLE OFFSET CALCULATION

The example offset calculation is an example where a 1 mT external field (B_{EXT}) is applied along the sense field axis of the ADAF1080 as shown in Figure 47.

In this example, the following is assumed:

- ▶ A0 and A1 = VDD, G = 80
- ▶ VDD = VSET = 5 V and $S_{\text{COEFF1}} = 199.25 \text{ mV/mT}$ based on the typical value for the $\pm 2 \text{ mT}$ magnetic range
- ▶ The electrical offset of the ADAF1080 and its signal chain is 2 mV

In this setup, the expected output of the ADAF1080 is the following when FLIP_DRV = GND:

$$V_{\text{OUTFn}} = -199.25 \text{ mV/mT} \times 1 \text{ mT} + \frac{5 \text{ V}}{2} + 2 \text{ mV} = 2.303 \text{ V} \quad (11)$$

In this setup, the expected output of the ADAF1080 is the following when FLIP_DRV = V_{DD} :

$$V_{\text{OUTFp}} = 199.25 \text{ mV/mT} \times 1 \text{ mT} + \frac{5 \text{ V}}{2} + 2 \text{ mV} = 2.701 \text{ V} \quad (12)$$

By combining these two measurements, the electrical offset can then be calculated as follows:

$$V_{\text{OFFSET}} = \frac{V_{\text{OUTFn}} + V_{\text{OUTFp}}}{2} - \frac{V_{\text{SET}}}{2} = 2.502 \text{ V} - \frac{5 \text{ V}}{2} = 2 \text{ mV} \quad (13)$$

Once the electrical offset is calculated, the result can be used for all future measurement as shown as follows to remove electrical offset errors from the output magnetic sense field measurements:

$$V_{\text{OUT_OC}} = V_{\text{OUT}} - \frac{V_{\text{SET}}}{2} - V_{\text{OFFSET}} \quad (14)$$

APPLICATIONS INFORMATION

NONLINEARITY COMPENSATION

The ADAF1080 output has a predictable and repetitive third-order dependency on the sense field.

This third-order dependency creates an error that can be calibrated out in the digital domain by implementing the following calculation:

$$B_{CALC} = \frac{(V_{OUT} - V_{OFFSET}) + (S_{COEFF3} \times (V_{OUT}^3 - V_{OFFSET}))}{S_{CALC1}} \quad (15)$$

where:

B_{CALC} is the calculated field measured by the ADAF1080.

V_{OUT} is the measured output of the ADAF1080.

V_{OFFSET} is the output voltage when $B_{SENSE} = 0$ mT.

S_{CALC1} is the linear best fit coefficient for the compensated output voltage using the following equation:

$$V_{CALC} = (V_{OUT} - V_{OFFSET}) + (S_{COEFF3} \times (V_{OUT}^3 - V_{OFFSET})) \quad (16)$$

FLIP COIL AND MEASUREMENT TIMING

Flipping the polarity of the sense field axis of the sensor is achieved with a rising or falling edge on the FLIP_DRV pin. When an edge is captured by the ADAF1080, the sensor is not immediately flipped, as shown in [Figure 2](#), an internal delay (t_{DELAY}) is implemented to allow for a field measurement to be made before the current pulse. This delay is to minimize the time where the output of the sensor is invalid while the flip pulse is applied. Following t_{DELAY} , the sensor polarity is flipped, while the sensor is being flipped, the output is invalid for $t_{INVALID}$. Following $t_{INVALID}$, a further settling time, $t_{SETTLING}$, is required for the output to settle.

$t_{SETTLING}$ is determined by the bandwidth of the amplifier and the bandwidth of the output anti-alias filter. For large output signals, the flipping action can also trigger the ripple suppression, loop settling behavior that has a time constant of approximately 10 μ s.

FLIPPING FREQUENCY

Driving the FLIP_DRV pin with a flipping clock signal is recommended to cancel electrical-offset temperature coefficient and electrical-offset lifetime drift of the sensor and its signal chain. The flipping frequency must be significantly faster than any sense field variations to correctly capture the electrical offset for the periodic offset cancellation. Therefore, the flipping functionality of the ADAF1080 enables measurement free from electrical offset regardless of the signal chain used in the application.

Flipping and offset calculation can be performed at any time to achieve best-in-class offset and should be performed when the electrical offset changes.

FLIP COIL FILTER CONFIGURATION

The AMR sensor requires a short but high-current pulse ($I_{FLIP_ON} = 2.4$ A for 1.25 μ s at $T_A = 25^\circ\text{C}$) to flip the sensitivity polarity. Place a 10 μ F capacitor (C_{FLIP}) close to the VDD_FLIP pin to act as a charge reservoir and to provide the flip pulse. The average current required for the flipping functionality is as follows:

$$I_{FLIP_AVG} = \frac{1.25 \mu\text{s} \times 2 \times I_{FLIP_ON}}{t_{CLK_FLIP_DRV}} \quad (17)$$

where:

I_{FLIP_ON} is the peak current required to flip the sensor.

$t_{CLK_FLIP_DRV}$ is the clock applied at the FLIP_DRV pin, as shown in [Figure 2](#).

To limit the in-rush current from the supply, use a series resistance (R_{FLIP}) between the VDD and VDD_FLIP pins. The recommended values for C_{FLIP} and R_{FLIP} are designed to handle the maximum flip frequency while limiting the impact on the supply. [Table 16](#) shows the recommended R_{FLIP} and C_{FLIP} for different flipping frequencies.

Table 16. Recommended R_{FLIP} and C_{FLIP} Values for Different FLIP_DRV Frequencies

FLIP_DRV Frequency with 50% Duty Cycle	R_{FLIP} (Ω)	C_{FLIP} (μ F)	Average Current I_{FLIP_AVG} with $T_A = 25^\circ\text{C}$
Up to 10 Hz	250	10	Up to 60 μ A
Up to 100 Hz	50	10	Up to 600 μ A
Up to 1000 Hz	10	10	Up to 6 mA

C_{FLIP} must be carefully chosen to obtain a capacitance of 10 μ F. Note that the voltage rating and behavior over temperature are important parameters to ensure that the capacitor has enough capacitance to supply the flip current required for the flip coil.

VSET VOLTAGE

The V_{SET} voltage can set the output common-mode voltage to half of the voltage applied to the VSET pin when interfacing with an ADC. Set the VSET pin to the output voltage range of the ADC to maximize the usable input range of the ADC.

To ensure a ratiometric measurement, keep the V_{SET} voltage and the ADC reference voltage proportional to, or equal to, the supply voltage, V_{DD} .

The typical application diagram shown in [Figure 50](#) and the design example shown in [Figure 58](#) show a ratiometric measurement configuration coupled with a 3.3 V and a 5 V ADC, respectively.

APPLICATIONS INFORMATION

OUTPUT ANTI-ALIAS FILTER

The ADAF1080 integrates an output driver to directly drive ADC inputs without the need for additional active components.

A passive anti-alias low-pass filter is recommended (R_{OUT} and C_{OUT}) to prevent the ADC from aliasing higher frequency noise and interferers. Choose values for the output resistor (R_{OUT}) and capacitor (C_{OUT}), as shown in [Figure 50](#) and [Table 17](#), according to the bandwidth and noise requirements in the application. Take ADC requirements into account for determining these values.

For high bandwidth applications, the ADC sampling event can be synchronized with the chopping feature of the ADAF1080, as explained in the [Amplifier Synchronization](#) section, to avoid intermodulation distortion, using the SYNC pin set according to [Table 15](#).

[Table 17](#) details typical R_{OUT} and C_{OUT} values for different bandwidth requirements.

Table 17. Recommended R_{OUT} and C_{OUT} Values for Different Filter Bandwidth on the VOUT Pin and Recommended Amplifier Modes

3 dB Bandwidth	R_{OUT}	C_{OUT}	Recommended Chopping Mode
1 kHz	16 k Ω	10 nF	SYNC_EN = V_{DD} and SYNC = GND or f_{SYNC}
10 kHz	1.6 k Ω	10 nF	SYNC_EN = V_{DD} and SYNC = or f_{SYNC}
20 kHz	820 Ω	10 nF	SYNC_EN = V_{DD} and SYNC = or f_{SYNC}
25 kHz	620 Ω	10 nF	Chopping disabled: SYNC_EN = GND and SYNC = V_{DD} External sync: SYNC_EN = V_{DD} and SYNC = f_{SYNC}
100 kHz	200 Ω	8.2 nF	Chopping disabled: SYNC_EN = GND and SYNC = V_{DD} External sync: SYNC_EN = V_{DD} and SYNC = f_{SYNC}
200 kHz	200 Ω	3.9 nF	Chopping disabled: SYNC_EN = GND and SYNC = V_{DD} External sync: SYNC_EN = V_{DD} and SYNC = f_{SYNC}
1 MHz	200 Ω	750 pF	Chopping disabled: SYNC_EN = GND and SYNC = V_{DD} External sync: SYNC_EN = V_{DD} , SYNC = f_{SYNC}
2 MHz	200 Ω	330 pF	Chopping disabled: SYNC_EN = GND and SYNC = V_{DD} External sync: SYNC_EN = V_{DD} and SYNC = f_{SYNC}

APPLICATIONS INFORMATION

DIAGNOSTIC COIL DRIVER

The diagnostic coil can be used to verify the sensitivity of the ADAF1080 by applying a known reference current between the DIAG+ and DIAG- pins and measuring the output with and without the reference current. Figure 55 shows a typical discrete circuit to generate the reference current using the V_{DIAG} reference voltage and an R_{DIAG} reference resistor.

When using multiple ADAF1080 sensors, a single diagnostic coil driver circuit can be used to drive all the diagnostic coils in series by connecting the DIAG+ and DIAG- pins of the sensors in a daisy-chain fashion.

Figure 56 shows an example of daisy chaining multiple ADAF1080 devices together using a common diagnostic coil driver.

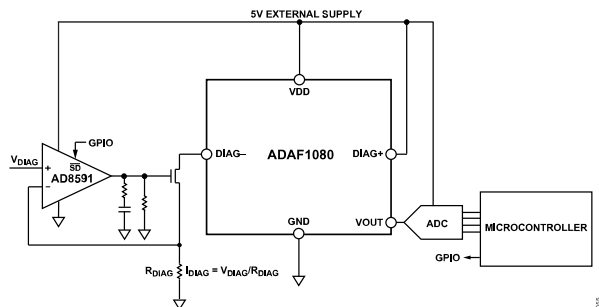


Figure 55. Diagnostic Coil Driver Example

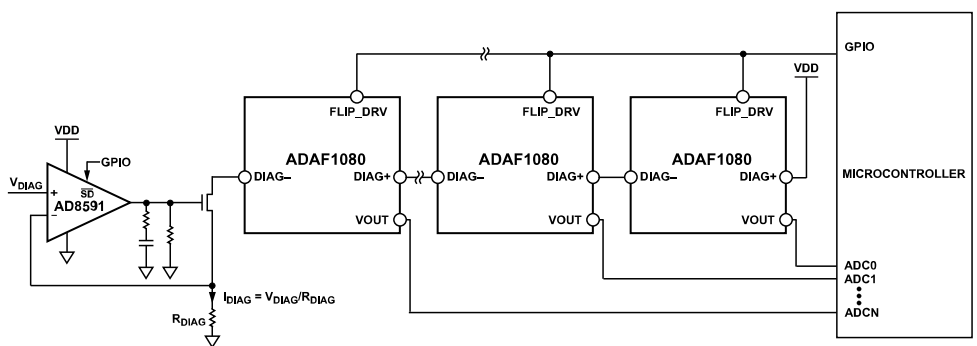


Figure 56. Multiple Sensors with the Diagnostic Coil Connected in a Daisy Chain

APPLICATIONS INFORMATION

TEMPERATURE MEASUREMENT

The VTEMP output pin is a voltage output for temperature monitoring purposes. This output voltage is ratiometric to the supply. For maximum accuracy, an initial calibration at a known temperature is recommended.

A temperature measurement can be extracted from the measurement of the VTEMP pin by the following equation:

$$T_{VTEMP} = \frac{V_{TEMP} - (V_{TEMP_{CAL}} - TC_{VTEMP} \times T_{CAL})}{TC_{VTEMP}} \quad (18)$$

where:

T_{VTEMP} is the calibrated temperature of the sensor.

V_{TEMP} is the output of the VTEMP pin.

$V_{TEMP_{CAL}}$ is the output of the VTEMP pin at the calibration temperature.

TC_{VTEMP} is the temperature coefficient of the sensor as shown in Table 8.

T_{CAL} is the temperature at which the calibration was performed.

VTEMP must be left disconnected when not in use.

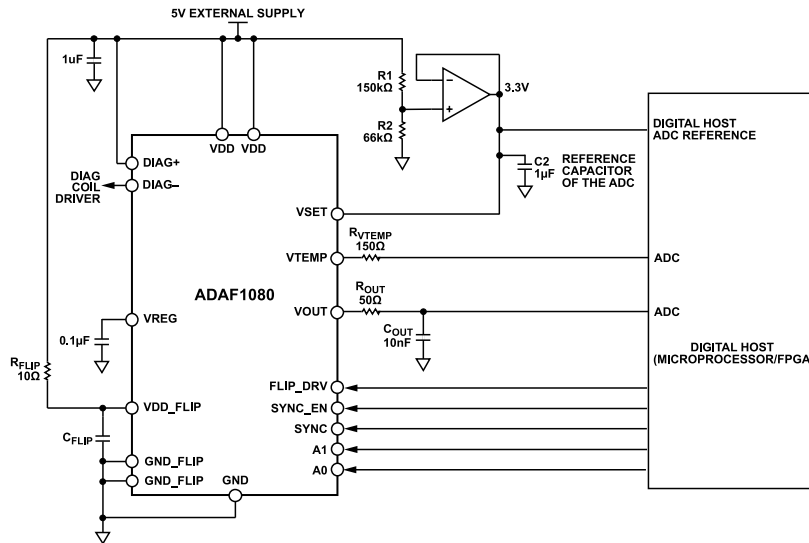


Figure 57. Circuit Diagram for Temperature Measurements Using VTEMP

APPLICATIONS INFORMATION

DESIGN EXAMPLES

Single-Axis Magnetic Field Sensor

A design example for a single-axis magnetometer capable of measuring a wide range of ± 8 mT magnetic fields using a single ADAF1080 is shown in Figure 58 where the ADAF1080 with $G =$

80 and a 20 kHz output filter is connected to an AD4002 ADC with a 5 V reference voltage. A microcontroller connected to such a configuration can be used as a single-axis magnetometer measuring a wide range of ± 8 mT or for accurate contactless current measurement.

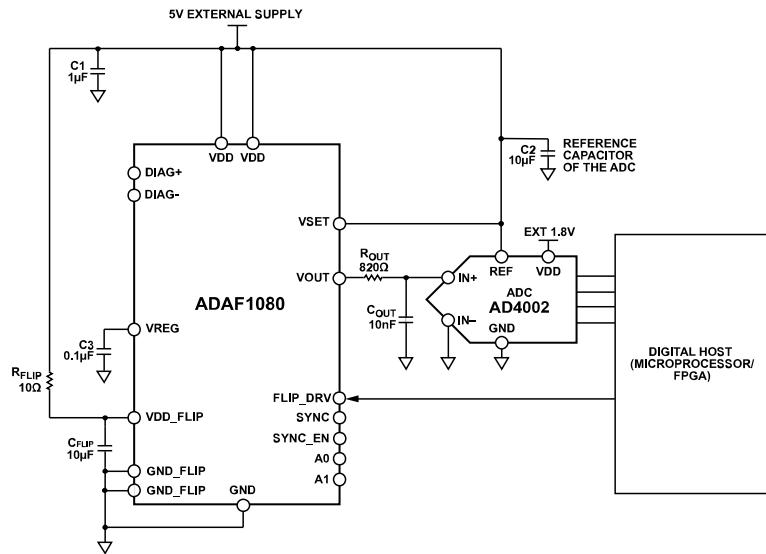


Figure 58. Design Example with 5 V ADC and 20 kHz Filter

Table 18. Component Values for the Design Example with 5 V ADC and 20 kHz Filter

Component	Description	Suggested Part Number
ADAF1080	Integrated ± 8 mT AMR magnetic field sensor and signal conditioner	ADAF1080BCPZ
AD4002	18-bit, 2 MSPS, precision, pseudo differential, SAR ADC	AD4002BRMZ
C1	1 μ F ceramic capacitor, 16 V, 0603	CGA3E1X7R1C105K080AC
C2 and C _{FLIP}	10 μ F ceramic capacitors, 25 V, 0805	GRM21BR61E106KA73L
C3	0.1 μ F ceramic capacitor	CL10B104KB8NNWC
C _{OUT}	10 nF ceramic capacitor	06035C103JAT2A
R _{OUT}	820 Ω resistor, 1/10 W, 1%, 0603, surface-mount device (SMD)	RC0603FR-10820RL
R _{FLIP}	10 Ω resistor, 1/10 W, 1%, 0603, SMD	WR06X10R0FTL
C _{FLIP}	10 μ F ceramic capacitors, 25 V, 0805	GRM21BR61E106KA73L

APPLICATIONS INFORMATION

Contactless Current Measurement up to ±640 A Using Three ADAF1080 Sensors in a Ring Architecture

Three ADAF1080 sensors can be used in a ring architecture to achieve contactless current measurements up to ±200 A nominal with ±640 A over current detection by measuring the magnetic

field generated by a conductor. A reference design of this ring architecture that uses three ADAF1080 sensors is available as the EVAL-ADAF1080-3EBZ customer evaluation board. Figure 59 shows three ADAF1080 devices, G = 80, connected to a summing amplifier and a 14.7 kHz filter to average the output of the three sensors and to minimize error due to mechanical tolerances and nearby magnetic field interference.

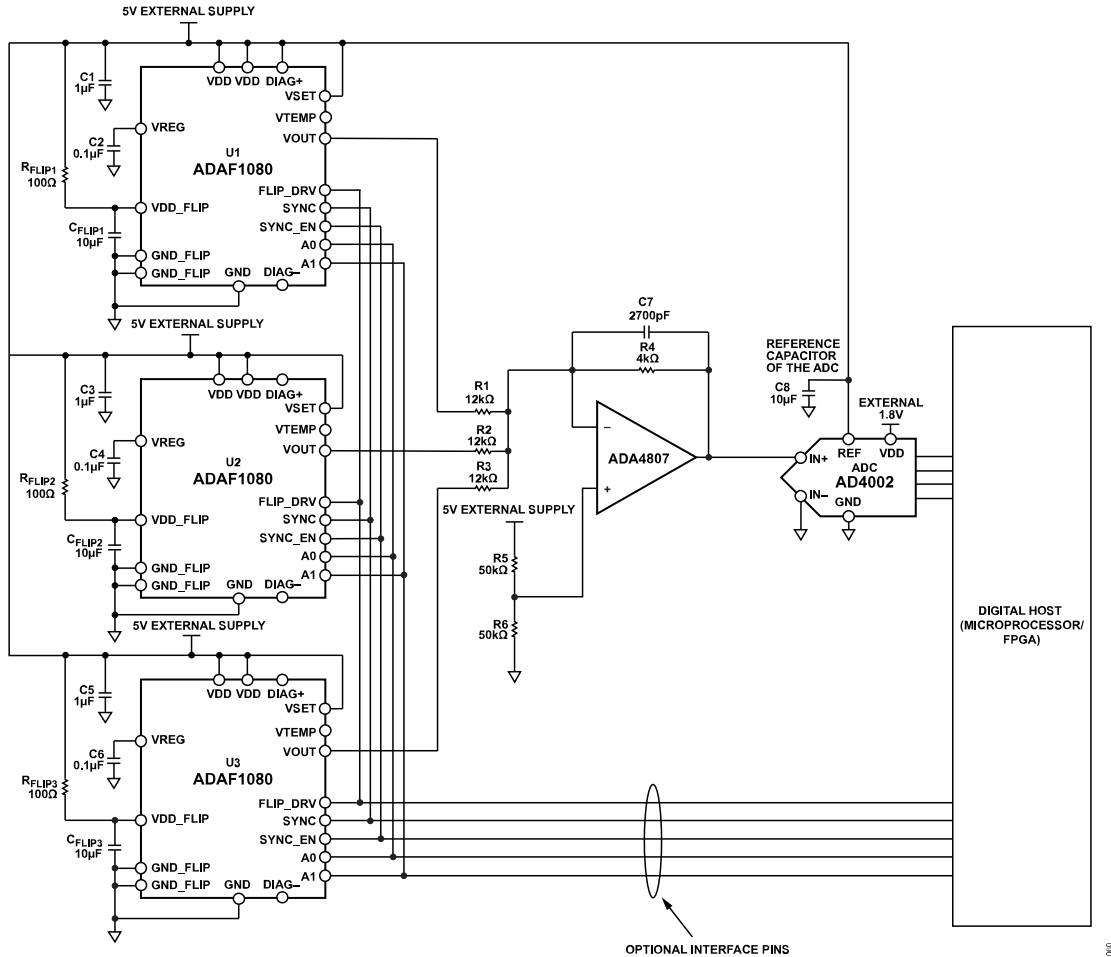


Figure 59. Design Example with the EVAL-ADAF1080-3EBZ Evaluation Board

Table 19. Component Values for the Design Example with the EVAL-ADAF1080-3EBZ

Component	Description	Suggested Part Number
U1, U2, U3	Integrated ±8 mT AMR magnetic field sensor and signal conditioner	ADAF1080BCPZ
AD4002	18-bit, 2 MSPS, precision, pseudo differential, SAR ADC	AD4002BRMZ
ADA4807	Low noise 180 MHz, rail-to-rail Input/output amplifiers	ADA4807-1AKSZ
C1, C3, C5	1 µF ceramic capacitors, 16 V, 0603	CGA3E1X7R1C105K080AC
C2, C4, C6	0.1 µF ceramic capacitors	08055C104JAT2A
C7	2700 pF ceramic capacitor	C2012C0G1H272J060AA
C_FLIP1, C_FLIP2, C_FLIP3, C8	10 µF ceramic capacitors, 25 V, 0805	GRM21BR61E106KA73L
R_FLIP1, R_FLIP2, R_FLIP3	100 Ω resistors, 1/10 W, 1%, 0603, SMD	WR06X1000FTL
R1, R2, R3	12 kΩ resistors, 1/10 W, 0.1%, 0603, SMD	RT0603BRE0712KL
R4	4 kΩ resistor, 1/10 W, 0.1%, 0603, SMD	RT0603BRD07100KL
R5, R6	50 kΩ resistors, 1/10 W, 0.1%, 0603, SMD	RT0603BRD0750KL

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Any current carrying traces near the ADAF1080 produce a magnetic field. To minimize the impact of these stray fields of measurement, Analog Devices, Inc., recommends the following:

1. Keep any current carrying traces as far from the ADAF1080 as possible.
2. Route any current carrying traces to the ADAF1080 on the same layer as the ADAF1080. To a first order, the resultant magnetic field is perpendicular to the ADAF1080 (through the top of the package), as shown in Figure 60.

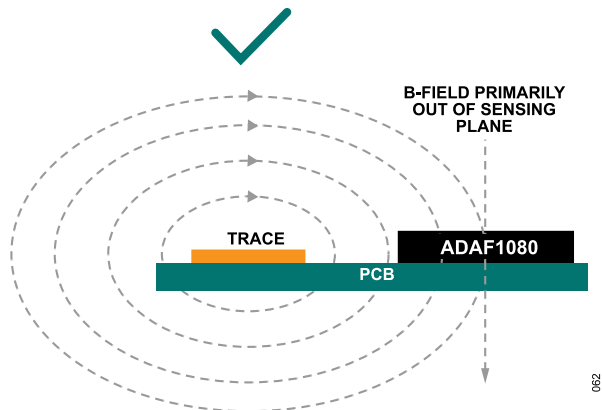


Figure 60. Current Carrying Traces on PCB Routed on the Same Layer as the ADAF1080

3. Keep any current carrying vias as far from the ADAF1080 as possible. The field generated from current carrying vias can result in a magnetic field vector in the same plane as the ADAF1080, which can be detected by the AMR sensor and impact the accuracy of the sense field measurement, as shown in Figure 61.

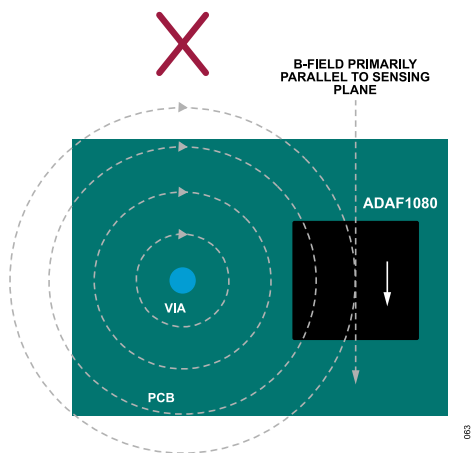
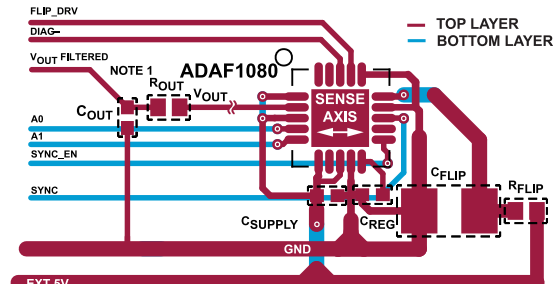


Figure 61. Current Carrying Vias Placed as Far Away from the ADAF1080 as Possible

4. Avoid magnetic materials near the ADAF1080 because these materials distort the magnetic fields near the device and can introduce a magnetic offset. Use nylon or plastic materials for mounting structures, screws, and supports.

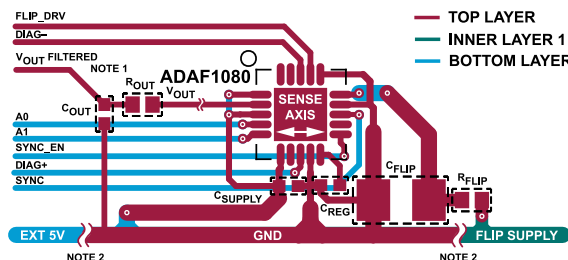
RECOMMENDED PCB LAYOUT

Figure 62 and Figure 63 show the recommended layouts for a single sensor for either a 2-layer PCB implementation or for a 3-layer or more PCB implementation.



- NOTES
1. PLACE R_{OUT} AND C_{OUT} CLOSE TO THE ADC.
 2. EXTERNAL 5V, FLIP SUPPLY, AND GND TRACE ARE RUNNING PARALLEL. EXTERNAL 5V IS ON THE BOTTOM LAYER. FLIP SUPPLY IS ON THE INNER LAYER 1. GND IS ON THE TOP LAYER.

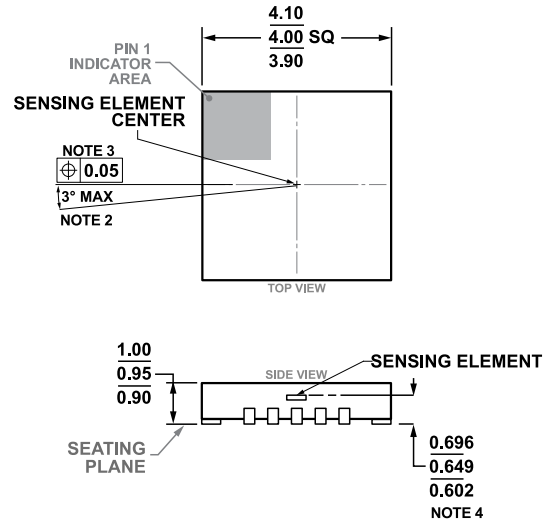
Figure 62. Recommended Layout for 2-Layer PCB



- NOTES
1. PLACE R_{OUT} AND C_{OUT} CLOSE TO THE ADC.
 2. EXTERNAL 5V, FLIP SUPPLY, AND GND TRACE ARE RUNNING PARALLEL. EXTERNAL 5V IS ON THE BOTTOM LAYER. FLIP SUPPLY IS ON THE INNER LAYER 1. GND IS ON THE TOP LAYER.

Figure 63. Recommended Layout for a 3-Layer PCB

MECHANICAL TOLERANCES



- NOTES**
1. DIMENSIONS ARE IN MILLIMETERS.
 2. MAXIMUM SENSOR ROTATION.
 3. THE CENTER OF THE SENSING ELEMENT IS ALIGNED WITH THE CENTER OF THE PACKAGE.
 4. THIS DIMENSION AND TRUE POSITION SPECIFY THE HEIGHT OF THE SENSING ELEMENT WITH RESPECT TO THE SEATING PLAN OF THE PACKAGE

Figure 64. Mechanical Drawing of the ADAF1080 Including Placement Tolerances

061