Data Sheet

ADAQ23878

18-Bit, 15 MSPS, µModule Data Acquisition Solution

FEATURES

- Integrated fully differential ADC driver with signal scaling
  - Wide input common-mode voltage range
  - High common-mode rejection
- Single-ended to differential conversion
- Pin selectable input range with overrange
  - Input ranges with 4.096 V REFBUF: ±10 V, ±5 V, ±4.096 V, ±2.5 V, and ±1.5 V
- Gain/attenuation options: 0.37, 0.73, 0.87, 1.38, and 2.25
  - Critical passive components
  - 0.005% precision matched resistor array for FDA
- 9 mm × 9 mm, 0.8 mm pitch, 100-ball CSP_BGA package
  - 2.5× footprint reduction vs. discrete solution
- Low power, dynamic power scaling, power-down mode
  - 143 mW typical at 15 MSPS
- Throughput: 15 MSPS, no pipeline delay
- INL error: ±3.1 ppm typical, ±6.2 ppm maximum
  - (Gain = 0.73, gain = 0.87, gain = 1.38, gain = 2.25)
- SINAD: 90.4 dB typical at 20 kHz (gain = 0.73)
- THD: −117 dB at 1 kHz, −110 dB at 100 kHz (gain = 0.73)
- Gain error: ±0.005%FS typical
- Gain error drift: ±0.13 ppm/°C typical
- On-board reference buffer with VCMO generation
- Serial LVDS interface
- Wide operating temperature range: −40°C to +85°C

APPLICATIONS

- Automatic test equipment
- Data acquisition
- Hardware in the Loop (HiL)
- Power analyzers
- Nondestructive test (acoustic emissions)
- Mass spectrometry
- Traveling wave fault location
- Medical imaging and instruments

GENERAL DESCRIPTION

The ADAQ23878 is a precision, high speed, µModule® data acquisition solution that reduces the development cycle of precision measurement systems by transferring the design burden of component selection, optimization, and layout from the designer to the device.

Using system-in-package (SIP) technology, the ADAQ23878 reduces end system component count by combining multiple common signal processing and conditioning blocks in a single device, including a low noise, fully differential ADC driver amplifier (FDA), a stable reference buffer, and a high speed, 18-bit, 15 MSPS successive approximation register (SAR) ADC.

The ADAQ23878 also incorporates the critical passive components with superior matching and drift characteristics using Analog Devices, Inc., iPassive® technology to minimize temperature dependent error sources and to offer optimized performance. The fast settling of the ADC driver stage and no latency of the SAR ADC provide a unique solution for high channel count, multiplexed signal chain architectures and control loop applications.

The small footprint, 9 mm × 9 mm, 0.8 mm pitch, 100-ball CSP_BGA package enables smaller form factor instruments without sacrificing performance. The system integration solves many design challenges while the device still provides the flexibility of a configurable ADC driver feedback loop to allow gain or attenuation adjustments, as well as fully differential or single-ended to differential input. A single 5 V supply operation is possible while achieving optimum performance from the device.

The ADAQ23878 features a serial low voltage differential signaling (LVDS) digital interface with one-lane or two-lane output modes, allowing the user to optimize the interface data rate for each application. The specified operation of the ADAQ23878 is from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

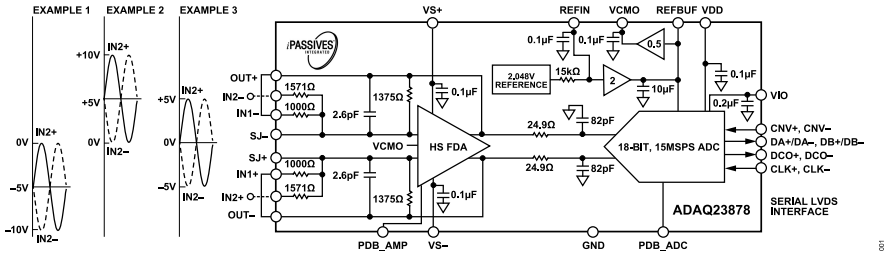

Figure 1. ADAQ23878 Configured for Gain = 0.37, ±10 V Differential Input Range

TABLE OF CONTENTS

REVISION HISTORY

2/2023—Rev. 0 to Rev. A

Changes to Transition Noise Parameter; Dynamic Range Parameter; Total RMS Noise, Referred to Output (RTO) Parameter; and Input Voltage Noise Parameter, Table 1 ... 3
Change to Figure 82 ... 30
Changes to Figure 83 ... 30

12/2021—Revision 0: Initial Version

SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V ± 5%, VS− = 0 V (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, sampling frequency (f_S) = 15 MSPS, gain = 0.37, 0.73, 0.87, 1.38, and 2.25, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. For all gain values, limit the differential input range, V_{IN}, to 95% to allow enough footroom for the ADC driver with VS− = 0 V to achieve the specified performance.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
RESOLUTION		18			Bits
ANALOG INPUT IMPEDANCE, Z_{IN}	IN1+, IN1−, IN2+, IN2−, SJ+, and SJ− single-ended to differential configuration				
	Gain = 0.37 (resistor feedback (R_F) = 1375 Ω || 1000 Ω), V_{IN} = 20 V p-p		1816		Ω
	Gain = 0.73 (R_F = 1571 Ω[2] || 1375 Ω), V_{IN} = 10 V p-p		1268		Ω
	Gain = 0.87, V_{IN} = 8.1912 V p-p		2050		Ω
	Gain = 1.38, V_{IN} = 5 V p-p		1407		Ω
	Gain = 2.25 (R_F = 1571 Ω || 1000 Ω), V_{IN} = 3 V p-p		935		Ω
	Fully differential configuration				
	Gain = 0.37 (R_F = 1375 Ω || 1000 Ω), V_{IN} = 20 V p-p		3143		Ω
	Gain = 0.73 (R_F = 1571 Ω || 1375 Ω), V_{IN} = 10 V p-p		2000		Ω
	Gain = 0.87, V_{IN} = 8.1912 V p-p		3143		Ω
	Gain = 1.38, V_{IN} = 5 V p-p		2000		Ω
	Gain = 2.25 (R_F = 1571 Ω || 1000 Ω), V_{IN} = 3 V p-p		1222		Ω
Input Capacitance	IN1+, IN1−		3.3		pF
Differential Input Voltage Range, V_{IN}[3]	Gain = 0.37, V_{IN} = 22.141 V p-p	−11		+11	V
	Gain = 0.73, V_{IN} = 11.222 V p-p	−5.6		+5.6	V
	Gain = 0.87, V_{IN} = 9.416 V p-p	−4.7		+4.7	V
	Gain = 1.38, V_{IN} = 5.936 V p-p	−2.9		+2.9	V
	Gain = 2.25, V_{IN} = 3.64 V p-p	−1.8		+1.8	V
THROUGHPUT					
Complete Cycle		66.6			ns
Conversion Time		54	58	63	ns
Acquisition Phase[4]			Time between conversions (t_{CYC}) − 39		ns
Throughput Rate[5]		0.02		15	MSPS
Transient Response[6]	Full-scale step		52		ns
DC ACCURACY	Single-ended and differential configuration				
No Missing Codes		18			Bits
Integral Nonlinearity (INL) Error					
	Gain = 0.37 single-ended	−7.5	−7, +1.5	+2.5	LSB
		−23.4	−21.8, +4.6	+7.8	ppm
	Gain = 0.37 differential	−2.5	±1.5	+2.5	LSB
		−7.8	±4.6	+7.8	ppm
	Gain = 0.73, gain = 0.87, gain = 1.38, and gain = 2.25	−2.0	±1.0	+2.0	LSB
		−6.2	±3.1	+6.2	ppm
Differential Nonlinearity (DNL) Error	All gains	−0.9	±0.5	+0.9	LSB
Transition Noise	Gain = 0.37 and gain = 0.73		2.46		LSB_{RMS}
	Gain = 0.87, gain = 1.38, and gain = 2.25		2.77		LSB_{RMS}
Gain Error	All gains	−0.025	±0.005	+0.025	%FS
Gain Error Drift		−0.36	±0.13	+0.36	ppm/°C
Offset Error		−2.1		+2.1	mV

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Offset Error Drift		−12	±2.2	+12	ppm/°C
Common-Mode Rejection Ratio (CMRR), Input Referred	$\Delta V_{ICM}/\Delta V_{OSDIFF}$				
	All gains		100		dB
Power Supply Rejection Ratio (PSRR)					
Positive	VDD = 4.75 V to 5.25 V				
	All gains		107		dB
Negative	VS+ = +5 V, VS− = −0.75 V to −1.25 V				
	All gains		105		dB
1/f Noise[7]	Bandwidth = 0.1 Hz to 10 Hz		9		µV p-p
Input Current Noise	f = 100 kHz		1		pA/√Hz
AC ACCURACY[8]	Single-ended and differential configuration				
Dynamic Range	Input frequency (f_{IN}) = 1 kHz, −60 dB input				
	Gain = 0.37 and gain = 0.73	89.5	91.5		dB
	Gain = 0.87, gain = 1.38, and gain = 2.25		90.5		dB
Total RMS Noise, Referred to Output (RTO)	Gain = 0.37 and gain = 0.73		77		μV_{RMS}
	Gain = 0.87, gain = 1.38, and gain = 2.25		86.47		μV_{RMS}
Input Voltage Noise	Gain = 0.37 and gain = 0.73		9.49		nV/√Hz
	Gain = 0.87, gain = 1.38, and gain = 2.25		10.64		nV/√Hz
Signal-to-Noise Ratio (SNR)	f_{IN} = 1 kHz, −1 dBFS	85.5			dB
	Gain = 0.37 and gain = 0.73		91		dB
	Gain = 0.87, gain = 1.38, and gain = 2.25		90		dB
	f_{IN} = 100 kHz				
	Gain = 0.37 and gain = 0.73		90.5		dB
	Gain = 0.87, gain = 1.38, and gain = 2.25		89.5		dB
	f_{IN} = 1MHz				
	Gain = 0.73		83.2		dB
	Gain = 0.87, gain = 1.38, and gain = 2.25		80		dB
Signal-to-Noise-and-Distortion (SINAD)	f_{IN} = 1 kHz	85.4			dB
	Gain = 0.37 and gain = 0.87		90.4		dB
	Gain = 1.38 and gain = 2.25		88.7		dB
	f_{IN} = 100 kHz				
	Gain = 0.37 and gain = 0.73		89.3		dB
	Gain = 0.87 and gain = 1.38		88.4		dB
	Gain = 2.25		87.7		dB
	f_{IN} = 1MHz				
	Gain = 0.73		67.7		dB
	Gain = 0.87		65.6		dB
	Gain = 1.38		63.8		dB
	Gain = 2.25		61.7		dB
Total Harmonic Distortion (THD)	f_{IN} = 1 kHz				
	Gain = 0.37		−109.9		dB
	Gain = 0.73, gain = 0.87, and gain = 1.38		−117		dB
	Gain = 2.25		−114.3		dB
	f_{IN} = 100 kHz				
	Gain = 0.37		−107.8		dB
	Gain = 0.73 and gain = 2.25		−110		dB
	Gain = 0.87 and gain = 1.38		−111.4		dB
	f_{IN} = 1MHz				

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
	Gain = 0.73		−67.9		dB
	Gain = 0.87		−65.8		dB
	Gain = 1.38		−63.9		dB
	Gain = 2.25		−61.8		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1 kHz				
	Gain = 0.37 and gain = 0.87		110.1		dB
	Gain = 0.73, gain = 1.38 and gain = 2.25		117.5		dB
	f_{IN} = 100 kHz				
	Gain = 0.37 and gain = 0.87		104.1		dB
	Gain = 0.73, gain = 1.38, and gain = 2.25		105.8		dB
	f_{IN} = 1MHz				
	Gain = 0.73		68.7		dB
	Gain = 0.87		66.5		dB
	Gain = 1.38		64.6		dB
	Gain = 2.25		62.5		dB
−3 dB Input Bandwidth, RC Filter	Output voltage (V_{OUT}) differential ($V_{OUTDIFF}$) = 2 V p-p		42		MHz
Aperture Delay[9]			0		ns
Aperture Jitter[10]			0.25		ps_{RMS}
REFERENCE					
REFIN, Internal Reference Output Voltage	Output current (I_{OUT}) = 0 µA	2.028	2.048	2.068	V
Temperature Coefficient			±5	±20	ppm/°C
Output Impedance			15		kΩ
Line Regulation	VDD = 4.75 V to 5.25 V		0.3		mV/V
Input Voltage Range	REFIN overdriven	2.028	2.048	2.068	V
Reference Buffer Output Voltage, REFBUF	REFIN = 2.048 V	4.056	4.096	4.136	V
Input Voltage Range	REFBUF overdriven[10]	4.056	4.096	4.136	V
Load Current	REFBUF = 4.096 V (REFBUF overdriven)		1.75	1.95	mA
	REFBUF = 4.096 V (REFBUF overdriven)		0.5		mA
VCMO[11]					
Common-Mode Output Voltage	REFBUF = 4.096 V, I_{OUT} = 0 µA	2.028	2.048	2.028	V
Output Impedance	–1 mA < I_{OUT} < +1 mA		15		Ω
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage, V_{IL}	VIO = 2.5 V			0.6	V
Input High Voltage, V_{IH}	VIO = 2.5 V	1.7			V
Digital Input Current	V_{IN} = 0 V to 2.5 V	−10		+10	µA
Input Pin Capacitance			3		pF
CNV+/CNV– and CLK+/CLK– (LVDS Clock Input)					
Differential Input Voltage, V_{ID}		175	350	650	mV
Common-Mode Input Voltage, V_{ICM}		0.8	1.25	1.7	V
DCO+/DCO–, DA+/DA–, DB+/DB– (LVDS Outputs)					
Differential Output Voltage, V_{OD}	100 Ω differential load	247	350	454	mV
Common-Mode Output Voltage, V_{OS}	100 Ω differential load	1.125	1.25	1.375	V
POWER-DOWN MODE					
ADC Driver (PDB_AMP)/ADC (PDB_ADC)					
Low	Power-down mode		<1		V
High	Enabled, normal operation		>1.7		V

SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
POWER REQUIREMENTS					
VDD		4.75	5	5.25	V
VS+		3	5	VS− + 10	V
VS−		VS+ − 10	0	+0.1	V
VIO		2.375	2.5	2.625	V
Total Standby Current[12, 13]	Static, all devices enabled		45	52	mA
	Static, all devices disabled		0.1	0.4	µA
ADAQ23878 Current Draw					
VDD			4.6	5.5	mA
VS+/VS−			4	5.5	mA
VIO			40	42	mA
ADAQ23878 Power Dissipation	VDD = 5 V, VS+ = 5 V, VS− = 0 V				
VDD			19	26.25	mW
VS+/VS−	Gain = 0.37		24	28.875	mW
VIO	One-lane mode[14]		100	110.25	mW
Total			143	165.375	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] The LSB unit means least significant bit. The weight of the LSB, referred to input, changes depending on the input voltage range.

[2] For accurate resistor iPassive value IN2±, gain resistor (R_G) = 1.571.4286

[3] The differential input ranges, V_{IN}, must be within the allowed input common-mode range as per Figure 61 to Figure 65. V_{IN} is dependent on the VS+/VS− supply rails used.

[4] The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADAQ23878 running at a throughput rate of 15 MSPS.

[5] f_S = 15 MHz, and the REFBUF current (I_{REFBUF}) varies linearly with the throughput rate.

[6] Transient response is the time required for the ADAQ23878 to acquire a full-scale input step to within ±1 LSB accuracy. Guaranteed by design, not subject to test.

[7] See the 1/f noise plot in Figure 66

[8] All ac specifications expressed in decibels are referenced to the full-scale input range (FSR) and are tested with an input signal at 1 dB below full scale, unless otherwise specified.

[9] Guaranteed by design, not subject to test.

[10] When REFBUF is overdriven, turn off the internal reference buffer by setting REFIN = 0 V. Refer to the Voltage Reference Input section for more information.

[11] The VCMO voltage can be used for other circuitry. However, drive the voltage with a buffer to ensure the VCMO voltage remains stable as per the specified range.

[12] With all digital inputs forced to VIO or GND, as required.

[13] During the acquisition phase.

[14] In two-lane mode, the VIO power dissipation is about 10 mW higher than one-lane mode.

SPECIFICATIONS

TIMING SPECIFICATIONS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V ± 5%, VS− = 0 V (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, sampling frequency (f_S) = 15 MSPS, gain = 0.37, 0.73, 0.87, 1.38, and 2.25, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Digital Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_{SMPL}	0.02		15	MSPS
Conversion Time—CNV± Rising Edge to Data Available	t_{CONV}	54	58	63	ns
Acquisition Phase	t_{ACQ}		t_{CYC} − 39		ns
Time Between Conversions	t_{CYC}	66.6		50,000	ns
CNV± High Time	t_{CNVH}	5			ns
CNV± Low Time	t_{CNVL}	8			ns
CNV± Rising Edge to First CLK± Rising Edge from the Same Conversion	$t_{FIRSTCLK}$	65			ns
CNV± Rising Edge to Last CLK± Falling Edge from the Previous Conversion	$t_{LASTCLK}$			49	ns
CLK± to DCO± Delay	t_{CLKDCO}	0.7	1.3	2.3	ns
CLK± Low Time	t_{CLKL}	1.25			ns
CLK± High Time	t_{CLKH}	1.25			ns
CLK± to DA±/DB± Delay	t_{CLKD}	0.7	1.3	2.3	ns
DCO± to DA±/DB± Skew	t_{SKEW}	−200	0	+200	ps
Sampling Delay Time	t_{AP}		0		ns
Sampling Delay Jitter	t_{JITTER}		0.25		ps_{RMS}

Timing Diagrams

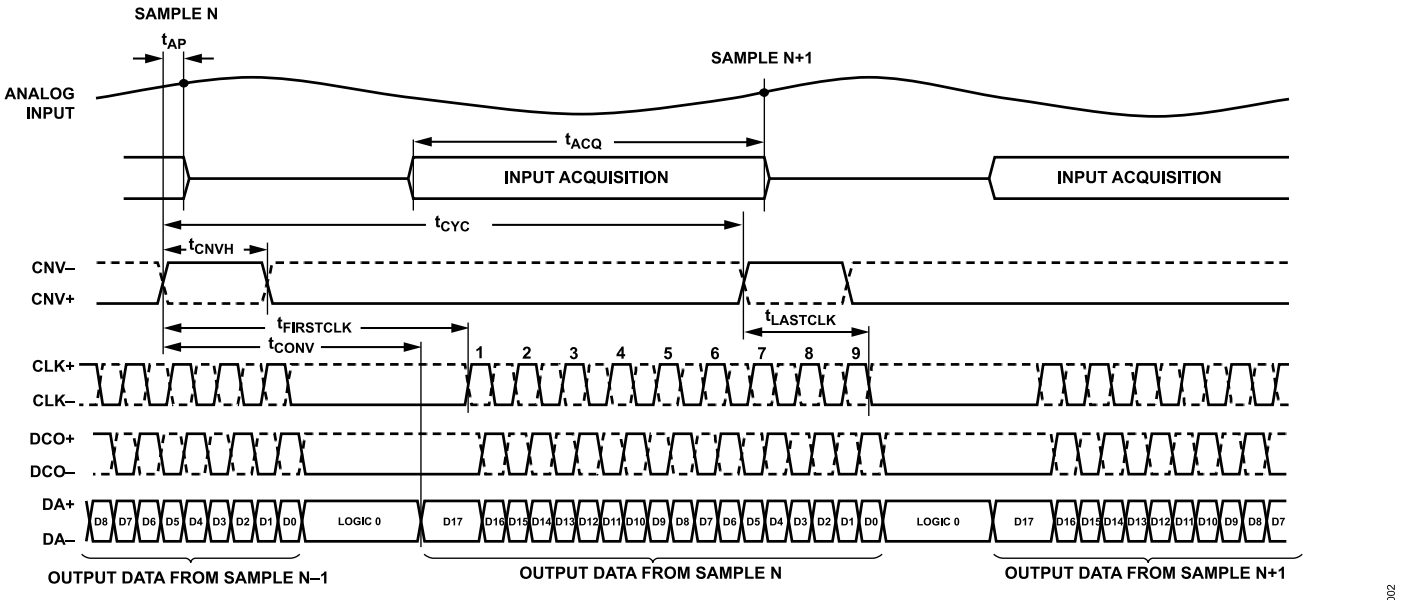

Figure 2. One-Lane Output Mode Timing Diagram

SPECIFICATIONS

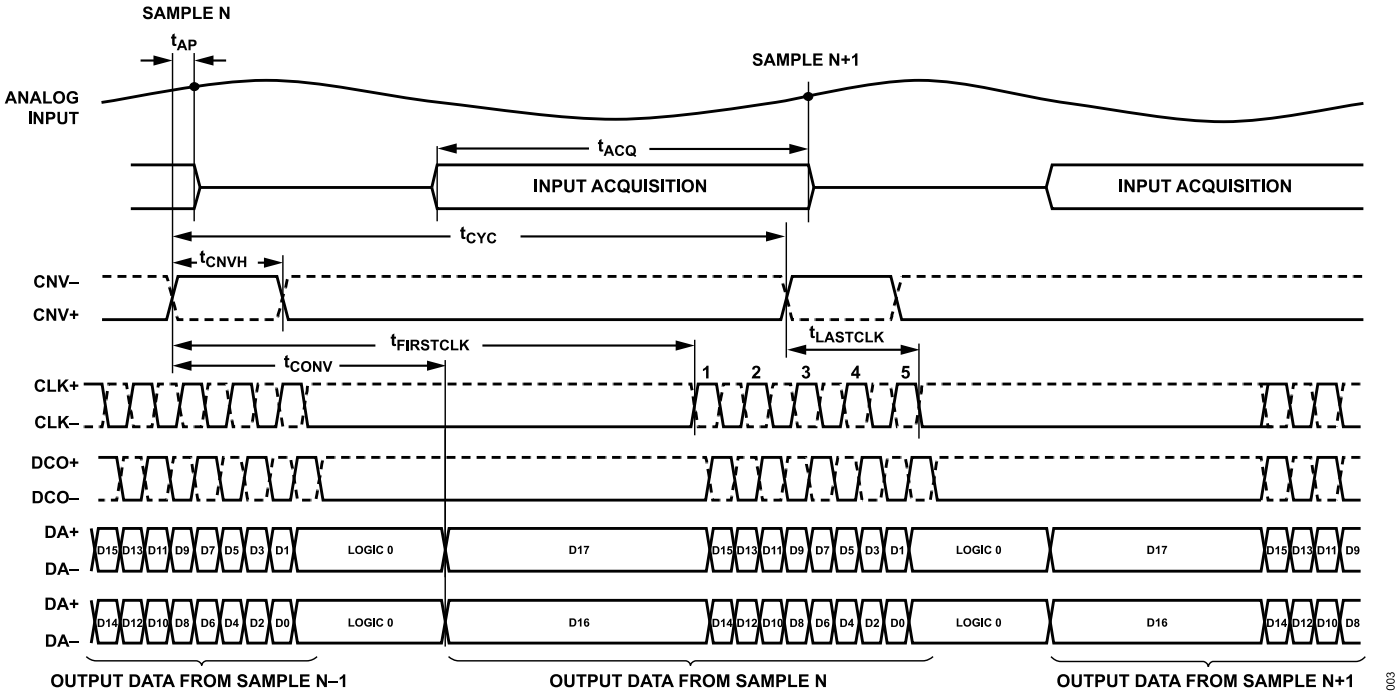

Figure 3. Two-Lane Output Mode Timing Diagram

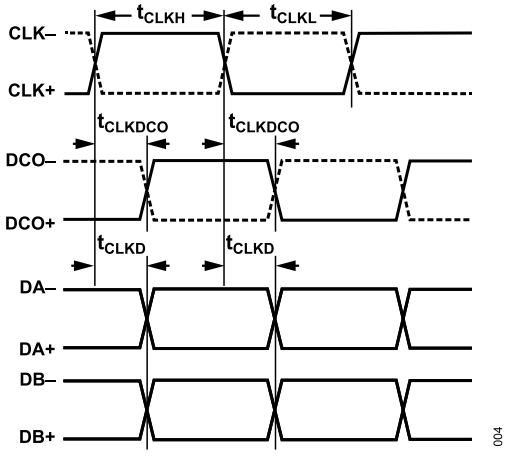

Figure 4. Data Output Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Inputs	
IN1+, IN1− to GND	−12 V to +12 V or 8 mA
IN2+, IN2− to GND	−12 V to +12 V or 12 mA
Supply Voltage	
VDD to GND	6 V
VIO to GND	2.8 V
VS+ to VS−	11 V
VS+ to GND	−0.3 V to +11 V
VS− to GND	−11 V to +0.3 V
REFBUF to GND	−0.3 V to VDD + 0.3 V
REFIN to GND	−0.3 V to +2.8 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow as per JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	Ψ_{JT}	Ψ_{JB}	$\theta_{JC\ BOTTOM}$	$\theta_{JC\ TOP}$	θ_{JB}	Unit
BC-100-7	48.43	4.64	27.89	9.9	35.15	33.24	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the $\theta_{JC\ TOP}$ which uses 1S0P JEDEC PCB.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for the handling of ESD sensitive devices in an ESD protected area only.

The human body model (HBM) is per ANSI/ESDA/JEDDEC JS-001.

The field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ23878

Table 5. ADAQ23878, 100-Ball CSP_BGA

ESD Model	Withstand Threshold (V)
HBM	2250
FICDM	1000

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10
A	GND	IN1−	IN1+	IN2−	IN2+	SJ−	GND	VIO	GND	CNV+
B	PDB_AMP	IN1−	IN1+	IN2−	IN2+	SJ+	GND	TWOLANES	GND	CNV−
C	OUT+	VS+	OUT−	VS+	VS−	GND	GND	GND	GND	GND
D	OUT+	GND	OUT−	GND	GND	VCMO	GND	GND	GND	CLK+
E	GND	GND	GND	VS+	GND	GND	GND	GND	GND	CLK−
F	NC	NC	GND	GND	GND	GND	GND	GND	GND	GND
G	GND	GND	GND	GND	GND	GND	GND	GND	GND	DCO+
H	VS+	GND	GND	GND	GND	GND	GND	GND	GND	DCO−
J	VS−	GND	REFBUF	REFBUF	GND	GND	GND	GND	GND	DA+
K	GND	GND	REFIN	GND	PDB_ADC	VDD	TESTPAT	DB−	DB+	DA−

005

Figure 5. 100-Ball CSP_BGA Pin Configuration, Top View

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1, A7, A9, B7, B9, C6, C7, C8, C9, C10, D2, D4, D5, D7, D8, D9, E1, E2, E3, E5, E6, E7, E8, E9, F3, F4, F5, F6, F7, F8, F9, F10, G1, G2, G3, G4, G5, G6, G7, G8, G9, H2, H3, H4, H5, H6, H7, H8, H9, J2, J5, J6, J7, J8, J9, K1, K2, K4	GND	P	Power Supply Ground.
A2, B2	IN1−	AI	Negative Input of the FDA Connected to 1000 Ω Resistor.
A3, B3	IN1+	AI	Positive Input of the FDA Connected to 1000 Ω Resistor.
A4, B4	IN2−	AI	Negative Input of the FDA Connected to 1571 Ω Resistor.
A5, B5	IN2+	AI	Positive Input of the FDA Connected to 1571 Ω Resistor.
A6	SJ−	AI	Negative Input of the FDA.
B6	SJ+	AI	Positive Input of the FDA.
A8	VIO	P	2.5 V Analog and Output Power Supply. The range of VIO is 2.375 V to 2.625 V. Bypass this pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
A10	CNV+	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample-and-hold in hold mode and starts a conversion cycle. CNV+ can be also driven with a 2.5 V CMOS signal if CNV− is connected to GND.
B1	PDB_AMP	DI	Active Low. Connect this pin to GND to power down the fully differential ADC driver. Otherwise, connect this pin to VS+.
B8	TWOLANES	DI	Digital Input that Enables Two-Lane Output Mode. When TWOLANES is connected high (two-lane output mode), the ADAQ23878 outputs two bits at a time on DA−/DA+ and DB−/DB+. When TWOLANES is low (one-lane output mode), the ADAQ23878 outputs one bit at a time on DA−/DA+, and DB−/DB+ are disabled. Logic levels are determined by VIO.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
B10	CNV−	DI	Conversion Start LVDS Input. A rising edge on CNV+ puts the internal sample-and-hold in hold mode and starts a conversion cycle. CNV+ can be also driven with a 2.5 V CMOS signal if CNV− is connected to GND.
C1, D1	OUT+	AO	Positive Output of the FDA.
C2, C4, E4, H1	VS+	P	FDA and Reference Buffer Positive Supply. The LDO output generating the VS+ supply of µModule must be bypassed with at least 2.2 µF (0402, X5R) ceramic capacitor to GND.
C3, D3	OUT−	AO	Negative Output of the FDA
C5, J1	VS−	P	FDA Negative Supply. Bypass this pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
D6	VCMO	AO	FDA Output Common-Mode Voltage. This pin is nominally REFBUF/2.
D10	CLK+	DI	LVDS Clock Input. This pin is an externally applied clock that serially shifts out the conversion result.
E10	CLK−	DI	LVDS Clock Input. This is an externally applied clock that serially shifts out the conversion result.
F1, F2	NC		No Connect.
G10	DCO+	DO	LVDS Data Clock Output. This is an echoed version of CLK+/CLK− that can be used to latch the data outputs.
H10	DCO−	DO	LVDS Data Clock Output. This is an echoed version of CLK+/CLK− that can be used to latch the data outputs.
J3, J4	REFBUF	AO	Reference Buffer Output Voltage. As a required component of SAR architecture, a 10 µF ceramic bypass capacitor is already laid out within the ADAQ23878 between REFBUF and GND. Therefore, adding a second, smaller capacitor in parallel with the 10 µF capacitor may degrade performance and is not recommended. The common-mode voltage of VCMO and LVDS pins are derived from the REFBUF. Therefore, a voltage at REFBUF pin must be stable after the ADAQ23878 is powered on or exits power-down mode before starting a conversion cycle.
J10	DA+	DO	Serial LVDS Data Output. In one-lane output mode, DB−/DB+ are not used and their LVDS driver is disabled to reduce power consumption.
K3	REFIN	P	Internal Reference Output/Reference Buffer Input. The output voltage of the internal reference, nominally 2.048 V, is output on this pin. An external reference can be applied to REFIN if a more accurate reference is required. If the internal reference buffer is not used, connect REFIN to GND to power down the buffer and connect an external buffered reference to REFBUF.
K5	PDB_ADC	DI	Digital Input that Enables the Power-Down Mode. When PDB_ADC is low, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) is shutdown. When PDB_ADC is high, the device operates normally. Logic levels are determined by VIO.
K6	VDD	P	5 V Analog Power Supply. The range of VDD is 4.75 V to 5.25 V. Bypass the VDD pin to GND with an at least 2.2 µF (0402, X5R) ceramic capacitor.
K7	TESTPAT	DI	Digital Input that Forces the LVDS Data Outputs to be a Test Pattern. When TESTPAT is high, the digital outputs are test pattern. When TESTPAT is low, the digital outputs are the ADAQ23878 conversion result. Logic levels are determined by VIO.
K8	DB−	DO	Serial LVDS Data Output. In one-lane output mode, DA−/DA+ are not used and their LVDS driver is disabled to reduce power consumption.
K9	DB+	DO	Serial LVDS Data Outputs. In one-lane output mode, DA−/DA+ are not used and their LVDS driver is disabled to reduce power consumption.
K10	DA−	DO	Serial LVDS Data Outputs. In one-lane output mode, DB−/DB+ are not used and their LVDS driver is disabled to reduce power consumption.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, NC is no connection, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 5 V ± 5%, VS+ = 5 V ± 5%, VS− = −1 V ± 5%, VS− = 0 V (95% of V_{IN}), VIO = 2.375 V to 2.625 V, REFBUF = 4.096 V, sampling frequency (f_S) = 15 MSPS, gain = 0.37, 0.73, 0.87, 1.38, and 2.25, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

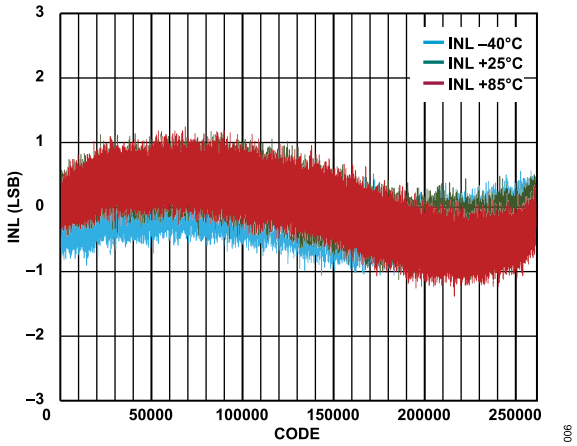

Figure 6. INL vs. Code for Various Temperatures, Gain = 2.25, Gain = 1.38, Gain = 0.87, Gain = 0.73, Differential, Single-Ended

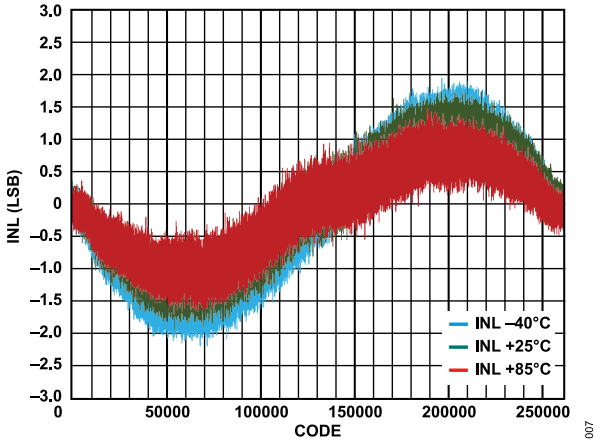

Figure 7. INL vs. Code for Various Temperatures, Gain = 0.37, Differential

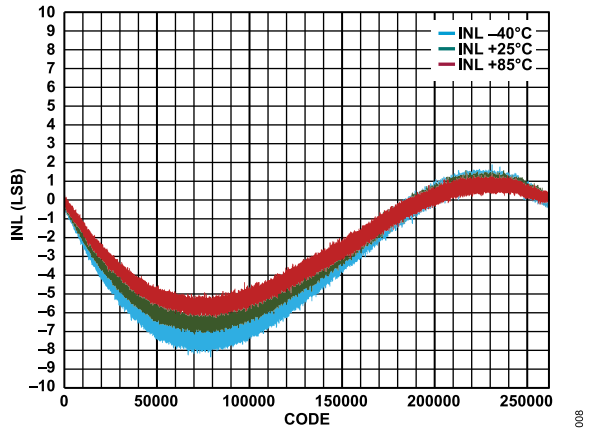

Figure 8. INL vs. Code for Various Temperatures, Gain = 0.37, Single-Ended

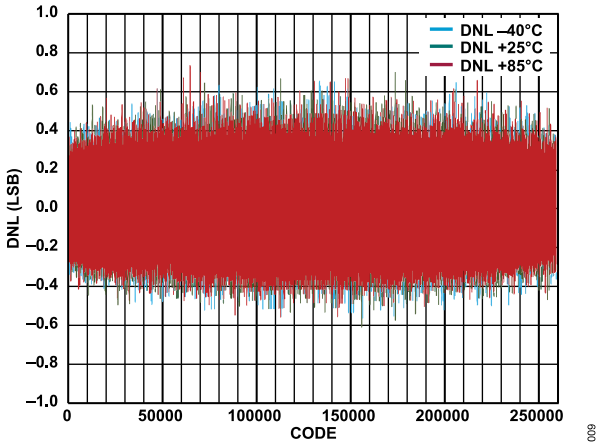

Figure 9. DNL vs. Code for Various Temperatures

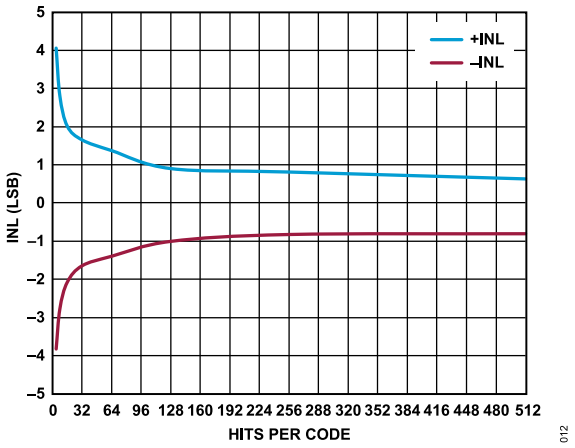

Figure 10. INL vs. Hits per Code, Gain = 2.25, Differential

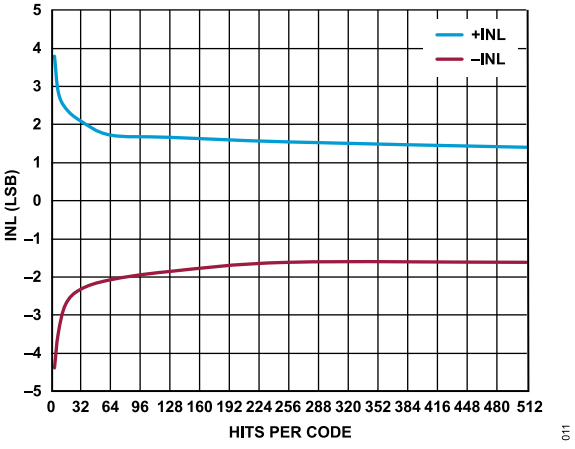

Figure 11. INL vs. Hits per Code, Gain = 0.37, Differential

TYPICAL PERFORMANCE CHARACTERISTICS

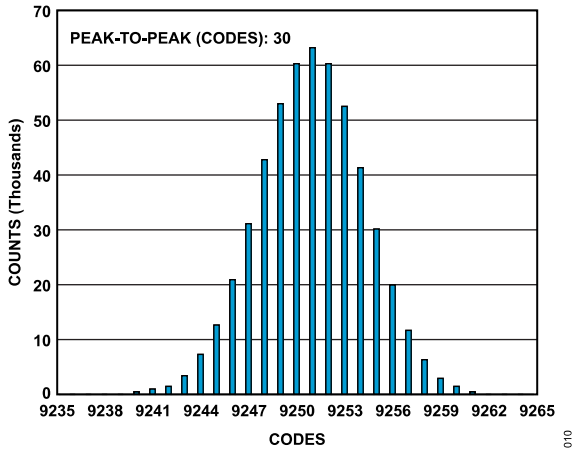

Figure 12. Histogram of a DC Input at the Code Transition

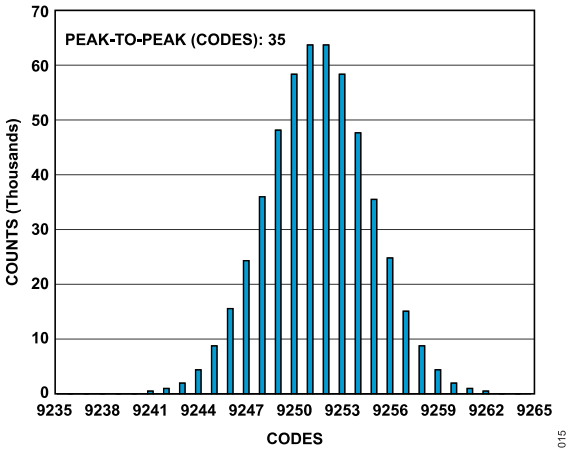

Figure 15. Histogram of a DC Input at the Code Center

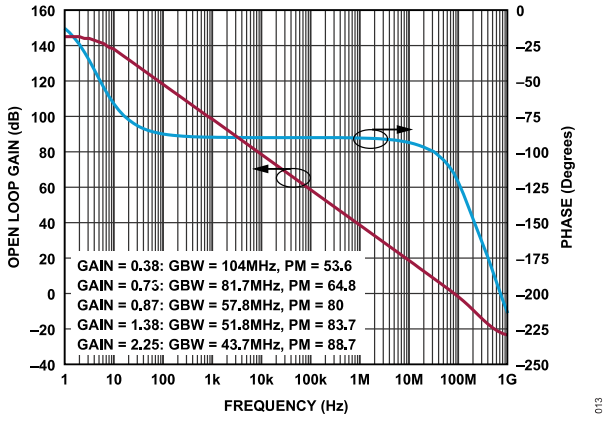

Figure 13. ADC Driver Open-Loop Gain and Phase vs. Frequency (GBW Is Gain Bandwidth, PM is Phase Margin)

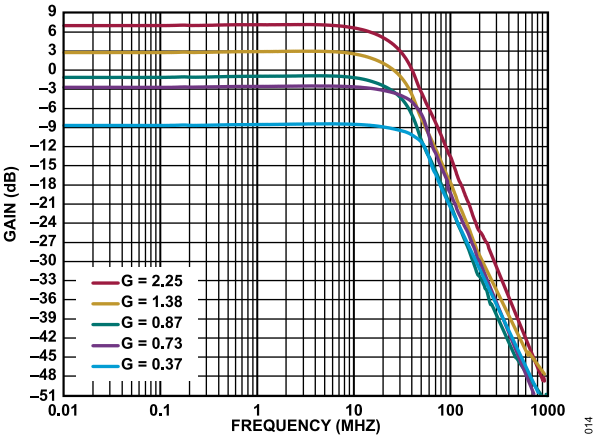

Figure 16. ADC Driver Frequency Response

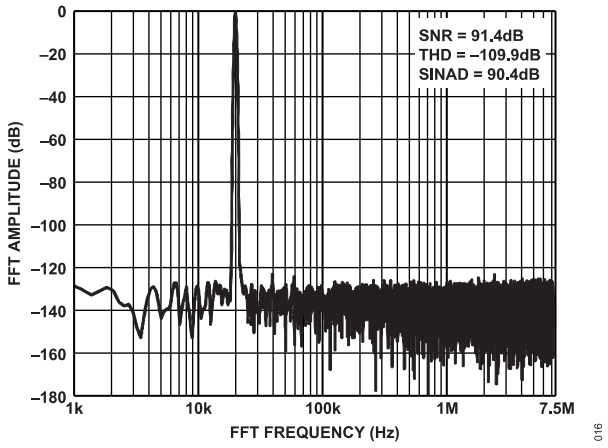

Figure 14. 20 kHz, −1 dBFS Input Tone Fast Fourier Transform (FFT), Wide View, Gain = 0.37, Differential

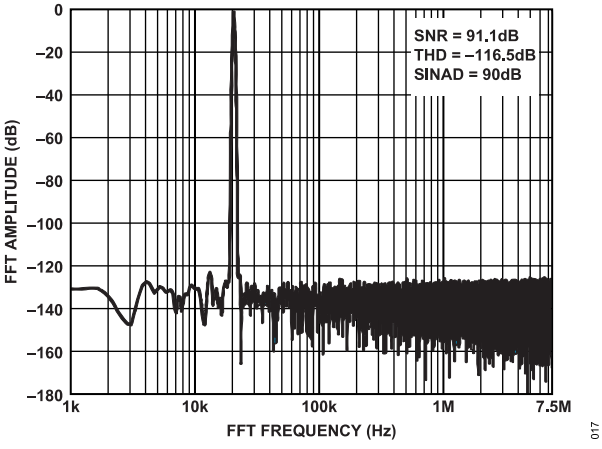

Figure 17. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.73, Differential

TYPICAL PERFORMANCE CHARACTERISTICS

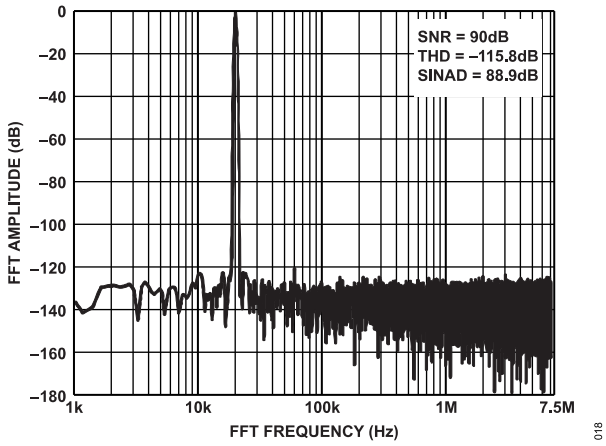

Figure 18. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.87, Differential

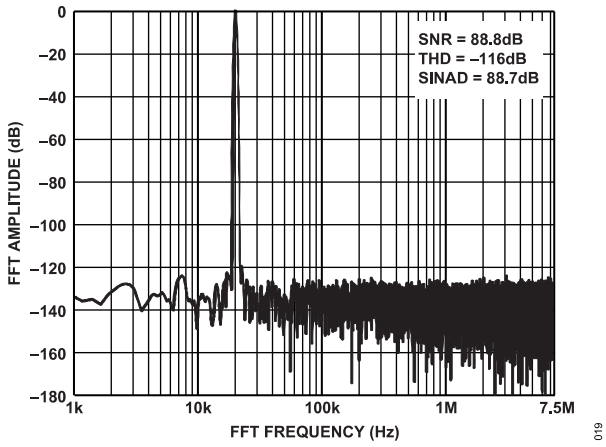

Figure 19. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 1.38, Differential

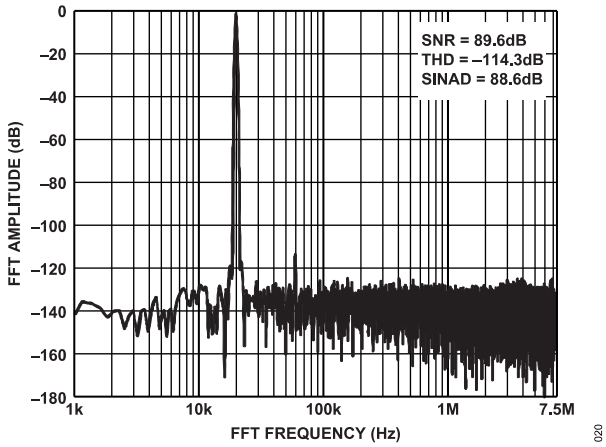

Figure 20. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 2.25, Differential

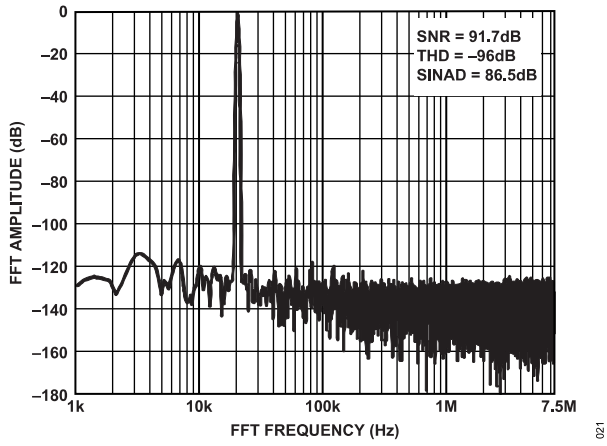

Figure 21. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.37, Single-Ended, VCMO = 0 V

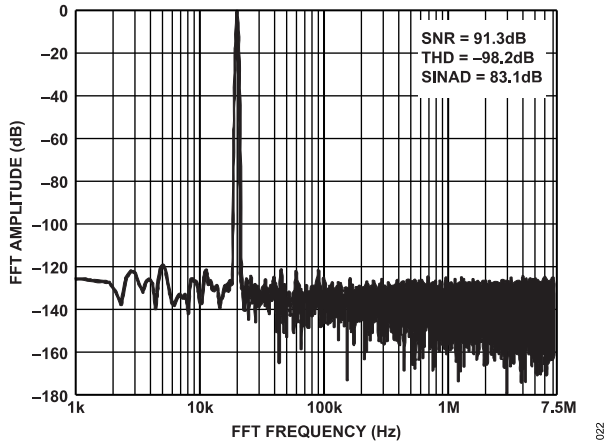

Figure 22. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.73, Single-Ended, VCMO = 0 V

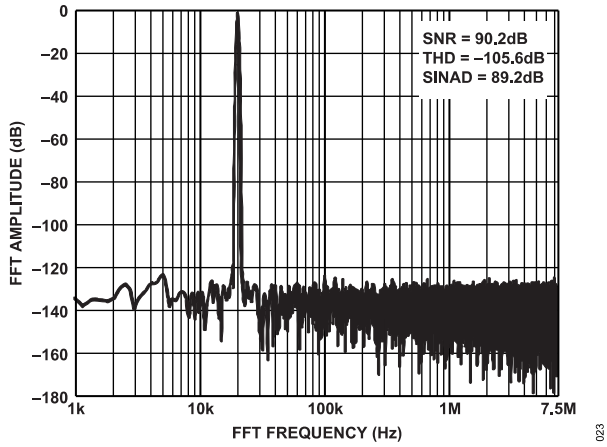

Figure 23. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.87, Single-Ended, VCMO = 0 V

TYPICAL PERFORMANCE CHARACTERISTICS

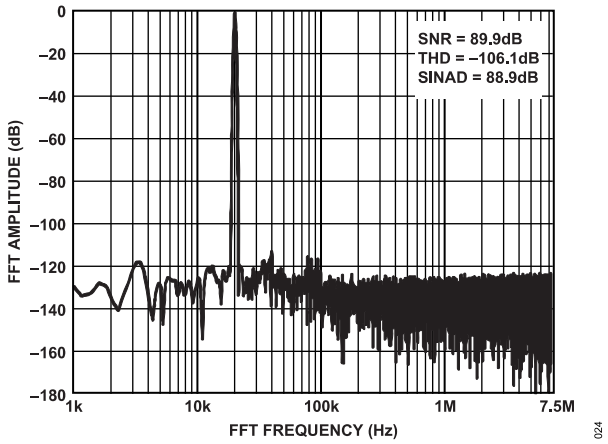

Figure 24. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 1.38, Single-Ended, VCMO = 0 V

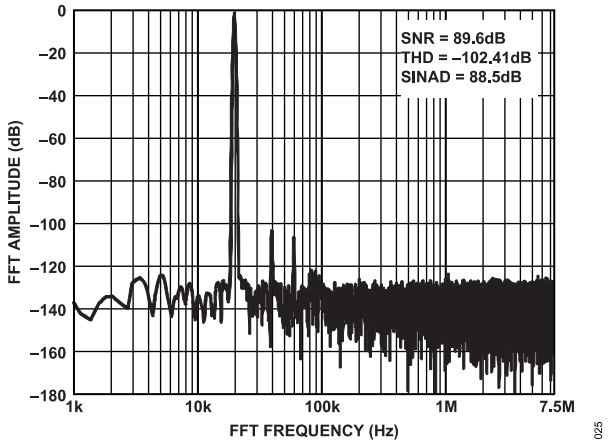

Figure 25. 20 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 2.25, Single-Ended, VCMO = 0 V

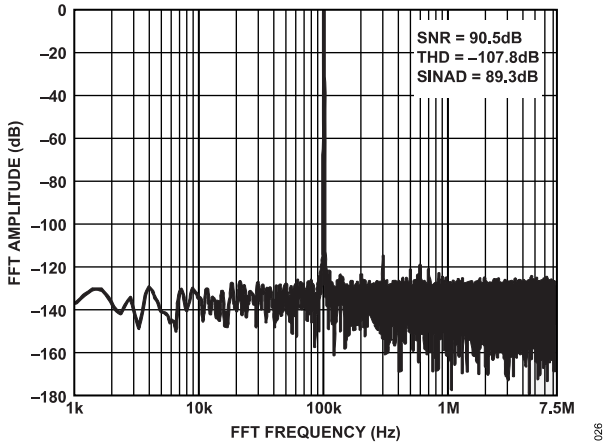

Figure 26. 100 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.37, Differential

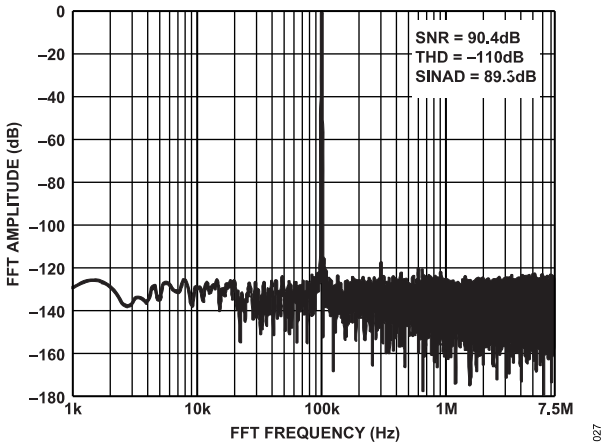

Figure 27. 100 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.73, Differential

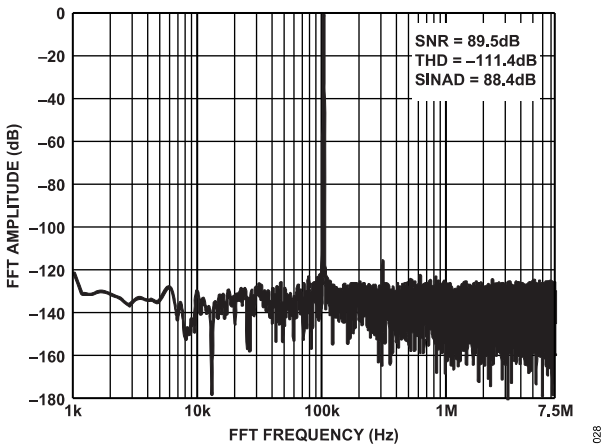

Figure 28. 100 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.87, Differential

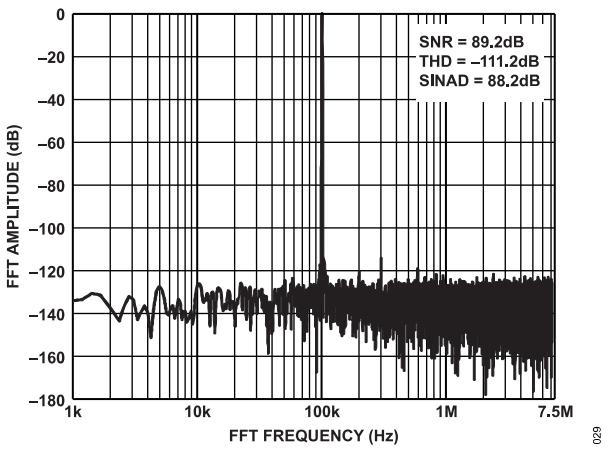

Figure 29. 100 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 1.38, Differential

TYPICAL PERFORMANCE CHARACTERISTICS

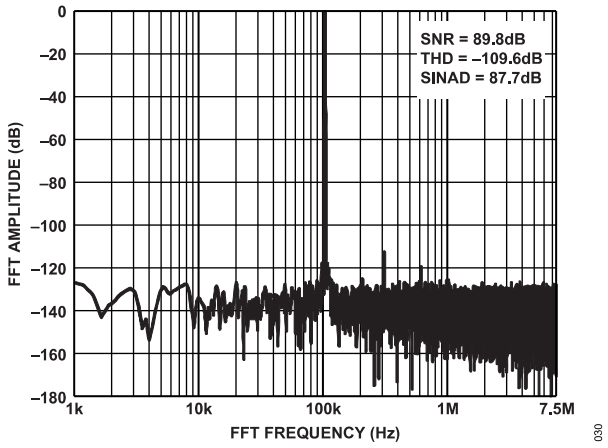

Figure 30. 100 kHz, −1 dBFS Input Tone FFT, Wide View, Gain = 2.25, Differential

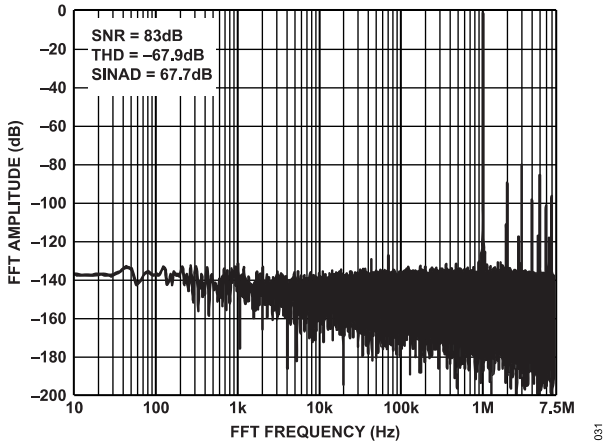

Figure 31. 1 MHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.73, Differential

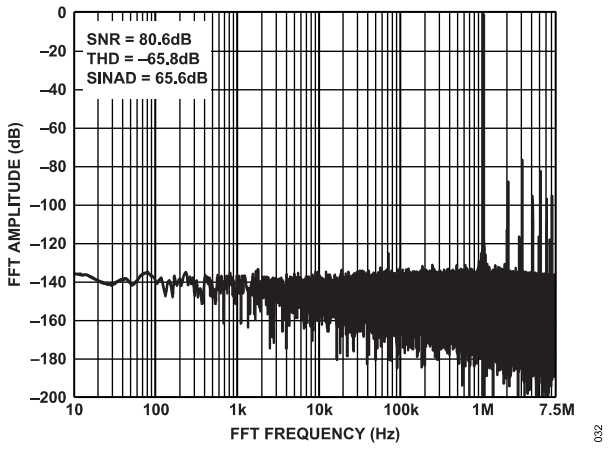

Figure 32. 1 MHz, −1 dBFS Input Tone FFT, Wide View, Gain = 0.87, Differential

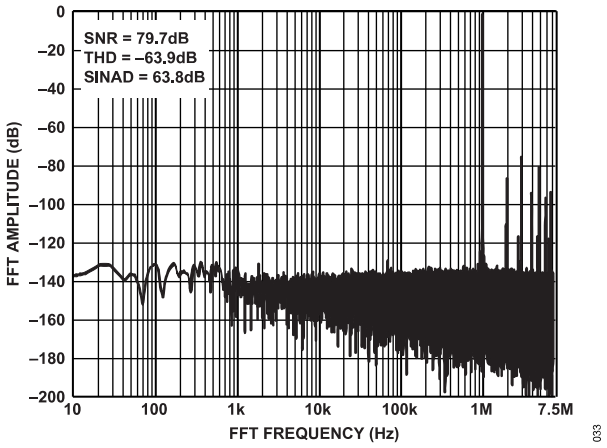

Figure 33. 1 MHz, −1 dBFS Input Tone FFT, Wide View, Gain = 1.38, Differential

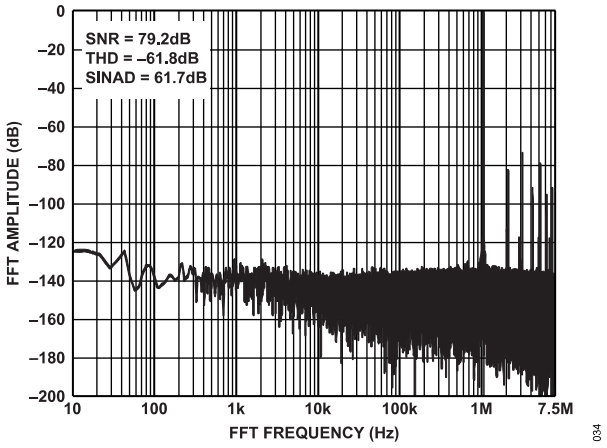

Figure 34. 1 MHz, −1 dBFS Input Tone FFT, Wide View, Gain = 2.25, Differential

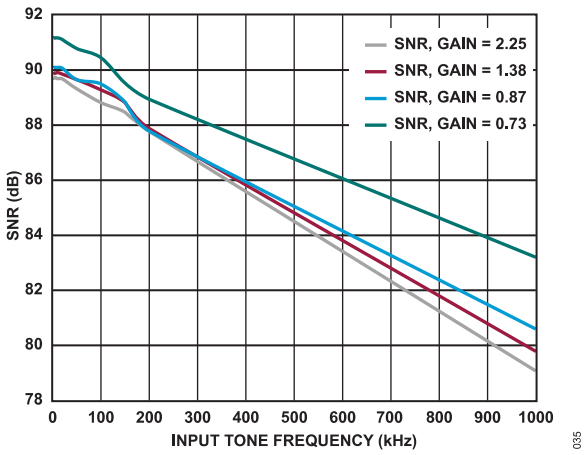

Figure 35. SNR vs. Input Tone Frequency, Gain = 0.73, Gain = 0.87, Gain = 1.38, and Gain = 2.25

TYPICAL PERFORMANCE CHARACTERISTICS

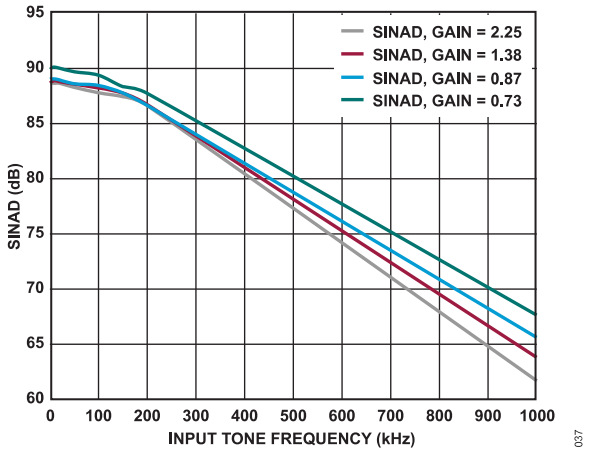

Figure 36. SINAD vs. Input Tone Frequency, Gain = 0.73, Gain = 0.87, Gain = 1.38, Gain = 2.25

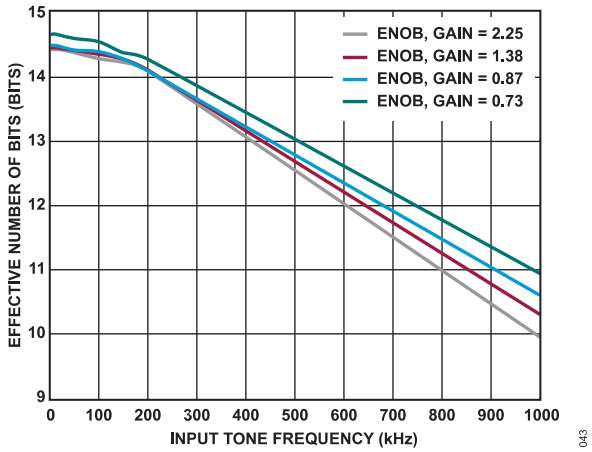

Figure 39. Effective Number of Bits vs. Input Tone Frequency, Gain = 0.73, Gain = 0.87, Gain =1.38, and Gain = 2.25

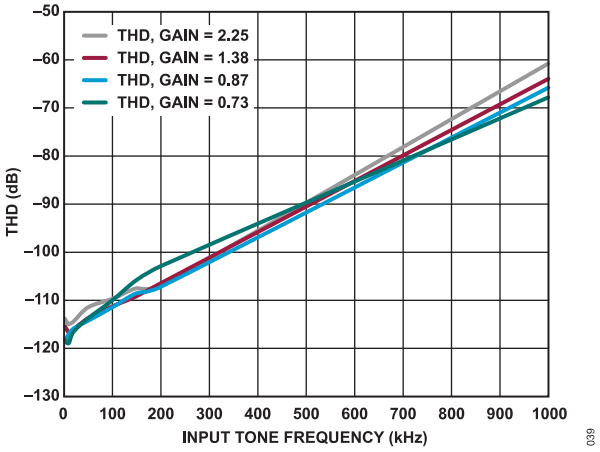

Figure 37. THD vs. Input Tone Frequency, Gain = 0.73, Gain = 0.87, Gain = 1.38, Gain = 2.25

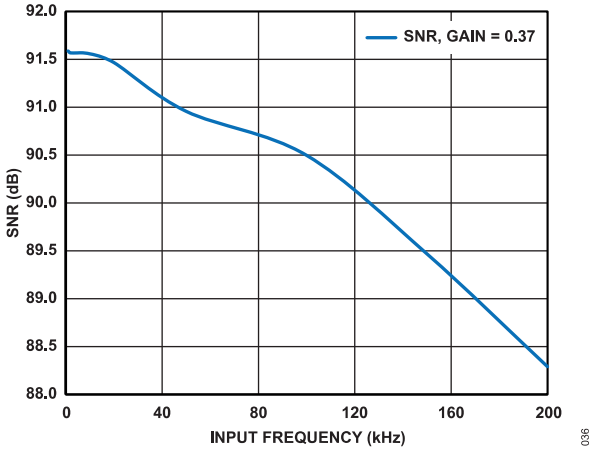

Figure 40. SNR vs. Input Frequency, Gain = 0.37

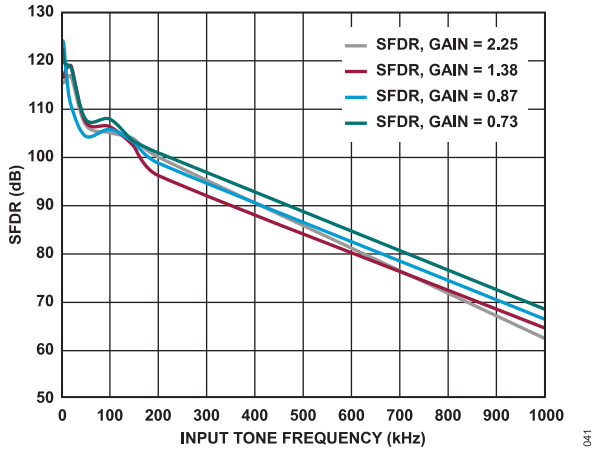

Figure 38. SFDR vs. Input Tone Frequency, Gain = 0.73, Gain = 0.87, Gain = 1.38, and Gain = 2.25

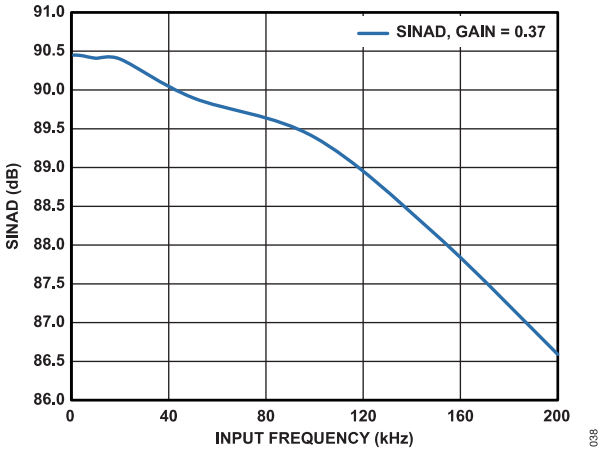

Figure 41. SINAD vs. Input Frequency, Gain = 0.37

TYPICAL PERFORMANCE CHARACTERISTICS

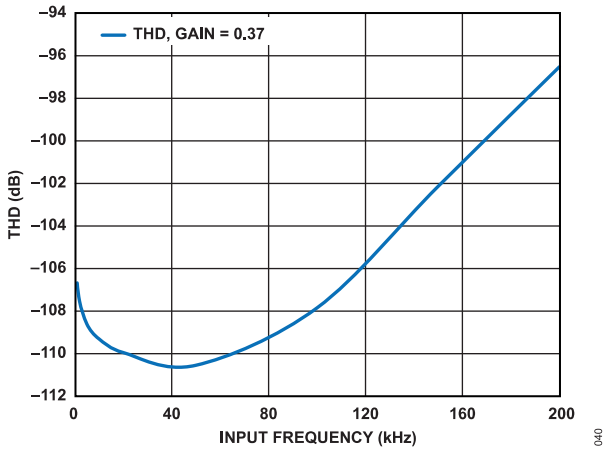

Figure 42. THD vs. Input Frequency, Gain = 0.37

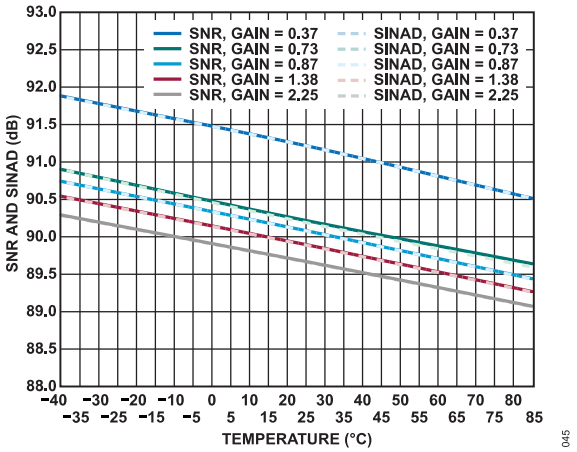

Figure 45. SNR and SINAD vs. Temperature, Gain, f_{IN} = 1 kHz

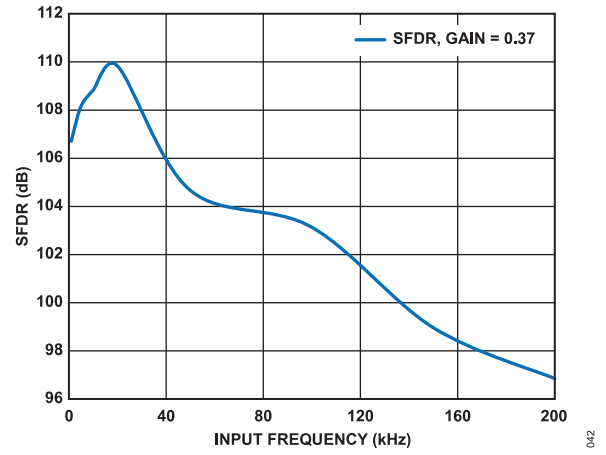

Figure 43. SFDR vs. Input Frequency, Gain = 0.37

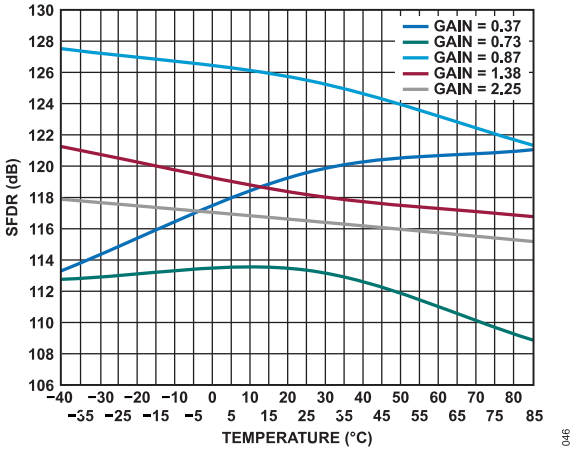

Figure 46. SFDR vs. Temperature, Gain, f_{IN} = 1 kHz

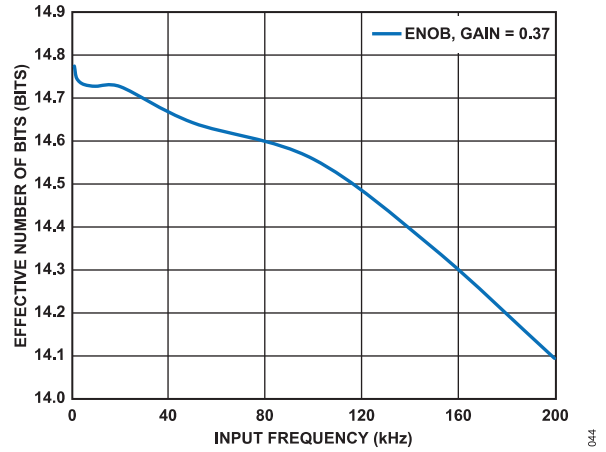

Figure 44. Effective Number of Bits vs. Input Frequency, Gain = 0.37

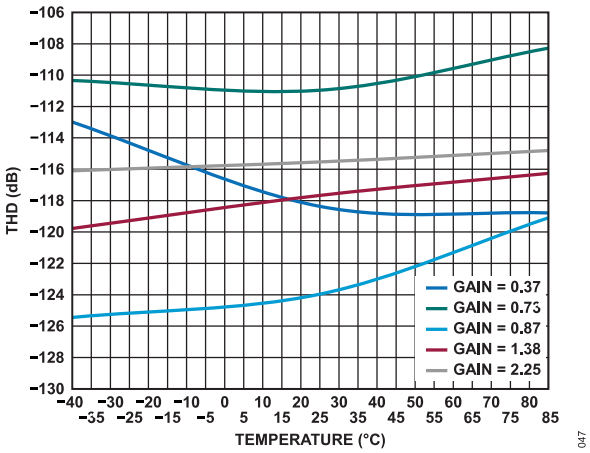

Figure 47. THD vs. Temperature, Gain, f_{IN} = 1 kHz,

TYPICAL PERFORMANCE CHARACTERISTICS

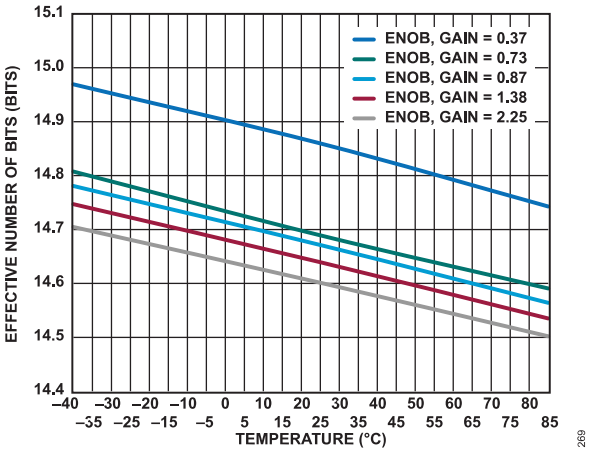

Figure 48. Effective Number of Bits vs. Temperature, Gain, f_{IN}= 1 kHz

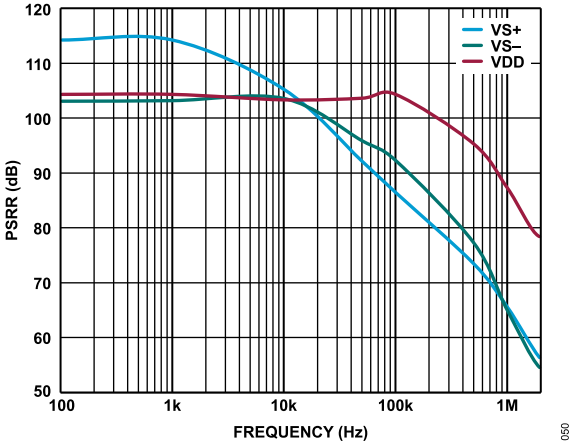

Figure 51. PSRR vs. Frequency

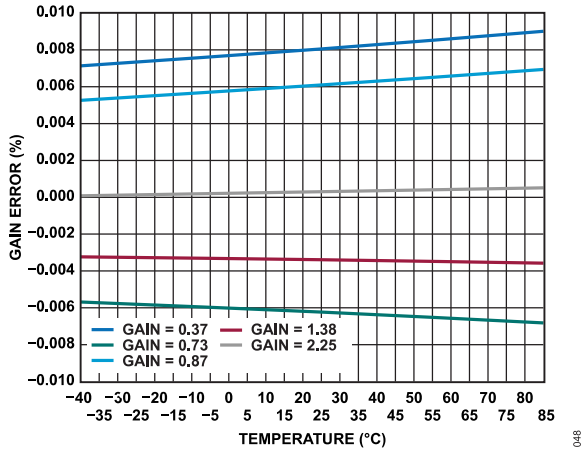

Figure 49. Gain Error vs. Temperature

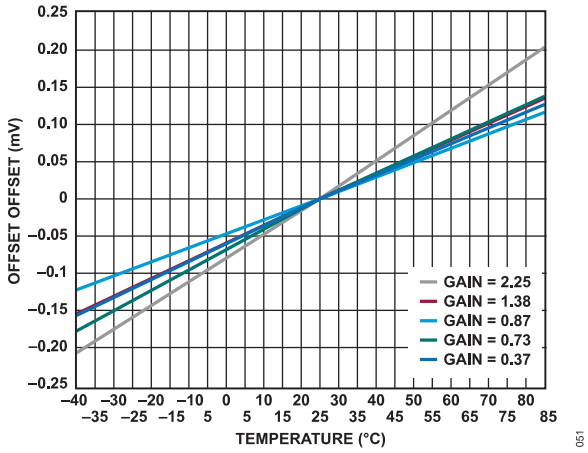

Figure 52. Offset Error vs. Temperature

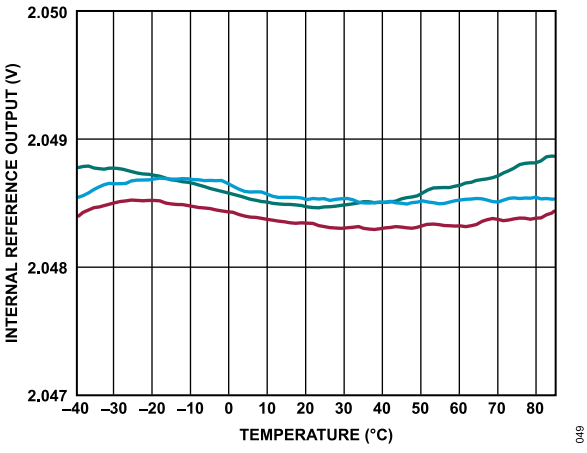

Figure 50. Internal Reference Output vs. Temperature

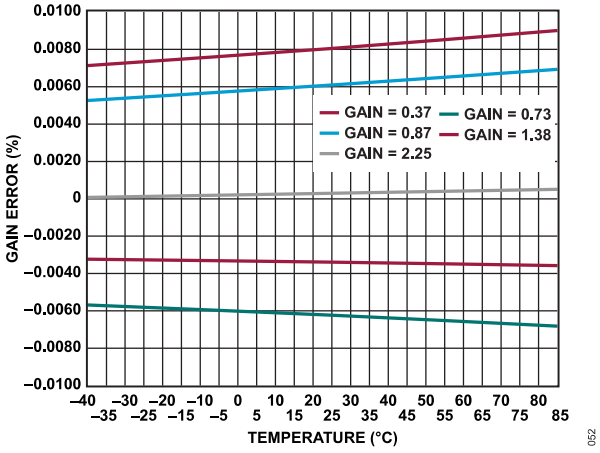

Figure 53. Gain Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

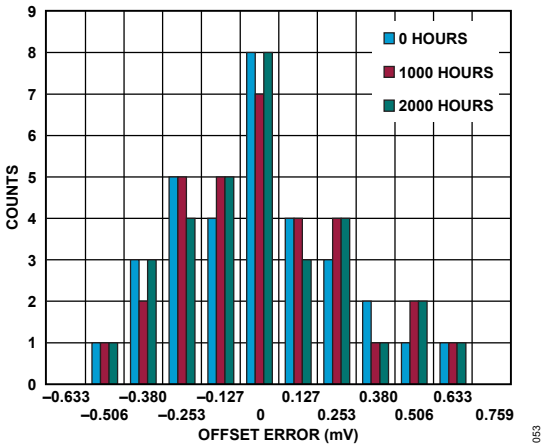

Figure 54. Long Term Drift Offset Error, Gain = 1.38

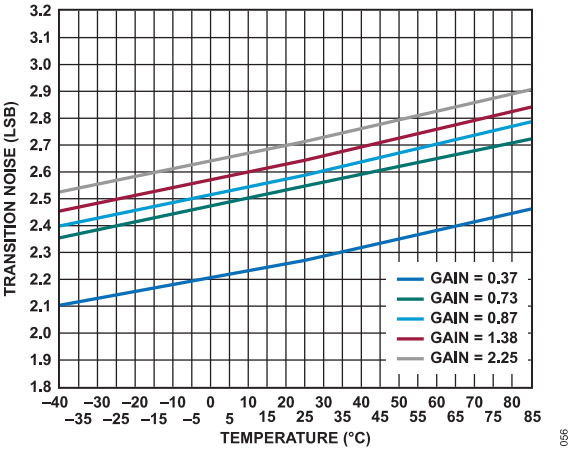

Figure 57. Transition Noise vs. Temperature, Gain

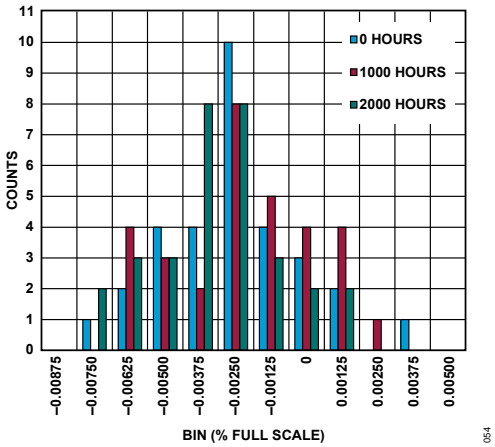

Figure 55. Long Term Drift Gain Error, Gain = 0.37

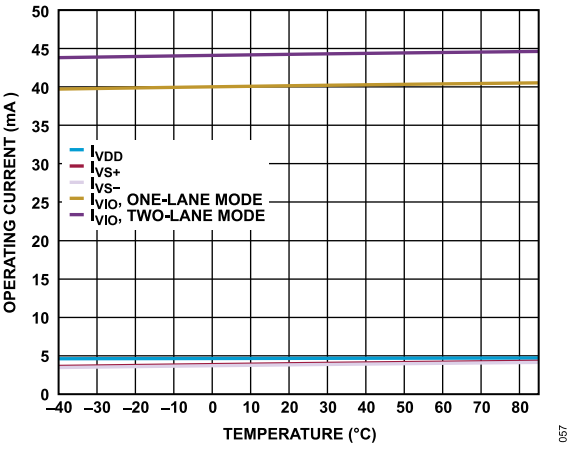

Figure 58. Operating Current vs. Temperature (I_{VDD} = VDD Current, I_{VS+} = VS+ Current, I_{VS-} = VS− Current, I_{VIO} = VIO Current)

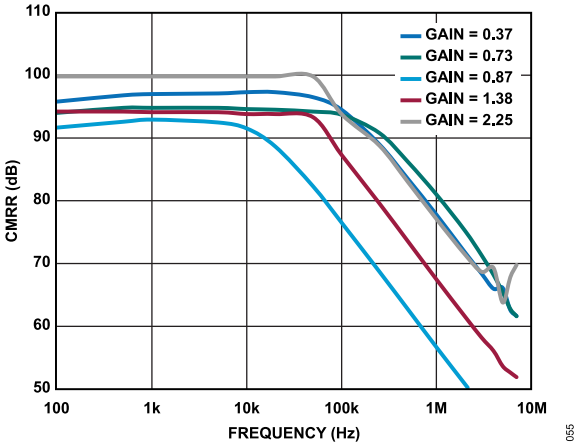

Figure 56. CMRR vs. Frequency

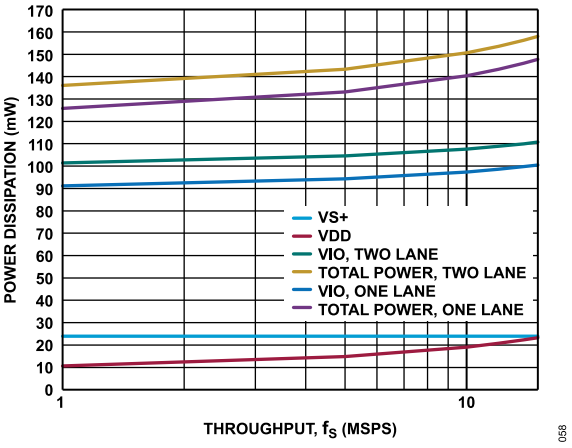

Figure 59. Power Dissipation vs. Throughput, 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

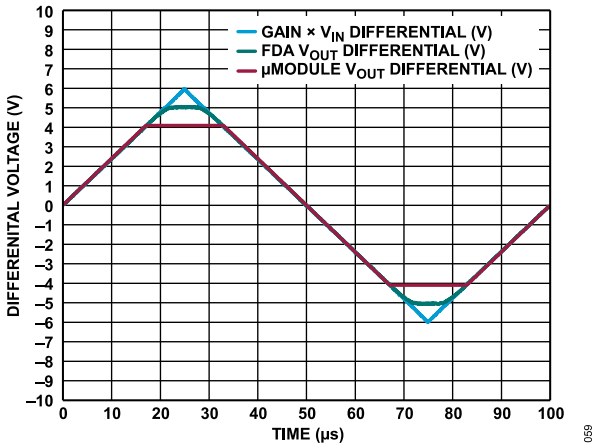

Figure 60. Differential Voltage vs. Time, f_{IN} = 10 kHz

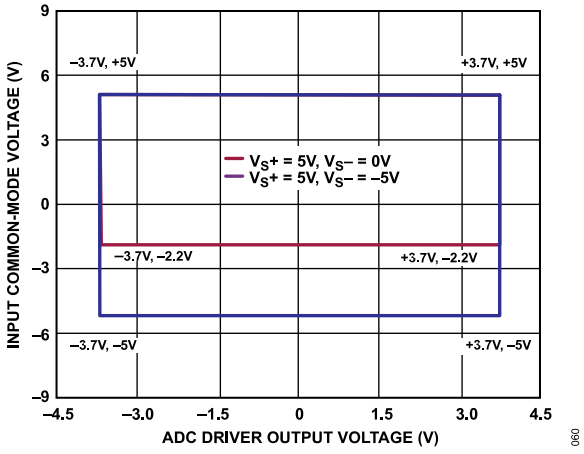

Figure 61. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 0.37, ±10 V Differential Input

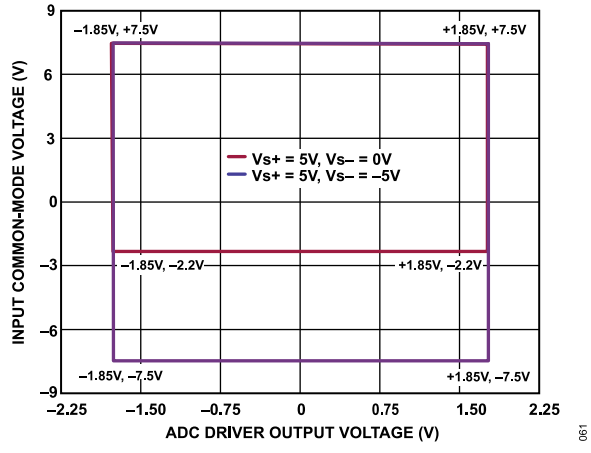

Figure 62. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 0.73, ±5 V Differential Input

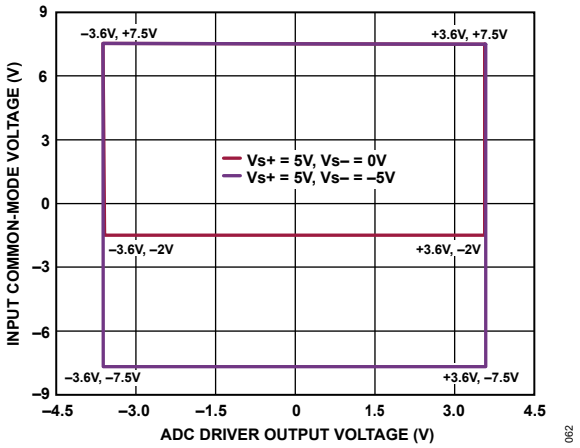

Figure 63. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 0.87, ±4.096 V Differential Input

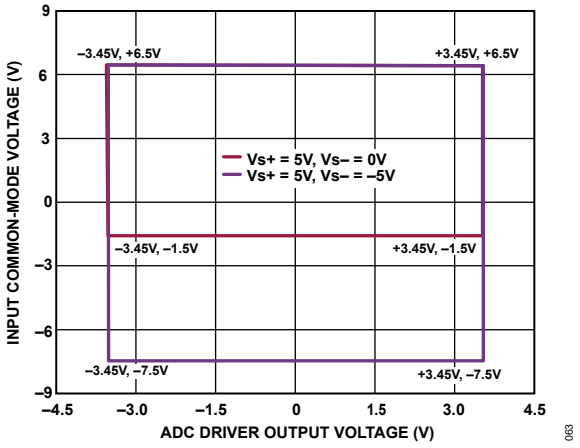

Figure 64. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 1.38, ±2.5 V Differential Input

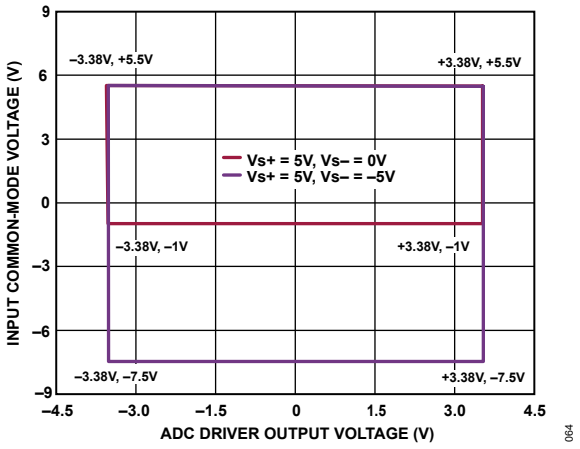

Figure 65. Input Common-Mode Voltage vs. ADC Driver Output Voltage, Gain = 2.25, ±1.5 V Differential Input

TYPICAL PERFORMANCE CHARACTERISTICS

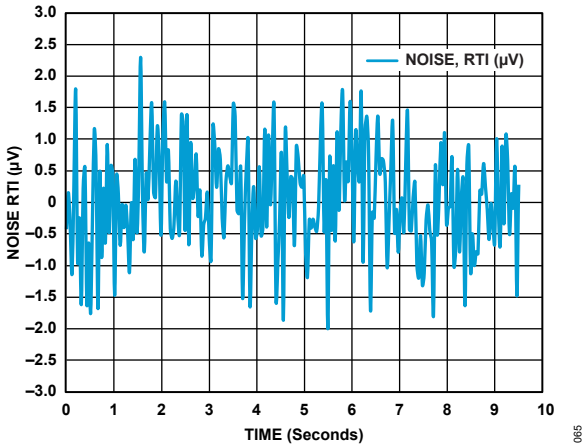

Figure 66. Voltage Noise for 0.1 Hz to 10 Hz Bandwidth, f_S = 100 kSPS, 256 Samples Averaged per Reading, OSR = 4096

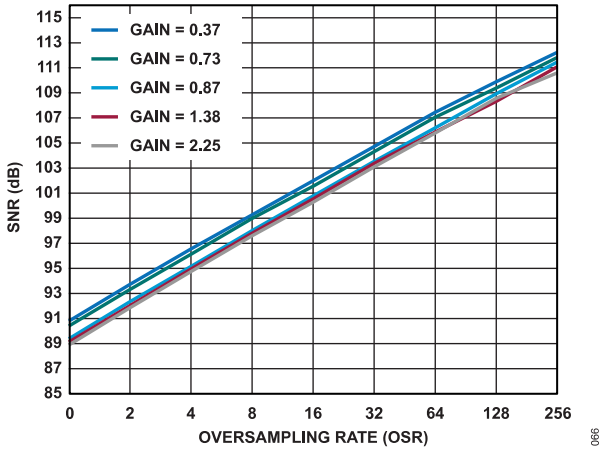

Figure 67. SNR vs. Oversampling Rate for Input Frequencies, f_{IN} = 1 kHz

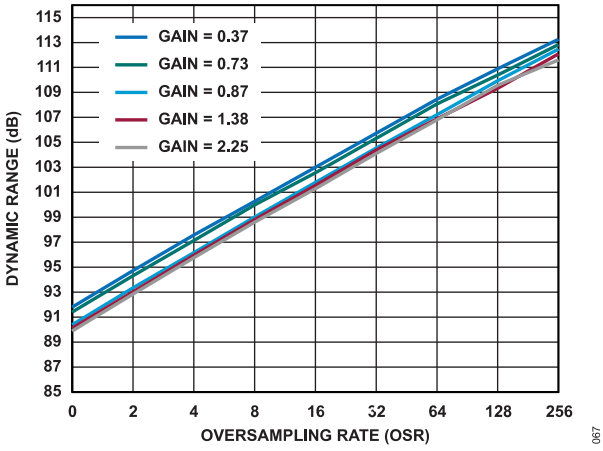

Figure 68. Dynamic Range vs. Oversampling Rate

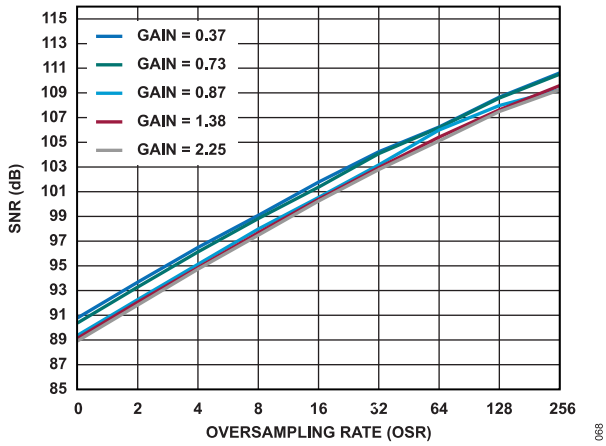

Figure 69. SNR vs. Oversampling Rate for Input Frequencies, f_{IN} = 10 kHz

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity (DNL)

In an ideal µModule, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The first transition occurs at a level ½ LSB above analog ground (15.625 µV for the gain = 1.38, ±2.5 V range). Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift

Drift offset error drift is the ratio of the offset error change due to a temperature change of 1°C and the full-scale code range (gain = 1.38, ±2.5 V range). This drift is expressed in parts per million per degree Celsius as follows:

Offset Error Drift (ppm/°C) = 106 × (*Offset Error_*T_{MAX} − *Offset Error_*T_{MIN})/ (T_{MAX} − T_{MIN})

where: T_{MAX} = 85°C and T_{MIN} = −40°C.

Gain Error

The first transition (from 100…000 to 1000…001) occurs at a level ½ LSB above nominal negative full scale and the last transition (from 011…110 to 011…111) occurs for an analog voltage 1½ LSB below the nominal positive full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the ideal levels after the offset error is removed. In addition, the absolute accuracy of the reference used for the µModule can be a large source of error. Therefore, this error source is removed by measuring its value and using it to determine positive full scale (PFS) and negative full scale (NFS) for the gain error calculation. If the reference used cannot be measured, its deviation from ideal must be factored into the gain error calculation.

This error is expressed in percentage as follows:

$$Gain\_Error(\%) = 100 \times \left((PFS - NFS)_{ACTUAL\_CODE} - (PFS - NFS)_{IDEAL\_CODE}\right) / (PFS - NFS)_{IDEAL\_CODE}$$

where:
PFS is positive full scale.
NFS is negative full scale.

Gain Error Drift

Gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range (gain = 0.37, ±10 V range). This drift is expressed in parts per million per degree Celsius as follows:

Gain Error Drift (ppm/°C) = 106 × (*Gain Error_*T_{MAX} – *Gain Error_*T_{MIN})/(T_{MAX} − T_{MIN})

where: T_{MAX} = 85°C and T_{MIN} = −40°C.

Spurious-Free Dynamic Range (SFDR)

SFDR is defined as the difference, in dB, between the peak spurious or harmonic component in the ADC output spectrum (up to $f_S/2$ and excluding dc) and the rms value of the fundamental.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD and expressed in bits as follows:

ENOB = ($SINAD_{dB}$ − 1.76)/6.02

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response

Transient response is the time required for the µModule to acquire a full-scale input step to ±1 LSB accuracy.

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 1.3 V p-p sine wave applied to the input common-mode voltage of frequency, f.

$$CMRR \text{ (dB)} = 10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT})$$

where:
$P_{\mu Module\_IN}$ is the common-mode power at the frequency, f, applied to the inputs.
$P_{\mu Module\_OUT}$ is the power at the frequency, f, in the µModule output.

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of the power in the µModule output at the frequency, f, to the power of a 500 mV p-p sine wave applied to the VDD and VS+ supply voltage centered at 5 V and 100 mV p-p for a VS− supply voltage centered at − 1 V of frequency, f.

$$PSRR \text{ (dB)} = 10\log(P_{\mu Module\_IN}/P_{\mu Module\_OUT})$$

where:
$P_{\mu Module\_IN}$ is the power at the frequency, f, at each of the VDD, VS+, and VS− supply pins.
$P_{\mu Module\_OUT}$ is the power at the frequency, f, in the µModule output.

THEORY OF OPERATION

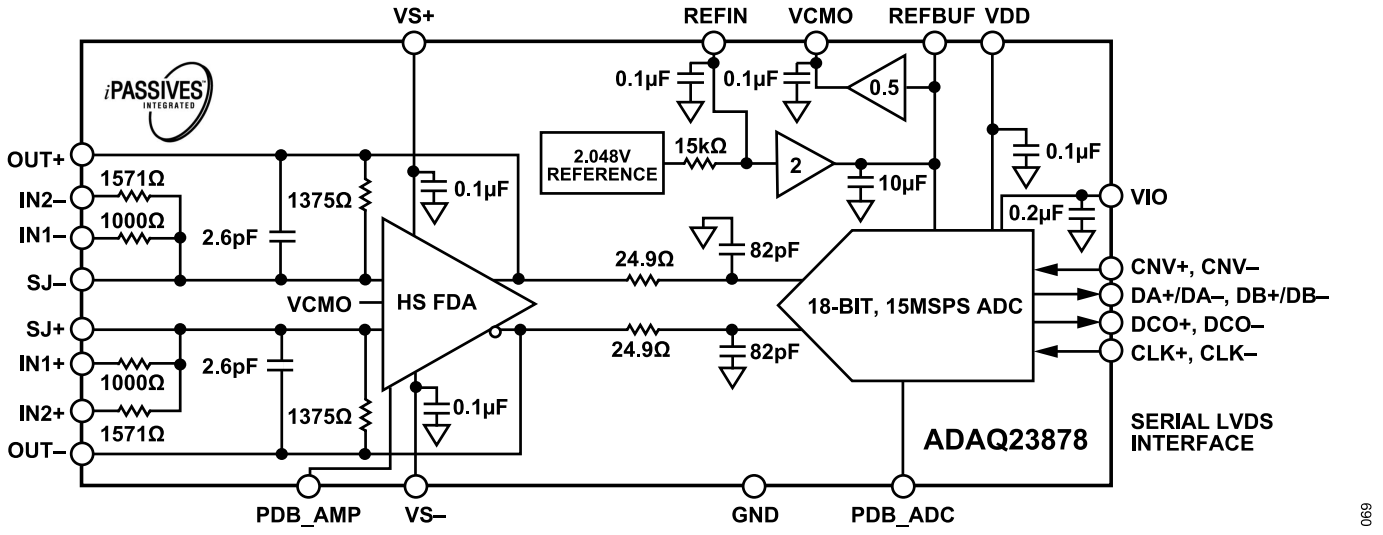

Figure 70. ADAQ23878 µModule Simplified Block Diagram

CIRCUIT INFORMATION

The ADAQ23878 is a precision, high speed, µModule data acquisition solution that reduces the development cycle of precision measurement systems by transferring the design burden of component selection, optimization, and layout from the designer to the device. The ADAQ23878 reduces the end system component count by combining multiple common signal processing and conditioning blocks in a single device, including a low noise, fully differential ADC driver, a stable reference buffer, and a high speed, 18-bit, 15 MSPS SAR ADC. The device also incorporates the Analog Devices proprietary iPassives technology components necessary for optimum performance. The superior matching and drift characteristics of the resistors minimizes temperature dependent error sources.

The ADAQ23878 includes a precision internal 2.048 V reference, as well as an internal reference buffer. The ADAQ23878 also has a high speed serial LVDS interface that can output one or two bits at a time. The fast 15 MSPS throughput with no pipeline latency makes the ADAQ23878 ideally suited for a wide variety of high speed applications. The ADAQ23878 dissipates only 143 mW at 15 MSPS.

TRANSFER FUNCTION

The ADAQ23878 µModule digitizes the full-scale voltage of 2× V_{REF} in to 2^{18} levels, resulting in an LSB size of 31.25 µV with REFBUF = 4.096 V. The output data is in twos complement format. The ideal transfer function is shown in Figure 71. The ideal offset binary transfer function can be obtained from the twos complement transfer function by inverting the MSB of each output code.

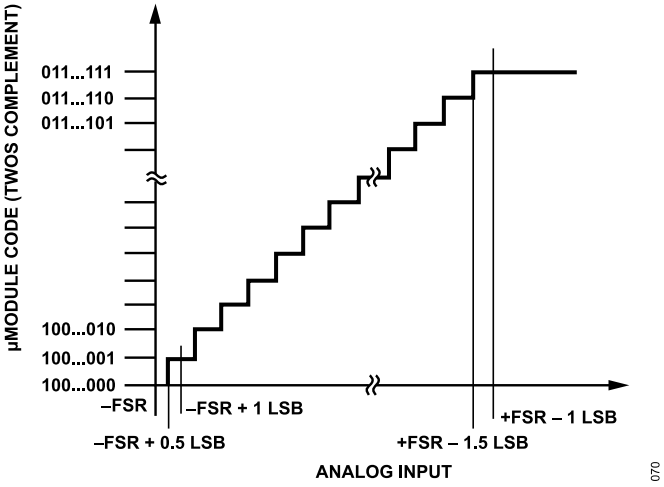

Figure 71. ADAQ23878 Transfer Function (FSR Is Full-Scale Range)

Table 7. Output Codes and Ideal Input Voltages

Description	Inputs Voltages	Digital Output Code (Twos Complement, Hex)
FSR − 1 LSB	(131,071 × V_{REF})/ (131,072 × gain)	0x1FFFF
Midscale + 1 LSB	V_{REF}/(131,072 × gain)	0x00001
Midscale	0 V	0x00000
Midscale − 1 LSB	−V_{REF}/ (131,072 × gain)	0x3FFFF
−FSR + 1 LSB	−(131,071 × V_{REF})/ (131,072 × gain)	0x20001
−FSR	−V_{REF} × gain	0x20000

APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

Figure 72 to Figure 76 shows the typical application examples of differential signals applied to each of the ADAQ23878 inputs for a given gain with varying common-mode voltages. Figure 77 to Figure 81 shows the typical application example of a single-ended signal applied to one of the ADAQ23878 inputs for a given gain with a fixed common-mode voltage of 0 V.

Table 8 shows how to apply the input signal for a given gain or input range option.

Table 8. Gain Configuration and Input Range

Gain	Input Range	Input Signal on Pins	Test Conditions
0.37	±10 V	IN2+, IN2−	Connect the OUT+, IN1−, OUT−, and IN1+ pins together (see Figure 72 and Figure 77)
0.73	±5 V	IN1+, IN1−	Connect the OUT+, IN2−, OUT−, and IN2+ pins together (seeFigure 73 and Figure 78)
0.87	±4.096 V	IN2+, IN2−	Leave the IN1+ and IN1− pins floating (see Figure 74 and Figure 79)
1.38	±2.5 V	IN1+, IN1−	Leave the IN2+ and IN2− pins floating (see Figure 75 and Figure 79)
2.25	±1.5 V	IN2+/IN1+, IN2−/IN1−	Connect the IN2−, IN1−, IN2+, and IN1+ pins together (see Figure 76 and Figure 81)

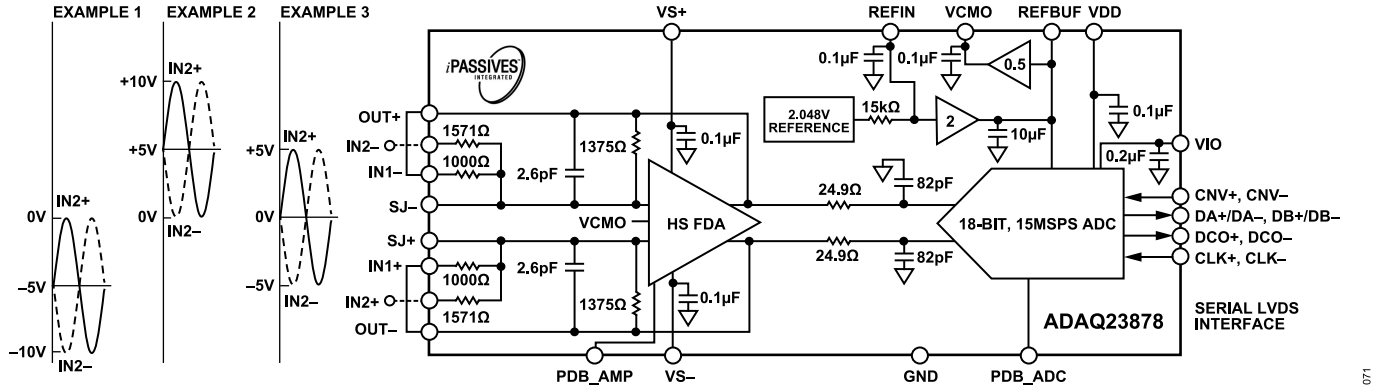

Figure 72. ADAQ23878 Differential Input Configuration with Gain = 0.37, ±10V Input Range

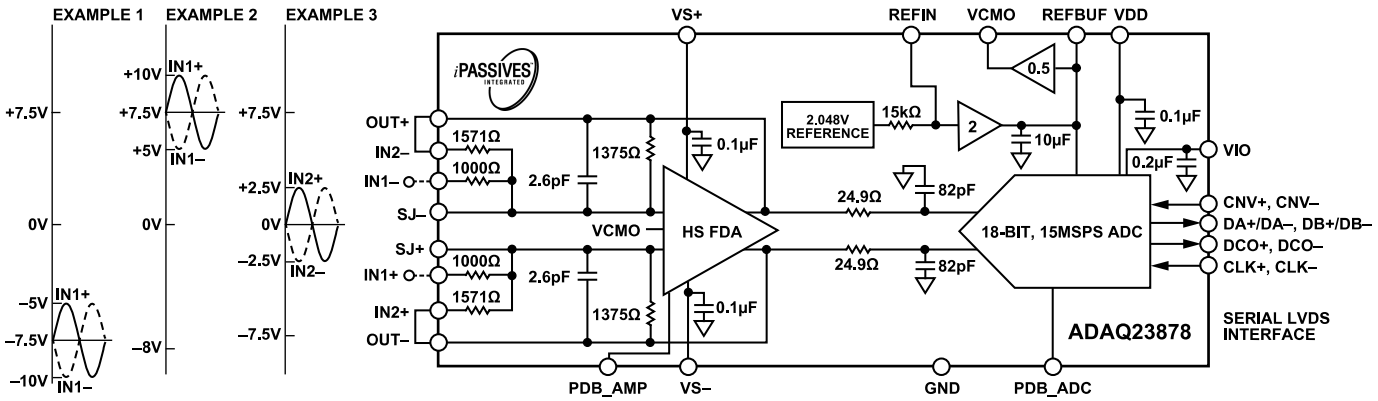

Figure 73. ADAQ23878 Differential Input Configuration with Gain = 0.73, ±5V Input Range

APPLICATIONS INFORMATION

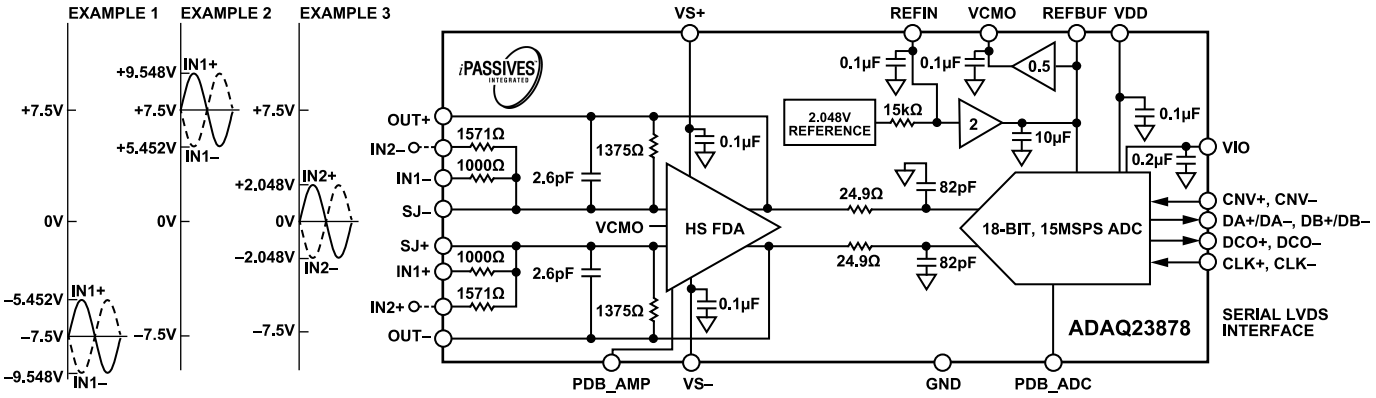

Figure 74. ADAQ23878 Differential Input Configuration with Gain = 0.87, ±4.096V Input Range

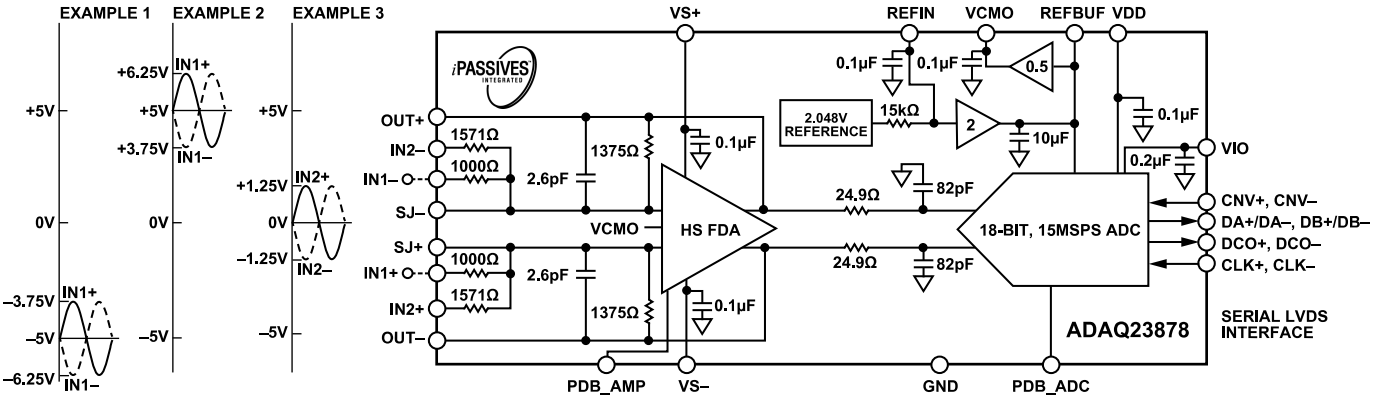

Figure 75. ADAQ23878 Differential Input Configuration with Gain = 1.38, ±2.5V Input Range

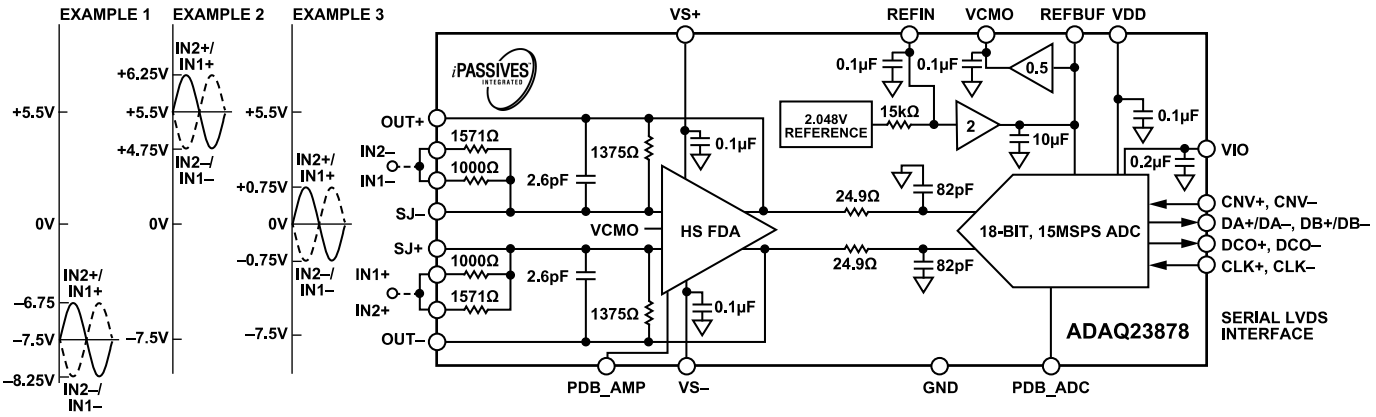

Figure 76. ADAQ23878 Differential Input Configuration with Gain = 2.25, ±1.5V Input Range

APPLICATIONS INFORMATION

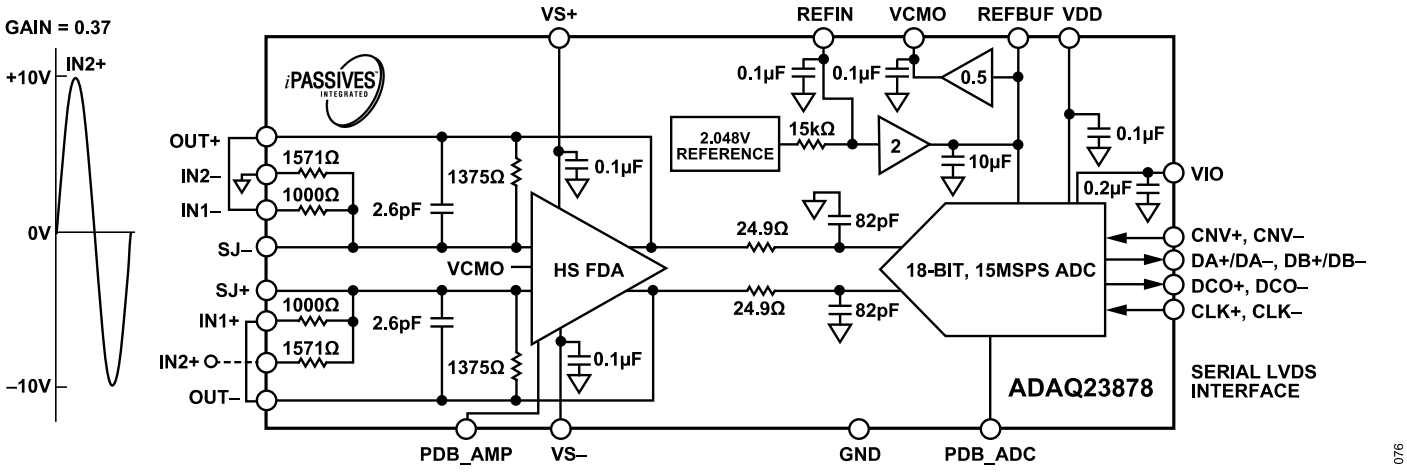

Figure 77. ADAQ23878 Single-Ended Input Configuration with Gain = 0.37

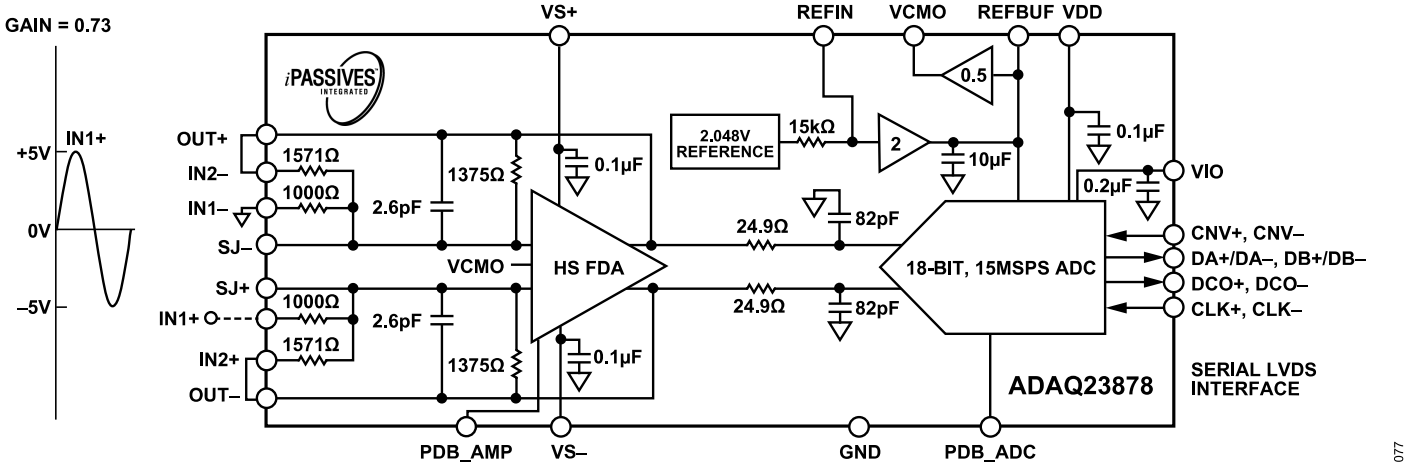

Figure 78. ADAQ23878 Single-Ended Input Configuration with Gain = 0.73

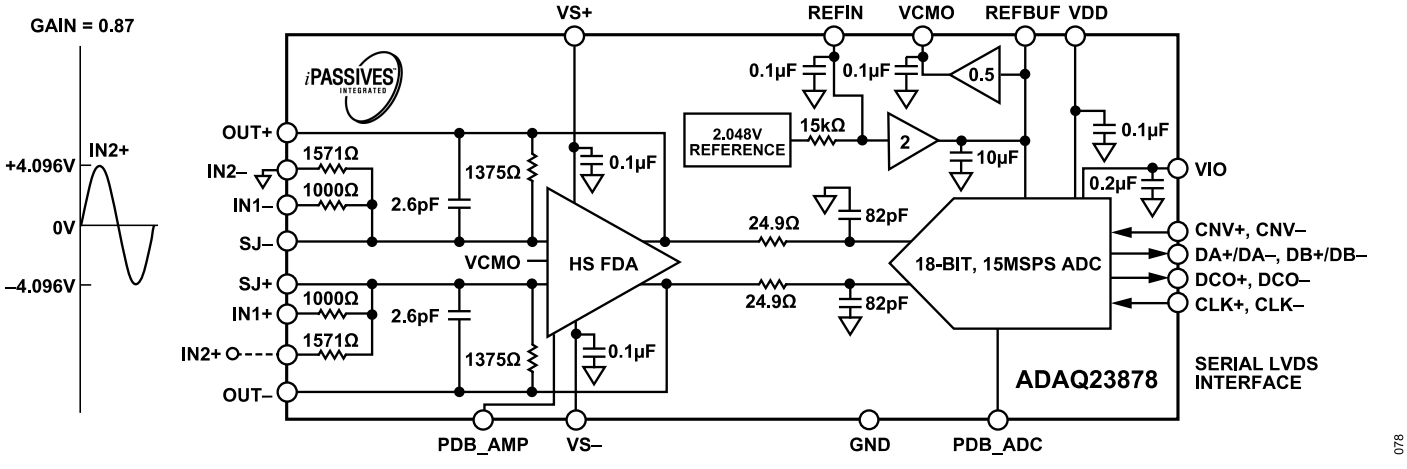

Figure 79. ADAQ23878 Single-Ended Input Configuration with Gain = 0.87

APPLICATIONS INFORMATION

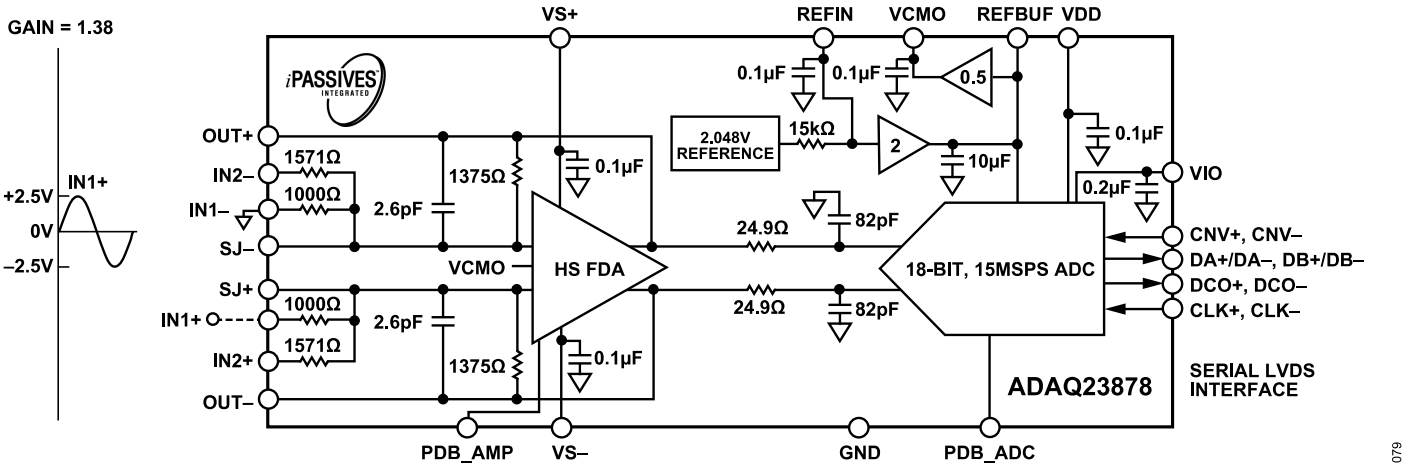

Figure 80. ADAQ23878 Single-Ended Input Configuration with Gain = 1.38

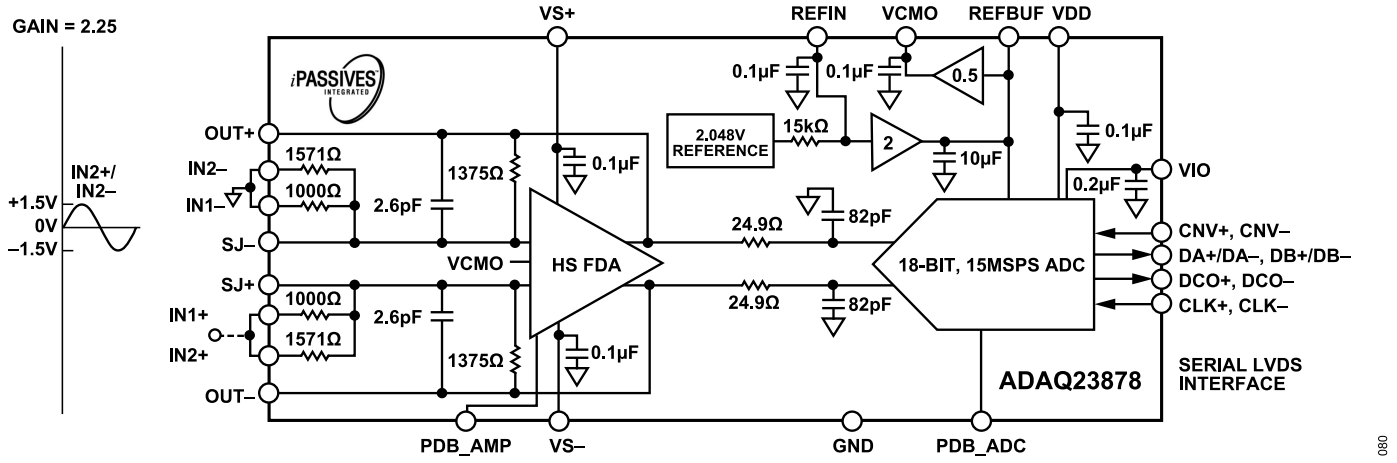

Figure 81. ADAQ23878 Single-Ended Input Configuration with Gain = 2.25

APPLICATIONS INFORMATION

VOLTAGE REFERENCE INPUT

The ADAQ23878 µModule has an internal low noise, low drift (20 ppm/°C), band gap reference connected to REFIN. An internal reference buffer gains the REFIN voltage by 2× to 4.096 V at the REFBUF pin. The voltage difference between REFBUF and GND determines the full-scale input range of the ADAQ23878. The common-mode voltage of VCMO and LVDS pins are derived from REFBUF. Therefore, a voltage at REFBUF pin must be stable after the ADAQ23878 is powered on or exits power-down mode before starting a conversion cycle. The reference and reference buffer can also be externally driven if desired. Also housed in the ADAQ23878 is a 10 µF decoupling capacitor between REFBUF and GND that is ideally laid out within the device. This decoupling capacitor is a required component of the SAR architecture. Adding a second, smaller capacitor in parallel with the 10 µF capacitor may degrade performance and is not recommended.

Internal Reference with Internal Reference Buffer

To use the internal reference and internal reference buffer, bypass the REFIN pin to GND with a 0.1 µF ceramic capacitor.

External Reference with Internal Reference Buffer

If more accuracy and/or lower drift is desired, REFIN can be directly overdriven by an external 2.048 V reference as shown in Figure 82. Analog Devices offers a portfolio of high performance references designed to meet the needs of many applications. With small size, low power, and high accuracy, the LTC6655 is well suited for use with the ADAQ23878 when overdriving the internal reference. The LTC6655 offers 0.025% (maximum) initial accuracy and 2 ppm/°C (maximum) temperature coefficient for high precision applications.

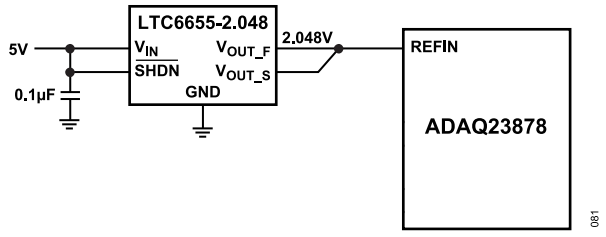

Figure 82. Using the LTC6655 as an External Reference

External Reference Buffer

The internal reference buffer can also be overdriven with an external 4.096 V reference at REFBUF as shown in Figure 83. To do so, REFIN must be grounded to disable the reference buffer. The external reference must have a fast transient response and be able to drive the 0.5 mA to 1.6 mA load at the REFBUF pin. The LTC6655 is recommended when overdriving REFBUF.

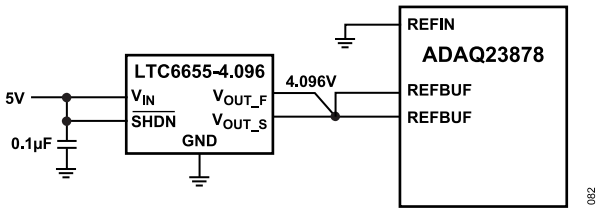

Figure 83. Overdriving REFBUF Using the LTC6655

COMMON-MODE OUTPUT

The VCMO pin is an output that provides one half the voltage present on the REFBUF pin. This voltage is used to set the common mode of a differential amplifier driving the analog inputs. If VCMO is not used, it can be left floating, but the parasitic capacitance on the pin must be under 10 pF.

POWER SUPPLY

The ADAQ23878 uses four power supplies: an internal ADC core supply (VDD), a digital input/output interface supply (VIO), a fully differential ADC driver positive supply (VS+), and a negative supply (VS−). Figure 59 shows the typical total power dissipation including individual consumption for each of the VS+, VDD, and VIO supplies. It is recommended to bypass each of the supply pins (VDD, VIO, VS+, and VS−) with a 2.2 µF (0402, X5R) ceramic decoupling capacitor connected to GND. See the Board Layout section for the layout guidelines.

Power Supply Sequencing

The ADAQ23878 does not have any specific power supply sequencing requirements. The internal ADC core of ADAQ23878 has a power-on-reset (POR) circuit that resets the ADAQ23878 at initial power-up or whenever VDD drops well below the minimum values. After the supply voltage re-enters the nominal supply voltage range, the POR reinitializes the ADAQ23878. After the ADAQ23878 is powered on or exits power-down mode, conversion data is invalid for the first two conversion cycles. The subsequent conversion results are accurate as long as the time between conversions meets the t_{CYC} specification.

Power-Down Mode

The power-down mode of fully differential ADC driver is asserted by applying a low logic level (GND) to the PDB_AMP pin to minimize the quiescent current consumed when the ADAQ23878 is not being used. When the PDB_AMP pin is connected to GND, the fully differential ADC driver output is high impedance. When PDB_ADC is low logic level, an internal ADC core enters power-down mode, and all circuitry (including the LVDS interface) is shut down. When PDB_AMP and PDB_ADC are connected to a high logic level, the ADAQ23878 operates normally. The logic levels for both the PDB_AMP and PDB_ADC pins are determined by VS+ and VIO, respectively.

APPLICATIONS INFORMATION

In power-down state, all internal ADC functions, including the reference and LVDS outputs, are turned off and subsequent conversion requests are ignored. This mode can be used if the ADAQ23878 is inactive for a long period of time and the user wants to minimize power dissipation. The amount of time required to recover from power-down mode depends on how REFBUF is configured. When using the internal reference buffer, the internal ADC core stabilizes after 20 ms. If REFBUF is externally driven, the recovery time can be significantly less.

DIGITAL INTERFACE

The ADAQ23878 conversion is controlled by the CNV+ and CNV– inputs, which can be driven directly with an LVDS signal. Alternatively, the CNV+ pin can be driven with a 0 V to 2.5 V CMOS signal when CNV– is connected to GND. A rising edge on CNV+ samples the analog inputs and initiates a conversion. The pulse width of CNV+ must meet the t_{CNVH} and t_{CNVL} specifications in the timing table (see Table 2).

After the ADAQ23878 is powered on or exits power-down mode, conversion data is invalid for the first two conversion cycles. The subsequent conversion results are accurate as long as the time between conversions meets the t_{CYC} specification. If the analog input signal has not completely settled when it is sampled, the ADAQ23878 noise performance is affected by jitter on the rising edge of CNV+. In this case, drive the rising edge of CNV+ with a clean, low jitter signal. Note that the ADAQ23878 is less sensitive to jitter on the falling edge of CNV+. In applications that are insensitive to jitter, CNV can be driven directly from a field programmable gate array (FPGA).

The ADAQ23878 has an internal clock that is trimmed to achieve a maximum conversion time of 63 ns. With a typical acquisition time of 27.7 ns, throughput performance of 15 MSPS is achieved.

The ADAQ23878 has a serial LVDS digital interface that is easy to connect to an FPGA. Three LVDS pairs are required: CLK±, DCO±, and DA±. A fourth LVDS pair, DB±, is optional (see Figure 84). Route the LVDS signals on the PCB as 100 Ω differential transmission lines and terminated at the receiver with 100 Ω resistors. The optional LVDS output, DB±, is enabled, and data is output two bits at a time on DA± and DB±. Enabling the DB± output increases the supply current from VIO by about 3.6 mA. In two-lane mode, four clock pulses are required for CLK± (see Figure 88).

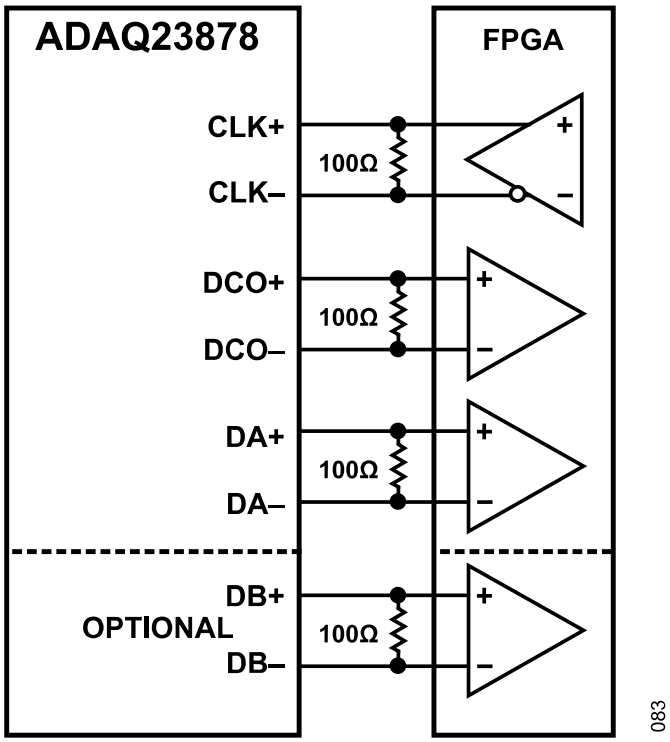

Figure 84. Digital Output Interface to an FPGA

ONE-LANE OUTPUT MODE

A conversion is started by the rising edge of CNV+. When the conversion is complete, the most significant data bit is output on DA±. Data is then ready to be shifted out by applying a burst of eight clock pulses to the CLK± input. The data on DA± is updated by every edge of CLK±. An echoed version of CLK± is output on DCO±. The edges of DA± and DCO± are aligned. Therefore, DCO± can be used to latch DA± in the FPGA. The timing of a single conversion is shown in Figure 85 and Figure 86. Data must be clocked out after the current conversion is complete, and before the next conversion finishes. The valid time window for clocking out data is shown in Figure 87. Note that it is allowed to be still clocking out data when the next conversion begins.

TWO-LANE OUTPUT MODE

At high sample rates, the required LVDS interface data rate can reach >400 Mbps. Most FPGAs can support this rate, but if a lower data rate is desired, the two-lane output mode can be used. When the TWOLANES input pin is connected high (VIO), the ADAQ23878 outputs two bits at a time on DA−/DA+ and DB−/DB+, as shown in Figure 88.

DIGITAL INTERFACE

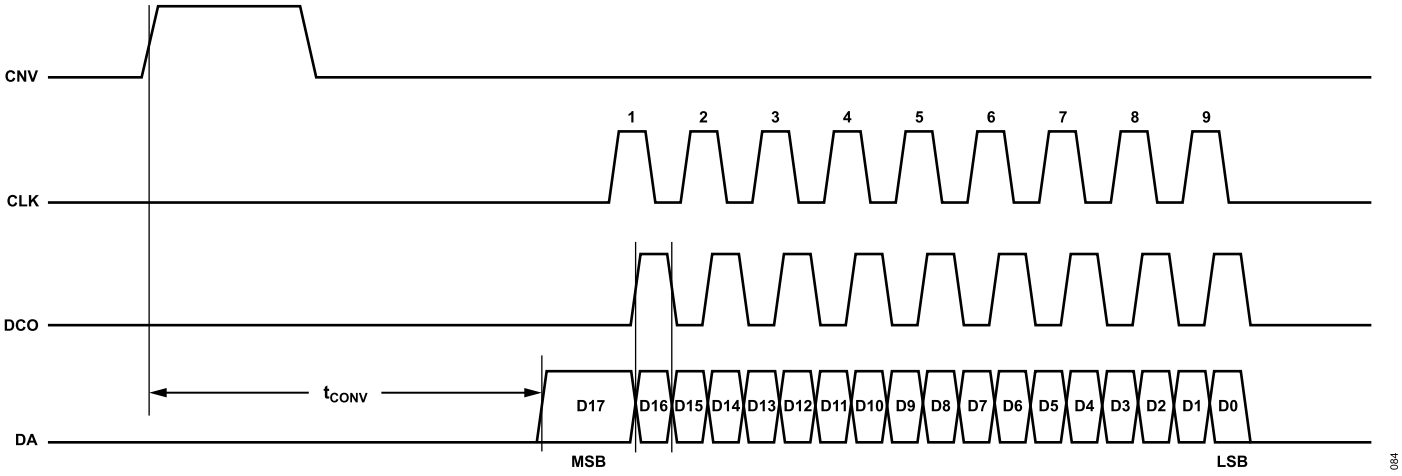

Figure 85. Timing Diagram for a Single Conversion in One-Lane Mode

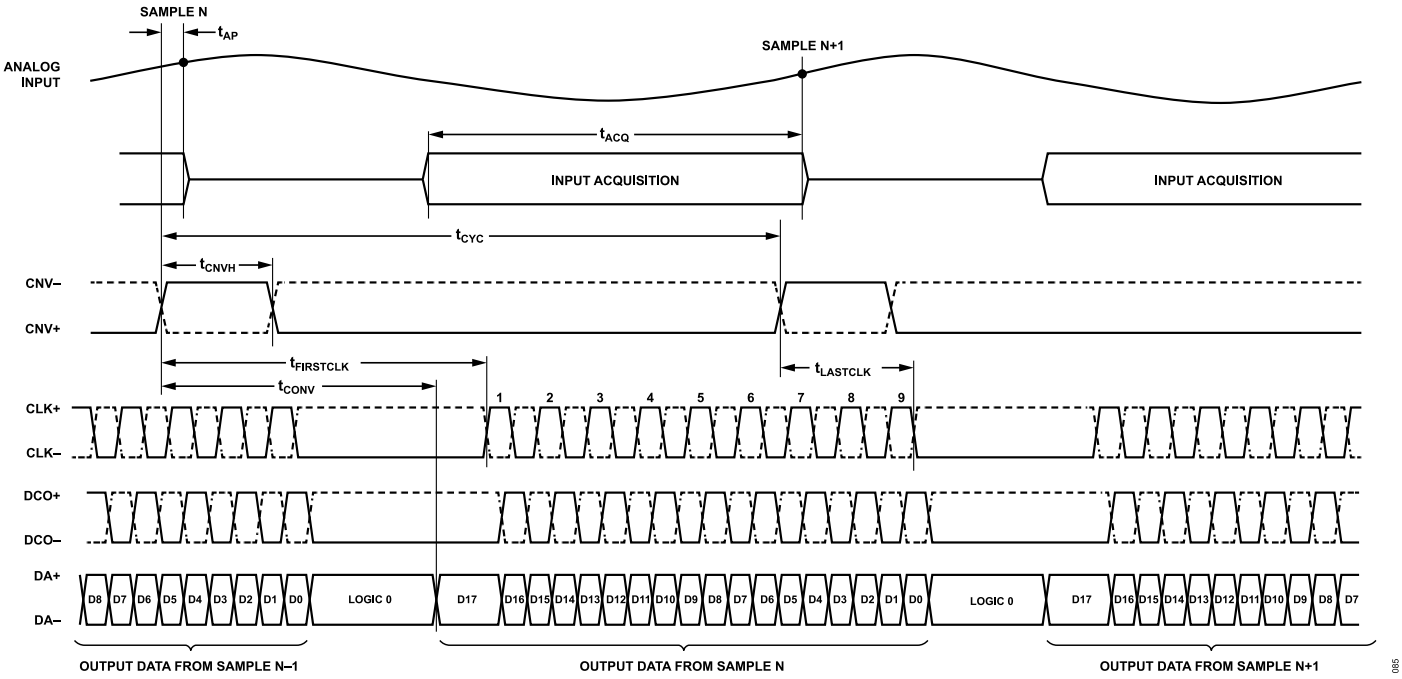

Figure 86. Timing Diagram for Multiple Conversions in One-Lane Output Mode

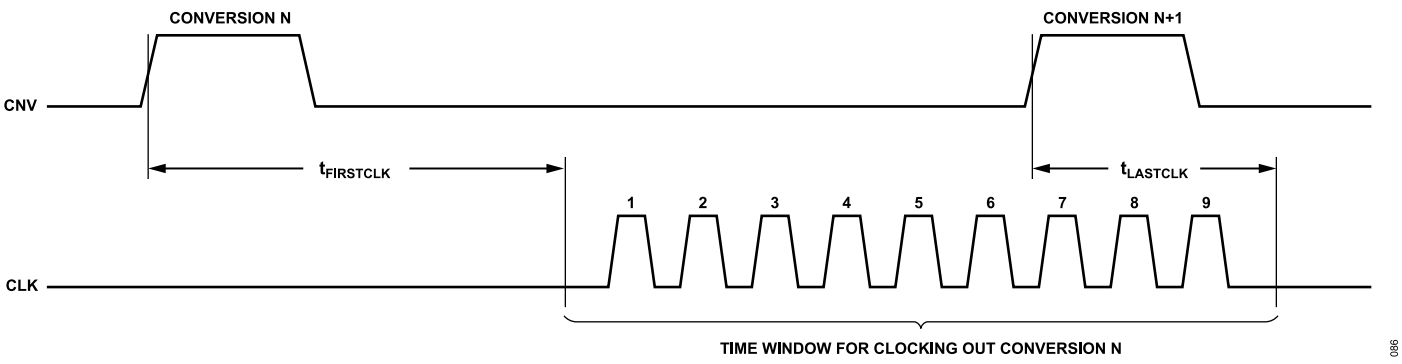

Figure 87. Valid Time Window for Clocking Out Data

DIGITAL INTERFACE

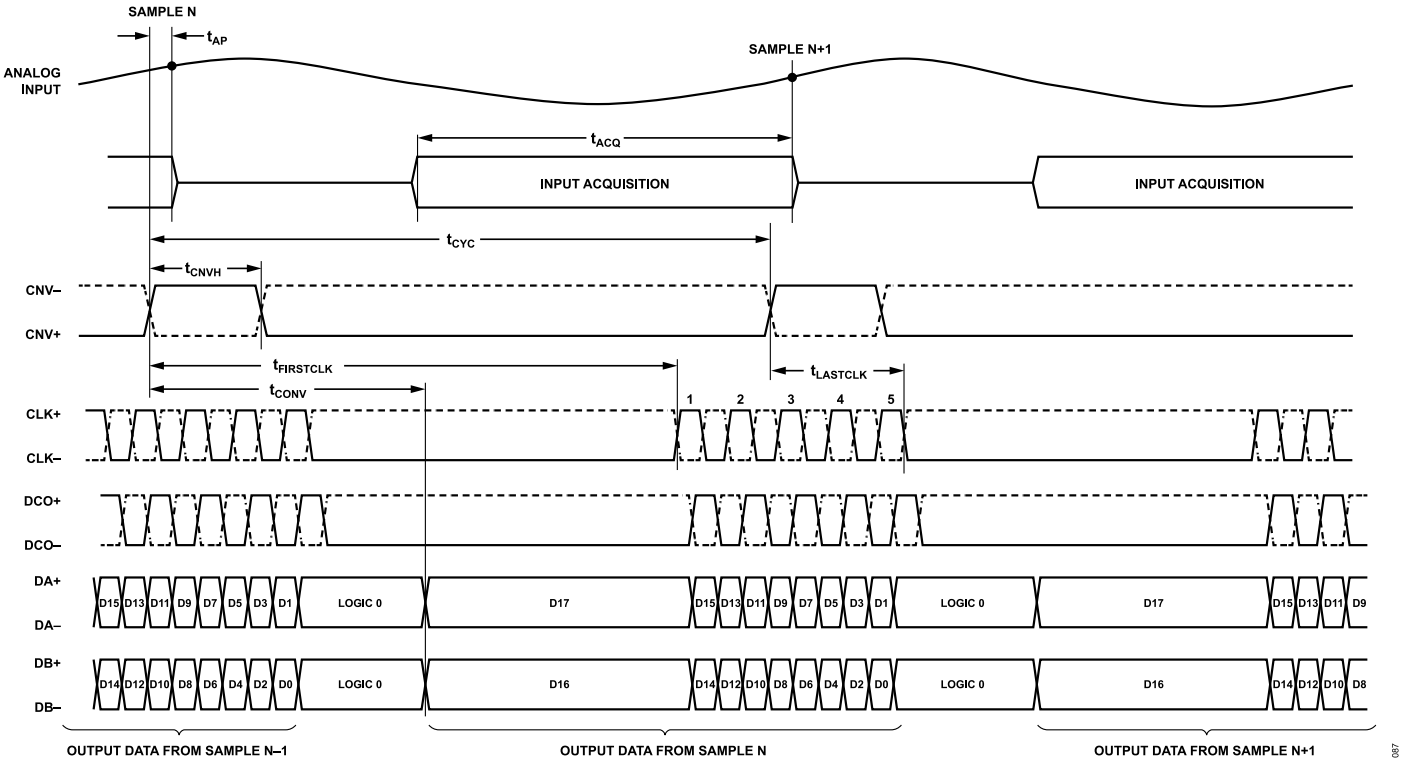

Figure 88. Two-Lane Output Mode

DIGITAL INTERFACE

OUTPUT TEST PATTERNS

The test pattern is enabled when the TESTPAT pin is brought high (VIO) to allow in-circuit testing of the digital interface of the ADAQ23878 and forces the LVDS data outputs to be a test pattern. The ADAQ23878 digital data outputs known values as a test pattern as follows:

- One-lane mode: 10 1000 0001 1111 1100
- Two-lane mode: 11 0011 0000 1111 1100

When the TESTPAT pin is connected low (GND), the ADAQ23878 digital data outputs the conversion results.

BOARD LAYOUT

The PCB layout is critical for preserving signal integrity and achieving the expected performance from the ADAQ23878. A multilayer board with an internal, clean ground plane in the first layer beneath the ADAQ23878 is recommended. Care must be taken with the placement of individual components and routing of various signals on the board. It is highly recommended to route input and output signals symmetrically. Solder the ground pins of the ADAQ23878 directly to the ground plane of the PCB using multiple vias. Remove the ground and power planes beneath the input and output pins of ADAQ23878 to avoid undesired parasitic capacitance. Any undesired parasitic capacitance could impact the distortion and linearity performance of the ADAQ23878.

The pinout of the ADAQ23878 eases the layout and allowing its analog signals on the left side and its digital signals on the right side. The sensitive analog and digital sections must be separated on the PCB while keeping the power supply circuitry away from the analog signal path. Fast switching signals, such as CNV± or CLK±, and digital outputs DA± and DB± must not run near or cross over analog signal paths to prevent noise coupling to the ADAQ23878.

Good quality ceramic bypass capacitors of at least 2.2 µF (0402, X5R) must be placed between each of supply pins (VDD, VIO, VS+, and VS−) of the ADAQ23878 and GND to minimize electromagnetic interference (EMI) susceptibility and to reduce the effect of glitches on the power supply lines. All the other required bypass capacitors are laid out within the ADAQ23878, saving extra board space and cost.

Figure 89 shows the FFT sampling of the ADAQ23878 at 15 MSPS with the inputs shorted when the external decoupling capacitors on the REFIN, VDD, and VIO pins near the µModule are removed and how well µModule rejects any supply noise and reduces sensitivity to perturbations. This performance impact was verified on the EVAL-ADAQ23878FMCZ and no spurs are present in the noise floor, regardless of whether these external decoupling capacitors are used or removed. The recommended board layout is described in the EVAL-ADAQ23878FMCZ user guide.

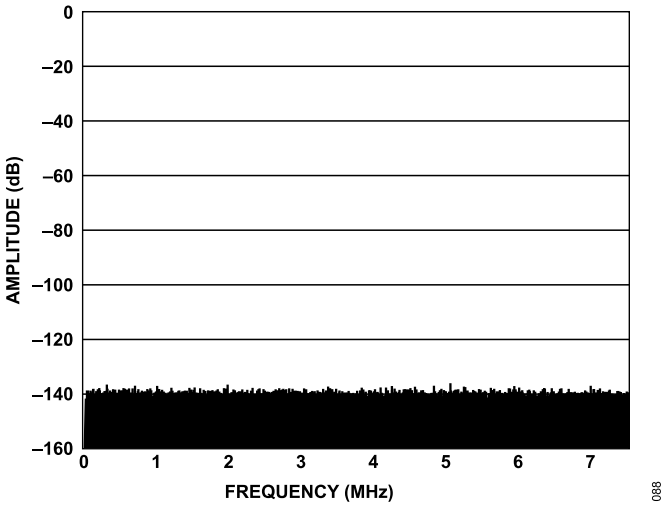

Figure 89. FFT with Shorted Inputs

MECHANICAL STRESS SHIFT

The mechanical stress of mounting a device to a board may cause subtle changes to the SNR and internal voltage reference. The best soldering method is to use IR reflow or convection soldering with a controlled temperature profile. Hand soldering with a heat gun or a soldering iron is not recommended.