14-Bit, 105 MSPS, μModule

FEATURES

- Dual-channel simultaneously sampling ADC
- Integrated differential amplifier/ADC driver
- Single-ended to differential conversion
- Package footprint, 7 mm × 6 mm, 72-ball CSP_BGA
- 6× footprint reduction vs. discrete solution
- On-chip reference circuitry with V_{OCM} generation
- CMOS, DDR CMOS, or DDR LVDS outputs
- Optional data output randomizer
- Optional clock duty-cycle stabilizer
- Shutdown and nap modes
- Serial SPI port for configuration

APPLICATIONS

- Communications
- Cellular base stations
- GPS receiver
- Nondestructive testing
- Portable medical imaging
- Multichannel data acquisition

GENERAL DESCRIPTION

The ADAQ8092 is a 14-bit, 105 MSPS, high-speed dual-channel data acquisition (DAQ) μModule® solution. The device incorporates signal conditioning, an analog-to-digital (ADC) driver, a voltage reference, and an ADC in a single package via system in package (SiP) technology. μModule solutions simplify the development of high-speed data acquisition systems by transferring the design burden, component selection, optimization, and layout from the designer to the device. The ADAQ8092 enables a 6× footprint reduction.

Built-in power supply decoupling capacitors enhance power supply rejection performance, making it a robust DAQ solution. The operating temperature range of the ADAQ8092 is −40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

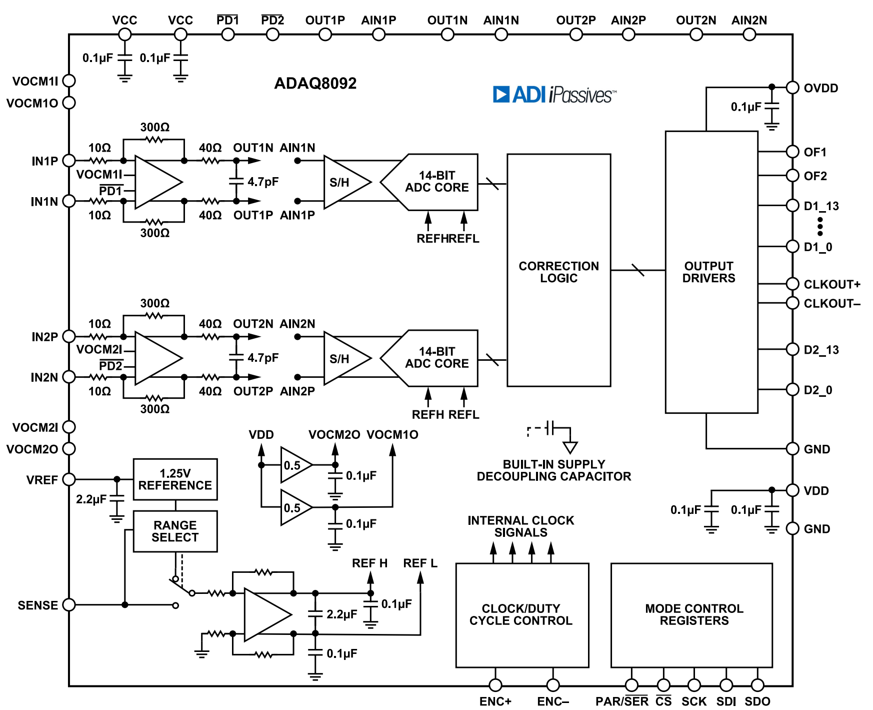

Figure 1.

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REVISION HISTORY

7/2022—Revision 0: Initial Version

SPECIFICATIONS

VCC = 3.3 V, VDD = OVDD = 1.8 V, internal reference, Channel 1 input voltage (V_{IN1P}), Channel 2 input voltage (V_{IN2P}) = 0.1 V p-p (refer to Figure 33), SENSE = 0 V, sampling frequency (f_S) = 90 MSPS, all specifications are at T_{AMB} = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
RESOLUTION	No missing codes	14			Bits
ANALOG INPUT					
Input Resistance (IN1P, IN1N, IN2P, IN2N)	Differential		20		Ω
	Single-ended		19.4		Ω
Input Capacitance	IN1P, IN1N, IN2P, IN2N		1		pF
Analog Input Voltage Range (V_{IN1P}, V_{IN2P})	Refer to Figure 33 and Figure 34			0.1	V p-p diff
Analog Input Common-Mode Voltage Range ($V_{IN,CM}$)		0.3		1.2	V
THROUGHPUT					
Throughput Rate		1		105	MSPS
Sample-and-Hold Acquisition Delay Time			0		ns
Sample-and-Hold Jitter	Single-ended encode		0.08		ps rms
	Differential encode		0.10		ps rms
DC ACCURACY					
Integral Linearity Error (INL)	Input tone: 500 kHz sine wave		−0.5 to +1.7		LSB
Differential Linearity Error (DNL)	Input tone: 500 kHz sine wave		±0.3		LSB
Transition Noise			3.3		LSB_{RMS}
Gain Error	Internal reference		±6		%FS
Gain Error Drift			±25		ppm/°C
Offset Error			±3		mV
Offset Error Drift			±20		μV/°C
Common-Mode Rejection Ratio (CMRR)			84		dB
Power-Supply Rejection Ratio (PSRR)					
VCC			94		dB
OVDD			80		dB
VDD			59		dB
AC ACCURACY	Input frequency (f_{IN}) = 65 MHz				
Single-Ended Input Configuration	See Figure 33				
Effective Number of Bits (ENOB)			9.7		Bits
Signal-to-Noise Ratio (SNR)			60.3		dBFS
Signal-to-Noise-and-Distortion (SINAD)			60.2		dBFS
Spurious-Free Dynamic Range (SFDR)			80.8		dBFS
Differential Input Configuration	See Figure 34				
ENOB		9.3	9.7		Bits
SNR		57.8	60.5		dBFS
SINAD		57.3	60		dBFS
SFDR	65 MHz		75		dBFS
Crosstalk			80		dBc
f_{3dB}, Analog Input to ADC	Refer to Figure 33		186		MHz
REFERENCE					
VREF, Internal Reference Output Voltage	Output current (I_{OUT}) = 0 mA	1.225	1.250	1.275	V
Output Temperature Drift			±25		ppm/°C
Output Impedance	−600 μA < I_{OUT} < +1 mA		4		Ω
Line Regulation	1.7 V < VDD < 1.9 V		0.6		mV/V
ENCODE INPUTS (ENC+, ENC−)					
Differential Encode Mode	ENC− not connected to GND				
Differential Input Voltage (V_{ID})[2]		0.2			V

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
Common-Mode Input Voltage (V_{ICM})			1.2		V
	Externally set[2]	1.1		1.6	V
Input Voltage Range (V_{IN})	ENC+, ENC− to GND	0.2		3.6	V
Input Resistance (R_{IN})			10		kΩ
Input Capacitance (C_{IN})[2]			3.5		pF
Single-Ended Encode Mode	ENC− connected to GND				
High Level Input Voltage (V_{IH})		1.2			V
Low Level Input Voltage (V_{IL})				0.6	V
Input Voltage Range (V_{IN})	ENC+ to GND	0		3.6	V
Input Resistance (R_{IN})			30		kΩ
Input Capacitance (C_{IN})[2]			3.5		pF
DIGITAL INPUT	$\overline{CS}$, SDI, SCK				
High Level Input Voltage (V_{IH})	VDD = 1.8 V	1.3			V
Low Level Input Voltage (V_{IL})	VDD = 1.8 V			0.6	V
Input Current (I_{IN})	V_{IN} = 0 V to 3.6 V	−10		+10	µA
Input Capacitance (C_{IN})[2]			3		pF
PAR/$\overline{SER}$ Input Leakage Current	0 V < PAR/$\overline{SER}$ < VDD	−1.5		+1.5	µA
SENSE Input Leakage Current	SENSE = 0 V or 0.625 V	−3		+3	µA
SDO OUTPUT	Serial programming mode, open-drain output; requires 2 kΩ pull-up resistor if SDO is used				
Logic-Low Output Resistance to GND (R_{OL})	VDD = 1.8 V, SDO = 0 V		200		Ω
Logic-High Output Leakage Current (I_{OH})	SDO = 0 V to 3.6 V	−10		+10	µA
Output Capacitance (C_{OUT})[2]			3		pF
DIGITAL DATA OUTPUTS	Full data and double data rate (DDR) modes				
Output Voltage					
High Level	OVDD = 1.8 V, I_{OUT} = −500 µA	1.75	1.79		V
	OVDD = 1.5 V, I_{OUT} = −500 µA		1.488		V
	OVDD = 1.2 V, I_{OUT} = −500 µA		1.185		V
Low Level	OVDD = 1.8 V, I_{OUT} = 500 µA		0.010	0.050	V
	OVDD = 1.5 V, I_{OUT} = 500 µA		0.010		V
	OVDD = 1.2 V, I_{OUT} = 500 µA		0.010		V
LVDS Mode					
Differential Output Voltage (V_{OD})	100 Ω differential load, 3.5 mA mode	247	350	454	mV
	100 Ω differential load, 1.75 mA mode		175		mV
Common-Mode Output Voltage (V_{OCM})	100 Ω differential load, 3.5 mA mode	1.125	1.25	1.375	V
	100 Ω differential load, 1.75 mA mode		1.25		V
On-Chip Termination (R_{TERM})	Termination enabled, OVDD = 1.8 V		100		Ω
POWER-DOWN MODE					
ADC Driver ($\overline{PD1}$, $\overline{PD2}$)					
Low	Power-down mode		<0.8		V
High	Enabled, normal operation		>1.3		V
Turn-Off Time			1		µs
Turn-On Time			1		µs
VCC Current (I_{VCC})	Power-down mode		3.6		mA
ADC	Sleep mode		1		mW
	Nap mode		16		mW
POWER REQUIREMENTS					
VDD	Full data rate and DDR modes	1.7	1.8	1.9	V
	LVDS output mode	1.7	1.8	1.9	V

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit[1]
VCC	All output modes	3.2		5	V
OVDD	Full data rate and DDR modes	1.1	1.8	1.9	V
	LVDS modes	1.7	1.8	1.9	V
Total Standby Current	Static, all devices enabled		155		mA
ADAQ8092 Current Draw	Sine-wave input				
VDD Current (I_{VDD})	Full rate, DDR CMOS modes		83	92	mA
	LVDS 1.75 mA mode		85		mA
	LVDS 3.5 mA mode		86	97	mA
OVDD Current (I_{OVDD})[3]	Full rate, DDR CMOS modes		10		mA
	LVDS 1.75 mA mode		35		mA
	LVDS 3.5 mA mode		66	76	mA
I_{VCC}	For all output modes		70		mA
Total Power Dissipation	Full and DDR CMOS		394		mW
OPERATING TEMPERATURE RANGE	T_{MIN} to T_{MAX}	−40		+105	°C

[1] FS is full scale.

[2] Guaranteed by design; not subject to test.

[3] The actual value for I_{OVDD} is a function of parasitic capacitance on the data lines and is ideally less than 5 pF to ground per line.

TIMING SPECIFICATIONS

VDD = OVDD = 1.8 V, f_S = 105 MHz, LVDS outputs, differential ENC+/ENC− = 2 V p-p sine wave. All specifications are at T_{AMB} = 25°C, unless noted otherwise.

Table 2. Digital Interface Timing

Parameter	Test Conditions/Comments	Symbol	Min	Typ	Max	Unit
SAMPLING FREQUENCY[1]		f_S	1		105	MHz
ENC[2]						
Low Time	Duty-cycle stabilizer off	t_L	4.52	4.76	500	ns
	Duty-cycle stabilizer on		2	4.76	500	ns
High Time	Duty-cycle stabilizer off	t_H	4.52	4.76	500	ns
	Duty-cycle stabilizer on		2	4.76	500	ns
SAMPLE-AND-HOLD ACQUISITION DELAY TIME		t_{AP}		0		ns
DIGITAL DATA OUTPUTS (CMOS MODES)	Full data rate and double data rate					
ENC± to Data Delay[2]	Load capacitance (C_L) = 5 pF	t_D	1.1	1.7	3.1	ns
ENC± to CLKOUT± Delay[2]	C_L = 5 pF	t_C	1	1.4	2.6	ns
DATA to CLKOUT± Skew[2]	$t_D - t_C$	t_{SKEW}	0	0.3	0.6	ns
Pipeline Latency	Full data rate mode			6		Cycles
	Double data rate mode			6.5		Cycles
DIGITAL DATA OUTPUTS (LVDS Mode)						
ENC± to Data Delay[2]	C_L = 5 pF	t_D	1.1	1.8	3.2	ns
ENC± to CLKOUT± Delay[2]	C_L = 5 pF	t_C	1	1.5	2.7	ns
DATA to CLKOUT± Skew[2]	$t_D - t_C$	t_{SKEW}	0	0.3	0.6	ns
Pipeline Latency				6.5		Cycles
SPI PORT TIMING[2]						
SCK Period	Write mode	t_{SCK}	40			ns
	Readback mode, SDO capacitance (C_{SDO}) = 20 pF, pull-up resistance (R_{PULLUP}) = 2 kΩ		250			ns
$\overline{CS}$ to SCK Setup Time		t_S	5			ns

SPECIFICATIONS

Table 2. Digital Interface Timing

Parameter	Test Conditions/Comments	Symbol	Min	Typ	Max	Unit
SCK to $\overline{CS}$ Setup Time		t_H	5			ns
SDI Setup Time		t_{DS}	5			ns
SDI Hold Time		t_{DH}	5			ns
SCK Falling to SDO Valid	Readback mode, C_{SDO} = 20 pF, R_{PULLUP} = 2 kΩ	t_{DO}			125	ns

[1] Recommended operating conditions.

[2] Guaranteed by design, but not subject to test.

Timing Diagram

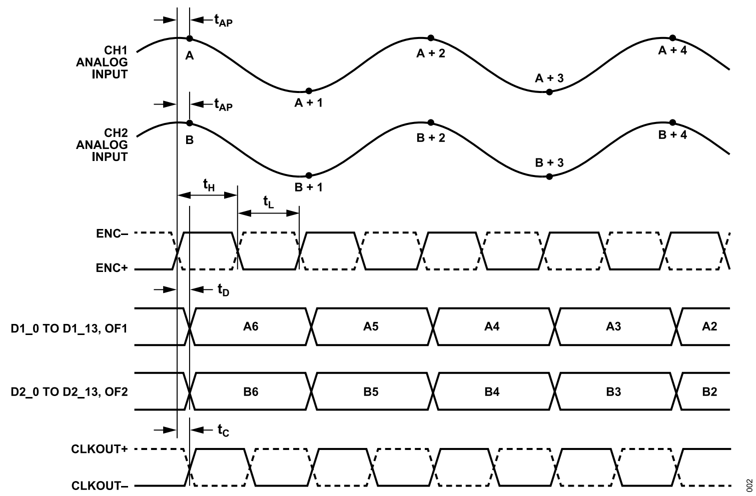


Figure 2. Full Rate CMOS Output Mode Timing (All Outputs Are Single-Ended and Have CMOS Levels)

SPECIFICATIONS

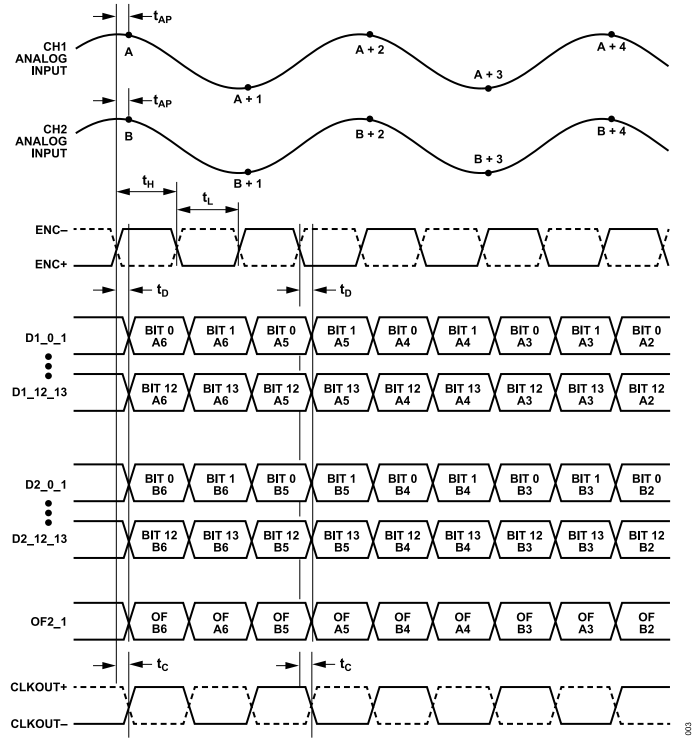


Figure 3. Double Data-Rate CMOS Output Mode Timing (All Outputs Are Single-Ended and Have CMOS Levels)

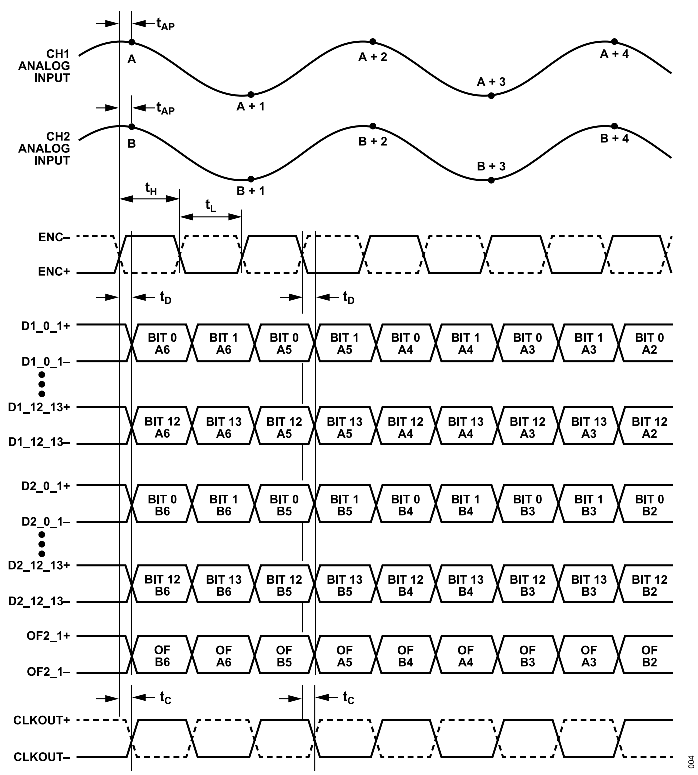


Figure 4. Double Data-Rate LVDS Output Mode Timing (All Outputs Are Differential and Have LVDS Levels)

SPECIFICATIONS

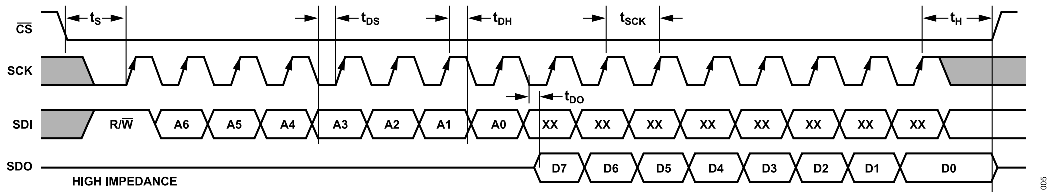


Figure 5. SPI Port Timing (Readback Mode)

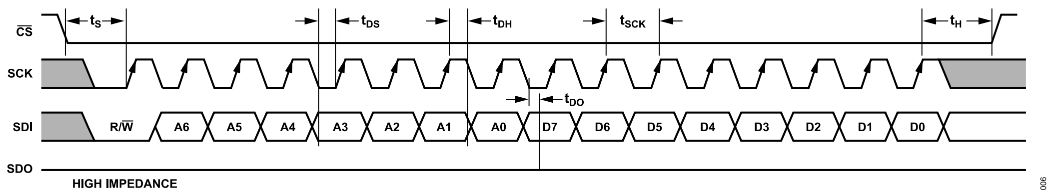


Figure 6. SPI Port Timing (Write Mode)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Analog Inputs	VCC + 0.8 V, or −0.8 V
INxP, INxN	2 V
INxP − INxN, INxN − INxP	VCC + 0.5 V
VOCMxI/VOCMxO	VDD + 0.2 V
AINx	VDD + 0.2 V
Digital Inputs	3.9 V
Supply Voltages	
VCC	5.5 V
VDD, VDDO	2 V
Storage Temperature Range	−55°C to +125°C
Junction Temperature	150°C
Lead Temperature Soldering as per JEDEC J-STD-020	260°C reflow

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC_TOP}	θ_{JC_BOTTOM}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
BC-72-5	41.8	31.8	17.5	21.9	12.9	21.6	°C/W

1 Test Condition 1: Thermal impedance simulated values are based on use of a 2S2P with vias JEDEC PCB excluding the θ_{JC_TOP}, which uses 1S0P JEDEC PCB.

Thermal resistance values specified in Table 4 are simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

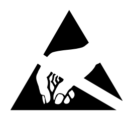
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADAQ8092

Table 5. ADAQ8092, 72-Ball CSP_BGA

ESD Model	Withstand Voltage (V)	Class
HBM	±3000	2
FICDM	±1500	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

FULL DATA-RATE CMOS OUTPUT MODE

ADAQ8092
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9
A	IN1P	AIN1N	AIN1P	GND	SENSE	D1_13	D1_10	D1_7	D1_4
B	IN1N	OUT1N	OUT1P	VDD	VREF	D1_12	D1_9	D1_6	D1_3
C	$\overline{\text{PD1}}$	VOCM1I	VOCM1O	VCC	GND	D1_11	D1_8	D1_5	D1_2
D	PAR/$\overline{\text{SER}}$	OF1	OF2	SDO	SCK	D1_0	D1_1	OVDD	CLKOUT+
E	$\overline{\text{PD2}}$	GND	GND	$\overline{\text{CS}}$	SDI	D2_13	D2_12	GND	CLKOUT–
F	IN2P	VOCM2I	VOCM2O	VCC	GND	D2_11	D2_10	D2_9	D2_8
G	IN2N	OUT2N	OUT2P	GND	ENC–	D2_7	D2_6	D2_5	D2_4
H	GND	AIN2N	AIN29	VDD	ENC+	D2_0	D2_1	D2_2	D2_3

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Figure 7. Pin Configuration (Full Data-Rate CMOS Output Mode)

Table 6. Pin Function Descriptions (Full Data-Rate CMOS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
A1	IN1P	AI	ADC Driver Noninverting Input, Channel 1.
A2	AIN1N	AI	ADC Inverting Analog Input, Channel 1.
A3	AIN1P	AI	ADC Noninverting Analog Input, Channel 1.
A4, C5, E2, E3, E8, F5, G4, H1	GND	P	Ground Reference for VCC, VDD, and OVDD.
A5	SENSE	AI	Internal Reference. Connect to ground to select the internal reference or apply 0.625 V to this pin to provide a 1 V p-p input range. Connect to VDD to select a 2 V p-p input range.
B1	IN1N	AI	ADC Driver Inverting Input, Channel 1.
B2	OUT1N	AO	ADC Driver Inverting Output, Channel 1.
B3	OUT1P	AO	ADC Driver Noninverting output, Channel 1.
B4, H4	VDD	P	Power-Supply Pin of the ADC. VDD has two 0.1 μF decoupling capacitors.
B5	VREF	AO	Reference Voltage Output. VREF is normally 1.25 V and has a built-in 2.2 μF bypass capacitor.
C1	$\overline{\text{PD1}}$	P	Power-Down Pin, Channel 1. When this pin is floating or directly connected to VCC, the Channel 1 ADC driver is in normal (active) operating mode. When this pin is connected to GND, the Channel 1 ADC driver is in a low-power shutdown state with high-Z outputs.
C2	VOCM1I	AI	ADC Driver, Channel 1 Common-Mode Voltage, Channel 1.
C3	VOCM1O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 1.
C4, F4	VCC	P	ADC Driver Power Supply. VCC has two 0.1 μF decoupling capacitors.
D1	PAR/$\overline{\text{SER}}$	P	Programming Mode Selection Pin. Connect this pin to ground to enable the serial programming mode. $\overline{\text{CS}}$, SCK, SDI, and SDO together become a serial interface that controls the analog-to-digital operating modes. Connect PAR/$\overline{\text{SER}}$ to VDD to enable the parallel programming mode where $\overline{\text{CS}}$, SCK, SDI, and SDO become parallel logic inputs that control a reduced set of the analog-to-digital operating modes. PAR/$\overline{\text{SER}}$ must be connected directly to ground or VDD, and not be driven by a logic signal.
D2	OF1	DO	Channel 1 Overflow/Underflow Digital Output. OF1 is high when an overflow or underflow has occurred.
D3	OF2	DO	Channel 2 Overflow/Underflow Digital Output. OF2 is high when an overflow or underflow has occurred.
D4	SDO	DO/DI	Serial Interface Data Output or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDO Is the optional serial interface data output. Data on SDO is read back from the serial programming mode registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2 kΩ pull-up resistor to 1.8 V to 3.3 V. If readback from the serial programming mode

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Full Data-Rate CMOS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
			registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDO can be used together with SDI to power down the device (see Table 11). When used as an input, SDO can be driven with 1.8 V to 3.3 V logic through a 1 kΩ series resistor.
D5	SCK	DI	Serial Interface Clock Input or Digital Output Mode Control. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SCK is the aerial interface clock input. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SCK controls the digital output mode (see Table 11). SCK can be driven with 1.8 V to 3.3 V logic.
D6, D7, C9, B9, A9, C8, B8, A8, C7, B7, A7, C6, B6, A6	D1_0, D1_1, D1_2, D1_3, D1_4, D1_5, D1_6, D1_7, D1_8, D1_9, D1_10, D1_11, D1_12, D1_13	DO	Channel 1 Digital Outputs. D1_13 is the MSB.
D8	OVDD	DO	Digital Output-Driver Power Supply. This pin has an internal 0.1 μF decoupling capacitor
D9	CLKOUT+	DO	Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT+. The phase of CLKOUT+ can also be delayed relative to the digital outputs by programming the serial programming mode registers.
E1	$\overline{\text{PD2}}$	AO	Power-Down Pin, Channel 2. When this pin is floating or directly connected to VCC, the Channel 2 ADC driver is in the normal (active) operating mode. When this pin is connected to GND, the Channel 2 ADC driver is in a low-power shutdown state with high-Z outputs.
E4	$\overline{\text{CS}}$	DI	Serial Interface Chip-Select Input or Clock Duty-Cycle Stabilizer Control. In serial programming mode, (PAR/$\overline{\text{SER}}$ = 0 V), $\overline{\text{CS}}$ is the serial interface chip-select input. When $\overline{\text{CS}}$ is low, SCK is enabled for shifting data on SDI into the serial programming mode registers. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), $\overline{\text{CS}}$ controls the clock duty-cycle stabilizer (see Table 11). $\overline{\text{CS}}$ can be driven with 1.8 V to 3.3 V logic.
E5	SDI	DI	Serial Interface Data Input or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDI Is the serial interface data input. Data on SDI is clocked into the serial programming mode registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDI can be used together with SDO to power down the device (see Table 11). SDI can be driven with 1.8 V to 3.3 V logic.
E9	CLKOUT−	DO	Inverted Version of CLKOUT+.
F1	IN2P	AI	ADC Driver Noninverting input, Channel 2.
F2	VOCM2I	AI	ADC Driver, Channel 2 Common-Mode Voltage.
F3	VOCM2O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 2.
G1	IN2N	AI	ADC Driver Inverting Input, Channel 2.
G2	OUT2N	AO	ADC Driver Inverting Output, Channel 2.
G3	OUT2P	AO	ADC Driver Noninverting Output, Channel 1.
G5	ENC−	DI	Encode Complement Input. Conversion starts on the falling edge. Connect ENC− to GND for single-ended encode mode.
H2	AIN2N	AI	ADC Inverting Analog Input, Channel 2.
H3	AIN2P	AI	ADC Noninverting Analog Input, Channel 2.
H5	ENC+	DI	Encode Input. Conversion starts on the rising edge.
H6, H7, H8, H9, G9, G8, G7, G6, F9, F8, F7, F6, E7, E6	D2_0, D2_1, D2_2, D2_3, D2_4, D2_5, D2_6, D2_7, D2_8, D2_9, D2_10, D2_11, D2_12, D2_13	DO	Channel 2 Digital Outputs. D2_13 is the MSB.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

DOUBLE DATA-RATE CMOS OUTPUT MODE

ADAQ8092
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9
A	IN1P	AIN1N	AIN1P	GND	SENSE	D1_12_13	DNC	D1_6_7	DNC
B	IN1N	OUT1N	OUT1P	VDD	VREF	DNC	D1_8_9	DNC	D1_2_3
C	$\overline{\text{PD1}}$	VOCM1I	VOCM1O	VCC	GND	D1_10_11	DNC	D1_4_5	DNC
D	PAR/$\overline{\text{SER}}$	OF2_1	DNC	SDO	SCK	DNC	D1_0_1	OVDD	CLKOUT+
E	$\overline{\text{PD2}}$	GND	GND	$\overline{\text{CS}}$	SDI	D2_12_13	DNC	GND	CLKOUT–
F	IN2P	VOCM2I	VOCM2O	VCC	GND	D2_10_11	DNC	D2_8_9	DNC
G	IN2N	OUT2N	OUT2P	GND	ENC–	D2_6_7	DNC	D2_4_5	DNC
H	GND	AIN2N	AIN29	VDD	ENC+	DNC	D2_0_1	DNC	D2_2_3

NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT ANYTHING TO THIS PIN.

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Figure 8. Pin Configuration (Double Data-Rate CMOS Output Mode)

Table 7. Pin Function Descriptions (Double Data-Rate CMOS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
A1	IN1P	AI	ADC Driver Noninverting Input, Channel 1.
A2	AIN1N	AI	ADC Inverting Analog Input, Channel 1.
A3	AIN1P	AI	ADC Noninverting Analog Input, Channel 1.
A4, C5, E2, E3, E8, F5, G4, H1	GND	P	Ground Reference for VCC, VDD, and OVDD.
A5	SENSE	AI	Internal Reference. Connect to ground to select the internal reference or apply 0.625 V to this pin to provide a 1 V p-p input range. Connect to VDD to select a 2 V p-p input range.
A7, A9, B6, B8, C7, C9, D3, D6, E7, F7, F9, G7, G9, H6, H8	DNC	NC	Do Not Connect. Do not connect anything on this pin.
B1	IN1N	AI	ADC Driver Inverting Input, Channel 1.
B2	OUT1N	AO	ADC Driver Inverting Output, Channel 1.
B3	OUT1P	AO	ADC Driver Noninverting output, Channel 1.
B4, H4	VDD	P	Power-Supply Pin of the ADC. VDD has two 0.1 µF decoupling capacitors.
B5	VREF	AO	Reference Voltage Output. VREF is normally 1.25 V and has a built-in 2.2 µF bypass capacitor.
C1	$\overline{\text{PD1}}$	P	Power-Down Pin, Channel 1. When this pin is floating or directly connected to VCC, the Channel 1 ADC driver is in normal (active) operating mode. When this pin is connected to GND, the Channel 1 ADC driver is in a low-power shutdown state with high-Z outputs.
C2	VOCM1I	AI	ADC Driver, Channel 1 Common-Mode Voltage, Channel 1.
C3	VOCM1O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 1.
C4, F4	VCC	P	ADC Driver Power Supply. VCC has two 0.1 µF decoupling capacitors.
D1	PAR/$\overline{\text{SER}}$	P	Programming Mode Selection Pin. Connect this pin to ground to enable the serial programming mode. $\overline{\text{CS}}$, SCK, SDI, and SDO together become a serial interface that controls the analog-to-digital operating modes. Connect PAR/$\overline{\text{SER}}$ to VDD to enable the parallel programming mode where $\overline{\text{CS}}$, SCK, SDI, and SDO become parallel logic inputs that control a reduced set of the analog-to-digital operating modes. PAR/$\overline{\text{SER}}$ must be connected directly to ground or VDD, and not be driven by a logic signal.
D2	OF2_1	DO	Overflow/Underflow Digital Output. OF2_1 is high when an overflow or underflow has occurred. The overflow and underflow for both channels are multiplexed onto this pin. Channel 2 appears when CLKOUT+ is low, and Channel 1 appears when CLKOUT+ is high.
D4	SDO	DO/DI	Serial Interface Data Output or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDO is the optional serial interface data output. Data on SDO

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions (Double Data-Rate CMOS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
			is read back from the serial programming mode registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2 kΩ pull-up resistor to 1.8 V to 3.3 V. If readback from the serial programming mode registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDO can be used together with SDI to power down the device (see Table 11). When used as an input, SDO can be driven with 1.8 V to 3.3 V logic through a 1 kΩ series resistor.
D5	SCK	DI	Serial Interface Clock Input or Digital Output Mode Control. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SCK controls the digital output mode (see Table 11). SCK can be driven with 1.8 V to 3.3 V logic.
D7, B9, C8, A8, B7, C6, A6	D1_0_1, D1_2_3, D1_4_5, D1_6_7, D1_8_9, D1_10_11, D1_12_13	DO	Channel 1 Double Data-Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT+ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT+ is high.
D8	OVDD	DO	ADC Output-Driver Power Supply. OVDD has a 0.1 µF decoupling capacitor.
D9	CLKOUT+	DO	Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT+. The phase of CLKOUT+ can also be delayed relative to the digital outputs by programming the serial programming mode registers.
E1	$\overline{\text{PD2}}$	AO	Power-Down Pin, Channel 2. When this pin is floating or directly connected to VCC, the Channel 2 ADC driver is in the normal (active) operating mode. When this pin is connected to GND, the Channel 2 ADC driver is in a low-power shutdown state with high-Z outputs.
E4	$\overline{\text{CS}}$	DI	Serial Interface Chip-Select Input or Clock Duty-Cycle Stabilizer Control. In serial programming mode, (PAR/$\overline{\text{SER}}$ = 0 V), $\overline{\text{CS}}$ is the serial interface chip-select input. When $\overline{\text{CS}}$ is low, SCK is enabled for shifting data on SDI into the serial programming mode registers. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), $\overline{\text{CS}}$ controls the clock duty-cycle stabilizer (see Table 11). $\overline{\text{CS}}$ can be driven with 1.8 V to 3.3 V logic.
E5	SDI	DI	Serial Interface Data Input or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDI Is the serial interface data input. Data on SDI is clocked into the serial programming mode registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDI can be used together with SDO to power down the device (see Table 11). SDI can be driven with 1.8 V to 3.3 V logic.
E9	CLKOUT−	DO	Inverted Version of CLKOUT+.
F1	IN2P	AI	ADC Driver Noninverting input, Channel 2.
F2	VOCM2I	AI	ADC Driver, Channel 2 Common-Mode Voltage.
F3	VOCM2O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 2.
G1	IN2N	AI	ADC Driver Inverting Input, Channel 2.
G2	OUT2N	AO	ADC Driver Inverting Output, Channel 2.
G3	OUT2P	AO	ADC Driver Noninverting Output, Channel 1.
G5	ENC−	DI	Encode Complement Input. Conversion starts on the falling edge. Connect ENC− to GND for single-ended encode mode.
H2	AIN2N	AI	ADC Inverting Analog Input, Channel 2.
H3	AIN2P	AI	ADC Noninverting Analog Input, Channel 2.
H5	ENC+	DI	Encode Input. Conversion starts on the rising edge.
H7, H9, G8, G6, F8, F6, E6	D2_0_1, D2_2_3, D2_4_5, D2_6_7, D2_8_9, D2_10_11, D2_12_13	DO	Channel 2 Double Data-Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT+ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT+ is high.

[1] AI is analog input, AO is analog output, P is power, NC is no connect, DI is digital input, and DO is digital output.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

DOUBLE DATA-RATE LVDS OUTPUT MODE

ADAQ8092
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9
A	IN1P	AIN1N	AIN1P	GND	SENSE	D1_12_13+	D1_10_11–	D1_6_7+	D1_4_5–
B	IN1N	OUT1N	OUT1P	VDD	VREF	D1_12_13–	D1_8_9+	D1_6_7–	D1_2_3+
C	$\overline{\text{PD1}}$	VOCM1I	VOCM1O	VCC	GND	D1_10_11+	D1_8_9–	D1_4_5+	D1_2_3–
D	PAR/$\overline{\text{SER}}$	OF2_1+	OF2_1–	SDO	SCK	D1_0_1–	D1_0_1+	OVDD	CLKOUT+
E	$\overline{\text{PD2}}$	GND	GND	$\overline{\text{CS}}$	SDI	D2_12_13+	D2_12_13–	GND	CLKOUT–
F	IN2P	VOCM2I	VOCM2O	VCC	GND	D2_10_11+	D2_10_11–	D2_8_9+	D2_8_9–
G	IN2N	OUT2N	OUT2P	GND	ENC–	D2_6_7+	D2_6_7–	D2_4_5+	D2_4_5–
H	GND	AIN2N	AIN29	VDD	ENC+	D2_0_1–	D2_0_1+	D2_2_3–	D2_2_3+

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Figure 9. Pin Configuration (Double Data-Rate LVDS Output Mode)

Table 8. Pin Function Descriptions (Double Data-Rate LVDS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
A1	IN1P	AI	ADC Driver Noninverting Input, Channel 1.
A2	AIN1N	AI	ADC Inverting Analog Input, Channel 1.
A3	AIN1P	AI	ADC Noninverting Analog Input, Channel 1.
A4, C5, E2, E3, E8, F5, G4, H1	GND	P	Ground Reference for VCC, VDD, and OVDD.
A5	SENSE	AI	Internal Reference. Connect to ground to select the internal reference or apply 0.625 V to this pin to provide a 1 V p-p input range. Connect to VDD to select a 2 V p-p input range.
B1	IN1N	AI	ADC Driver Inverting Input, Channel 1.
B2	OUT1N	AO	ADC Driver Inverting Output, Channel 1.
B3	OUT1P	AO	ADC Driver Noninverting output, Channel 1.
B4, H4	VDD	P	Power-Supply Pin of the ADC. VDD has two 0.1 µF decoupling capacitors.
B5	VREF	AO	Reference Voltage Output. VREF is normally 1.25 V and has a built-in 2.2 µF bypass capacitor.
C1	$\overline{\text{PD1}}$	P	Power-Down Pin, Channel 1. When this pin is floating or directly connected to VCC, the Channel 1 ADC driver is in normal (active) operating mode. When this pin is connected to GND, the Channel 1 ADC driver is in a low-power shutdown state with high-Z outputs.
C2	VOCM1I	AI	ADC Driver, Channel 1 Common-Mode Voltage, Channel 1.
C3	VOCM1O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 1.
C4, F4	VCC	P	ADC Driver Power Supply. VCC has two 0.1 µF decoupling capacitors.
D1	PAR/$\overline{\text{SER}}$	P	Programming Mode Selection Pin. Connect this pin to ground to enable the serial programming mode. $\overline{\text{CS}}$, SCK, SDI, and SDO together become a serial interface that controls the analog-to-digital operating modes. Connect PAR/$\overline{\text{SER}}$ to VDD to enable the parallel programming mode where $\overline{\text{CS}}$, SCK, SDI, and SDO become parallel logic inputs that control a reduced set of the analog-to-digital operating modes. PAR/$\overline{\text{SER}}$ must be connected directly to ground or VDD, and not be driven by a logic signal.
D2, D3	OF2_1+, OF2_1−	DO	Overflow/Underflow Digital Outputs. OF2_1+ is high when an overflow or underflow has occurred. The overflow and underflow for both channels are multiplexed onto OF2_1+. Channel 2 appears when CLKOUT+ is low, and Channel 1 appears when CLKOUT+ is high.
D4	SDO	DO/DI	Serial Interface Data Output or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDO is the optional serial interface data output. Data on SDO is read back from the serial programming mode registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2 kΩ pull-up resistor to 1.8 V to 3.3 V. If readback from the serial programming mode

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 8. Pin Function Descriptions (Double Data-Rate LVDS Output Mode)

Pin No.	Mnemonic	Type[1]	Description
			registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDO can be used together with SDI to power down the device (see Table 11). When used as an input, SDO can be driven with 1.8 V to 3.3 V logic through a 1 kΩ series resistor.
D5	SCK	DI	Serial Interface Clock Input or Digital Output Mode Control. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SCK is the serial interface clock input. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SCK controls the digital output mode (see Table 11). SCK can be driven with 1.8 V to 3.3 V logic.
D6, D7, C9, B9, A9, C8, B8, A8, C7, B7, A7, C6, B6, A6	D1_0_1−, D1_0_1+, D1_2_3−, D1_2_3+, D1_4_5−, D1_4_5+, D1_6_7−, D1_6_7+, D1_8_9−, D1_8_9+, D1_10_11−, D1_10_11+, D1_12_13−, D1_12_13+	DO	Channel 1 Double Data-Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT+ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT+ is high.
D8	OVDD	DO	Digital Output-Driver Power Supply. This pin has a 0.1 µF internal decoupling capacitor.
D9	CLKOUT+	DO	Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT+. The phase of CLKOUT+ can also be delayed relative to the digital outputs by programming the serial programming mode registers.
E1	$\overline{\text{PD2}}$	AO	Power-Down Pin, Channel 2. When this pin is floating or directly connected to VCC, the Channel 2 ADC driver is in the normal (active) operating mode. When this pin is connected to GND, the Channel 2 ADC driver is in a low-power shutdown state with high-Z outputs.
E4	$\overline{\text{CS}}$	DI	Serial Interface Chip-Select Input or Clock Duty-Cycle Stabilizer Control. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), $\overline{\text{CS}}$ is the serial interface chip-select input. When $\overline{\text{CS}}$ is low, SCK is enabled for shifting data on SDI into the serial programming mode registers. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), $\overline{\text{CS}}$ controls the clock duty-cycle stabilizer (see Table 11). $\overline{\text{CS}}$ can be driven with 1.8 V to 3.3 V logic.
E5	SDI	DI	Serial Interface Data Input or Power-Down Pin. In serial programming mode (PAR/$\overline{\text{SER}}$ = 0 V), SDI Is the serial interface data input. Data on SDI is clocked into the serial programming mode registers on the rising edge of SCK. In parallel programming mode (PAR/$\overline{\text{SER}}$ = VDD), SDI can be used together with SDO to power down the device (see Table 11). SDI can be driven with 1.8 V to 3.3 V logic.
E9	CLKOUT−	DO	Inverted Version of CLKOUT+.
F1	IN2P	AI	ADC Driver Noninverting Input, Channel 2.
F2	VOCM2I	AI	ADC Driver, Channel 2 Common-Mode Voltage.
F3	VOCM2O	AO	Common-Mode Bias Output, Nominally Equal to VDD/2. Used to bias the common mode of the analog inputs, Channel 2.
G1	IN2N	AI	ADC Driver Inverting Input, Channel 2.
G2	OUT2N	AO	ADC Driver Inverting Output, Channel 2.
G3	OUT2P	AO	ADC Driver Noninverting Output, Channel 1.
G5	ENC−	DI	Encode Complement Input. Conversion starts on the falling edge. Connect ENC− to GND for single-ended encode mode.
H2	AIN2N	AI	ADC Inverting Analog Input, Channel 2.
H3	AIN2P	AI	ADC Noninverting Analog Input, Channel 2.
H5	ENC+	DI	Encode Input. Conversion starts on the rising edge.
H6, H7, H8, H9, G9, G8, G7, G6, F9, F8, F7, F6, E7, E6	D2_0_1−, D2_0_1+, D2_2_3−, D2_2_3+, D2_4_5−, D2_4_5+, D2_6_7−, D2_6_7+, D2_8_9−, D2_8_9+, D2_10_11−, D2_10_11+, D2_12_13−, D2_12_13+	DO	Channel 2 Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT+ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT+ is high.

[1] AI is analog input, AO is analog output, P is power, DI is digital input, and DO is digital output.

TYPICAL PERFORMANCE CHARACTERISTICS

VCC = 3.3 V, VDD = OVDD = 1.8 V, internal reference, V_{IN1P} = V_{IN2P} = 0.1 V p-p (refer to Figure 33), SENSE = 0 V, f_S = 90 MSPS, all specifications are at T_{AMB} = 25°C, unless otherwise noted.

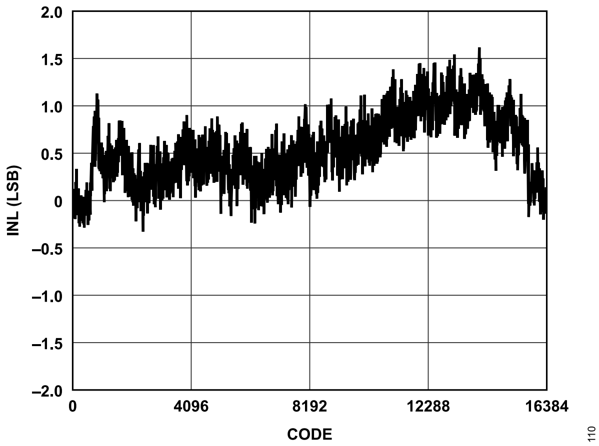

Figure 10. INL vs. Code

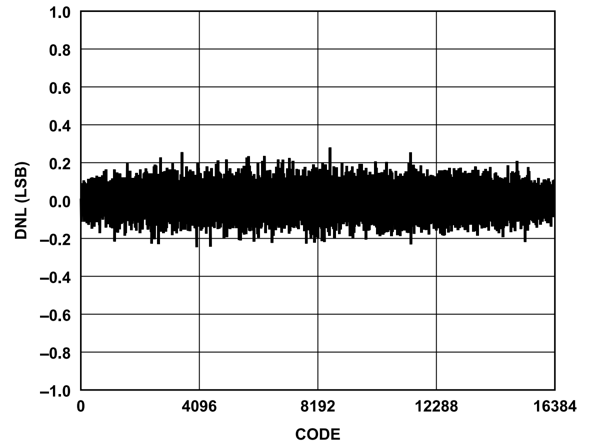

Figure 13. DNL vs. Code

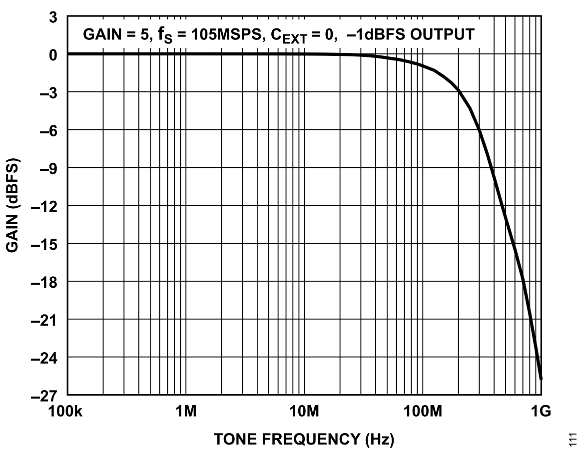

Figure 11. Frequency Response for G = 5

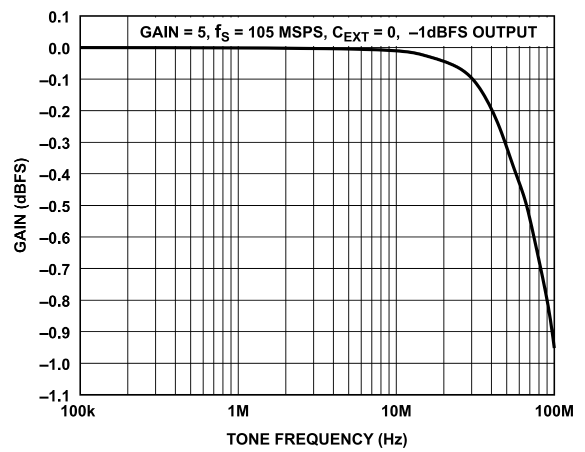

Figure 14. 0.1 dB Frequency Response for G = 5

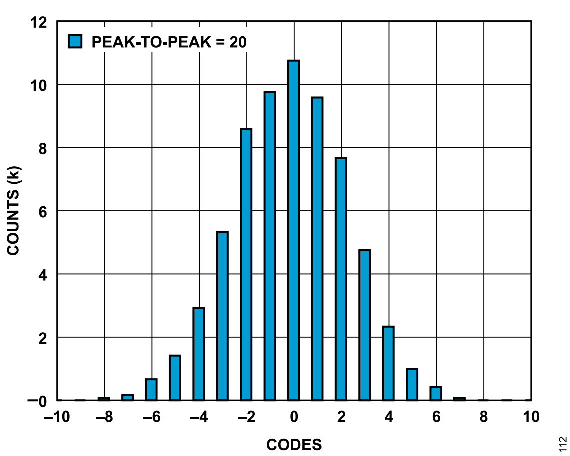

Figure 12. Histogram of a DC Input at the Code Center

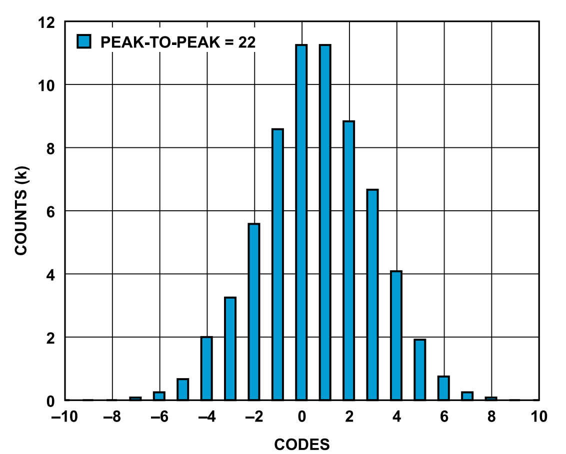

Figure 15. Histogram of a DC Input at the Code Transition

TYPICAL PERFORMANCE CHARACTERISTICS

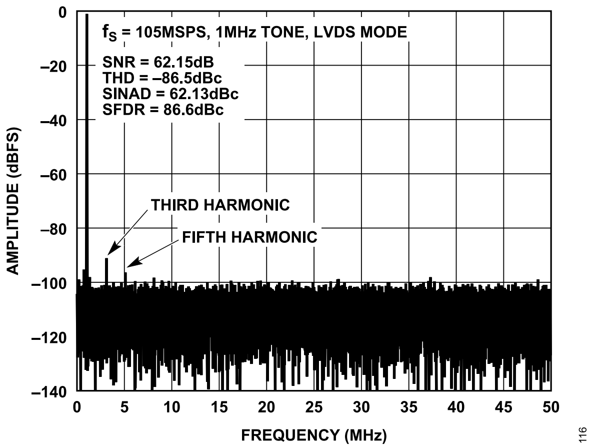

Figure 16. 1 MHz FFT

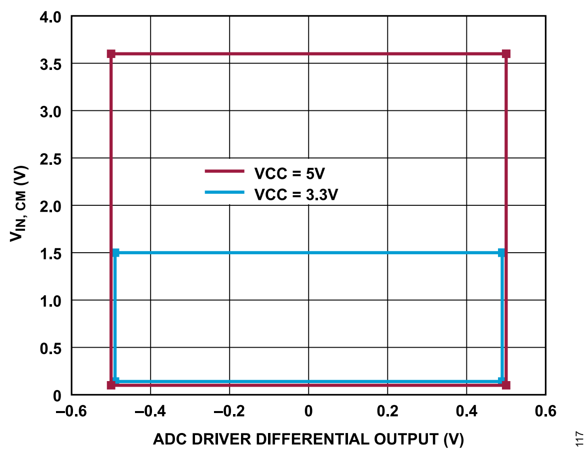

Figure 17. Input Common-Mode Voltage ($V_{IN,CM}$) vs. ADC Driver Differential Output

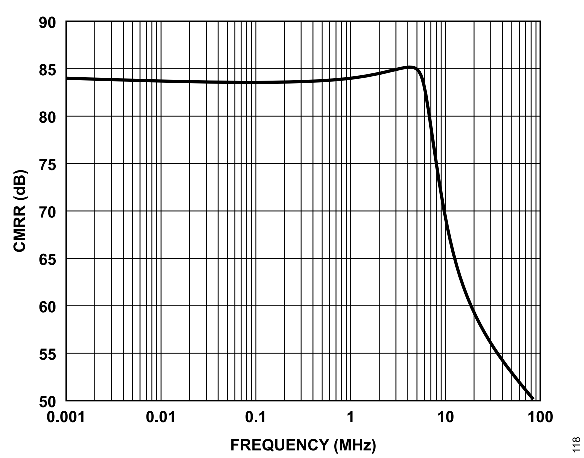

Figure 18. CMRR vs. Frequency

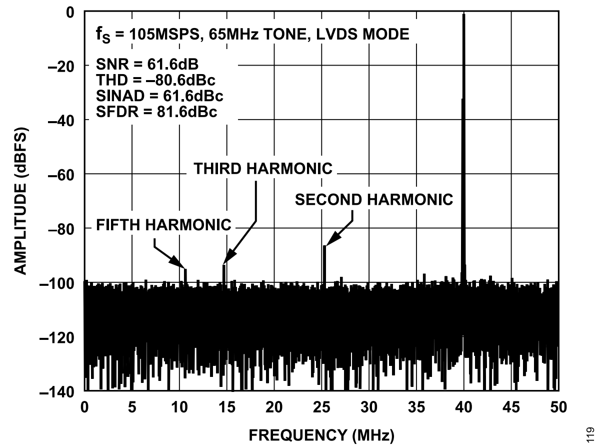

Figure 19. 65 MHz FFT

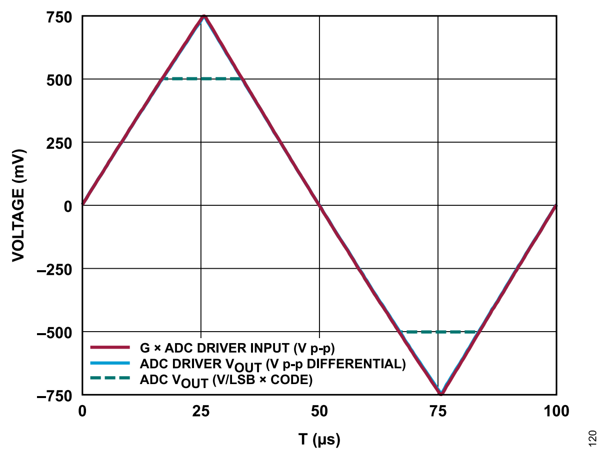

Figure 20. Output Overdrive Recovery

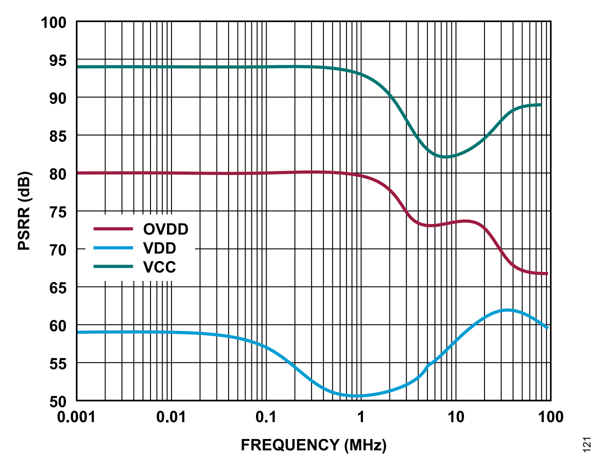

Figure 21. PSRR vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

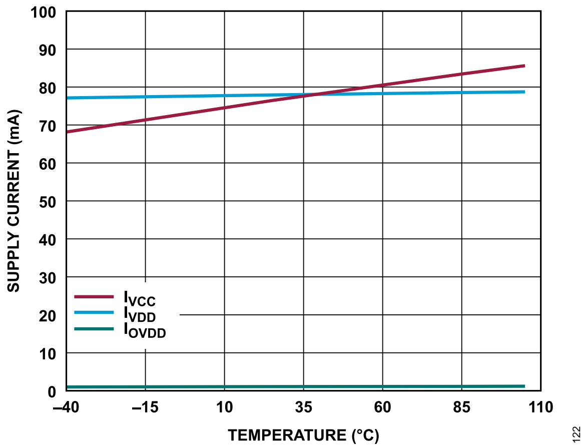

Figure 22. Supply Current vs. Temperature, Static Mode

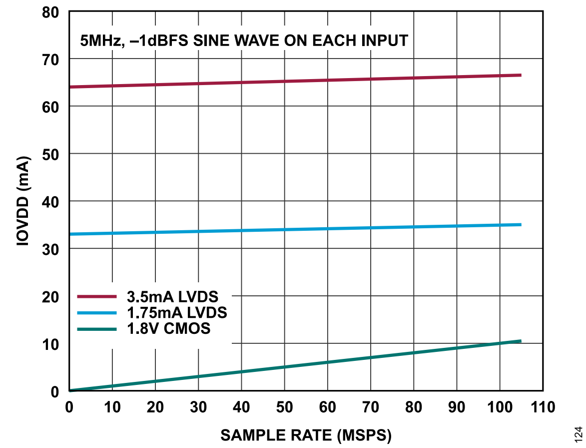

Figure 24. I_{OVDD} vs. Sample Rate

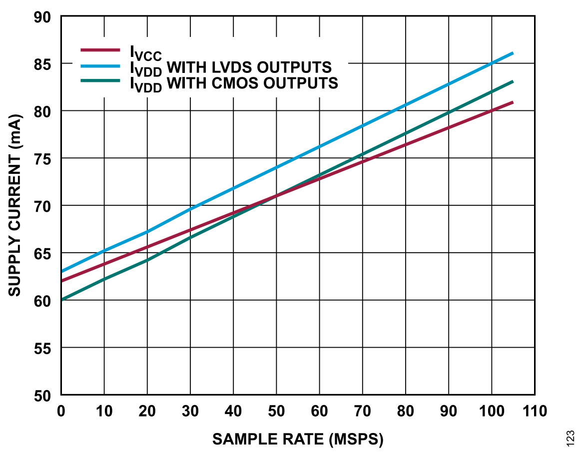

Figure 23. Supply Current vs. Sample Rate

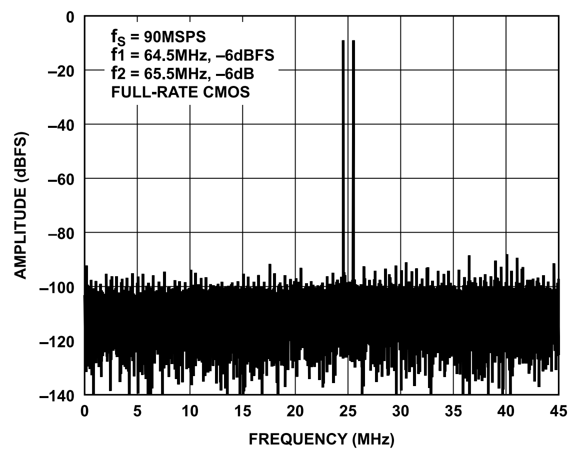

Figure 25. Two-Tone IMD

TERMINOLOGY

Integral Nonlinearity (INL)

INL is the deviation of each code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity (DNL)

In an ideal μModule, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error (OE)

Offset error is the difference between the ideal midscale input voltage and the actual voltage producing the midscale output code.

Offset Error Drift

Offset error drift is the ratio of offset error change due to a temperature change of 1°C and the full-scale code range as follows:

$$OE\ \ Drift = \left(OE_{T_{MAX}} - OE_{T_{MIN}}\right)/(T_{MAX} - T_{MIN}) \quad (1)$$

Gain Error

The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above nominal negative full scale. The last transition (from 011 … 10 to 011 … 11) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual levels of the last and first transitions from the ideal levels after the offset error is removed. The absolute accuracy of the reference used for the μModule can be a large source of error. Therefore, this error source is removed by measuring its value and using it to determine the actual full scale (FS_{ACTUAL}) for the gain error calculation.

This error is expressed in percentage as follows:

$$Gain\_Error\ (\%) = 100 \times (1 - FS_{ACTUAL}/FS_{IDEAL}) \quad (2)$$

Dynamic Range

Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, f1 and f2, active devices with nonlinearities create distortion products at sum and difference frequencies of mf1 and nf2, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the secondorder terms include (f1 + f2) and (f1 – f2), and the third-order terms include (2f1 + f2), (2f1 – f2), (f1 + 2f2), and (f1 − 2f2). IMD is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. ENOB is related to SINAD as follows:

$$ENOB = (SINAD - 1.76)/6.02 \quad (3)$$

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the voltage applied at the common-mode input of the μModule to the output.

$$CMRR\ (\text{dB}) = 20\log(VCM_{\mu Module}/V_{\mu Module\_OUT}) \quad (4)$$

Power Supply Rejection Ratio (PSRR)

PSRR is the ratio of a small voltage change applied to a supply line of the μModule to the change in voltage measured at the μModule output.

$$PSRR\ (\text{dB}) = 20\log(\Delta Vs\_{\mu Module}/\Delta V_{\mu Module\_OUT}) \quad (5)$$

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CIRCUIT INFORMATION

The ADAQ8092 is a 14-bit, 105 MSPS, high-speed, dual-channel DAQ µModule solution. The device consists of a dual-channel differential ADC driver stage, a differential low-pass filter (LPF), and a dual-channel, simultaneously sampling ADC.

The LPF outputs and the ADC analog inputs are available on the OUTxP/OUTxN pins and on AINxP/AINxN pins, respectively.

Connecting the LPF outputs to the ADC inputs forms a complete signal chain. An external capacitor connected across the LPF outputs adjusts the analog bandwidth, as shown in Figure 27.

The internal ADC driver and LPF can be bypassed by connecting an external ADC driver to the ADC analog inputs to achieve user-defined analog performance.

The ADAQ8092 operates on 3.3 V to 5 V analog and 1.8 V digital supplies. The digital outputs can be CMOS, double data-rate CMOS, or double data-rate LVDS.

REFERENCE

The ADAQ8092 has an internal 1.25 V voltage reference output with a built-in 2.2 µF bypass capacitor.

SENSE

Connecting SENSE to VDD selects the internal reference and 2 V input range to the ADC. Connecting SENSE to ground selects the internal reference and a 1 V input range to the ADC. An external reference between 0.625 V and 1.3 V applied to SENSE selects an input range of ±0.8 × V_{SENSE}.

When using the internal voltage reference, connect this pin to ground. When using the external voltage reference, apply a 0.625 V to provide the same analog-to-digital input range (1 V p-p).

ANALOG INPUTS

ADC Driver Inputs

The internal ADC driver of each channel is set to a differential gain of 30 by a 300 Ω feedback resistor and a 10 Ω gain resistor. For gains lower than 30, connect an external resistor (R_{EXT}) in series with each input (IN1P, IN1N, IN2P, IN2N).

The full-scale output amplitude of the internal ADC driver must not exceed 1 V p-p differential when the SENSE input is at ground to limit the maximum signal input amplitude to (R_{EXT} + 10)/300 V p-p differential.

With VCC = 5 V and SENSE connected to VDD, the full-scale ADC driver output is 2 V p-p differential, setting the maximum input amplitude to (R_{EXT} + 10)/150 V p-p differential.

ADC Analog Inputs

The analog inputs are differential CMOS sample-and-hold circuits, as shown in Figure 26. Drive these inputs differentially around a common-mode voltage set by VOCM1I and VOCM2I, nominally set to VDD/2. The inputs are sampled simultaneously by a shared encode circuit.

In Figure 26, $C_{PARASITIC}$ is the parasitic capacitance, R_{ON} is the on resistance, and C_{SAMPLE} is the sampling capacitance.

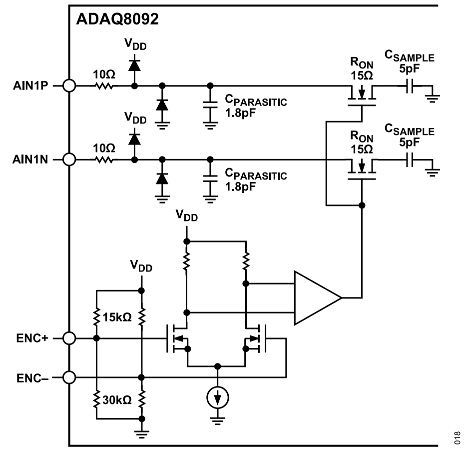

Figure 26. ADC Analog Input Equivalent Circuit

LOW-PASS FILTER

The internal LPF consists of 40 Ω resistors in series with each ADC driver output and a 4.7 pF capacitor across the ADC inputs to set the maximum signal bandwidth at the ADC inputs to 186 MHz when the input is set to a single-ended gain of 5. An external capacitor, C_{EXT}, connected between OUT1x and OUT2x lowers the signal bandwidth. See Figure 27 .

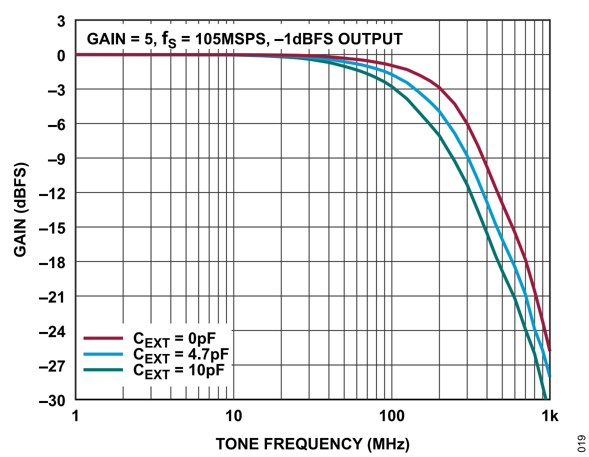

Figure 27. Gain vs. Tone Frequency at Selected C_{EXT} Values, for Gain = 5

ENCODE INPUT

The signal quality of the encode inputs strongly affects the analog-to-digital noise performance. The encode inputs must be treated as

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analog signals and not be routed next to digital traces on the circuit board.

There are two modes of operation for the encode inputs: differential encode mode and single-ended encode mode.

Differential encode mode is recommended for sinusoidal, PECL, or LVDS encode inputs. The encode inputs are internally biased to 1.2 V through 10 kΩ equivalent resistance. The encode inputs can be driven higher than VDD, and the common-mode range is from 1.1 V to 1.6 V. In the differential encode mode, ENC− must stay at least 200 mV above ground to avoid falsely triggering the single-ended encode mode. For optimal jitter performance, ENC+ and ENC− must have fast rise and fall times.

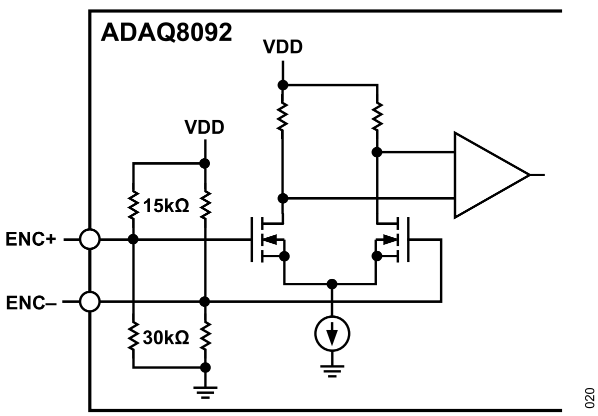

Figure 28. Equivalent Encode Input for Differential Encode Mode

Single-ended encode mode is recommended for CMOS encode inputs. To select this mode, ENC− is connected to ground and ENC+ is driven with a square-wave encode input. ENC+ can be driven higher than VDD so that 1.8 V to 3.3 V CMOS logic levels can be used. The ENC+ threshold is 0.9 V. For optimal jitter performance, ENC+ must have fast rise and fall times. If the encode signal is turned off, connected to GND, or drops below approximately 500 kHz, the analog-to-digital core automatically enters nap mode.

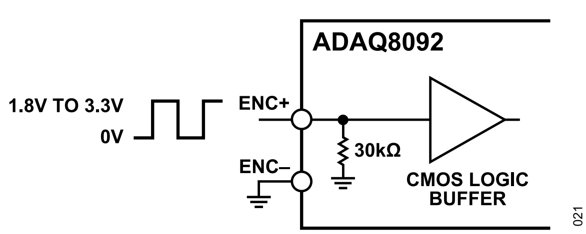

Figure 29. Equivalent Encode Input for Single-Ended Encode Mode

CLOCK DUTY-CYCLE STABILIZER

For optimal performance, the encode signal must have a 50% (±5%) duty cycle. If the optional clock duty-cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty-cycle stabilizer maintains a constant 50% internal duty cycle. If the encode signal changes frequency, the duty-cycle stabilizer circuit requires 100 clock cycles to lock onto the input clock. The duty-cycle stabilizer is enabled by the timing register, Register A2 (serial programming mode), or by $\overline{\text{CS}}$ (parallel programming mode). For applications where the sample rate needs to be changed quickly, the clock duty-cycle stabilizer can be disabled. If the duty-cycle stabilizer is disabled, ensure that the sampling clock has a 50% (±5%) duty cycle. Do not use the duty-cycle stabilizer below 5 MSPS.

OUTPUT MODES

The ADAQ8092 has three different output modes that can be used. The output mode is set by the output mode register, Register A3 (serial programming mode), or by SCK (parallel programming mode). Note that double data rate CMOS cannot be selected in the parallel programming mode.

Full Data Rate CMOS Mode

The data outputs, overflow, and the data output clocks have CMOS output levels. The outputs is powered by OVDD, which can range from 1.1 V to 1.9 V, allowing 1.2 V through 1.8 V CMOS logic outputs.

For optimal performance, the digital outputs must drive minimal capacitive loads. If the load capacitance is larger than 10 pF, a digital buffer must be used.

Double Data Rate CMOS Mode

In this mode, two data bits are multiplexed and output on each data pin, which reduces the number of digital lines by 15, simplifying board routing and reducing the number of input pins needed to receive the data. The data outputs, overflow, and the data output clocks have CMOS output levels. The outputs is powered by OVDD, which can range from 1.1 V to 1.9 V, allowing 1.2 V through 1.8 V CMOS logic outputs. Note that the overflow for both ADC channels is multiplexed onto OF2_1.

For optimal performance, the digital outputs must drive minimal capacitive loads. If the load capacitance is larger than 10 pF, a digital buffer must be used.

Double Data-Rate LVDS Mode

In this mode, two data bits are multiplexed and output on each differential output pair. There are seven LVDS output pairs per ADC channel for the digital output data. The overflow and the data output clock each have an LVDS output pair. Note that the overflow for

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both ADC channels in multiplexed onto the OF2_1+/OF2_1− output pair.

By default, the outputs are the standard LVDS levels: 3.5 mA output current and a 1.25 V output common-mode voltage. An external 100 Ω differential termination resistor is required for each LVDS output pair. The termination resistors must be located as close as possible to the LVDS receiver.

In addition, an optional internal 100 Ω termination resistor can be enabled by serially programming the output mode register, Register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output-driver current is doubled to maintain the same output-voltage swing.

The output current can be adjusted by serially programming the output mode register, Register A3. Available current levels are 1.75 mA, 2.1 mA, 2.5 mA, 3.0 mA, 3.5 mA, 4.0 mA, and 4.5 mA.

The outputs are powered by OVDD and must be 1.8 V.

OVERFLOW BIT

The overflow output bit is a bit that shows the condition of the analog input. If the overflow output bit is high, the analog input is either overranged or underranged. This bit has the same pipeline latency as the data bits. In full rate CMOS mode, each ADC channel has its own overflow pin (OF1 for Channel 1, OF2 for Channel 2). In DDR CMOS or DDR LVDS mode, the overflow for both ADC channels is multiplexed onto the OF2_1 output.

PHASE SHIFTING THE OUTPUT CLOCK

In full rate CMOS mode, the data output bits normally change at the same time as the falling edge of CLKOUT+. Therefore, the rising edge of CLKOUT+ can be used to latch the output data. In double data-rate CMOS and LVDS modes, the data output bits normally change at the same time as the falling and rising edges of CLKOUT+. To allow adequate setup and hold time when latching the data, the CLKOUT+ signal may need to be phase shifted relative to the data output bits. Most field-programmable gate arrays (FPGAs) have this phase shifting feature. The FPGA is generally the best place to adjust the timing.

Phase shifting the CLKOUT+/CLKOUT– signals can also be implemented by serially programming the timing register, Register A2. The output clock can be shifted by 0°, 45°, 90°, or 135°. To use the phase shifting feature, the clock duty-cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT+ and CLKOUT– independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (see Figure 30).

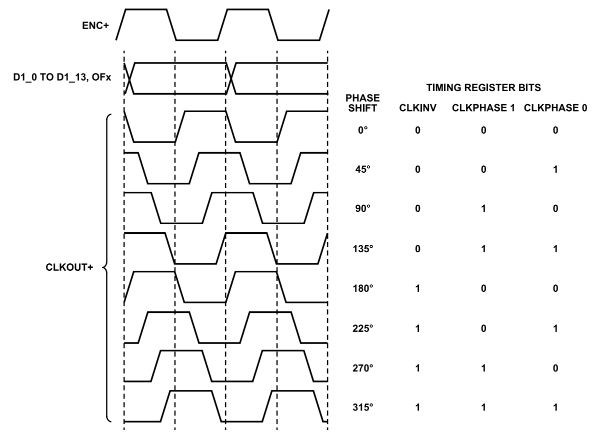

Figure 30. Phase Shifting CLKOUT+

DATA FORMAT

The ADAQ8092 data output format can be either offset binary or twos complement format. The default data output format is offset binary. The twos complement format can be selected by serially programming mode the data format register, Register A4.

Table 9. Input Voltage vs. Output Codes

ADC Input Voltage (V)	OFx	D13 to D0 (Offset Binary)	D13 to D0 (Twos Complement)
>0.500000	1	11 1111 1111 1111	01 1111 1111 1111
+0.499938	0	11 1111 1111 1111	01 1111 1111 1111
+0.499877	0	11 1111 1111 1110	01 1111 1111 1110
+0.000061	0	10 0000 0000 0001	00 0000 0000 0001
+0.000000	0	10 0000 0000 0000	00 0000 0000 0000
−0.000061	0	01 1111 1111 1111	11 1111 1111 1111
−0.000122	0	01 1111 1111 1110	11 1111 1111 1110
−0.499938	0	00 0000 0000 0001	10 0000 0000 0001
−0.500000	0	00 0000 0000 0000	10 0000 0000 0000
≤−0.50000	1	00 0000 0000 0000	10 0000 0000 0000

DIGITAL OUTPUT RANDOMIZER

Interference from the analog-to-digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized, which reduces the unwanted tone amplitude.

The digital output is randomized by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied. An exclusive-OR operation is applied between the LSB and all other bits. The LSB, OFx, and CLKOUT± outputs are not affected. The output randomizer is enabled by serially programming the data format register, Register A4.

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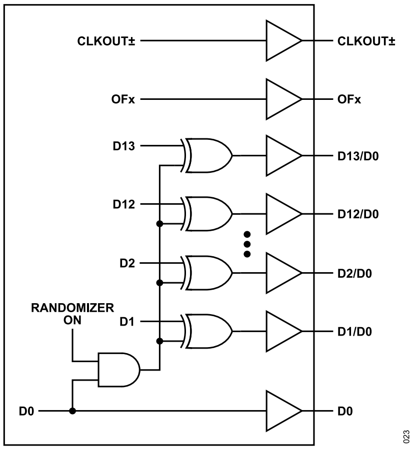

Figure 31. Functional Equivalent of Digital Output Randomizer

ALTERNATE BIT POLARITY

Another feature that reduces digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12), OFx, and CLKOUT± are not affected. This node can reduce digital currents in the circuit board ground plane and reduce digital noise.

When there is a very small signal at the input of the analog-to-digital core that is centered around midscale, the digital outputs toggle between mostly 1s and mostly 0s. This simultaneous switching of most of the bits causes large currents in the ground plane. By inverting every other bit, the alternate bit polarity mode makes half of the bits transition high while half of the bits transition low, which cancels current flow in the ground plane, reducing the digital noise.

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13). The alternate bit polarity and digital output randomizer functions can be enabled or disabled independently of each other. The alternate bit polarity mode is enabled by serially programming the data format register, Register A4.

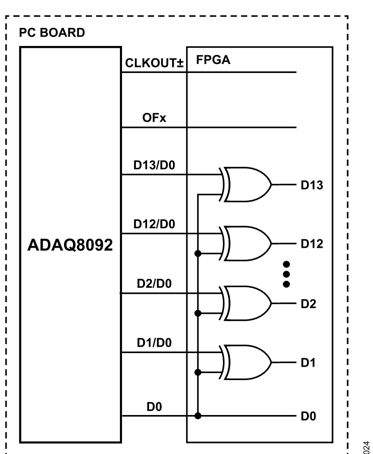

Figure 32. Unrandomizing a Randomized Digital Output Signal

DIGITAL OUTPUT TEST PATTERNS

The ADAQ8092 can force the ADC data outputs (overflow, D13 to D0) to known values that can be used as a quick check of the device functionality by serially programming the data format register, Register A4.

Table 10. Digital Output Test Pattern Settings in Register A4

Pattern	Description
All 1s	All outputs are 1.
All 0s	All outputs are 0.
Alternating	Outputs change from all 1s to all 0s on alternating samples.
Checkerboard	Output change from 101010101010101 to 010101010101010 on alternating samples.

When enabled, the test patterns override all other formatting modes: twos complement, randomizer, and alternate bit polarity.

OUTPUT DISABLE

The ADAQ8092 can disable its digital outputs (data outputs, overflow, CLKOUT±) by serially programming the output mode register, Register A3. When the outputs are disabled, both channels are put into either sleep mode or nap mode.

SLEEP MODE

In sleep mode and power-down mode, the ADAQ8092 analog-to-digital core and internal reference circuits are powered down, resulting in 1 mW power consumption (P_{ADC}). The amount of time required to recover from sleep mode is >2 ms.

Sleep mode can be enabled through the power-down register, Register A1 (serial programming mode), or by SDI and SDO (parallel programming mode).

NAP MODE

In nap mode, the ADAQ8092 analog-to-digital core is powered down while the internal reference circuits stay active, allowing faster wake-up than from sleep mode. The amount of time required to recover from nap mode is at least 100 clock cycles. If the application demands higher precision DC settling, allow an additional 50 μs so that the on-chip references can settle from the slight temperature shift caused by the change in supply current as the analog-to-digital core leaves nap mode. Either Channel 2 or both channels can be placed in nap mode. It is not possible to have Channel 1 in nap mode and Channel 2 operating normally.

This mode can be enabled through the power-down register, Register A1 (serial programming mode), or by SDI and SDO (parallel programming mode).

SERIAL PROGRAMMING MODE

To use the serial programming mode, connect PAR/$\overline{SER}$ to ground. The $\overline{CS}$, SCK, SDI, and SDO pins become a serial interface that programs the analog-to-digital serial programming mode registers,

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A0 to A4. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

A serial-data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/W bit. The next seven bits are the address of the register. The final eight bits are the register data.

If the R/$\overline{W}$ bit is low, serial data (D7:D0) is written to the register whose address is specified by Bits[A4:A0]. If the R/$\overline{W}$ bit is high, data in the selected register is read back on the SDO pin (see the Timing Diagram section). During a readback command, the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200 Ω impedance. If register data is read back through SDO, an external 2 kΩ pull-up resistor is required. If serial data is only written and readback is not needed, SDO can be left floating and no pull-up resistor is needed.

PARALLEL PROGRAMMING MODE

To use the parallel programming mode, tie PAR/$\overline{SER}$ to VDD. The $\overline{CS}$, SCK, SDI, and SDO pins are binary logic inputs that set certain operating modes. These pins can be tied to VDD or ground, or driven by 1.8 V, 2.5 V, or 3.3 V CMOS logic. When used as an input, SDO must be driven through a 1 kΩ series resistor. Table 11 shows the modes set by $\overline{CS}$, SCK, SDI, and SDO, with PAR/$\overline{SER}$ = VDD.

Table 11. Parallel Programming Mode Control Bits

Pin	Description
$\overline{CS}$	Clock duty cycle stabilizer control bit 0 = clock duty cycle stabilizer off 1 = clock duty cycle stabilizer on
SCK	Digital output mode control bit 0 = full rate CMOS output mode 1 = double data rate LVDS output mode (3.5 mA LVDS current, internal termination off)
SDI/SDO	Power-down control bit 00 = normal operation 01 = Channel 1 in normal operation, Channel 2 in nap mode 10 = Channel 1 and Channel 2 in nap mode 11 = sleep mode (entire device powered down)

SOFTWARE RESET

If serial programming is used, the serial programming mode registers must be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset, which resets all register data bits to Logic 0. To perform a software reset, Bit D7 in the reset register is written with a Logic 1. After the reset SPI write command is complete, Bit D7 is automatically set back to zero.

POWER-SUPPLY DECOUPLING

The ADAQ8092 features internal decoupling capacitors on the VCC, VDD, and OVDD pins.

POWER-UP SEQUENCING

When $\overline{PD1}$ and $\overline{PD2}$ are not used, but are tied to VCC, follow these steps:

1. Turn VCC on.
2. Wait approximately 500 ms.
3. Turn VDD on.

When $\overline{PD1}$ and $\overline{PD2}$ are active, follow these steps:

1. Keep $\overline{PD1}$ and $\overline{PD2}$ off and tied to GND.
2. Turn VCC and VDD on.
3. Wait approximately 500 ms.
4. Turn $\overline{PD1}$ and $\overline{PD2}$ on, and connect to VCC.

SERIAL PROGRAMMING MODE REGISTER MAP

REGISTER A0: RESET REGISTER (ADDRESS 0X00)

Table 12. Register A0: Reset Register (Address 0x00) Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
Reset	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]

[1] X means don't care.

Table 13. Reset Register Bit Descriptions

Bit(s)	Bit Name	Description
7	Reset	Software reset bit. 0 = not used. 1 = software reset. All serial programming mode registers are reset to 0x00. The ADC is momentarily placed in sleep mode. This bit is automatically set back to 0 at the end of the SPI write command. The reset register is write only. Data read back from the reset register is random.
[6:0]	Unused	Don't care bits.

REGISTER A1: POWER-DOWN REGISTER (ADDRESS 0X01)

Table 14. Register A1: Power-Down Register (Address 0x01) Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	PWROFF1	PWROFF0

[1] X means don't care.

Table 15. Power-Down Register Bit Descriptions

Bit(s)	Bit Name	Description
[7:2]	Unused	Don't care bits.
[1:0]	PWROFF[1:0]	Power-down control bits. 00 = normal operation. 01 = Channel 1 in normal operation, Channel 2 in nap mode. 10 = Channel 1 and Channel 2 in nap mode. 11 = sleep mode.

REGISTER A2: TIMING REGISTER (ADDRESS 0X02)

Table 16. Register A2: Timing Register (Address 0x02) Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
X[1]	X[1]	X[1]	X[1]	CLKINV	CLKPHASE1	CLKPHASE0	DCS

[1] X means don't care.

Table 17. Timing Register Bit Descriptions

Bit(s)	Bit Name	Description
[7:4]	Unused	Don't care bits.
3	CLKINV	Output clock invert bit. 0 = normal CLKOUT± polarity. 1 = inverted CLKOUT± polarity.
[2:1]	CLKPHASE[1:0]	Output clock phase delay bits. If the CLKOUT± phase delay feature is used, the clock duty-cycle stabilizer must also be turned on. 00 = no CLKOUT delay.

SERIAL PROGRAMMING MODE REGISTER MAP

Table 17. Timing Register Bit Descriptions

Bit(s)	Bit Name	Description
		01 = CLKOUT+/CLKOUT− delayed by 45° (clock period × 1/8). 10 = CLKOUT+/CLKOUT− delayed by 90° (clock period × 1/4). 11 = CLKOUT+/CLKOUT− delayed by 135° (clock period × 3/8).
0	DCS	Clock duty-cycle stabilizer bit. 0 = clock duty-cycle stabilizer off. 1 = clock duty-cycle stabilizer on.

REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 0X03)

Table 18. Register A3: Output Mode Register (Address 0x03) Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
X[1]	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE1	OUTMODE0

[1] X means don't care.

Table 19. Output Mode Register Bit Descriptions

Bit(s)	Bit Name	Description
7	Unused	Don't care bit.
[6:4]	ILVDS[2:0]	LVDS output current bits. 000 = 3.5 mA LVDS output-driver current. 001 = 4.0 mA LVDS output-driver current. 010 = 4.5 mA LVDS output-driver current. 011 = not used. 100 = 3.0 mA LVDS output-driver current. 101 = 2.5 mA LVDS output-driver current. 110 = 2.1 mA LVDS output-driver current. 111= 1.75 mA LVDS output-driver current.
3	TERMON	LVDS internal termination bit. 0 = internal termination off. 1 = internal termination on. LVDS output driver current is two times the current set by Bits[6:4] (ILVDSx).
2	OUTOFF	Output disable bit. 0 = digital outputs are enabled. 1 = digital outputs are disabled and have a high output impedance. If the digital outputs are disabled, the device must also be put in either sleep or nap mode (both channels).
[1:0]	OUTMODE[1:0]	Digital output mode control bits. 00 = full rate CMOS output mode. 01 = double data-rate LVDS output mode. 10 = double data-rate CMOS output mode. 11 = not used.

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 0X04)

Table 20. Register A4: Data Format Register (Address 0x04) Bit Map

D7	D6	D5	D4	D3	D2	D1	D0
X[1]	X[1]	OUTTEST2	OUTTEST1	OUTTEST0	ABP	RAND	TWOSCOMP

[1] X means don't care.

Table 21. Data Format Register Bit Descriptions

Bit(s)	Bit Name	Description
[7:6]	Unused	Don't care bits.

SERIAL PROGRAMMING MODE REGISTER MAP

Table 21. Data Format Register Bit Descriptions

Bit(s)	Bit Name	Description
[5:3]	OUTTEST[2:0]	Digital output test pattern bits. 000 = digital output test patterns off. 001 = all digital outputs = 0. 011 = all digital outputs = 1. 101 = checkerboard output pattern. OFx and D13 to D0 alternate between 1 01 0101 0101 0101 and 0 10 1010 1010 1010. 111= alternating output current. OFx and D13 to D0 alternate between 0 00 0000 0000 0000 and 1 11 1111 1111 1111. Other bit combinations are not used.
2	ABP	Alternate bit polarity mode control bit. 0 = alternate bit polarity mode off. 1 = alternate bit polarity mode on. Forces the output format to be offset binary.
1	RAND	Data output randomizer mode control bit. 0 = data output randomizer mode off. 1 = data output randomizer mode on.
0	TWOSCOMP	Twos complement mode control bit. 0 = offset binary data format. 1 = twos complement data format.

APPLICATIONS INFORMATION

Figure 33 shows an example of how to interface a single-ended IQ demodulator to the ADAQ8092. DC blocking capacitors at the ADAQ8092 input isolate the demodulator common-mode bias from the ADAQ8092. The input circuit of Figure 33 forms a high-pass filter with corner frequency (f_C) = 27.4 kHz. A 100 mV p-p signal with frequency > 27.4 kHz at VIN1 generates a 1 V p-p full scale at the ADC input.

Figure 34 shows an example of how to use a balun to interface a single-ended demodulator to the ADAQ8092. The input circuit of Figure 34 forms a high-pass filter with f_C = 33.5 kHz. A 100 mV p-p signal with frequency > 33.5 kHz at VIN1 generates a 1 V p-p full scale at the ADC input.

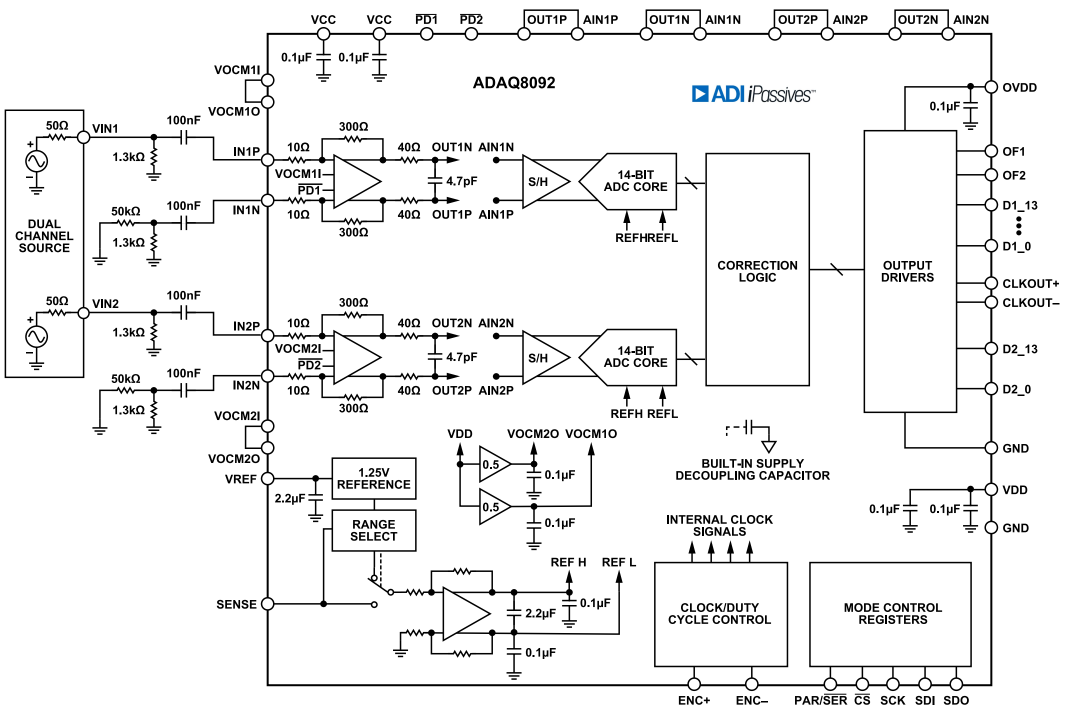

Figure 33. Dual-Channel, Single-Ended Input to the ADAQ8092

APPLICATIONS INFORMATION

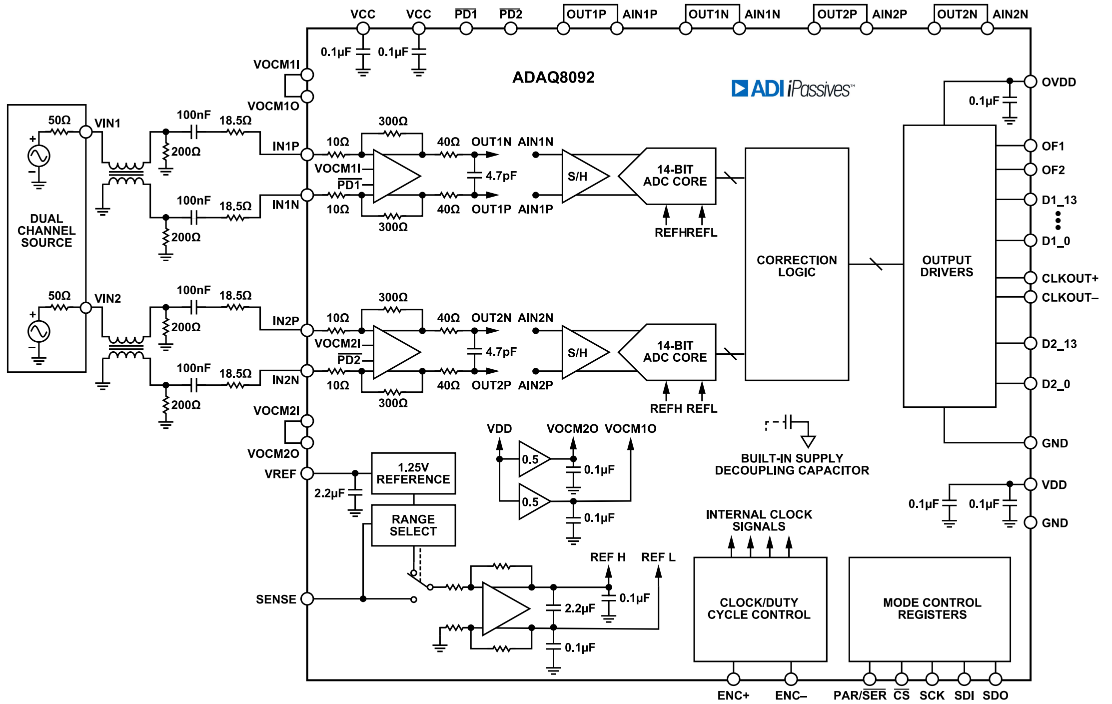

Figure 34. Dual-Channel, Differential Input to the ADAQ8092