

FEATURES

- Programmable audio processing engine
 - 192 kHz processing path
 - Biquad filters, limiters, volume controls, mixing
- Low latency, 24-bit ADCs and DACs
 - 102 dB SNR (signal through PGA and ADC with A-weighted filter)
 - 107 dB combined SNR (signal through DAC and headphone with A-weighted filter)
- Serial port sample rates from 8 kHz to 192 kHz
- 38 μ s analog-to-analog latency
- 4 single-ended analog inputs—configurable as microphone or line inputs
- Dual stereo digital microphone inputs
- Stereo analog audio output—single-ended or differential, configurable as either line output or headphone driver
- PLL supporting any input clock rate from 8 MHz to 27 MHz
- Full-duplex, asynchronous sample rate converters (ASRCs)
- Power supplies
 - Analog and digital I/O of 1.8 V to 3.3 V
 - Digital signal processing (DSP) core of 1.1 V to 1.8 V

- Low power (15 mW for typical noise cancelling solution)
- I²C and SPI control interfaces, self-boot from I²C EEPROM
- 7 MP pins supporting dual stereo digital microphone inputs, stereo PDM output, mute, DSP bypass, push-button volume controls, and parameter bank switching

APPLICATIONS

- Noise cancelling handsets, headsets, and headphones
- Bluetooth ANC handsets, headsets, and headphones
- Personal navigation devices
- Digital still and video cameras

GENERAL DESCRIPTION

The ADAU1772 is a codec with four inputs and two outputs that incorporates a digital processing engine to perform filtering, level control, signal level monitoring, and mixing. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise cancelling headsets. With the addition of just a few passive components, a crystal, and an EEPROM for booting, the ADAU1772 provides a complete headset solution.

FUNCTIONAL BLOCK DIAGRAM

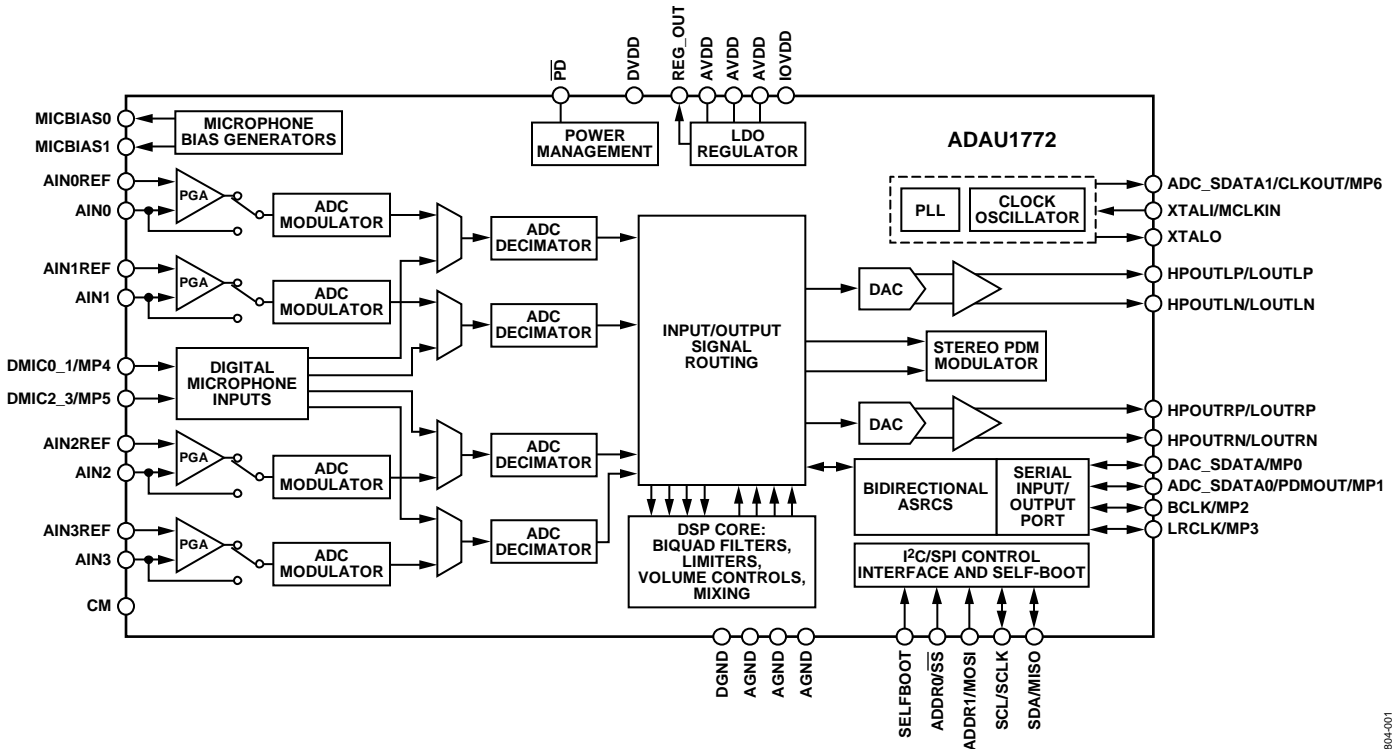


Figure 1.

Rev. C

Document Feedback

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REVISION HISTORY

3/14—Rev. B to Rev. C

| | |
|---|----|
| Changes to Figure 60 and Figure 62 Captions | 25 |
| Added Figure 64, Figure 65, Figure 66, Figure 67, Figure 68, and Figure 69, Renumbered Sequentially | 26 |
| Added Figure 70, and Figure 71 | 27 |

12/12—Rev. A to Rev. B

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8/12—Rev. 0 to Rev. A

| | |
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| Changes to Figure 69 | 31 |
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7/12—Revision 0: Initial Version

SPECIFICATIONS

Master clock = core clock = 12.288 MHz, serial input sample rate = 48 kHz, measurement bandwidth = 20 Hz to 20 kHz, word width = 24 bits, ambient temperature = 25°C, outputs line loaded with 10 kΩ.

ANALOG PERFORMANCE SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted. PLL disabled, direct master clock.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|--|-----|-----------|-----|-------|
| ANALOG-TO-DIGITAL CONVERTERS | | | | | |
| ADC Resolution | All ADCs | | 24 | | Bits |
| Digital Attenuation Step | | | 0.375 | | dB |
| Digital Attenuation Range | | | 95 | | dB |
| INPUT RESISTANCE | | | | | |
| Single-Ended Line Input | Gain settings do not include 10 dB gain from PGA_x_BOOST settings; this additional gain does not affect input impedance; PGA_POP_DISx = 1 0 dB gain | | 14.3 | | kΩ |
| PGA Inputs | −12 dB gain | | 32.0 | | kΩ |
| | 0 dB gain | | 20 | | kΩ |
| | +35.25 dB gain | | 0.68 | | kΩ |
| SINGLE-ENDED LINE INPUT | | | | | |
| Full-Scale Input Voltage | PGA_ENx = 0, PGA_x_BOOST = 0, PGA_POP_DISx = 1 Scales linearly with AVDD | | AVDD/3.63 | | V rms |
| | AVDD = 1.8 V | | 0.49 | | V rms |
| | AVDD = 1.8 V, 0 dBFS | | 1.38 | | V p-p |
| | AVDD = 3.3 V | | 0.90 | | V rms |
| | AVDD = 3.3 V, 0 dBFS | | 2.54 | | V p-p |
| Dynamic Range ¹ | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 97 | | dB |
| | AVDD = 3.3 V | | 102 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 94 | | dB |
| | AVDD = 3.3 V | | 99 | | dB |
| Signal-to-Noise Ratio (SNR) ² | | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 98 | | dB |
| | AVDD = 3.3 V | | 103 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 96 | | dB |
| | AVDD = 3.3 V | | 100 | | dB |
| Interchannel Gain Mismatch | | | 40 | | mdB |
| Total Harmonic Distortion + Noise (THD + N) | 20 Hz to 20 kHz, −1 dBFS | | | | |
| | AVDD = 1.8 V | | −90 | | dB |
| | AVDD = 3.3 V | | −94 | | dB |
| Offset Error | | | ±0.1 | | mV |
| Gain Error | | | ±0.2 | | dB |
| Interchannel Isolation | CM capacitor = 22 μF | | 100 | | dB |
| Power Supply Rejection Ratio | CM capacitor = 22 μF 100 mV p-p at 1 kHz | | 55 | | dB |
| SINGLE-ENDED PGA INPUT | | | | | |
| Full-Scale Input Voltage | PGA_ENx = 1, PGA_x_BOOST = 0 Scales linearly with AVDD | | AVDD/3.63 | | V rms |
| | AVDD = 1.8 V | | 0.49 | | V rms |
| | AVDD = 1.8 V, 0 dBFS | | 1.38 | | V p-p |
| | AVDD = 3.3 V | | 0.90 | | V rms |
| | AVDD = 3.3 V, 0 dBFS | | 2.54 | | V p-p |
| Dynamic Range ¹ | 20 Hz to 20 kHz, −60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 96 | | dB |
| | AVDD = 3.3 V | | 102 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 94 | | dB |
| | AVDD = 3.3 V | | 99 | | dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|--|-----|---|-----|---|
| Total Harmonic Distortion + Noise | 20 Hz to 20 kHz, -1 dBFS AVDD = 1.8 V AVDD = 3.3 V | | -88 -90 | | dB dB |
| Signal-to-Noise Ratio ² With A-Weighted Filter (RMS) | AVDD = 1.8 V AVDD = 3.3 V | | 96 102 | | dB dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V AVDD = 3.3 V | | 94 99 | | dB dB |
| PGA Gain Variation With -12 dB Setting | Standard deviation | | 0.05 | | dB |
| With +35.25 dB Setting | Standard deviation | | 0.15 | | dB |
| PGA Boost | PGA_x_BOOST | | 10 | | dB |
| PGA Mute Attenuation | PGA_MUTEx | | -65 | | dB |
| Interchannel Gain Mismatch | | | 0.005 | | dB |
| Offset Error | | | 0 | | mV |
| Gain Error | | | ±0.2 | | dB |
| Interchannel Isolation | | | 83 | | dB |
| Power Supply Rejection Ratio | CM capacitor = 22 µF, 100 mV p-p at 1 kHz | | 63 | | dB |
| MICROPHONE BIAS | MIC_ENx = 1 | | | | |
| Bias Voltage 0.65 × AVDD | AVDD = 1.8 V, MIC_GAINx = 1 AVDD = 3.3 V, MIC_GAINx = 1 | | 1.16 2.12 | | V V |
| 0.90 × AVDD | AVDD = 1.8 V, MIC_GAINx = 0 AVDD = 3.3 V, MIC_GAINx = 0 | | 1.63 2.97 | | V V |
| Bias Current Source | | | | 3 | mA |
| Output Impedance | | | 1 | | Ω |
| MICBIASx Isolation | MIC_GAINx = 0 MIC_GAINx = 1 | | 95 99 | | dB dB |
| Noise in the Signal Bandwidth ³ | AVDD = 1.8 V, 20 Hz to 20 kHz MIC_GAINx = 0 MIC_GAINx = 1 AVDD = 3.3 V, 20 Hz to 20 kHz MIC_GAINx = 0 MIC_GAINx = 1 | | 27 16 35 19 | | nV/√Hz nV/√Hz nV/√Hz nV/√Hz |
| DIGITAL-TO-ANALOG CONVERTERS | | | | | |
| DAC Resolution | All DACs | | 24 | | Bits |
| Digital Attenuation Step | | | 0.375 | | dB |
| Digital Attenuation Range | | | 95 | | dB |
| DAC SINGLE-ENDED OUTPUT | Single-ended operation, HPOUTLP and HPOUTRP pins | | | | |
| Full-Scale Output Voltage | Scales linearly with AVDD AVDD = 1.8 V AVDD = 1.8 V, 0 dBFS AVDD = 3.3 V AVDD = 3.3 V, 0 dBFS | | AVDD/3.4 0.53 1.5 0.97 2.74 | | V rms V rms V p-p V rms V p-p |
| Mute Attenuation | | | -72 | | dB |
| Dynamic Range ¹ With A-Weighted Filter (RMS) | Line output mode, 20 Hz to 20 kHz, -60 dB input AVDD = 1.8 V AVDD = 3.3 V | | 100 104 | | dB dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V AVDD = 3.3 V | | 97 101 | | dB dB |
| Signal-to-Noise Ratio ² With A-Weighted Filter (RMS) | Line output mode, 20 Hz to 20 kHz AVDD = 1.8 V AVDD = 3.3 V | | 100 104 | | dB dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V AVDD = 3.3 V | | 98 102 | | dB dB |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------------|---|-----|----------|-----|------------------|
| Interchannel Gain Mismatch | Line output mode | | 20 | | mdB |
| Total Harmonic Distortion + Noise | Line output mode, 20 Hz to 20 kHz, -1 dBFS | | | | dB |
| | AVDD = 1.8 V | | -93 | | dB |
| | AVDD = 3.3 V | | -94 | | dB |
| Gain Error | Line output mode | | ±0.1 | | dB |
| Dynamic Range ¹ | Headphone mode, 20 Hz to 20 kHz, -60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 100 | | dB |
| | AVDD = 3.3 V | | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 97 | | dB |
| | AVDD = 3.3 V | | 101 | | dB |
| Signal-to-Noise Ratio ² | Headphone mode, 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 100 | | dB |
| | AVDD = 3.3 V | | 104 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 98 | | dB |
| | AVDD = 3.3 V | | 102 | | dB |
| Interchannel Gain Mismatch | Headphone mode | | 50 | | mdB |
| Total Harmonic Distortion + Noise | Headphone mode, 20 Hz to 20 kHz, -1 dBFS | | | | |
| 32 Ω load | AVDD = 1.8 V, P _o = 6.7 mW | | -77 | | dB |
| | AVDD = 3.3 V, P _o = 22.4 mW | | -80 | | dB |
| 24 Ω load | AVDD = 1.8 V, P _o = 8.9 mW | | -76 | | dB |
| | AVDD = 3.3 V, P _o = 30 mW | | -79 | | dB |
| 16 Ω load | AVDD = 1.8 V, P _o = 13 mW | | -74 | | dB |
| | AVDD = 3.3 V, P _o = 44 mW | | -77 | | dB |
| Headphone Output Power | | | | | |
| 32 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 8.4 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 28.1 | | mW |
| 24 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 11.2 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 37.4 | | mW |
| 16 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 16.25 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 55.8 | | mW |
| Gain Error | Headphone mode | | ±0.1 | | dB |
| Offset Error | | | ±0.1 | | mV |
| Interchannel Isolation | 1 kHz, 0 dBFS input signal | | 100 | | dB |
| Power Supply Rejection Ratio | CM capacitor = 22 μF, 100 mV p-p at 1 kHz | | 70 | | dB |
| DAC DIFFERENTIAL OUTPUT | | | | | |
| Full-Scale Output Voltage | Differential operation | | AVDD/1.8 | | V _{rms} |
| | Scales linearly with AVDD | | | | |
| | AVDD = 1.8 V | | 1.0 | | V _{rms} |
| | AVDD = 1.8 V, 0 dBFS | | 2.58 | | V _{p-p} |
| | AVDD = 3.3 V | | 1.83 | | V _{rms} |
| | AVDD = 3.3 V, 0 dBFS | | 5.49 | | V _{p-p} |
| Mute Attenuation | | | -72 | | dB |
| Dynamic Range ¹ | Line output mode, 20 Hz to 20 kHz, -60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 104 | | dB |
| | AVDD = 3.3 V | | 107 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 101 | | dB |
| | AVDD = 3.3 V | | 105 | | dB |
| Signal-to-Noise Ratio ² | Line output mode, 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 105 | | dB |
| | AVDD = 3.3 V | | 108 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 102 | | dB |
| | AVDD = 3.3 V | | 105 | | dB |
| Interchannel Gain Mismatch | Line output mode | | 20 | | mdB |
| Total Harmonic Distortion + Noise | Line output mode, 20 Hz to 20 kHz, -1 dBFS | | | | dB |
| | AVDD = 1.8 V | | -96 | | dB |
| | AVDD = 3.3 V | | -96 | | dB |
| Gain Error | Line output mode | | | | % |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------------------------|--|-----|--------|-----|-------|
| Dynamic Range ¹ | Headphone mode, 20 Hz to 20 kHz, –60 dB input | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 104 | | dB |
| | AVDD = 3.3 V | | 107 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 102 | | dB |
| | AVDD = 3.3 V | | 104 | | dB |
| Signal-to-Noise Ratio ² | Headphone mode, 20 Hz to 20 kHz | | | | |
| With A-Weighted Filter (RMS) | AVDD = 1.8 V | | 105 | | dB |
| | AVDD = 3.3 V | | 108 | | dB |
| With Flat 20 Hz to 20 kHz Filter | AVDD = 1.8 V | | 103 | | dB |
| | AVDD = 3.3 V | | 106 | | dB |
| Interchannel Gain Mismatch | Headphone mode | | 75 | | mdB |
| Total Harmonic Distortion + Noise | Headphone mode | | | | |
| 32 Ω Load | –1 dBFS, AVDD = 1.8 V, P _o = 27 mW | | –75 | | dB |
| | –1 dBFS, AVDD = 3.3 V, P _o = 90 mW | | –83 | | dB |
| 24 Ω Load | –2 dBFS, AVDD = 1.8 V, P _o = 28 mW | | –75 | | dB |
| | –1 dBFS, AVDD = 3.3 V, P _o = 118 mW | | –77 | | dB |
| 16 Ω Load | –3 dBFS, AVDD = 1.8 V, P _o = 33 mW | | –75 | | dB |
| | –1 dBFS, AVDD = 3.3 V, P _o = 175 mW | | –83 | | dB |
| Headphone Output Power | | | | | |
| 32 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 32.5 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 111.8 | | mW |
| 24 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 37.6 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 148.3 | | mW |
| 16 Ω Load | AVDD = 1.8 V, <0.1% THD + N | | 41.5 | | mW |
| | AVDD = 3.3 V, <0.1% THD + N | | 189.2 | | mW |
| Gain Error | Headphone mode | | ±0.25 | | % |
| Offset Error | | | ±0.1 | | mV |
| Interchannel Isolation | 1 kHz, 0 dBFS input signal | | 100 | | dB |
| Power Supply Rejection Ratio | CM capacitor = 22 μF 100 mV p-p at 1 kHz | | 73 | | dB |
| CM REFERENCE | CM pin | | | | |
| Common-Mode Reference Output | | | AVDD/2 | | V |
| Common-Mode Source Impedance | | | 5 | | kΩ |
| REGULATOR | | | | | |
| Line Regulation | | | 1 | | mV/V |
| Load Regulation | | | 6 | | mV/mA |

¹ Dynamic range is the ratio of the sum of noise and harmonic power in the band of interest with a –60 dBFS signal present to the full-scale power level in decibels.

² SNR is the ratio of the sum of all noise power in the band of interest with no signal present to the full-scale power level in decibels.

³ These specifications are with 4.7 μF decoupling and 5.0 kΩ load on pin.

CRYSTAL AMPLIFIER SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted.

Table 2.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|------------------|--------------------------|-----|-----|-----|------|
| Jitter | | | 270 | 500 | ps |
| Frequency Range | | 8 | | 27 | MHz |
| Load Capacitance | | | | 20 | pF |

DIGITAL INPUT/OUTPUT SPECIFICATIONS

-40°C < T_A < +85°C, IOVDD = 3.3 V ± 10% and 1.8 V - 5%/+10%.

Table 3.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|-------------|-----|------|------|
| Input Voltage High (V _{IH}) | IOVDD = 3.3 V | 2.0 | | | V |
| | IOVDD = 1.8 V | 1.1 | | | V |
| Input Voltage Low (V _{IL}) | IOVDD = 3.3 V | | | 0.8 | V |
| | IOVDD = 1.8 V | | | 0.45 | V |
| Input Leakage | IOVDD = 3.3 V, I _{IH} at V _{IH} = 2.0 V | | | 10 | μA |
| | I _{IL} at V _{IL} = 0.8 V | | | 10 | μA |
| | IOVDD = 1.8 V, I _{IH} at V _{IH} = 1.1 V | | | 10 | μA |
| | I _{IL} at V _{IL} = 0.45 V | | | 10 | μA |
| Output Voltage High (V _{OH}) with Low Drive Strength | I _{OH} = 1 mA | IOVDD - 0.6 | | | V |
| Output Voltage High (V _{OH}) with High Drive Strength | I _{OH} = 3 mA | IOVDD - 0.6 | | | V |
| Output Voltage Low (V _{OL}) with Low Drive Strength | I _{OL} = 1 mA | | | 0.4 | V |
| Output Voltage Low (V _{OL}) with High Drive Strength | I _{OL} = 3 mA | | | 0.4 | V |
| Input Capacitance | | | | 5 | pF |

POWER SUPPLY SPECIFICATIONS

Supply voltages AVDD = IOVDD = 1.8 V, DVDD = 1.1 V, unless otherwise noted. PLL disabled, direct master clock.

Table 4.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|--|-------|------|------|------|
| SUPPLIES | | | | | |
| AVDD Voltage | | 1.71 | 1.8 | 3.63 | V |
| DVDD Voltage | | 1.045 | 1.1 | 1.98 | V |
| IOVDD Voltage | | 1.71 | 1.8 | 3.63 | V |
| Digital I/O Current with IOVDD = 1.8 V | Crystal oscillator enabled | | | | |
| Slave Mode | f _S = 48 kHz | | 0.35 | | mA |
| | f _S = 192 kHz | | 0.49 | | mA |
| | f _S = 8 kHz | | 0.32 | | mA |
| Master Mode | f _S = 48 kHz | | 0.53 | | mA |
| | f _S = 192 kHz | | 1.18 | | mA |
| | f _S = 8 kHz | | 0.35 | | mA |
| Power-Down | | | 0 | | μA |
| Digital I/O Current with IOVDD = 3.3 V | Crystal oscillator enabled | | | | |
| Slave Mode | f _S = 48 kHz | | 2.05 | | mA |
| | f _S = 192 kHz | | 2.28 | | mA |
| | f _S = 8 kHz | | 1.99 | | mA |
| Master Mode | f _S = 48 kHz | | 2.4 | | mA |
| | f _S = 192 kHz | | 3.62 | | mA |
| | f _S = 8 kHz | | 2.05 | | mA |
| Power-Down | | | 7 | | μA |
| Analog Current (AVDD) | See Table 5 | | | | |
| Power-Down | AVDD = 1.8 V | | 0.6 | | μA |
| | AVDD = 3.3 V | | 13.6 | | μA |
| DISSIPATION | | | | | |
| Operation | f _S = 192 kHz (see conditions in Table 5) | | | | |
| All Supplies | | | 15.5 | | mW |
| Digital I/O Supply | | | 0.7 | | mW |
| Analog Supply | Includes regulated DVDD current | | 14.8 | | mW |
| Power-Down, All Supplies | | | 1 | | μW |

TYPICAL POWER CONSUMPTION

Typical active noise cancelling (ANC) settings. Master clock = 12.288 MHz, $f_s = 192$ kHz. On-board regulator enabled. Two analog-to-digital converters (ADCs) with PGA enabled and two ADCs configured for line input; no input signal. Two digital-to-analog converters (DACs) configured for differential headphone operation; DAC outputs unloaded. Both MICBIAS0 and MICBIAS1 enabled. ASRCs and pulse density modulated (PDM) modulator disabled. Core running 26 out of 32 possible instructions. For total power consumption, add IOVDD at 8 kHz slave current listed in Table 4.

Table 5.

| Operating Voltage | Power Management Setting | Typical AVDD Power Consumption (mA) | Typical ADC THD + N (dB) | Typical HP Output THD + N (dB) |
|----------------------|--------------------------|-------------------------------------|--------------------------|--------------------------------|
| AVDD = IOVDD = 3.3 V | Normal (default) | 11.5 | -93 | -87.5 |
| | Extreme power saving | 9.4 | -93 | -86.5 |
| | Power saving | 9.8 | -93 | -86.5 |
| | Enhanced performance | 12.65 | -93 | -90.5 |
| AVDD = IOVDD = 1.8 V | Normal (default) | 9.37 | -86 | -91 |
| | Extreme power saving | 7.40 | -84.5 | -87 |
| | Power saving | 7.78 | -84.5 | -87.5 |
| | Enhanced performance | 10.4 | -86 | -94.5 |

DIGITAL FILTERS

Table 6.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|-----------------------------------|-------------------------------|-------|-----|---------------------|---------|
| ADC INPUT TO DAC OUTPUT PATH | | | | | |
| Pass-Band Ripple | DC to 20 kHz, $f_s = 192$ kHz | | | ± 0.02 | dB |
| Group Delay | $f_s = 192$ kHz | | 38 | | μ s |
| SAMPLE RATE CONVERTER | | | | | |
| Pass Band | LRCLK < 63 kHz | 0 | | $0.475 \times f_s$ | kHz |
| | 63 kHz < LRCLK < 130 kHz | 0 | | $0.4286 \times f_s$ | |
| | LRCLK > 130 kHz | 0 | | $0.4286 \times f_s$ | |
| Pass-Band Ripple | Upsampling, 96 kHz | -0.27 | | 0.05 | dB |
| | Upsampling, 192 kHz | -0.06 | | 0.05 | dB |
| | Downsampling, 96 kHz | 0 | | 0.07 | dB |
| | Downsampling, 192 kHz | 0 | | 0.07 | dB |
| Input/Output Frequency Range | | 8 | | 192 | kHz |
| Dynamic Range | | | 100 | | dB |
| Total Harmonic Distortion + Noise | | | -90 | | dB |
| Startup Time | | | | 15 | ms |
| PDM MODULATOR | | | | | |
| Dynamic Range (A-Weighted) | | | 112 | | dB |
| Total Harmonic Distortion + Noise | | | -92 | | dB |

DIGITAL TIMING SPECIFICATIONS

-40°C < T_A < +85°C, IOVDD = 1.71 V to 3.63 V, DVDD = 1.045 V to 1.98 V.

Table 7. Digital Timing

| Parameter | Limit | | Unit | Description |
|---|---------------------------|------------------------|------|---|
| | T _{MIN} | T _{MAX} | | |
| MASTER CLOCK | | | | |
| t _{MP} | 37 | 125 | ns | MCLKIN period; 8 MHz to 27 MHz input clock using PLL |
| t _{MCLK} | 77 | 82 | ns | Internal MCLK period; direct MCLK and PLL output divided by 2 |
| SERIAL PORT | | | | |
| t _{BL} | 40 | | ns | BCLK low pulse width (master and slave modes) |
| t _{BH} | 40 | | ns | BCLK high pulse width (master and slave modes) |
| t _{LS} | 10 | | ns | LRCLK setup; time to BCLK rising (slave mode) |
| t _{LH} | 10 | | ns | LRCLK hold; time from BCLK rising (slave mode) |
| t _{SS} | 5 | | ns | DAC_SDATA setup; time to BCLK rising (master and slave modes) |
| t _{SH} | 5 | | ns | DAC_SDATA hold; time from BCLK rising (master and slave modes) |
| t _{TS} | | 10 | ns | BCLK falling to LRCLK timing skew (master mode) |
| t _{SOD} | 0 | 34 | ns | ADC_SDATAx delay; time from BCLK falling (master and slave modes) |
| t _{SOTD} | | 30 | ns | BCLK falling to ADC_SDATAx driven in TDM tristate mode |
| t _{SOTX} | | 30 | ns | BCLK falling to ADC_SDATAx tristated in TDM tristate mode |
| SPI PORT | | | | |
| f _{SCLK} | | 6.25 | MHz | SCLK frequency |
| t _{CCPL} | 80 | | ns | SCLK pulse width low |
| t _{CCPH} | 80 | | ns | SCLK pulse width high |
| t _{CLS} | 5 | | ns | SS setup; time to SCLK rising |
| t _{CLH} | 100 | | ns | SS hold; time from SCLK rising |
| t _{CLPH} | 80 | | ns | SS pulse width high |
| t _{CDS} | 10 | | ns | MOSI setup; time to SCLK rising |
| t _{CDH} | 10 | | ns | MOSI hold; time from SCLK rising |
| t _{COD} | | 101 | ns | MISO delay; time from SCLK falling |
| I²C PORT | | | | |
| f _{SCL} | | 400 | kHz | SCL frequency |
| t _{SCLH} | 0.6 | | μs | SCL high |
| t _{SCLL} | 1.3 | | μs | SCL low |
| t _{SCS} | 0.6 | | μs | SCL rise setup time (to SDA falling), relevant for repeated start condition |
| t _{SCR} | | 250 | ns | SCL and SDA rise time, C _{LOAD} = 400 pF |
| t _{SCH} | 0.6 | | μs | SCL fall hold time (from SDA falling), relevant for start condition |
| t _{DS} | 100 | | ns | SDA setup time (to SCL rising) |
| t _{SCF} | | 250 | ns | SCL fall time; C _{LOAD} = 400 pF |
| t _{SDF} | | 250 | ns | SDA fall time; C _{LOAD} = 400 pF |
| t _{BFT} | 0.6 | | μs | SCL rise setup time (to SDA rising), relevant for stop condition |
| I²C EEPROM SELF-BOOT | | | | |
| t _{SCHE} | 26 × t _{MP} - 70 | | ns | SCL fall hold time (from SDA falling), relevant for start condition; t _{MP} is the input clock on the MCLKIN pin |
| t _{SCSE} | 38 × t _{MP} - 70 | | ns | SCL rise setup time (to SDA falling), relevant for repeated start condition |
| t _{BFTE} | 70 × t _{MP} - 70 | | ns | SCL rise setup time (to SDA rising), relevant for stop condition |
| t _{DSE} | 6 × t _{MP} - 70 | | ns | Delay from SCL falling to SDA changing |
| t _{BHTE} | 32 × t _{MP} | | ns | SDA rising in self-boot stop condition to SDA falling edge for external master start condition |
| MULTIPURPOSE AND POWER-DOWN PINS | | | | |
| t _{GIL} | | 1.5 × 1/f _S | μs | MPx input latency; time until high or low value is read by core |
| t _{RLPW} | 20 | | ns | PD low pulse width |

| Parameter | Limit | | Unit | Description |
|---------------------------|------------------|------------------|------|--|
| | T _{MIN} | T _{MAX} | | |
| DIGITAL MICROPHONE | | | | |
| t _{CF} | | 20 | ns | Digital microphone clock fall time |
| t _{CR} | | 20 | ns | Digital microphone clock rise time |
| t _{DS} | 40 | | | Digital microphone valid data start time |
| t _{DE} | | 0 | ns | Digital microphone valid data end time |
| PDM OUTPUT | | | | |
| t _{DCF} | | 20 | ns | PDM clock fall time |
| t _{DCR} | | 20 | ns | PDM clock rise time |
| t _{DDV} | 0 | 30 | ns | PDM delay time for valid data |

Digital Timing Diagrams

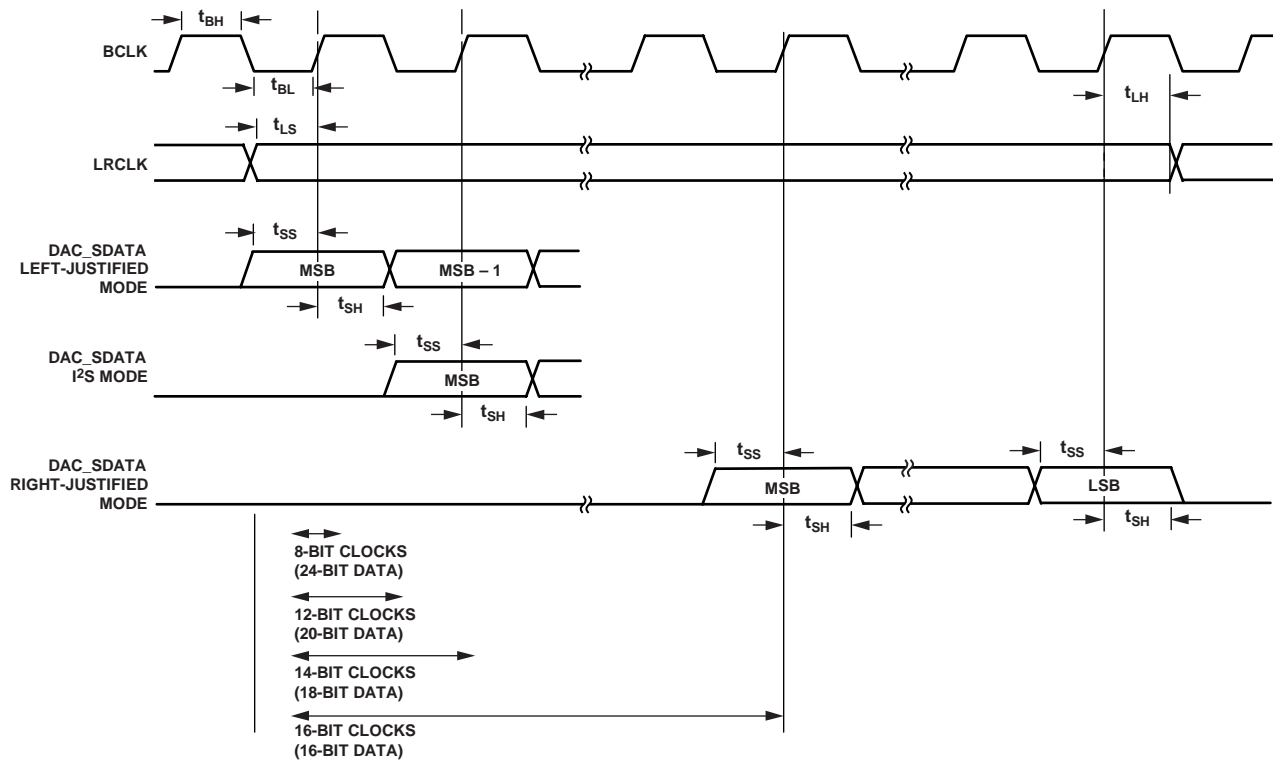


Figure 2. Serial Input Port Timing

10804-002

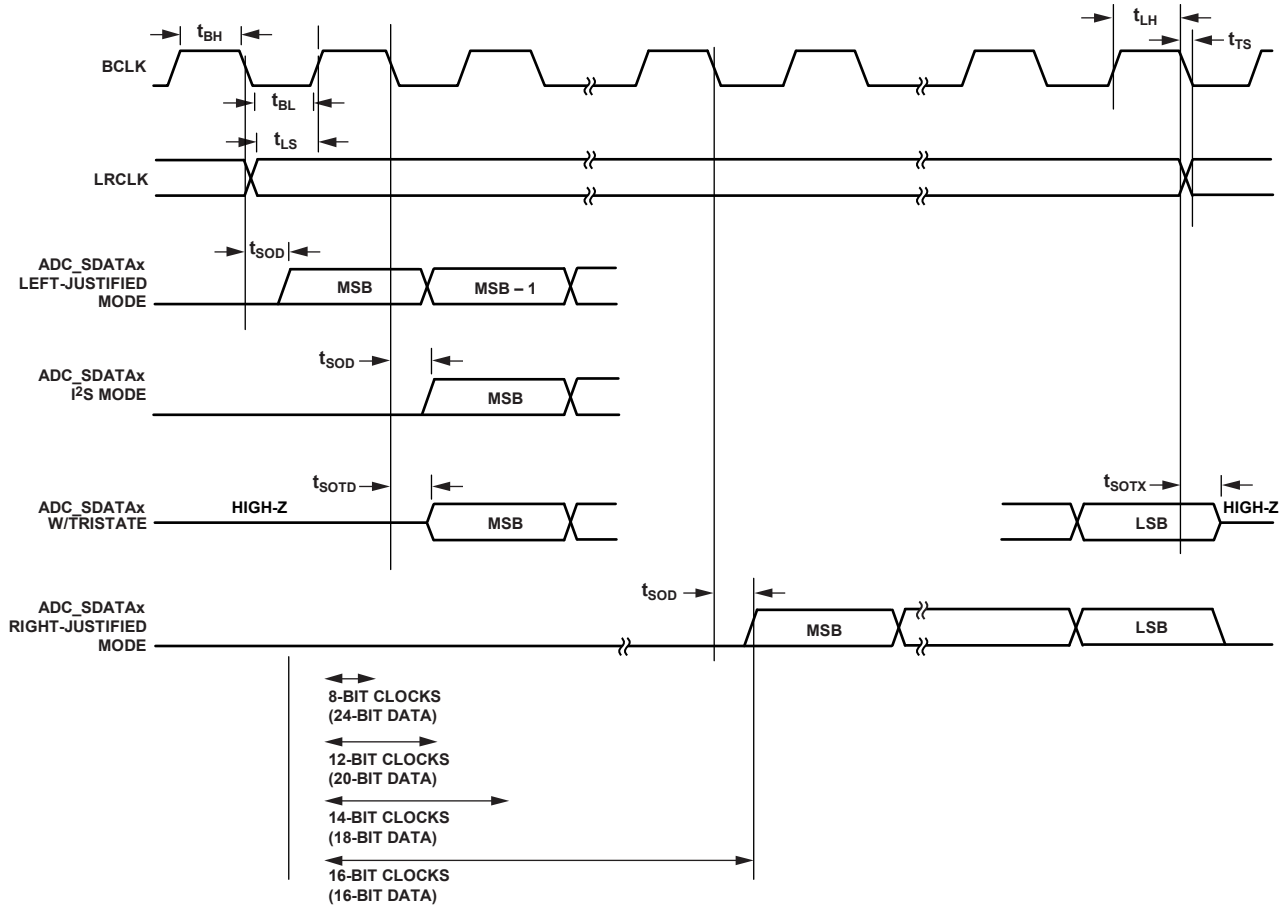


Figure 3. Serial Output Port Timing

10804-003

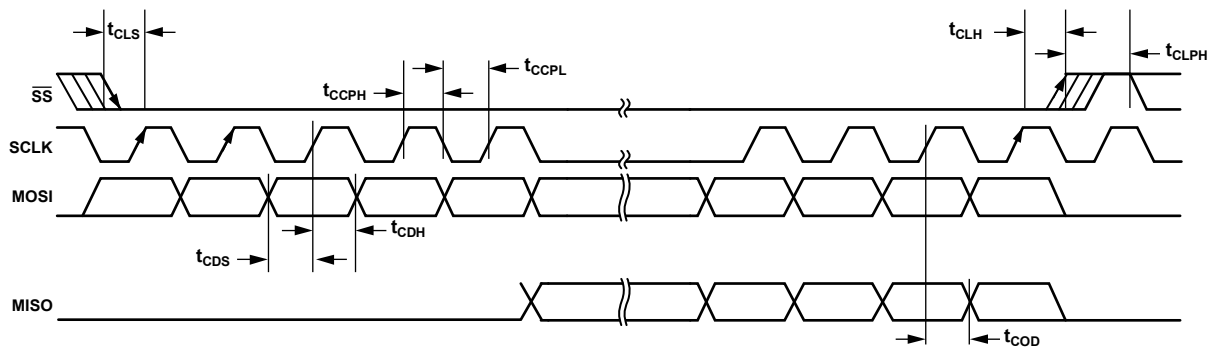


Figure 4. SPI Port Timing

10804-004

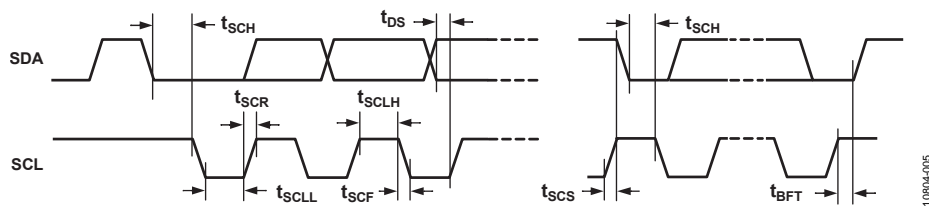


Figure 5. I²C Port Timing

10804-005

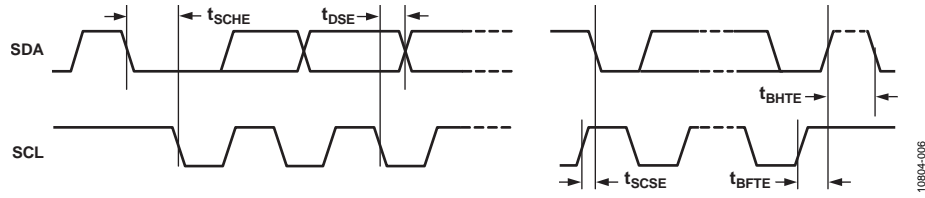


Figure 6. I²C Self-Boot Timing

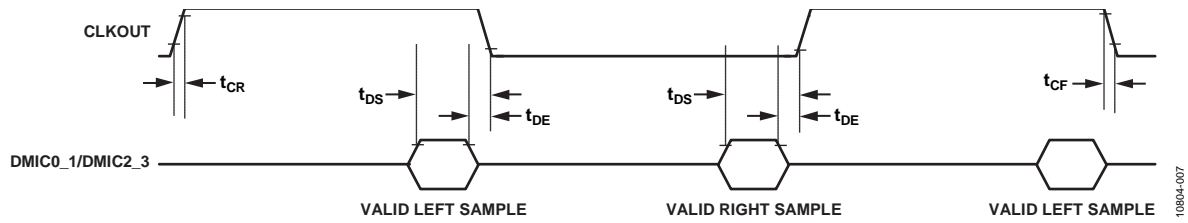


Figure 7. Digital Microphone Timing

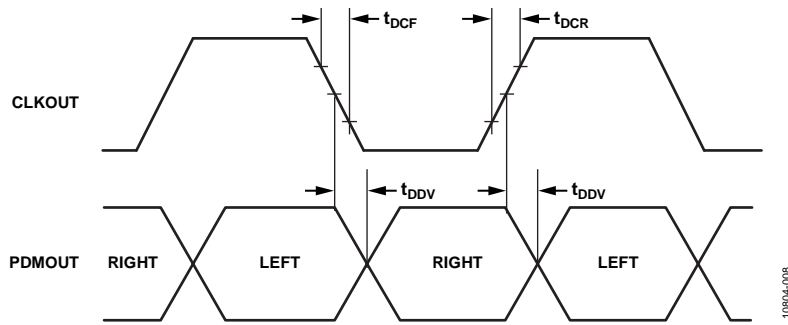


Figure 8. PDM Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 8.

| Parameter | Rating |
|-------------------------------------|------------------------|
| Power Supply (AVDD, IOVDD) | -0.3 V to +3.63 V |
| Digital Supply (DVDD) | -0.3 V to +1.98 V |
| Input Current (Except Supply Pins) | ±20 mA |
| Analog Input Voltage (Signal Pins) | -0.3 V to AVDD + 0.3 V |
| Digital Input Voltage (Signal Pins) | -0.3 to IOVDD + 0.3 V |
| Operating Temperature Range (Case) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} represents the junction-to-ambient thermal resistance; θ_{JC} represents the junction-to-case thermal resistance. Thermal numbers are simulated on a 4-layer JEDEC PCB with the exposed pad soldered to the PCB. θ_{JC} was simulated at the exposed pad on the bottom of the package.

Table 9. Thermal Resistance

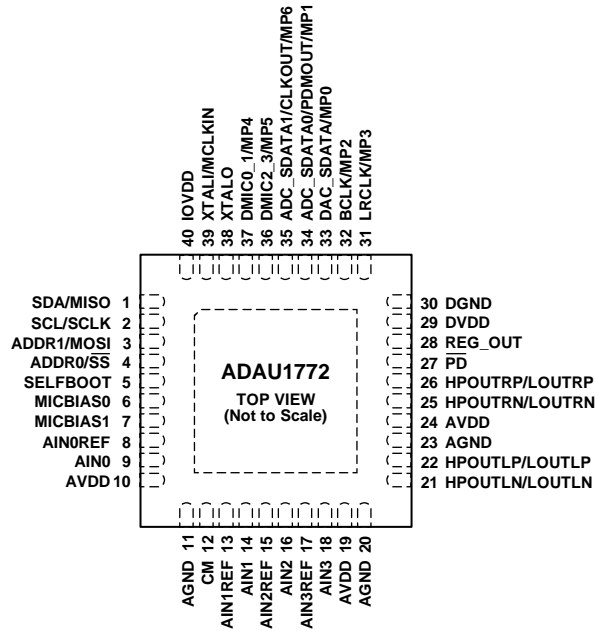
| Package Type | θ_{JA} | θ_{JC} | Unit |
|---------------|---------------|---------------|------|
| 40-Lead LFCSP | 29 | 1.8 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD IS CONNECTED INTERNALLY TO THE ADAU1772 GROUNDS. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE GROUND PLANE. SEE THE EXPOSED PAD PCB DESIGN SECTION FOR MORE INFORMATION.

10804-059

Figure 9. Pin Configuration

Table 10. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|------------------------|-------------------|---|
| 1 | SDA/MISO | D_IO | I ² C Data (SDA). This pin is a bidirectional open-collector. The line connected to this pin should have a 2.0 kΩ pull-up resistor. SPI Data Output (MISO). This SPI data output is used for reading back registers and memory locations. It is tristated when an SPI read is not active. |
| 2 | SCL/SCLK | D_IN | I ² C Clock (SCL). This pin is always an open-collector input when the device is in I ² C control mode. When the device is in self-boot mode, this pin is an open-collector output (I ² C master). The line connected to this pin should have a 2.0 kΩ pull-up resistor. |
| 3 | ADDR1/MOSI | D_IN | SPI Clock (SCLK). This pin can either run continuously or be gated off between SPI transactions. I ² C Address 1 (ADDR1). |
| 4 | ADDR0/ \overline{SS} | D_IN | SPI Data Input (MOSI). I ² C Address 0 (ADDR0). |
| 5 | SELFBOOT | D_IN | SPI Latch Signal (\overline{SS}). This pin must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction can take a different number of SCLK cycles to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction. |
| 6 | MICBIAS0 | A_OUT | Self-Boot. Pull this pin up to IOVDD at power-up to enable the self-boot mode. |
| 7 | MICBIAS1 | A_OUT | Bias Voltage for Electret Microphone. Decouple with a 1 μF capacitor. |
| 8 | AIN0REF | A_IN | Bias Voltage for Electret Microphone. Decouple with a 1 μF capacitor. |
| 9 | AIN0 | A_IN | ADC0 Input Reference. This reference pin should be ac-coupled to ground with a 10 μF capacitor. |
| 10 | AVDD | PWR | ADC0 Input. |
| 11 | AGND | PWR | 1.8 V to 3.3 V Analog Supply. This pin should be decoupled to AGND with a 0.1 μF capacitor. |
| 12 | CM | A_OUT | Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane. AGND should be decoupled to AVDD with a 0.1 μF capacitor. |
| | | | AVDD/2 V Common-Mode Reference. A 10 μF to 47 μF decoupling capacitor should be connected between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as they are not drawing current from CM (for example, the noninverting input of an op amp). |

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|------------------------|-------------------|--|
| 13 | AIN1REF | A_IN | ADC1 Input Reference. This reference pin should be ac-coupled to ground with a 10 µF capacitor. |
| 14 | AIN1 | A_IN | ADC1 Input. |
| 15 | AIN2REF | A_IN | ADC2 Input Reference. This reference pin should be ac-coupled to ground with a 10 µF capacitor. |
| 16 | AIN2 | A_IN | ADC2 Input. |
| 17 | AIN3REF | A_IN | ADC3 Input Reference. This reference pin should be ac-coupled to ground with a 10 µF capacitor. |
| 18 | AIN3 | A_IN | ADC3 Input. |
| 19 | AVDD | PWR | 1.8 V to 3.3 V Analog Supply. This pin should be decoupled to AGND with a 0.1 µF capacitor. |
| 20 | AGND | PWR | Analog Ground. |
| 21 | HPOUTLN/LOUTLN | A_OUT | Left Headphone Inverted (HPOUTLN). Line Output Inverted (LOUTLN). |
| 22 | HPOUTLP/LOUTLP | A_OUT | Left Headphone Noninverted (HPOUTLP). Line Output Noninverted, Single-Ended Line Output (LOUTLP). |
| 23 | AGND | PWR | Headphone Amplifier Ground. |
| 24 | AVDD | PWR | Headphone Amplifier Power, 1.8 V to 3.3 V Analog Supply. This pin should be decoupled to AGND with a 0.1 µF capacitor. The PCB trace to this pin should be wider to supply the higher current necessary for driving the headphone outputs. |
| 25 | HPOUTRN/LOUTRN | A_OUT | Right Headphone Inverted (HPOUTRN). Line Output Inverted (LOUTRN). |
| 26 | HPOUTRP/LOUTRP | A_OUT | Right Headphone Noninverted (HPOUTRP). Line Output Noninverted, Single-Ended Line Output (LOUTRP). |
| 27 | $\overline{\text{PD}}$ | D_IN | Active Low Power-Down. All digital and analog circuits are powered down. There is an internal pull-down resistor on this pin; therefore, the ADAU1772 is held in power-down mode if its input signal is floating while power is applied to the supply pins. |
| 28 | REG_OUT | A_OUT | Regulator Output Voltage. This pin should be connected to DVDD if the internal voltage regulator is being used to generate DVDD voltage. |
| 29 | DVDD | PWR | Digital Core Supply. The digital supply can be generated from an on-board regulator or supplied directly from an external supply. In each case, DVDD should be decoupled to DGND with a 0.1 µF capacitor. |
| 30 | DGND | PWR | Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane. |
| 31 | LRCLK/MP3 | D_IO | Serial Data Port Frame Clock (LRCLK). General-Purpose Input (MP3). |
| 32 | BCLK/MP2 | D_IO | Serial Data Port Bit Clock (BCLK). General-Purpose Input (MP2). |
| 33 | DAC_SDATA/MP0 | D_IO | DAC Serial Input Data (DAC_SDATA). General-Purpose Input (MP0). |
| 34 | ADC_SDATA0/PDMOUT/MP1 | D_IO | ADC Serial Data Output 0 (ADC_SDATA0). Stereo PDM Output to Drive a High Efficiency Class-D Amplifier (PDMOUT). General-Purpose Input (MP1). |
| 35 | ADC_SDATA1/CLKOUT/MP6 | D_IO | Serial Data Output 1 (ADC_SDATA1). Master Clock Output/Clock for the Digital Microphone Input and PDM Output (CLKOUT). General-Purpose Input (MP6). |
| 36 | DMIC2_3/MP5 | D_IN | Digital Microphone Stereo Input 2 and Digital Microphone Stereo Input 3 (DMIC2_3). General-Purpose Input (MP5). |
| 37 | DMIC0_1/MP4 | D_IN | Digital Microphone Stereo Input 0 and Digital Microphone Stereo Input 1 (DMIC0_1). General-Purpose Input (MP4). |
| 38 | XTALO | A_OUT | Crystal Clock Output. This pin is the output of the crystal amplifier and should not be used to provide a clock to other ICs in the system. If a master clock output is needed, use CLKOUT (Pin 35). |
| 39 | XTALI/MCLKIN | D_IN | Crystal Clock Input (XTALI). Master Clock Input (MCLKIN) |
| 40 | IOVDD | PWR | Supply for Digital Input and Output Pins. The digital output pins are supplied from IOVDD, and this sets the highest input voltage that should be seen on the digital input pins. The current draw of this pin is variable because it is dependent on the loads of the digital outputs. IOVDD should be decoupled to DGND with a 0.1 µF capacitor. |
| | EP | | Exposed Pad. The exposed pad is connected internally to the ADAU1772 grounds. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the ground plane. See the Exposed Pad PCB Design section for more information. |

¹ D_IO = digital input/output, D_IN = digital input, A_OUT = analog output, A_IN = analog input, PWR = power, A_IN = analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

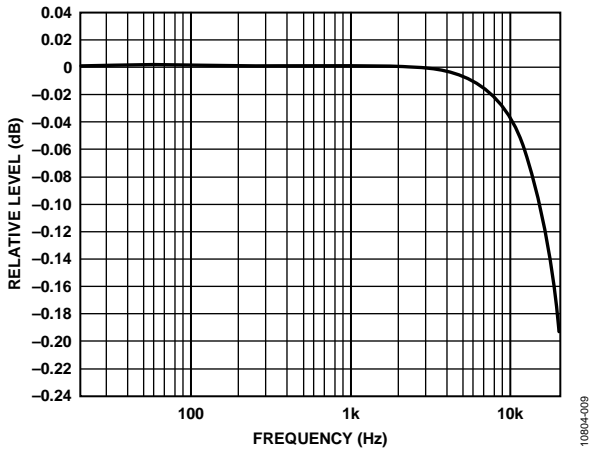


Figure 10. Relative Level vs. Frequency, $f_s = 48$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

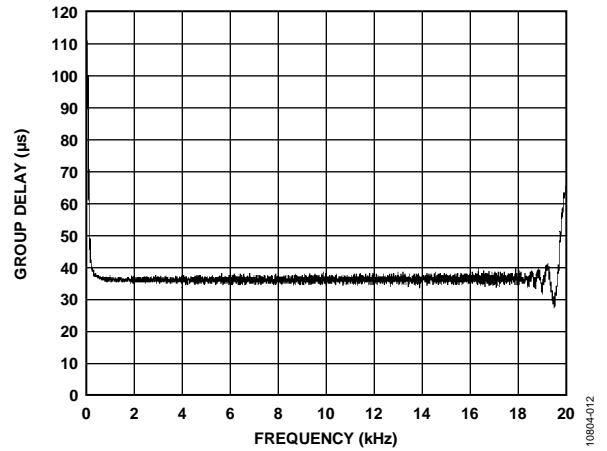


Figure 13. Group Delay vs. Frequency, $f_s = 48$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

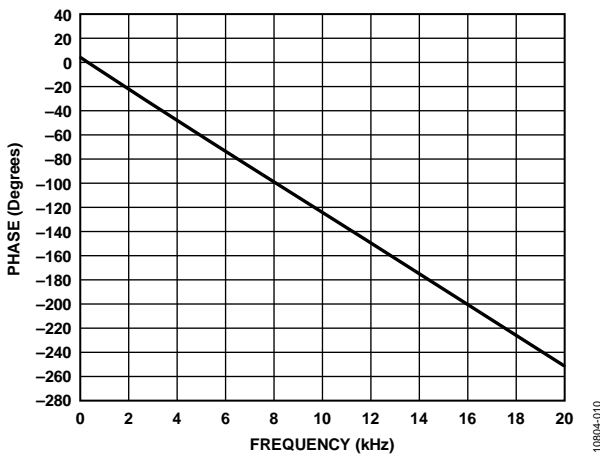


Figure 11. Phase vs. Frequency, 20 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

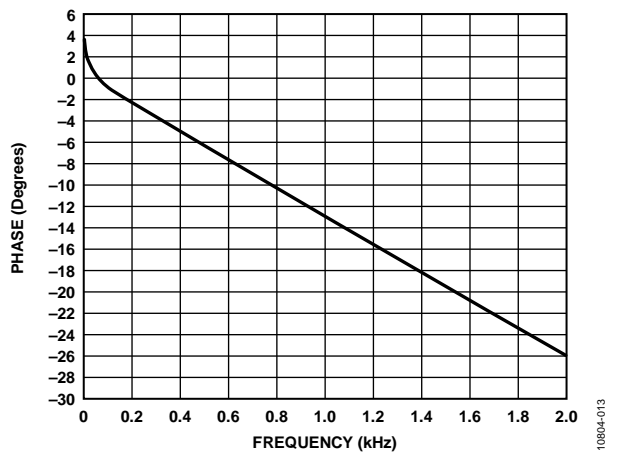


Figure 14. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

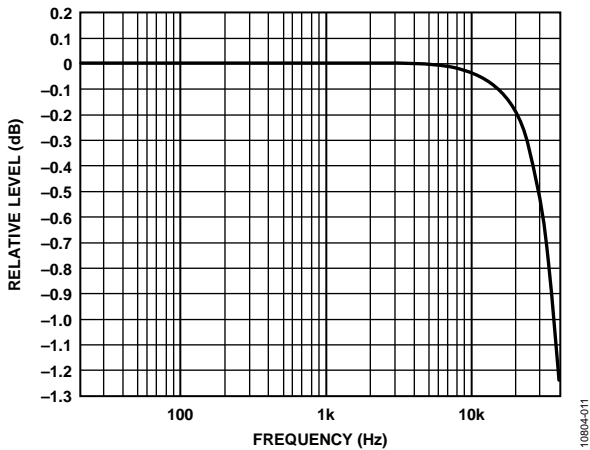


Figure 12. Relative Level vs. Frequency, $f_s = 96$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

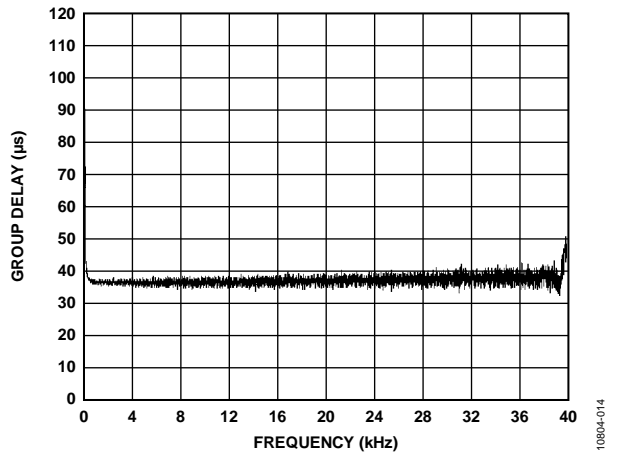


Figure 15. Group Delay vs. Frequency, $f_s = 96$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

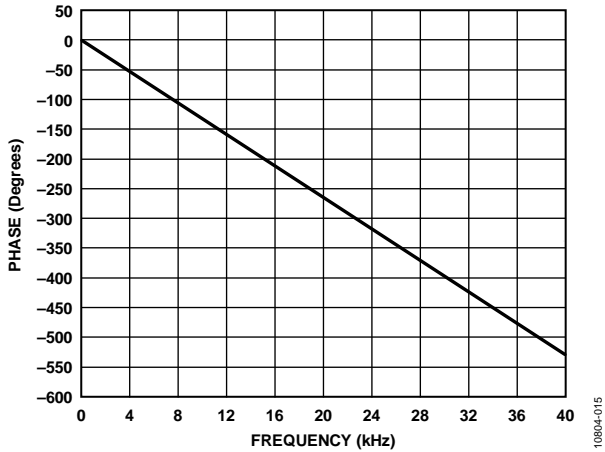


Figure 16. Phase vs. Frequency, 40 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

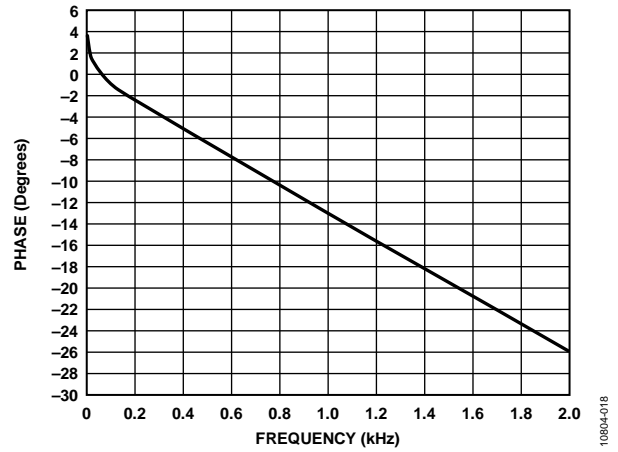


Figure 19. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

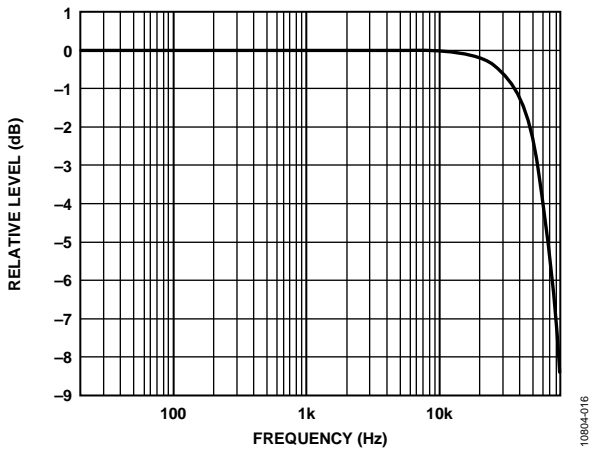


Figure 17. Relative Level vs. Frequency, $f_s = 192$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

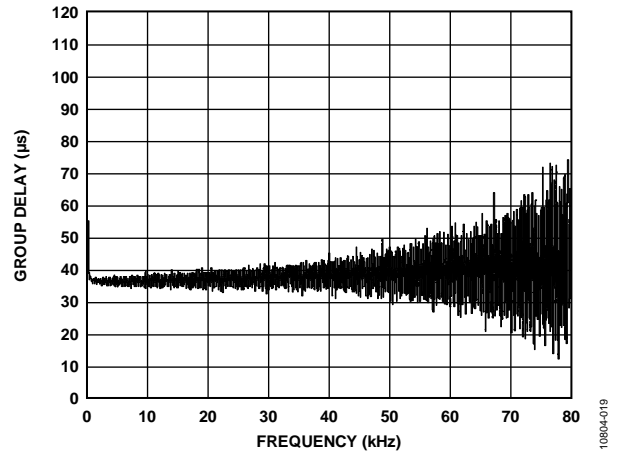


Figure 20. Group Delay vs. Frequency, $f_s = 192$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

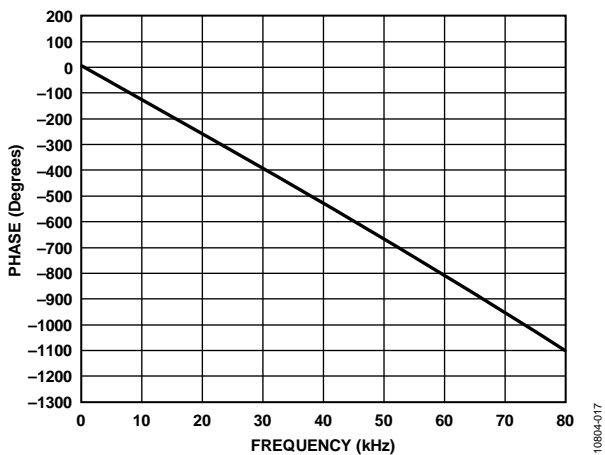


Figure 18. Phase vs. Frequency, 80 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

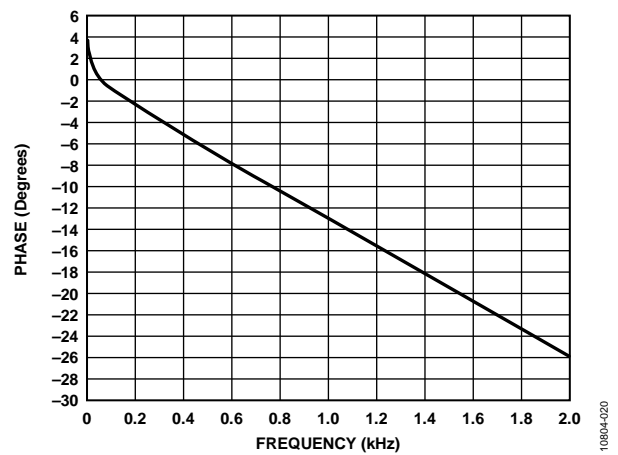


Figure 21. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = AIN0 to DSP (Without Processing) to LOU TLx

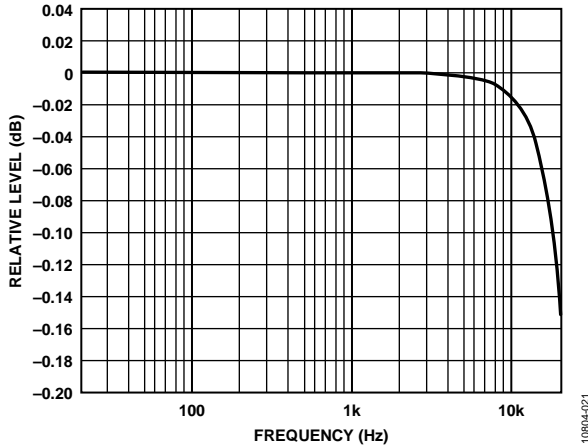


Figure 22. Relative Level vs. Frequency, $f_s = 48$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-021

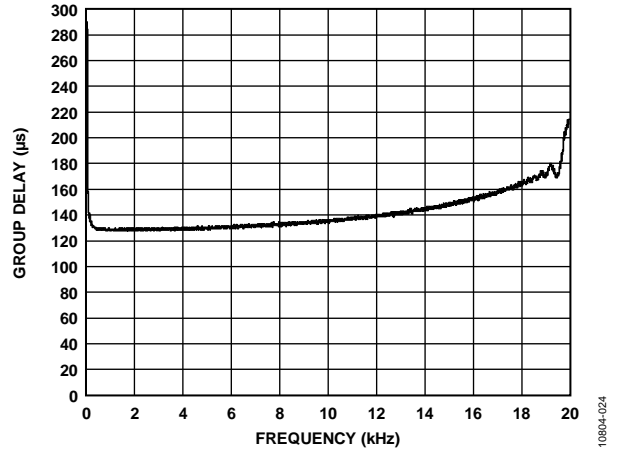


Figure 25. Group Delay vs. Frequency, $f_s = 48$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-024

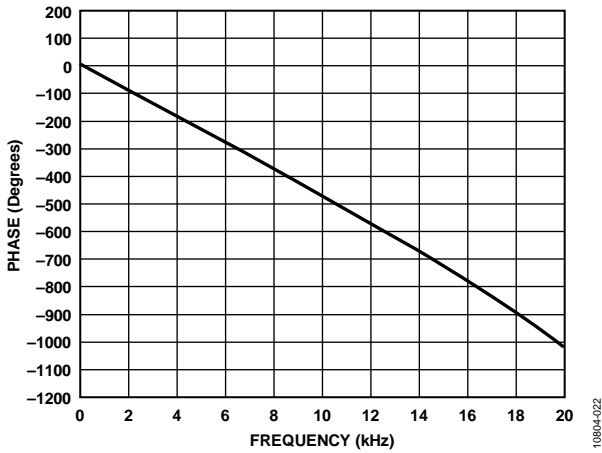


Figure 23. Phase vs. Frequency, 20 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-022

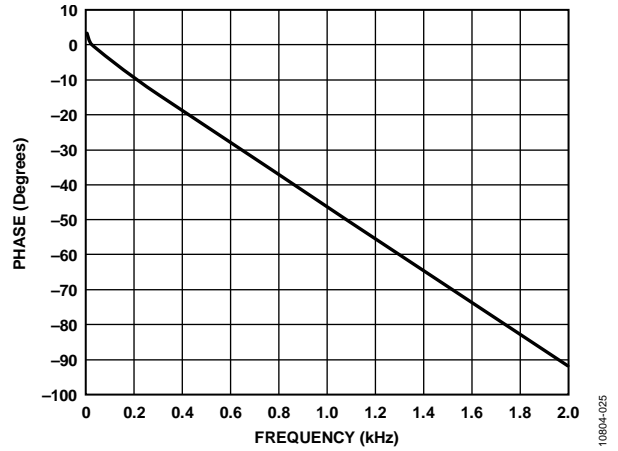


Figure 26. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-025

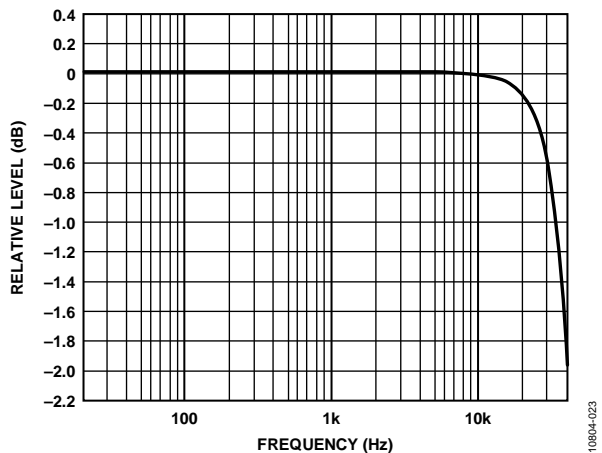


Figure 24. Relative Level vs. Frequency, $f_s = 96$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-023

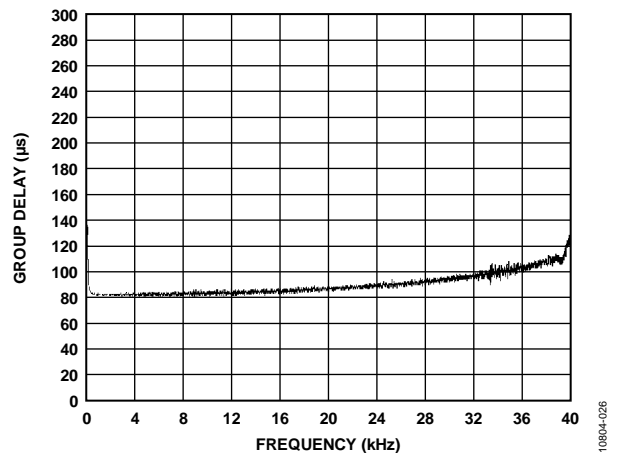


Figure 27. Group Delay vs. Frequency, $f_s = 96$ kHz, Signal Path = AIN0 to ASRC to ADC_SDATA0

10894-026

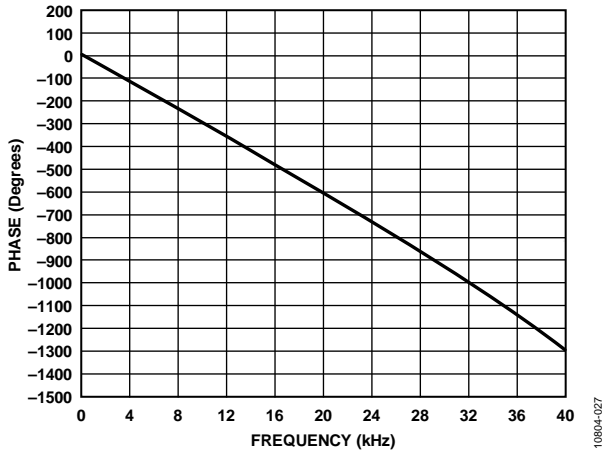


Figure 28. Phase vs. Frequency, 40 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-027

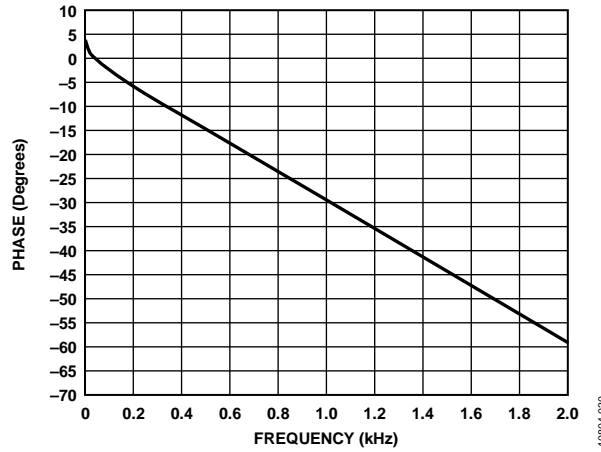


Figure 31. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-030

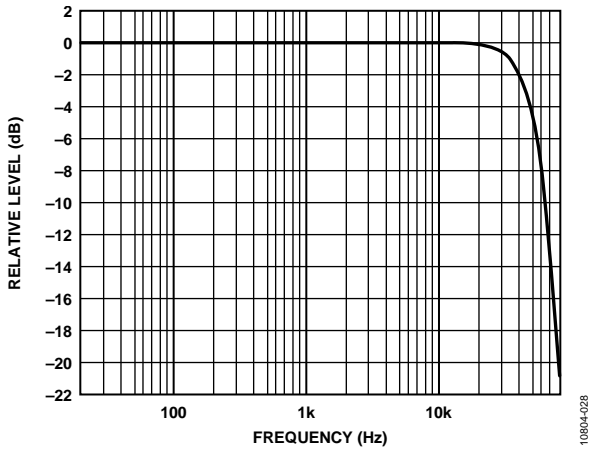


Figure 29. Relative Level vs. Frequency, $f_s = 192$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-028

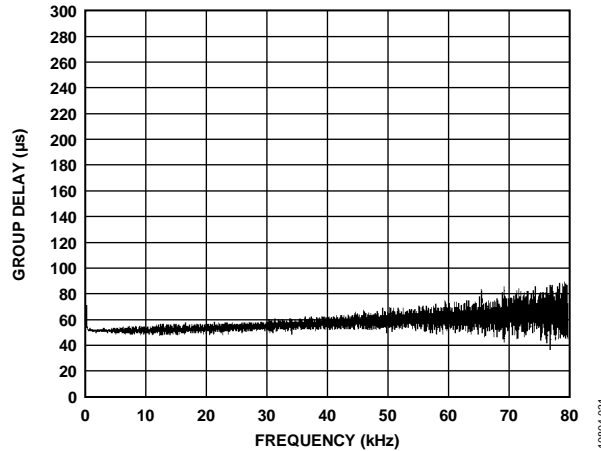


Figure 32. Group Delay vs. Frequency, $f_s = 192$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-031

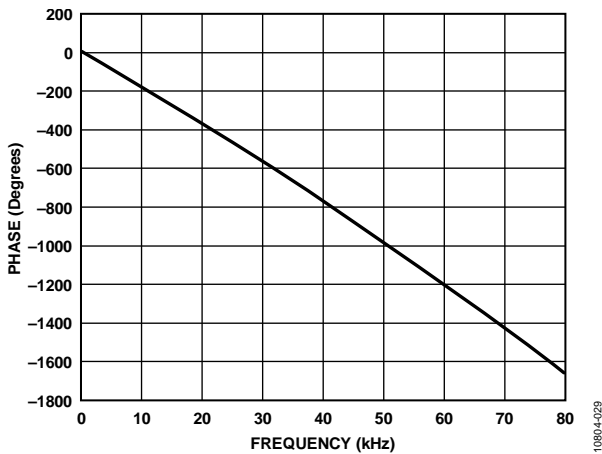


Figure 30. Phase vs. Frequency, 80 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-029

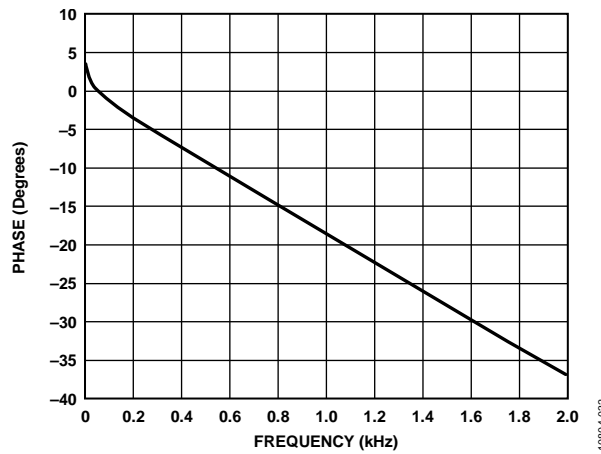


Figure 33. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = AIN0 to ASRC to ADC_SDAT0A0

10804-032

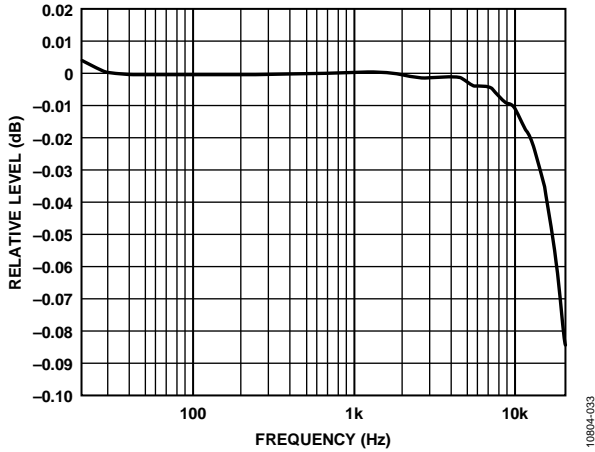


Figure 34. Relative Level vs. Frequency,
 $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-033

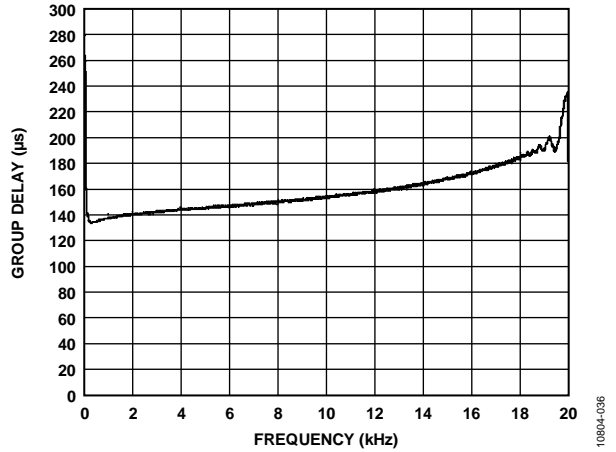


Figure 37. Group Delay vs. Frequency,
 $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-036

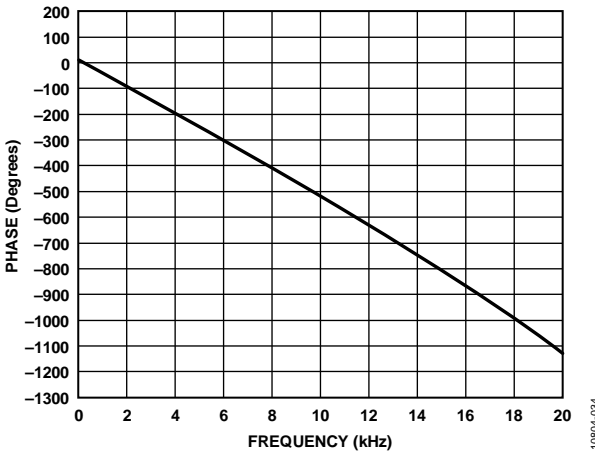


Figure 35. Phase vs. Frequency, 20 kHz Bandwidth,
 $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-034

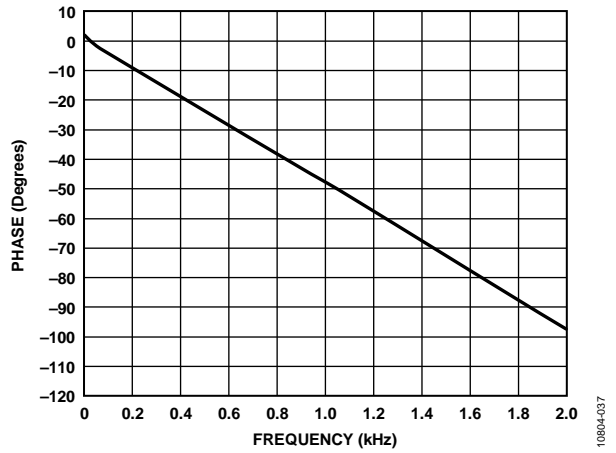


Figure 38. Phase vs. Frequency, 2 kHz Bandwidth,
 $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-037

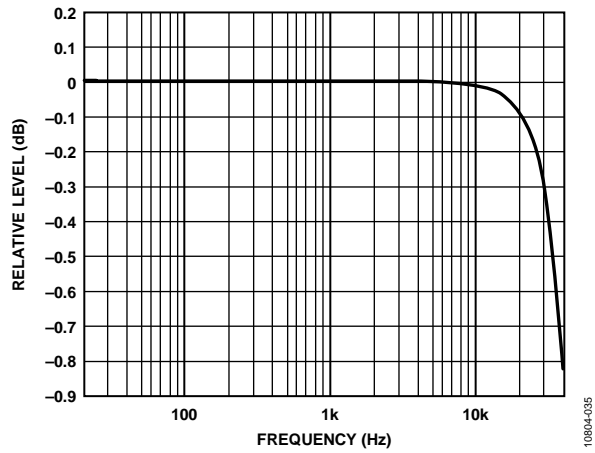


Figure 36. Relative Level vs. Frequency,
 $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-035

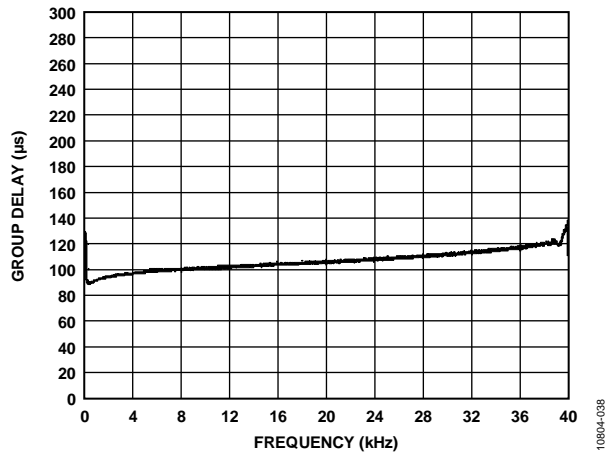
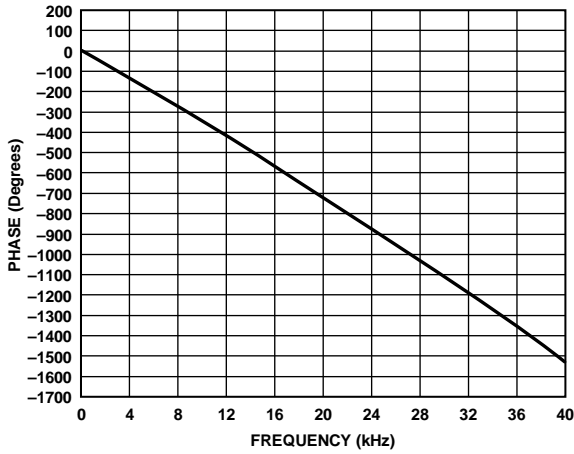


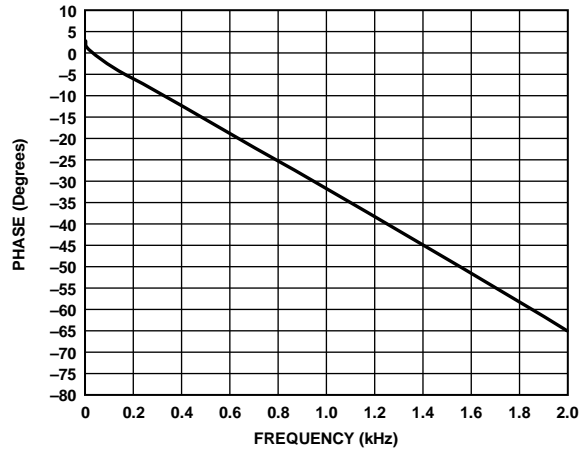
Figure 39. Group Delay vs. Frequency,
 $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

10804-038



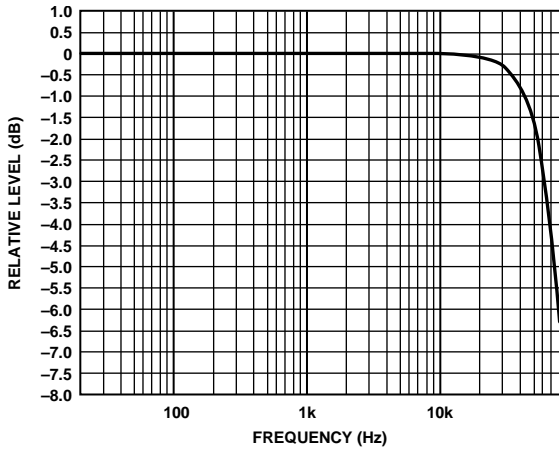
10804-039

Figure 40. Phase vs. Frequency, 40 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx



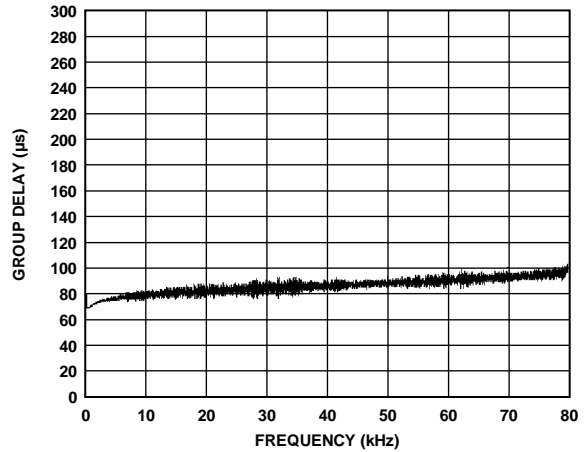
10804-042

Figure 43. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx



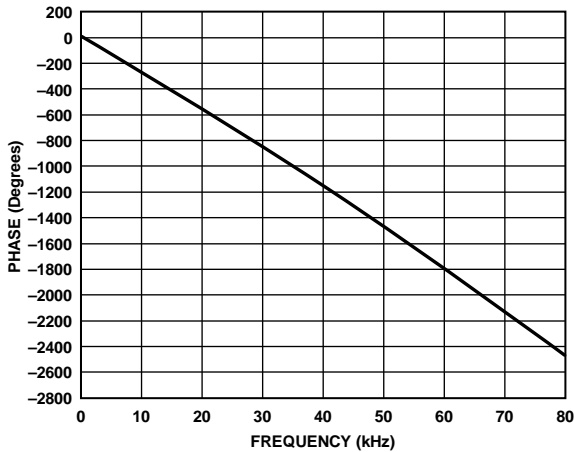
10804-040

Figure 41. Relative Level vs. Frequency, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx



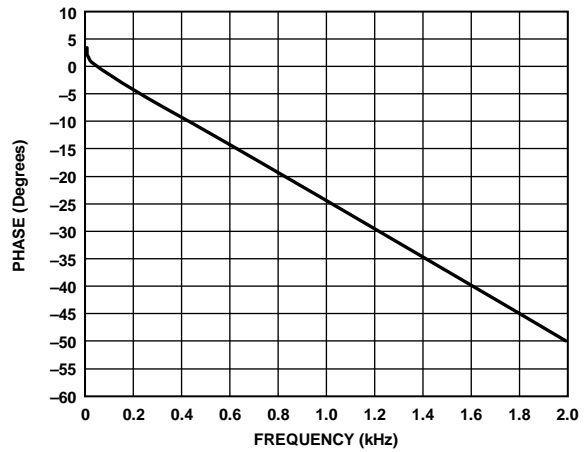
10804-043

Figure 44. Group Delay vs. Frequency, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx



10804-041

Figure 42. Phase vs. Frequency, 80 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx



10804-044

Figure 45. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to LOU TLx

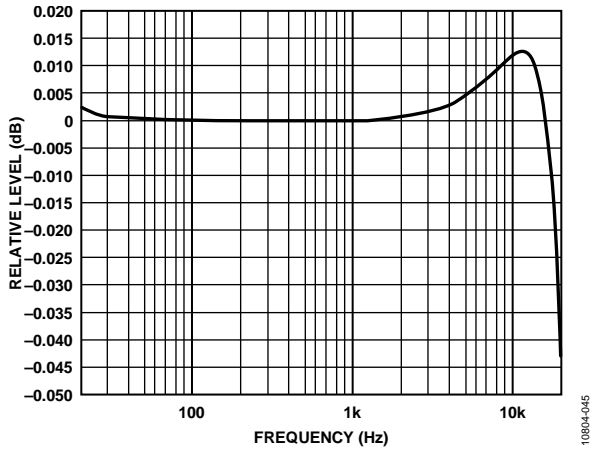


Figure 46. Relative Level vs. Frequency, $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

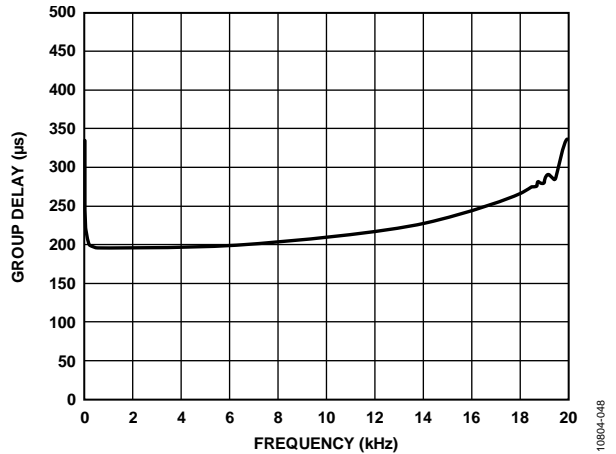


Figure 49. Group Delay vs. Frequency, $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

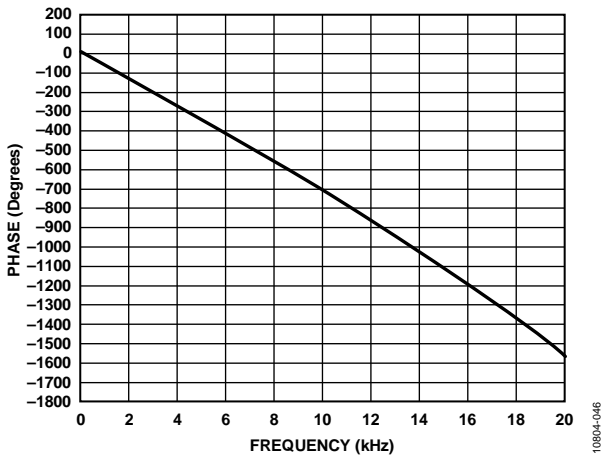


Figure 47. Phase vs. Frequency, 20 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

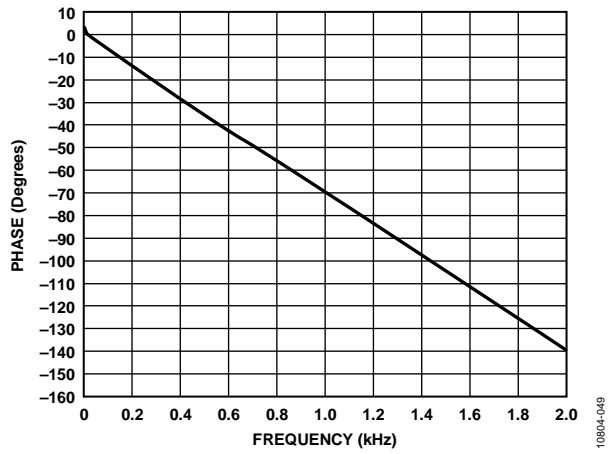


Figure 50. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 48$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

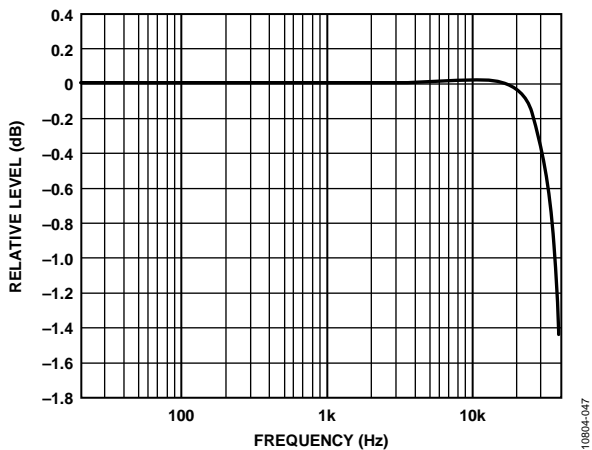


Figure 48. Relative Level vs. Frequency, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

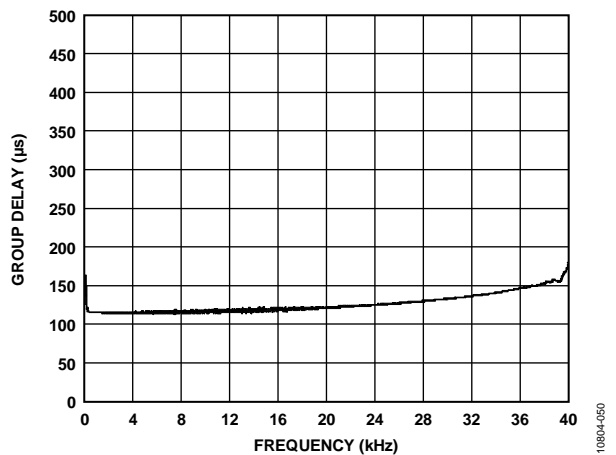


Figure 51. Group Delay vs. Frequency, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

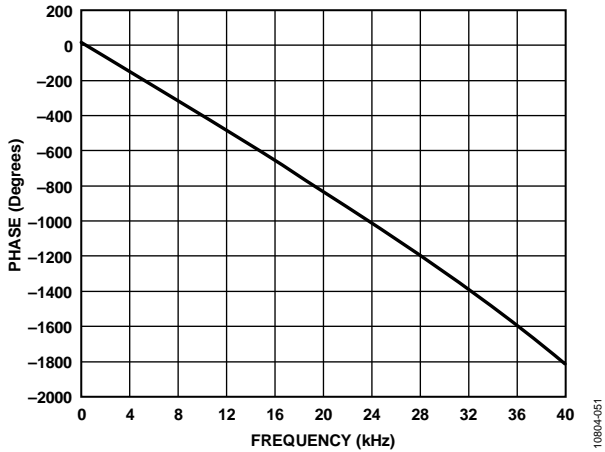


Figure 52. Phase vs. Frequency, 40 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

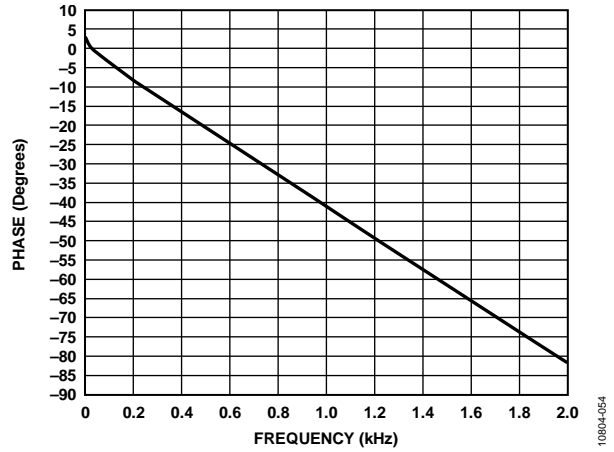


Figure 55. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 96$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

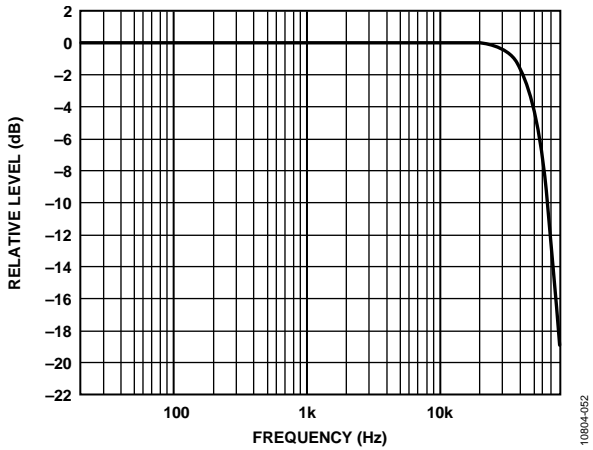


Figure 53. Relative Level vs. Frequency, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

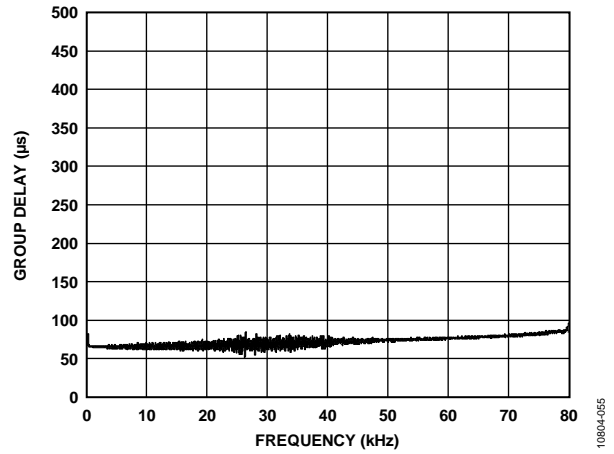


Figure 56. Group Delay vs. Frequency, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

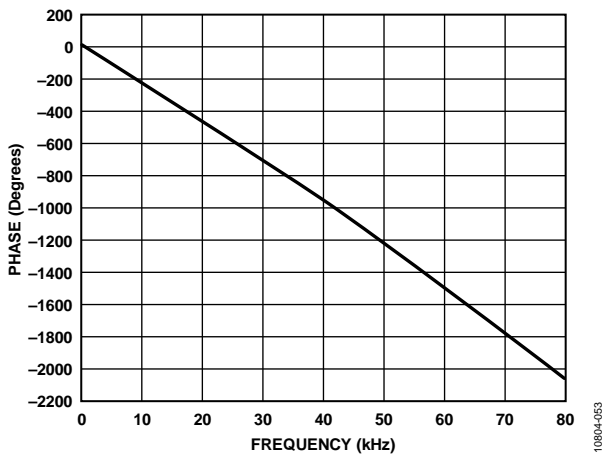


Figure 54. Phase vs. Frequency, 80 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

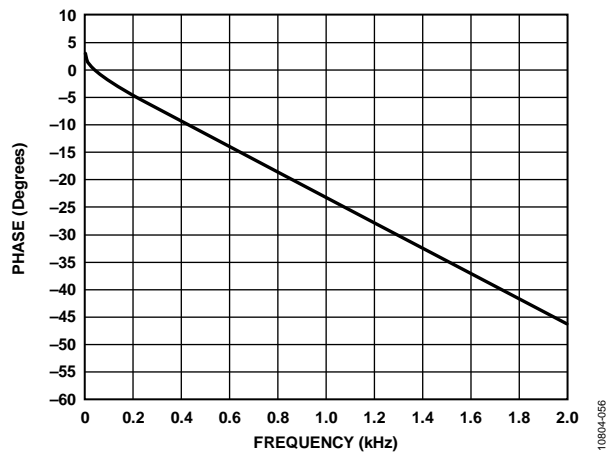


Figure 57. Phase vs. Frequency, 2 kHz Bandwidth, $f_s = 192$ kHz, Signal Path = DAC_SDATA to ASRC to DSP (Without Processing) to ASRC to ADC_SDATA0

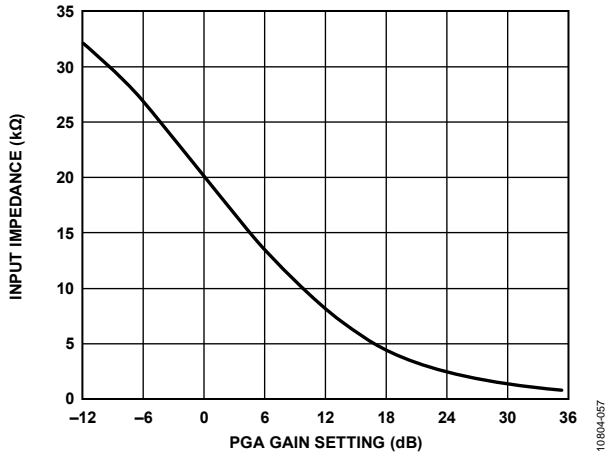


Figure 58. Input Impedance vs. PGA Gain (see the Input Impedance section)

10804-057

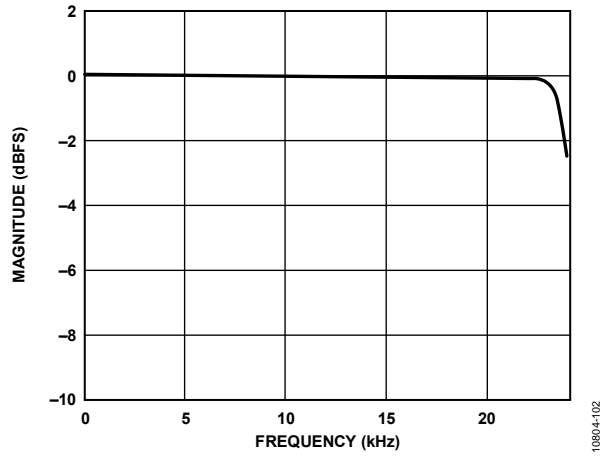


Figure 61. Decimation Pass-Band Response, $f_s = 192$ kHz

10804-102

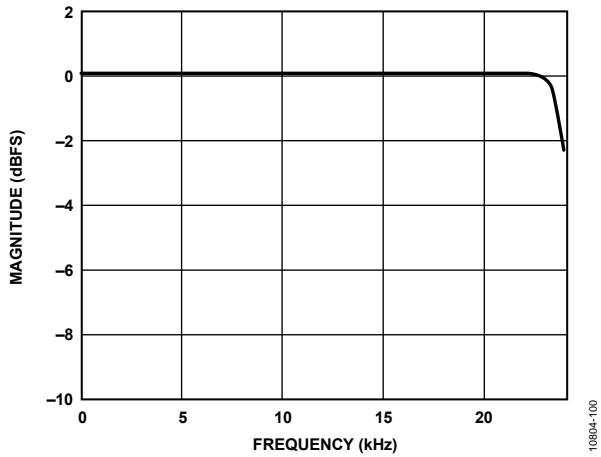


Figure 59. Decimation Pass-Band Response, $f_s = 96$ kHz

10804-100

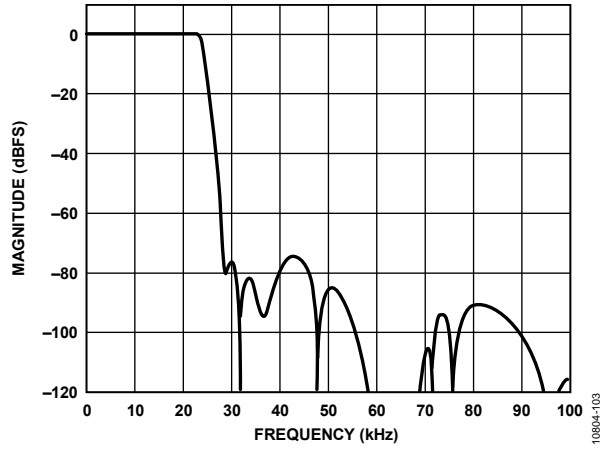


Figure 62. Total Decimation Response, Core $f_s = 192$ kHz, Serial Port $f_s = 48$ kHz

10804-103

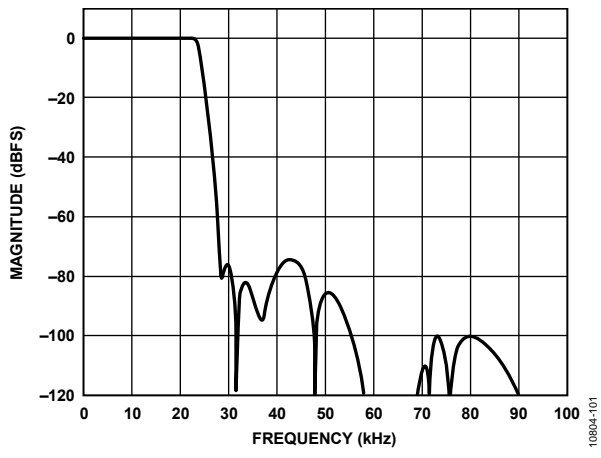


Figure 60. Total Decimation Response, Core $f_s = 96$ kHz, Serial Port $f_s = 48$ kHz

10804-101

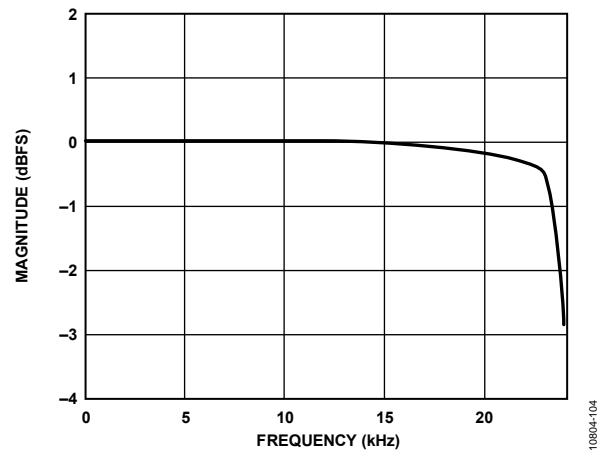


Figure 63. Interpolation Pass-Band Response, $f_s = 96$ kHz

10804-104

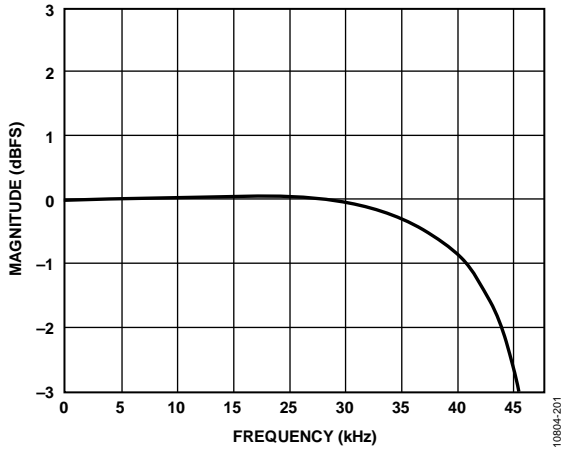


Figure 64. Decimation Pass-Band Response, Core $f_s = 96$ kHz, Serial Port $f_s = 96$ kHz

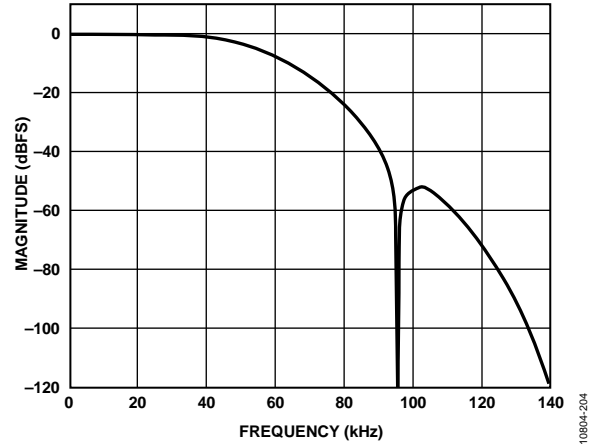


Figure 67. Total Decimation Response, Core $f_s = 96$ kHz, Serial Port $f_s = 192$ kHz

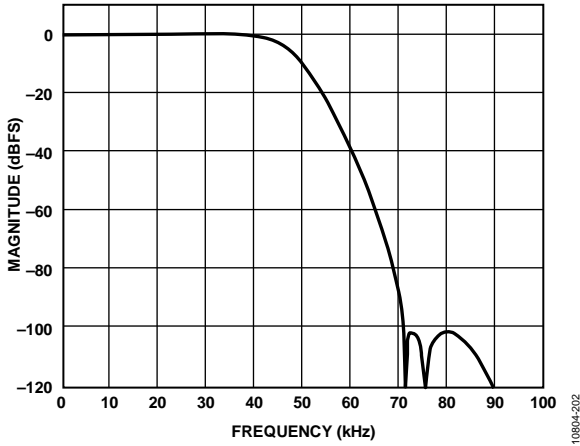


Figure 65. Total Decimation Response, Core $f_s = 96$ kHz, Serial Port $f_s = 96$ kHz

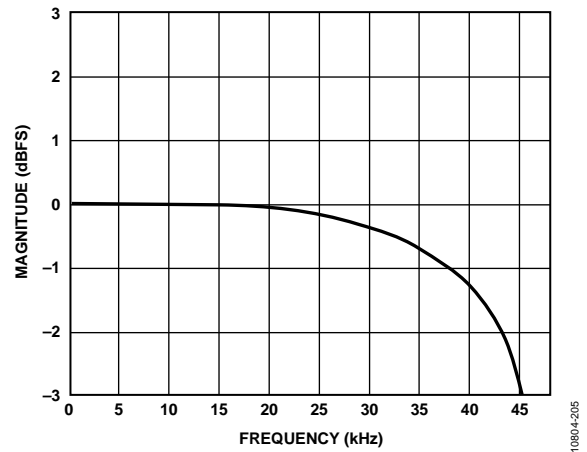


Figure 68. Decimation Pass-Band Response, Core $f_s = 192$ kHz, Serial Port $f_s = 96$ kHz

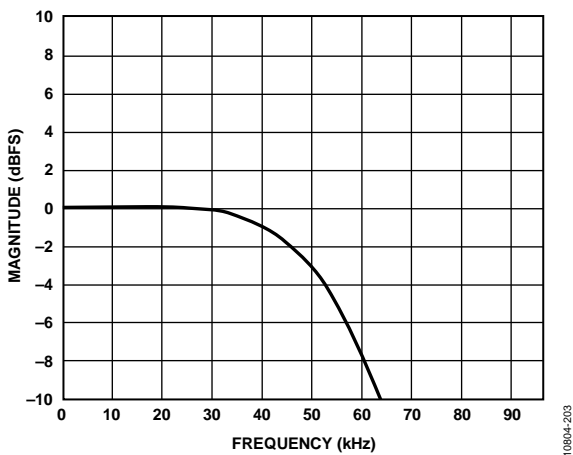


Figure 66. Decimation Pass-Band Response, Core $f_s = 96$ kHz, Serial Port $f_s = 192$ kHz

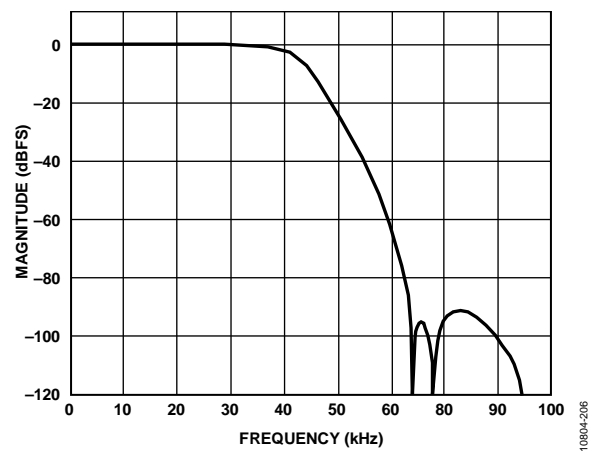


Figure 69. Total Decimation Response, Core $f_s = 192$ kHz, Serial Port $f_s = 96$ kHz

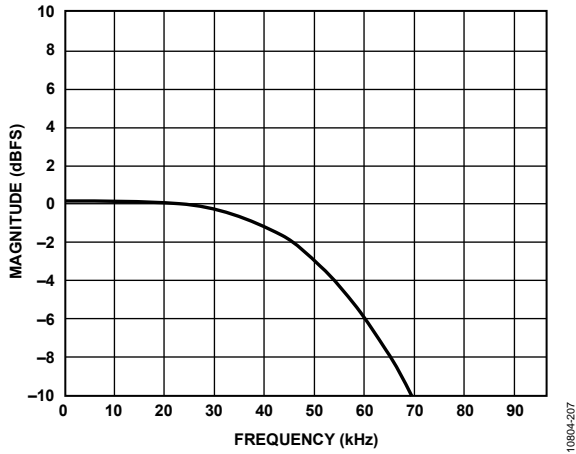


Figure 70. Decimation Pass-Band Response, Core $f_s = 192$ kHz, Serial Port $f_s = 192$ kHz

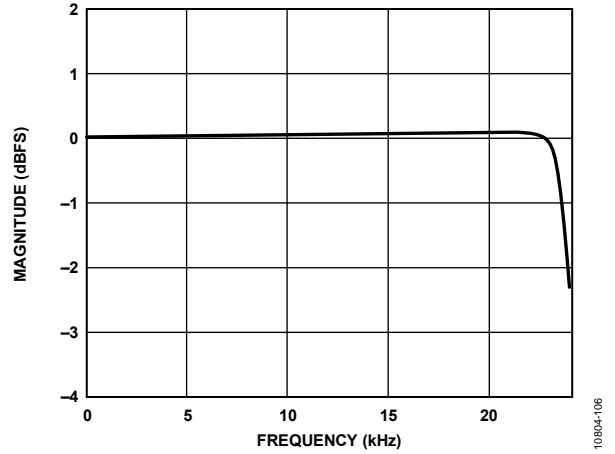


Figure 73. Interpolation Pass-Band Response, $f_s = 192$ kHz

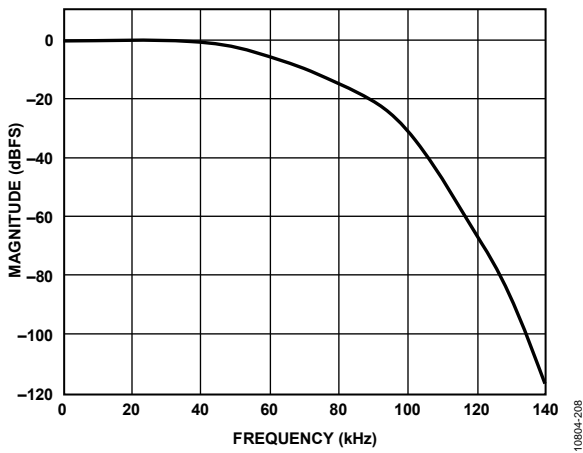


Figure 71. Total Decimation Response, Core $f_s = 192$ kHz, Serial Port $f_s = 192$ kHz

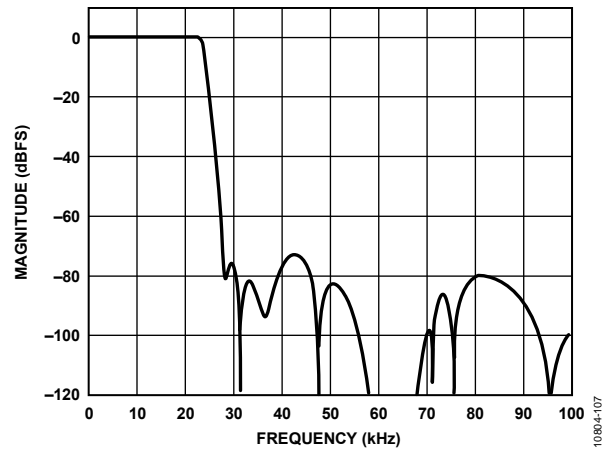


Figure 74. Total Interpolation Response, $f_s = 192$ kHz

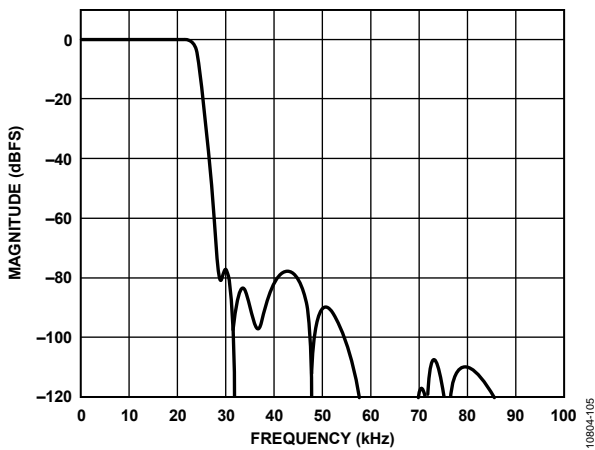


Figure 72. Total Interpolation Response, $f_s = 96$ kHz

SYSTEM BLOCK DIAGRAMS

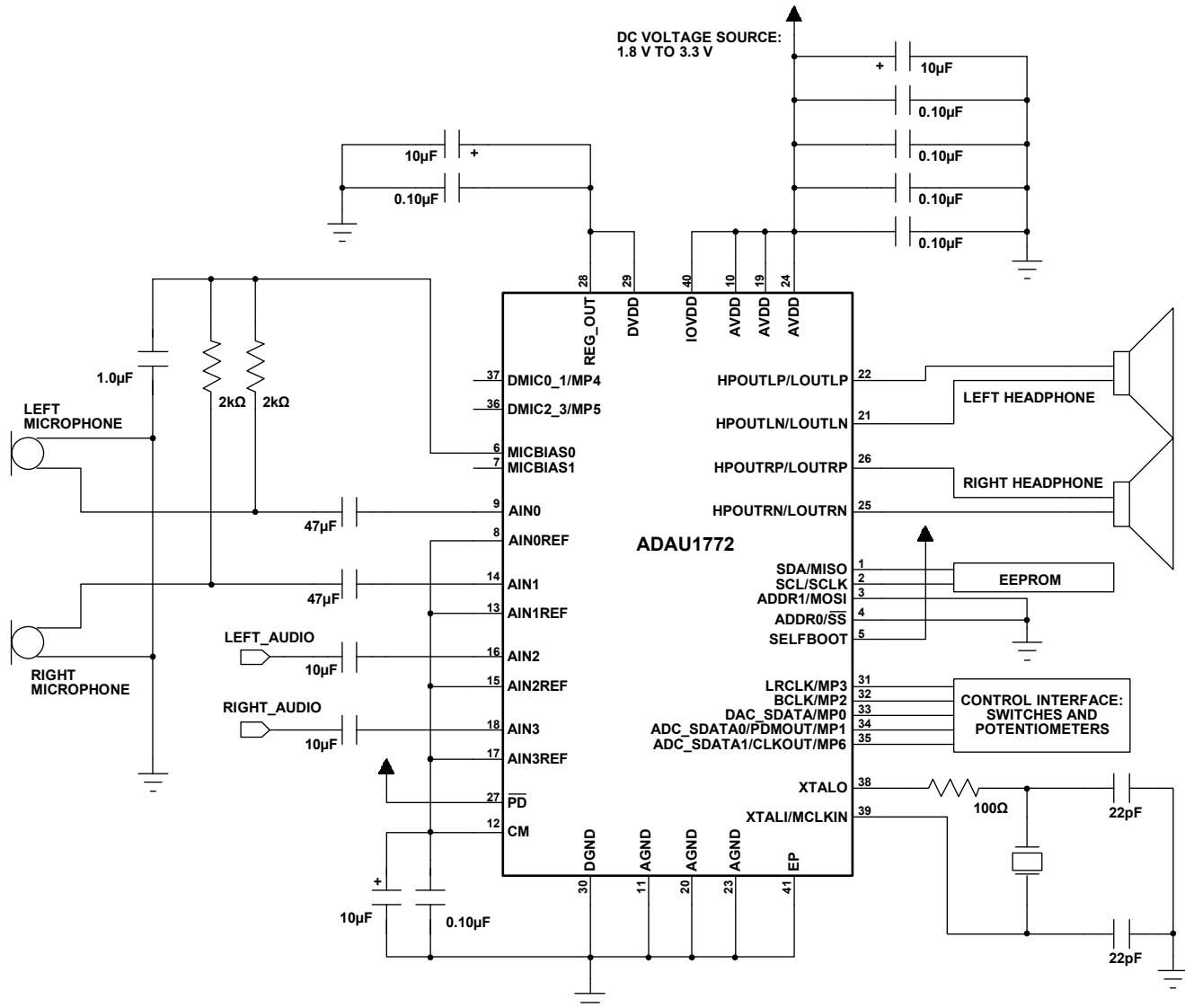


Figure 75. ADAU1772 System Block Diagram with Analog Microphones, Self-Boot Mode

10804-660

THEORY OF OPERATION

The ADAU1772 is a low power audio codec with an optimized audio processing core, making it ideal for noise cancelling applications that require high quality audio, low power, small size, and low latency. The four ADC and two DAC channels each have an SNR of at least +96 dB and a THD + N of at least -88 dB. The serial data port is compatible with I²S, left justified, right justified, and TDM modes, with tristating for interfacing to digital audio data. The operating voltage range is 1.8 V to 3.63 V, with an on-board regulator generating the internal digital supply voltage. If desired, the regulator can be powered down and the voltage can be supplied externally.

The input signal path includes flexible configurations that can accept single-ended analog microphone inputs as well as up to four digital microphone inputs. Two microphone bias pins provide seamless interfacing to electret microphones. Each input signal has its own programmable gain amplifier (PGA) for volume adjustment.

The ADCs and DACs are high quality, 24-bit Σ - Δ converters that operate at a selectable 192 kHz or 96 kHz sampling rate. The ADCs have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz. The ADCs and DACs also include very fine-step digital volume controls.

The stereo DAC output is capable of differentially driving a headphone earpiece speaker with 16 Ω impedance or higher. One side of the differential output can be powered down if single-ended operation is required. There is also the option to change to line output mode when the output is lightly loaded.

The core has a reduced instruction set that optimizes this codec for noise cancellation. The program and parameter RAMs can be loaded with custom audio processing signal flow built using the SigmaStudio™ graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM

control individual signal processing blocks. The ADAU1772 also has a self-boot function that can be used to load the program and parameter RAM along with the register settings on power-up using an external EEPROM.

The SigmaStudio software is used to program and control the core through the control port. Along with designing and tuning a signal flow, the tools can be used to configure all of the ADAU1772 registers. The SigmaStudio graphical interface allows anyone with digital or analog audio processing knowledge to easily design the DSP signal flow and port it to a target application. The interface also provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can connect graphical blocks (such as biquad filters, volume controls, and arithmetic operations), compile the design, and load the program and parameter files into the ADAU1772 memory through the control port. SigmaStudio also allows the user to download the design to an external EEPROM for self-boot operation. Signal processing blocks available in the provided libraries include the following:

- Single-precision biquad filters
- Second order filters
- Absolute value and two-input adder
- Volume controls
- Limiter

The ADAU1772 can generate its internal clocks from a wide range of input clocks by using the on-board fractional PLL. The PLL accepts inputs from 8 MHz to 27 MHz. For standalone operation, the clock can be generated using the on-board crystal oscillator.

The ADAU1772 is provided in a small, 40-lead, 6 mm × 6 mm LFCSP with an exposed bottom pad.

SYSTEM CLOCKING AND POWER-UP

CLOCK INITIALIZATION

The ADAU1772 can generate its clocks either from an externally provided clock or from a crystal oscillator. In both cases, the on-board PLL can be used or the clock can be fed directly to the core. When a crystal oscillator is used, it is desirable to use a 12.288 MHz crystal, and the crystal oscillator function must be enabled in the COREN bit (Address 0x0000). If the PLL is used, it should always be set to output 24.576 MHz. The PLL can be bypassed if a clock of 12.288 MHz or 24.576 MHz is available in the system. Bypassing the PLL saves system power.

The CC_MDIV and CC_CDIV bits should not be changed after setup, but the CLKSRC bit can be switched while the core is running.

The CC_MDIV and CC_CDIV bits should be set so that the core and internal master clock are always 12.288 MHz; for example, when using a 24.576 MHz external source clock or if using the PLL, it is necessary to use the internal divide by 2 (see Table 11).

Table 11. Clock Configuration Settings

| CC_MDIV | CC_CDIV | Description |
|---------|---------|--|
| 1 | 1 | Divide PLL/external clock by 1. Use these settings for a 12.288 MHz direct input clock source. |
| 0 | 0 | Divide PLL/external clock by 2. Use these settings for a 24.576 MHz direct input clock source or if using the PLL. |

PLL Bypass Setup

On power up, the ADAU1772 comes out of an internal reset after 12 ms. The rate of the internal master clock must be set properly using the CC_MDIV bit in the clock control register (Address 0x0000). When bypassing the PLL, the clock associated with MCLKIN must be either 12.288 MHz or 24.576 MHz. The internal master clock of the ADAU1772 is disabled until the COREN bit is asserted.

PLL Enabled Setup

The core clock of the ADAU1772 is disabled by the default setting of Bit COREN and should remain disabled during the PLL lock acquisition period. The user can poll the LOCK bit to determine when the PLL has locked. After lock is acquired, the ADAU1772 can be started by asserting the COREN bit. This bit enables the core clock for all the internal blocks of the ADAU1772.

To program the PLL during initialization or reconfiguration of the codec, the following procedure must be followed:

1. Ensure that PLL_EN (Bit 7, Address 0x0000) is set low.
2. Set/reset the PLL control registers (Address 0x0001 to Address 0x0005).
3. Enable the PLL using the PLL_EN bit.
4. Poll the PLL lock bit in Register 0x0006.
5. Set the COREN bit in Register 0x0000 after PLL lock is acquired.

Control Port Access During Initialization

During the lock acquisition period, only Register 0x0000 to Register 0x0006 are accessible through the control port. A read or write to any other register is prohibited until the core clock enable bit and the lock bit are both asserted.

After the CORE_RUN bit (Address 0x0009) is set high, the DAC_SOURCE0 and DAC_SOURCE1 register bits should not be changed. If these bits must be changed after the ADAU1772 is running, the CORE_RUN bit first must be disabled.

PLL

The PLL uses the MCLKIN signal as a reference to generate the core clock. The PLL settings are set in Register 0x0000 to Register 0x0005. Depending on the MCLK frequency, the PLL must be set for either integer or fractional mode. The PLL can accept input frequencies in the range of 8 MHz to 27 MHz.

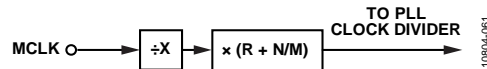


Figure 76. PLL Block Diagram

Input Clock Divider

Before reaching the PLL, the input clock signal goes through an integer clock divider to ensure that the clock frequency is within a suitable range for the PLL. The X bits in the PLL_CTRL4 register (Bits[2:1], Address 0x0005) sets the PLL input clock divide ratio.

Integer Mode

Integer mode is used when the clock input is an integer multiple of the PLL output.

For example, if MCLKIN = 12.288 MHz and $(X + 1) = 1$, and $f_s = 48$ kHz, then

$$PLL \text{ Required Output} = 24.576 \text{ MHz}$$

$$R/2 = 24.576 \text{ MHz}/12.288 \text{ MHz} = 2$$

where $R/2 = 2$ or $R = 4$.

In integer mode, the values set for N and M are ignored. Table 12 lists common integer PLL parameter settings for 48 kHz sampling rates.

Fractional Mode

Fractional mode is used when the clock input is a fractional multiple of the PLL output.

For example, if MCLKIN = 13 MHz, $(X + 1) = 1$, and $f_s = 48$ kHz, then

$$PLL \text{ Required Output} = 24.576 \text{ MHz}$$

$$(1/2) \times (R + (N/M)) = 24.576 \text{ MHz}/13 \text{ MHz} = (1/2) \times (3 + (1269/1625))$$

where:

$$R = 3.$$

$$N = 1269.$$

$$M = 1625.$$

Table 13 lists common fractional PLL parameter settings for 48 kHz sampling rates. When the PLL is used in fractional mode, it is very important that the N/M fraction be kept in the range of 0.1 to 0.9 to ensure correct operation of the PLL.

The PLL can output a clock in the range of 20.5 MHz to 27 MHz, which should be taken into account when calculating PLL values and MCLK frequencies.

CLOCK OUTPUT

The CLKOUT pin can be used as a master clock output to clock other ICs in the system or as the clock for the digital microphone inputs and PDM output. This clock can be generated from the 12.288 MHz master clock of the ADAU1772 by factors of 2, 1, $\frac{1}{2}$, $\frac{1}{4}$, and $\frac{1}{8}$. If PDM mode is enabled, only $\frac{1}{2}$, $\frac{1}{4}$, and $\frac{1}{8}$ settings produce a clock signal on CLKOUT. The factor of 2 multiplier works properly only if the input clock was previously divided by 2 using the CC_MDIV bit.

POWER SEQUENCING

AVDD and IOVDD can each be set to any voltage between 1.8 V and 3.3 V, and DVDD can be set between 1.1 V and 1.8 V or between 1.1 V and 1.2 V if using the on-board regulator.

On power-up, AVDD must be powered up before or at the same time as IOVDD. IOVDD should not be powered up when power is not applied to AVDD.

Enabling the $\overline{\text{PD}}$ pin powers down all analog and digital circuits. Before enabling $\overline{\text{PD}}$ (that is, setting it low), be sure to mute the outputs to avoid any pops when the IC is powered down.

$\overline{\text{PD}}$ can be tied directly to IOVDD for normal operation.

Power-Down Considerations

When powering down the ADAU1772, be sure to mute the outputs before AVDD power is removed; otherwise, pops or clicks may be heard. The easiest way to achieve this is to use a regulator that has a power good (PGOOD) signal to power the ADAU1772 or generate a power good signal using additional circuitry external to the regulator itself. Typically, on such regulators the power good signal changes state when the regulated voltage drops below ~90% of its target value. This power good signal can be connected to one of the ADAU1772 multipurpose pins and used to mute the DAC outputs by setting the multipurpose pin functionality to mute both DACs in Register 0x0038 to Register 0x003E. This ensures that the outputs are muted before power is completely removed.

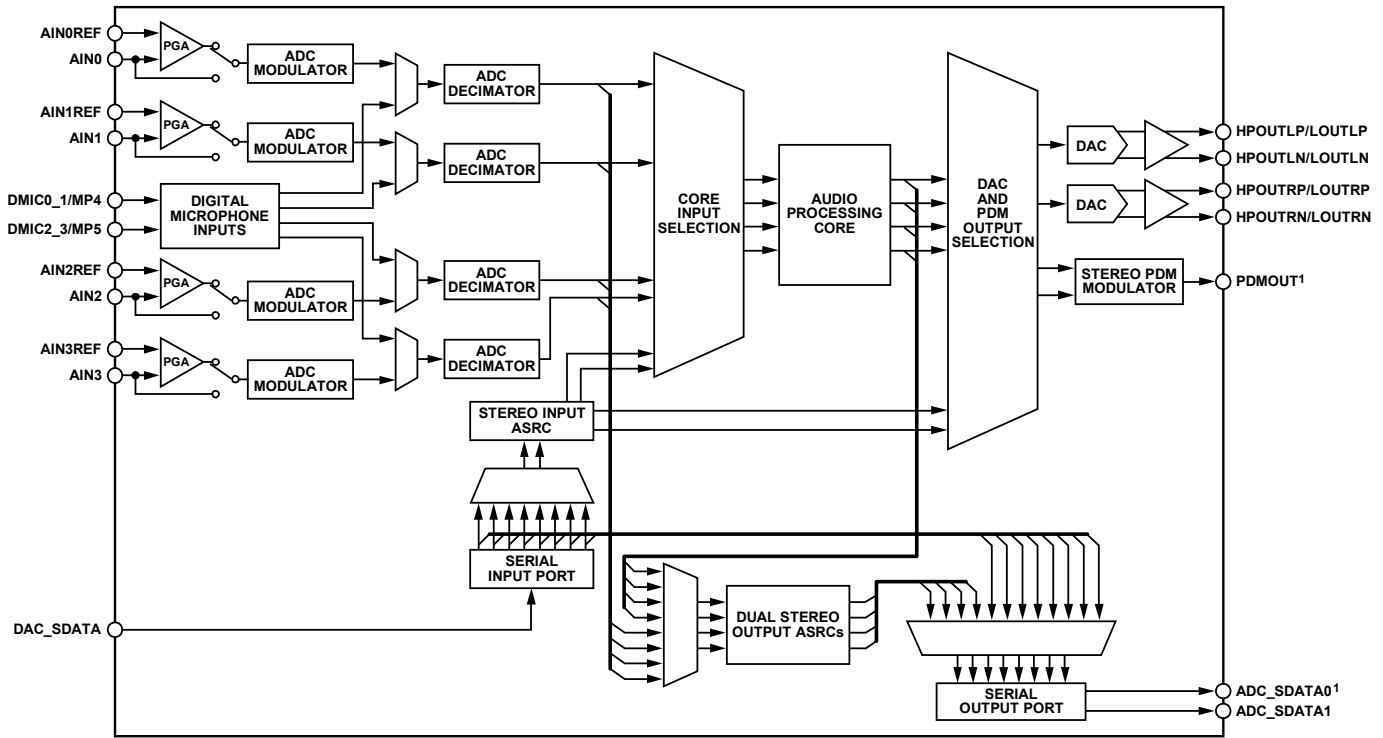
Table 12. Integer PLL Parameter Settings for PLL Output = 24.576 MHz

| MCLK Input (MHz) | Input Divider (X + 1) | Integer (R) | Denominator (M) | Numerator (N) | PLL_CTRL4 Settings (Address 0x0005) |
|------------------|-----------------------|-------------|-----------------|---------------|-------------------------------------|
| 12.288 | 1 | 4 | Don't care | Don't care | 0x20 |
| 24.576 | 1 | 2 | Don't care | Don't care | 0x10 |

Table 13. Fractional PLL Parameter Settings for PLL Output = 24.576 MHz

| MCLK Input (MHz) | Input Divider (X + 1) | Integer (R) | Denominator (M) | Numerator (N) | PLL_CTRL[4:0] Settings (Address 0x0005 to Address 0x0001) | | | | |
|------------------|-----------------------|-------------|-----------------|---------------|---|--------------------|--------------------|--------------------|--------------------|
| | | | | | PLL_CTRL4 (0x0005) | PLL_CTRL3 (0x0004) | PLL_CTRL2 (0x0003) | PLL_CTRL1 (0x0002) | PLL_CTRL0 (0x0001) |
| 8 | 1 | 6 | 125 | 18 | 0x31 | 0x12 | 0x00 | 0x7D | 0x00 |
| 13 | 1 | 3 | 1625 | 1269 | 0x19 | 0xF5 | 0x04 | 0x59 | 0x06 |
| 14.4 | 2 | 6 | 75 | 62 | 0x33 | 0x3E | 0x00 | 0x4B | 0x00 |
| 19.2 | 2 | 5 | 25 | 3 | 0x2B | 0x03 | 0x00 | 0x19 | 0x00 |
| 26 | 2 | 3 | 1625 | 1269 | 0x1B | 0xF5 | 0x04 | 0x59 | 0x06 |
| 27 | 2 | 3 | 1125 | 721 | 0x1B | 0xD1 | 0x02 | 0x65 | 0x04 |

SIGNAL ROUTING



¹THE ADC_SDATA0 AND PDMOUT FUNCTIONS SHARE A PHYSICAL PIN, SO ONLY ONE OF THESE FUNCTIONS CAN BE USED AT A TIME.

Figure 77. Input and Output Signal Routing

10894-102Z

INPUT SIGNAL PATHS

There are four input paths, from either an ADC or a digital microphone, that can be routed to the core. The input sources (ADC or digital microphone) must be configured in pairs (for example, 0 and 1, 2 and 3), but each channel can be routed individually. The core inputs can also be sourced from a stereo input ASRC.

ANALOG INPUTS

The ADAU1772 can accept both line level and microphone inputs. Each of the four analog input channels can be configured in a single-ended mode or a single-ended with PGA mode. There are also inputs for up to four digital microphones. The analog inputs are biased at $AVDD/2$. Unused input pins should be connected to the CM pin or ac-coupled to ground.

Signal Polarity

Signals routed through the PGAs are inverted. As a result, signals input through the PGA are output from the ADCs with a polarity that is opposite that of the input. Single-ended inputs are not inverted. The ADCs are noninverting.

Input Impedance

The input impedance of the analog inputs varies with the gain of the PGA. This impedance ranges from 0.68 k Ω at the 35.25 dB gain setting to 32.0 k Ω at the -12 dB setting. The input impedance on each pin can be calculated as follows:

$$R_{IN} = \frac{40}{10^{(Gain/20)} + 1} \text{ k}\Omega$$

where *Gain* is set by PGA_GAINx.

The optional 10 dB PGA boost set in PGA_x_BOOST does not affect the input impedance. This is an alternative way of increasing gain without decreasing input impedance; however, it causes some degradation in performance.

Analog Microphone Inputs

For microphone signals, the ADAU1772 analog inputs can be configured in single-ended with PGA mode.

The PGA settings are controlled in Register 0x0023 to Register 0x0026. The PGA is enabled by setting the PGA_ENx bits.

Connect the AINxREF pins to the CM pin and connect the microphone signal to the inverting input of the PGAs (AINx), as shown in Figure 78.

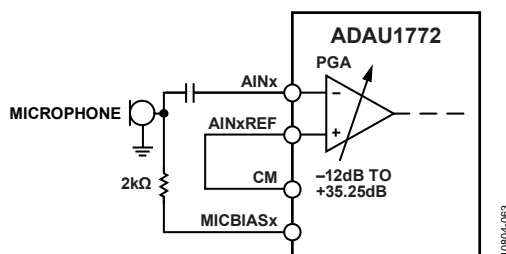


Figure 78. Single-Ended Microphone Configuration

Analog Line Inputs

Line level signals can be input on the AINx pins of the analog inputs. Figure 79 shows a single-ended line input using the AINx pins. The AINxREF pins should be tied to CM. When using single-ended line input, the PGA should be disabled using the PGA_ENx bits, and the corresponding PGA pop suppression bit should be disabled using the POP_SUPPRESS register (Address 0x0029).

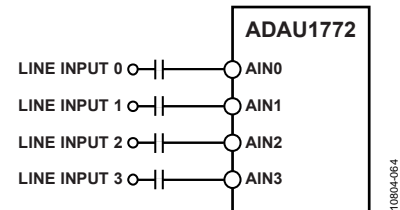


Figure 79. Single-Ended Line Inputs

Precharging Input Capacitors

Precharge amplifiers are enabled by default to quickly charge large series capacitors on the inputs and outputs. Precharging these capacitors helps to prevent pops in the audio signal. The precharge circuits are powered up by default on startup and can be disabled in the POP_SUPPRESS register. The precharge amplifiers are automatically disabled when the PGA or headphone amplifiers are enabled. For unused PGAs and headphone outputs, these precharge amplifiers should be disabled using the POP_SUPPRESS register. The precharging time is dependent on the input/output series capacitors. The impedance looking into the pin is 500 Ω in this mode. However, at startup, the impedance looking into the pin is dominated by the time constant of the CM pin because the precharge amplifiers reference the CM voltage.

Microphone Bias

The ADAU1772 includes two microphone bias outputs: MICBIAS0 and MICBIAS1. These pins provide a voltage reference for electret analog microphones. The MICBIASx pins can also be used to cleanly supply voltage to digital or analog MEMS microphones with separate power supply pins. The MICBIASx voltage is set in the microphone bias control register (Address 0x002D). Using this register, either the MICBIAS0 or MICBIAS1 output can be enabled and disabled. The gain options provide two possible voltages: $0.65 \times AVDD$ or $0.90 \times AVDD$.

Many applications require enabling only one of the two bias outputs. The two bias outputs should both be enabled when many microphones are used in the system or when the positioning of the microphones on the PCB does not allow one pin to bias all microphones.

DIGITAL MICROPHONE INPUT

When using a digital microphone connected to the DMIC0_1/MP4 and DMIC2_3/MP5 pins, the DCM_0_1 and DCM_2_3 bits in Register 0x001D and Register 0x001E must be set to enable the digital microphone signal paths. The pin functions should also be set to digital microphone input in the corresponding pin mode registers (Address 0x003C and Address 0x003D). The DMIC0/DMIC2 and DMIC1/DMIC3 channels can be swapped (left/right swap) by writing to the DMIC_SW0 and DMIC_SW1 bits in the ADC_CONTROL2 and ADC_CONTROL3 registers (Address 0x001D and Address 0x001E). In addition, the microphone polarity can be reversed by setting the DMIC_POLx bit, which reverses the phase of the incoming audio by 180°.

The digital microphone inputs are clocked from the CLKOUT pin. The digital microphone data stream must be clocked by this pin and not by a clock from another source, such as another audio IC, even if the other clock is of the same frequency as CLKOUT.

The digital microphone signal bypasses the analog input path and the ADCs and is routed directly into the decimation filters. The digital microphone and the ADCs share digital filters and, therefore, both cannot be used simultaneously. The digital microphone inputs are enabled in pairs. The ADAU1772 inputs can be set for either four analog inputs, four digital microphone inputs, or two analog inputs and two digital microphone inputs. Figure 80 depicts the digital microphone interface and signal routing.

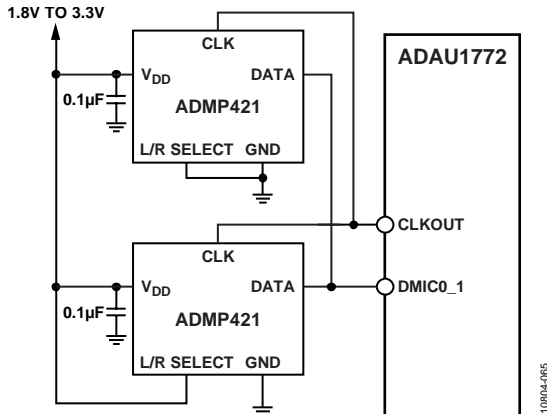


Figure 80. Digital Microphone Interface Block Diagram

Figure 80 shows two ADMP421 digital microphones connected to Pin DMIC0_1 of the ADAU1772. These microphones could also be connected to DMIC2_3 if that signal path is to be used for digital microphones. If more than two digital microphones are to be used in a system, then up to two microphones would be connected to both DMIC0_1 and DMIC2_3 and the CLKOUT signal would be fanned out to the clock input of all of the microphones.

ANALOG-TO-DIGITAL CONVERTERS

The ADAU1772 includes four 24-bit Σ-Δ analog-to-digital converters (ADCs) with a selectable sample rate of 192 kHz or 96 kHz.

ADC Full-Scale Level

The full-scale input to the ADCs (0 dBFS) scales linearly with AVDD. At AVDD = 3.3 V, the full-scale input level is 1 V rms. Signal levels above the full-scale value cause the ADCs to clip.

Digital ADC Volume Control

The volume setting of each ADC can be digitally attenuated in the ADCx_VOLUME registers (Address 0x001F to Address 0x0022). The volume can be set between 0 dB and -95.625 dB in 0.375 dB steps. The ADC volume can also be digitally muted in the ADC_CONTROLx registers (Address 0x001B to Address 0x001E).

High-Pass Filter

A high-pass filter is available on the ADC path to remove dc offsets; this filter can be enabled or disabled using the HP_x_x_EN bits. At fs = 192 kHz, the corner frequency of this high-pass filter can be set to 1 Hz, 4 Hz, or 8 Hz.

OUTPUT SIGNAL PATHS

Data from the serial input port can be routed to the core either directly or through a sample rate converter. Data can be routed to the serial output port, the stereo DAC, and the stereo PDM modulator.

The analog outputs of the ADAU1772 can be configured as differential or single-ended outputs. The analog output pins are capable of driving headphone or earpiece speakers. The line outputs can drive a load of at least 10 k Ω or can be put into headphone mode to drive headphones or earpiece speakers. The analog output pins are biased at AVDD/2.

ANALOG OUTPUTS

Headphone Output

The output pins can be driven by either a line output driver or a headphone driver by setting the HP_EN_L and HP_EN_R bits in the headphone line output select register (Address 0x0043). The headphone outputs can drive a load of at least 16 Ω .

Headphone Output Power-Up Sequencing

To prevent pops when turning on the headphone outputs, the user must wait at least 6 ms to unmute these outputs after enabling the headphone output using the HP_EN_x bits. Waiting 6 ms allows an internal capacitor to charge before these outputs are used. Figure 81 illustrates the headphone output power-up sequencing.

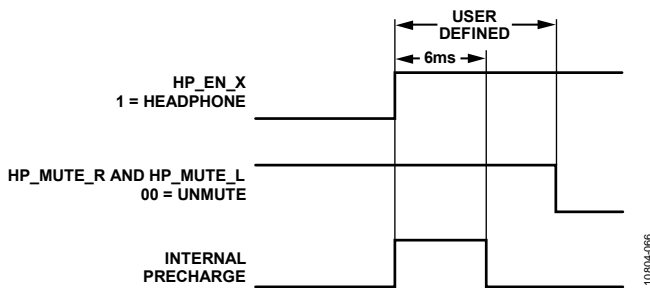


Figure 81. Headphone Output Power-Up Timing

Ground-Centered Headphone Configuration

The headphone outputs can also be configured as ground-centered outputs by connecting coupling capacitors in series with the output pins. Ground-centered headphones should use the AGND pin as the ground reference.

When the headphone outputs are configured in this manner, the capacitors create a high-pass filter on the outputs. The corner frequency of this filter, which has an attenuation of 3 dB at this point, is calculated by the following formula:

$$f_{3dB} = 1/(2\pi \times R \times C)$$

where :

R is the impedance of the headphones.

C is the capacitor value.

For a typical headphone impedance of 32 Ω and a 220 μF capacitor, the corner frequency is 23 Hz.

Pop-and-Click Suppression

On power-up, the precharge circuitry is enabled on all four analog output pins to suppress pops and clicks. After power-up, the precharge circuitry can be put into a low power mode using the HP_POP_DISx bits in the POP_SUPPRESS register (Address 0x0029).

The precharge time depends on the value of the capacitor connected to the CM pin and the RC time constant of the load on the output pin. For a typical line output load, the precharge time is between 2 ms and 3 ms. After this precharge time, the HP_POP_DISx bit can be set to low power mode.

To avoid clicks and pops, all analog outputs that are in use should be muted while changing any register settings that may affect the signal path. These outputs can then be unmuted after the changes have been made.

Line Outputs

The analog output pins (HPOUTLP/LOUTLP, HPOUTLN/LOUTLN, HPOUTRP/LOUTRP, and HPOUTRN/LOUTRN) can be used to drive both differential and single-ended loads. In their default settings, these pins can drive typical line loads of 10 k Ω or greater.

When the line output pins are used in single-ended mode, the HPOUTLP/LOUTLP and HPOUTRP/LOUTRP pins should be used to output the signals, and the HPOUTLN/LOUTLN and HPOUTRN/LOUTRN pins should be powered down.

DIGITAL-TO-ANALOG CONVERTERS

The ADAU1772 includes two 24-bit Σ - Δ digital-to-analog converters (DACs).

DAC Full-Scale Level

The full-scale output from the DACs (0 dBFS) scales linearly with AVDD. At AVDD = 3.3 V, the full-scale output level is 1.94 V rms for a differential output or 0.97 V rms for a single-ended output.

Digital DAC Volume Control

The volume of each DAC can be digitally attenuated using the DACx_VOLUME registers (Address 0x002F and Address 0x0030). The volume can be set to be between 0 dB and -95.625 dB in 0.375 dB steps.

PDM OUTPUT

The ADAU1772 includes a 2-channel pulse density modulated (PDM) modulator. The PDMOUT pin can be used to drive a PDM input amplifier, such as the SSM2517 mono 2.4 W amplifier. Two SSM2517 devices can be connected to the PDMOUT data stream to enable a stereo output. The PDM output signal is clocked by the CLKOUT pin output. The PDM output stream must be clocked by this pin and not by a clock from another source, such as another audio IC, even if the other clock is of the same frequency as CLKOUT. The PDM output data is clipped at the -6 dB level to prevent overdriving a connected amplifier like the SSM2517.

The ADAU1772 has the ability to output PDM control patterns to configure devices such as the SSM2517. Each pattern is a byte long and is written with a user defined pattern in the PDM_PATTERN register (Address 0x0037). The control pattern is enabled and the output channel selection is configured in the PDM_OUT register (Address 0x0036). The PDM pattern should not be changed while the ADAU1772 is outputting the control pattern to the external device. After the external device is configured, the control pattern can be disabled. For the SSM2517, the control pattern must be repeated a minimum of 128 times to configure the part. Table 14 describes typical control patterns for the SSM2517.

Table 14. SSM2517 PDM Control Pattern Descriptions

| Pattern | Control Description |
|---------|--|
| 0xAC | Power-down. All blocks off except for the PDM interface. Normal start-up time. |
| 0xD8 | Gain optimized for PVDD = 5 V operation. Overrides GAIN_FS pin setting. |
| 0xD4 | Gain optimized for PVDD = 3.6 V operation. Overrides GAIN_FS pin setting. |
| 0xD2 | Gain optimized for PVDD = 2.5 V operation. Overrides GAIN_FS pin setting. |
| 0xD1 | f _s set to opposite value determined by GAIN_FS pin. |
| 0xE1 | Ultralow EMI mode. |
| 0xE2 | Half clock cycle pulse mode for power savings. |
| 0xE4 | Special 32 kHz/128 × f _s operation mode. |

ASYNCHRONOUS SAMPLE RATE CONVERTERS

The ADAU1772 includes asynchronous sample rate converters (ASRCs) to enable synchronous full-duplex operation of the serial ports. Two stereo ASRCs are available for the digital outputs, and one stereo ASRC is available for the digital input signals.

The ASRCs can convert serial output data from the core rate of up to 192 kHz back down to less than 8 kHz. All intermediate frequencies and ratios are also supported.

SIGNAL LEVELS

The ADCs, DACs, and ASRCs have fixed gain settings that should be considered when configuring the system. These settings were chosen to maximize performance of the converters and to ensure that there is 0 dB gain for any signal path from the input of the ADAU1772 to its output. Therefore, the full-scale level of a signal in the processing core will be slightly different from a full-scale level external to the IC.

Input paths, such as through the ADCs and input ASRCs, are scaled by 0.75, or about -2.5 dB. Output paths, such as through the DACs or output ASRCs, are scaled by 1.33, or about 2.5 dB. This is shown in Figure 82.

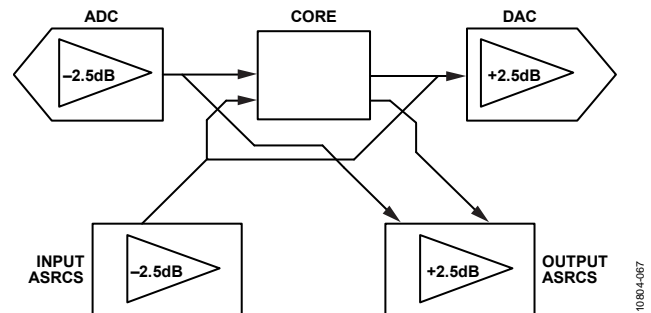


Figure 82. Signal Level Diagram

Because of this input and output scaling, output signals from the core should be limited to -2.5 dB full scale to prevent the DACs and ASRCs from clipping.

SIGNAL PROCESSING

The ADAU1772 processing core is optimized for active noise cancelling (ANC) processing. The processing capabilities of the core include biquad filters, limiters, volume controls, and mixing. The core has four inputs and four outputs. The core is controlled with a 10-bit program word, with a maximum of 32 instructions per frame.

INSTRUCTIONS

A complete list of instructions/processing blocks along with documentation can be found in the SigmaStudio software for the ADAU1772. The processing blocks available are

- Single-precision biquad/second order filters
- Absolute value
- Two-input addition
- T connection in SigmaStudio
- Limiter with/without external detector loop
- Linear gain
- Volume slider
- Mute
- DBREG level detection

DATA MEMORY

The ADAU1772 data path is 26 bits (5.21 format). The data memory is 32 words of 2×26 bits. The double length memory enables the core to double precision arithmetic with double length data and single length coefficients.

PARAMETERS

Parameters, such as filter coefficients, limiter settings, and volume control settings, are saved in parameter registers. Each parameter is a 32-bit number. The format of this number depends on whether it is controlling a filter or a limiter. The number formats of different parameters are shown in Table 15. When the parameter formats use less than the full 32-bit memory space, as with the limiter parameters, the data is LSB-aligned.

Table 15. Parameter Number Formats

| Parameter Type | Format |
|---------------------------------|----------------------|
| Filter Coefficient (B0, B1, B2) | 5.27 |
| Filter Coefficient (A1) | 2.27 (sign extended) |
| Filter Coefficient (A2) | 1.27 (sign extended) |
| Maximum Gain | 2.23 |
| Minimum Gain | 2.23 |
| Attack Time | 24.0 |
| Decay Time | 24.0 |
| Threshold | 2.23 |

There are two parameter banks available. Each bank can hold a full set of 160 parameters (32 filters \times 5 coefficients). Users can switch between Bank A and Bank B, allowing for two sets of parameters to be saved in memory and switched on the fly

while the codec is running. Bank switching can be achieved by writing to the CORE_CONTROL register (Address 0x0009) or by using the multipurpose push-button switches, but not using a combination of the two. Parameters in the active bank should not be updated while the core is running; this will likely result in noises on the outputs.

Parameters are assigned to instructions in the order in which the instructions are instantiated in the code. The instruction types that use parameters are the biquad filters and limiters.

Table 17 shows the addresses of each parameter in Bank A that are associated with each of the 32 instructions, and Table 18 shows the addresses of each parameter in Bank B. Table 16 shows the addresses of the LSB aligned, 10-bit program words.

Table 16. Program Addresses

| Instruction | Instruction Address |
|-------------|---------------------|
| 0 | 0x0080 |
| 1 | 0x0081 |
| 2 | 0x0082 |
| 3 | 0x0083 |
| 4 | 0x0084 |
| 5 | 0x0085 |
| 6 | 0x0086 |
| 7 | 0x0087 |
| 8 | 0x0088 |
| 9 | 0x0089 |
| 10 | 0x008A |
| 11 | 0x008B |
| 12 | 0x008C |
| 13 | 0x008D |
| 14 | 0x008E |
| 15 | 0x008F |
| 16 | 0x0090 |
| 17 | 0x0091 |
| 18 | 0x0092 |
| 19 | 0x0093 |
| 20 | 0x0094 |
| 21 | 0x0095 |
| 22 | 0x0096 |
| 23 | 0x0097 |
| 24 | 0x0098 |
| 25 | 0x0099 |
| 26 | 0x009A |
| 27 | 0x009B |
| 28 | 0x009C |
| 29 | 0x009D |
| 30 | 0x009E |
| 31 | 0x009F |

Table 17. Parameter Addresses, Bank A

| Assignment Order | B0/Max Gain | B1/Min Gain | B2/Attack | A1/Decay | A2/Threshold |
|------------------|-------------|-------------|-----------|----------|--------------|
| 0 | 0x00E0 | 0x0100 | 0x0120 | 0x0140 | 0x0160 |
| 1 | 0x00E1 | 0x0101 | 0x0121 | 0x0141 | 0x0161 |
| 2 | 0x00E2 | 0x0102 | 0x0122 | 0x0142 | 0x0162 |
| 3 | 0x00E3 | 0x0103 | 0x0123 | 0x0143 | 0x0163 |
| 4 | 0x00E4 | 0x0104 | 0x0124 | 0x0144 | 0x0164 |
| 5 | 0x00E5 | 0x0105 | 0x0125 | 0x0145 | 0x0165 |
| 6 | 0x00E6 | 0x0106 | 0x0126 | 0x0146 | 0x0166 |
| 7 | 0x00E7 | 0x0107 | 0x0127 | 0x0147 | 0x0167 |
| 8 | 0x00E8 | 0x0108 | 0x0128 | 0x0148 | 0x0168 |
| 9 | 0x00E9 | 0x0109 | 0x0129 | 0x0149 | 0x0169 |
| 10 | 0x00EA | 0x010A | 0x012A | 0x014A | 0x016A |
| 11 | 0x00EB | 0x010B | 0x012B | 0x014B | 0x016B |
| 12 | 0x00EC | 0x010C | 0x012C | 0x014C | 0x016C |
| 13 | 0x00ED | 0x010D | 0x012D | 0x014D | 0x016D |
| 14 | 0x00EE | 0x010E | 0x012E | 0x014E | 0x016E |
| 15 | 0x00EF | 0x010F | 0x012F | 0x014F | 0x016F |
| 16 | 0x00F0 | 0x0110 | 0x0130 | 0x0150 | 0x0170 |
| 17 | 0x00F1 | 0x0111 | 0x0131 | 0x0151 | 0x0171 |
| 18 | 0x00F2 | 0x0112 | 0x0132 | 0x0152 | 0x0172 |
| 19 | 0x00F3 | 0x0113 | 0x0133 | 0x0153 | 0x0173 |
| 20 | 0x00F4 | 0x0114 | 0x0134 | 0x0154 | 0x0174 |
| 21 | 0x00F5 | 0x0115 | 0x0135 | 0x0155 | 0x0175 |
| 22 | 0x00F6 | 0x0116 | 0x0136 | 0x0156 | 0x0176 |
| 23 | 0x00F7 | 0x0117 | 0x0137 | 0x0157 | 0x0177 |
| 24 | 0x00F8 | 0x0118 | 0x0138 | 0x0158 | 0x0178 |
| 25 | 0x00F9 | 0x0119 | 0x0139 | 0x0159 | 0x0179 |
| 26 | 0x00FA | 0x011A | 0x013A | 0x015A | 0x017A |
| 27 | 0x00FB | 0x011B | 0x013B | 0x015B | 0x017B |
| 28 | 0x00FC | 0x011C | 0x013C | 0x015C | 0x017C |
| 29 | 0x00FD | 0x011D | 0x013D | 0x015D | 0x017D |
| 30 | 0x00FE | 0x011E | 0x013E | 0x015E | 0x017E |
| 31 | 0x00FF | 0x011F | 0x013F | 0x015F | 0x017F |

Table 18. Parameter Addresses, Bank B

| Assignment Order | B0/Max Gain | B1/Min Gain | B2/Attack | A1/Decay | A2/Threshold |
|------------------|-------------|-------------|-----------|----------|--------------|
| 0 | 0x0180 | 0x01A0 | 0x01C0 | 0x01E0 | 0x0200 |
| 1 | 0x0181 | 0x01A1 | 0x01C1 | 0x01E1 | 0x0201 |
| 2 | 0x0182 | 0x01A2 | 0x01C2 | 0x01E2 | 0x0202 |
| 3 | 0x0183 | 0x01A3 | 0x01C3 | 0x01E3 | 0x0203 |
| 4 | 0x0184 | 0x01A4 | 0x01C4 | 0x01E4 | 0x0204 |
| 5 | 0x0185 | 0x01A5 | 0x01C5 | 0x01E5 | 0x0205 |
| 6 | 0x0186 | 0x01A6 | 0x01C6 | 0x01E6 | 0x0206 |
| 7 | 0x0187 | 0x01A7 | 0x01C7 | 0x01E7 | 0x0207 |
| 8 | 0x0188 | 0x01A8 | 0x01C8 | 0x01E8 | 0x0208 |
| 9 | 0x0189 | 0x01A9 | 0x01C9 | 0x01E9 | 0x0209 |
| 10 | 0x018A | 0x01AA | 0x01CA | 0x01EA | 0x020A |
| 11 | 0x018B | 0x01AB | 0x01CB | 0x01EB | 0x020B |
| 12 | 0x018C | 0x01AC | 0x01CC | 0x01EC | 0x020C |
| 13 | 0x018D | 0x01AD | 0x01CD | 0x01ED | 0x020D |
| 14 | 0x018E | 0x01AE | 0x01CE | 0x01EE | 0x020E |
| 15 | 0x018F | 0x01AF | 0x01CF | 0x01EF | 0x020F |

| Assignment Order | B0/Max Gain | B1/Min Gain | B2/Attack | A1/Decay | A2/Threshold |
|------------------|-------------|-------------|-----------|----------|--------------|
| 16 | 0x0190 | 0x01B0 | 0x01D0 | 0x01F0 | 0x0210 |
| 17 | 0x0191 | 0x01B1 | 0x01D1 | 0x01F1 | 0x0211 |
| 18 | 0x0192 | 0x01B2 | 0x01D2 | 0x01F2 | 0x0212 |
| 19 | 0x0193 | 0x01B3 | 0x01D3 | 0x01F3 | 0x0213 |
| 20 | 0x0194 | 0x01B4 | 0x01D4 | 0x01F4 | 0x0214 |
| 21 | 0x0195 | 0x01B5 | 0x01D5 | 0x01F5 | 0x0215 |
| 22 | 0x0196 | 0x01B6 | 0x01D6 | 0x01F6 | 0x0216 |
| 23 | 0x0197 | 0x01B7 | 0x01D7 | 0x01F7 | 0x0217 |
| 24 | 0x0198 | 0x01B8 | 0x01D8 | 0x01F8 | 0x0218 |
| 25 | 0x0199 | 0x01B9 | 0x01D9 | 0x01F9 | 0x0219 |
| 26 | 0x019A | 0x01BA | 0x01DA | 0x01FA | 0x021A |
| 27 | 0x019B | 0x01BB | 0x01DB | 0x01FB | 0x021B |
| 28 | 0x019C | 0x01BC | 0x01DC | 0x01FC | 0x021C |
| 29 | 0x019D | 0x01BD | 0x01DD | 0x01FD | 0x021D |
| 30 | 0x019E | 0x01BE | 0x01DE | 0x01FE | 0x021E |
| 31 | 0x019F | 0x01BF | 0x01DF | 0x01FF | 0x021F |

CONTROL PORT

The ADAU1772 has both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the memories and registers. The IC defaults to I²C mode but can be put into SPI control mode by pulling the \overline{SS} pin low three times.

The control port is capable of full read/write operation for all addressable memories and registers. Most signal processing parameters are controlled by writing new values to the parameter memories using the control port. Other functions, such as mute and input/output mode control, are programmed through the registers.

All addresses can be accessed in either single-address mode or burst mode. The first byte (Byte 0) of a control port write contains the 7-bit IC address plus the R/W bit. The next two bytes (Byte 1 and Byte 2) are the 16-bit subaddress of the memory or register location within the ADAU1772. All subsequent bytes (starting with Byte 3) contain the data, such as register data, program data, or parameter data. The number of bytes per word depends on the type of data that is being written. Table 19 shows the word length of the ADAU1772's different data types. The exact formats for specific types of writes are shown in Figure 85 and Figure 86.

Table 19. Data Word Sizes

| Data Type | Word Size (bytes) |
|------------|-------------------|
| Registers | 1 |
| Program | 2 |
| Parameters | 4 |

If large blocks of data need to be downloaded to the ADAU1772, the output of the core can be halted (using the CORE_RUN bit in the core control register (Address 0x0009)), new data can be loaded, and then the core can be restarted. This is typically done during the booting sequence at start-up or when loading a new program into memory.

Registers and bits shown as reserved in the register map read back 0s. When writing to these registers and bits, such as during a burst write across a reserved register, or when writing to reserved bits in a register with other used bits, write 0s.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 20 details these multiple functions.

Table 20. Control Port Pin Functions

| Pin | I ² C Mode | SPI Mode |
|------------------------|--------------------------------------|------------------------|
| SCL/SCLK | SCL—input | SCLK—input |
| SDA/MISO | SDA—open-collector output | MISO—output |
| ADDR1/MOSI | I ² C Address Bit 1—input | MOSI—input |
| ADDR0/ \overline{SS} | I ² C Address Bit 0—input | \overline{SS} —input |

BURST MODE COMMUNICATION

Burst mode addressing, in which the subaddresses are automatically incremented at word boundaries, can be used for writing

large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless the control port communication is stopped (that is, a stop condition is issued for I²C, or \overline{SS} is brought high for SPI). The registers and RAMs in the ADAU1772 range in width from one to four bytes, so the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location).

I²C PORT

The ADAU1772 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. I²C uses two pins—serial data (SDA) and serial clock (SCL)—to carry data between the ADAU1772 and the system I²C master controller. In I²C mode, the ADAU1772 is always a slave on the bus, except when the IC is self-booting. See the Self-Boot section for details about using the ADAU1772 in self-boot mode.

Each slave device is recognized by a unique 7-bit address. The ADAU1772 I²C address format is shown in Table 21. The LSB of this first byte sent from the I²C master sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Pin ADDR0 and Pin ADDR1 set the LSBs of the I²C address (Table 22); therefore, each ADAU1772 can be set to one of four unique addresses. This allows multiple ICs to exist on the same I²C bus without address contention. The 7-bit I²C addresses are shown in Table 22.

An I²C data transfer is always terminated by a stop condition.

Both SDA and SCL should have 2.0 k Ω pull-up resistors on the lines connected to them. The voltage on these signal lines should not be higher than IOVDD.

Table 21. I²C Address Format

| Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|
| 0 | 1 | 1 | 1 | 1 | ADDR1 | ADDR0 |

Table 22. I²C Addresses

| ADDR1 | ADDR0 | Slave Address |
|-------|-------|---------------|
| 0 | 0 | 0x3C |
| 0 | 1 | 0x3D |
| 1 | 0 | 0x3E |
| 1 | 1 | 0x3F |

Addressing

Initially, each device on the I²C bus is in an idle state and monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the

R/W bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/W bit determines the direction of the data. A Logic 0 on the LSB of the first byte indicates that the master will write information to the peripheral, whereas a Logic 1 indicates that the master will read information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 83 shows the timing of an I²C write, and Figure 84 shows an I²C read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the ADAU1772 immediately

jumps to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1772 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1772 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1772, and the part returns to the idle condition.

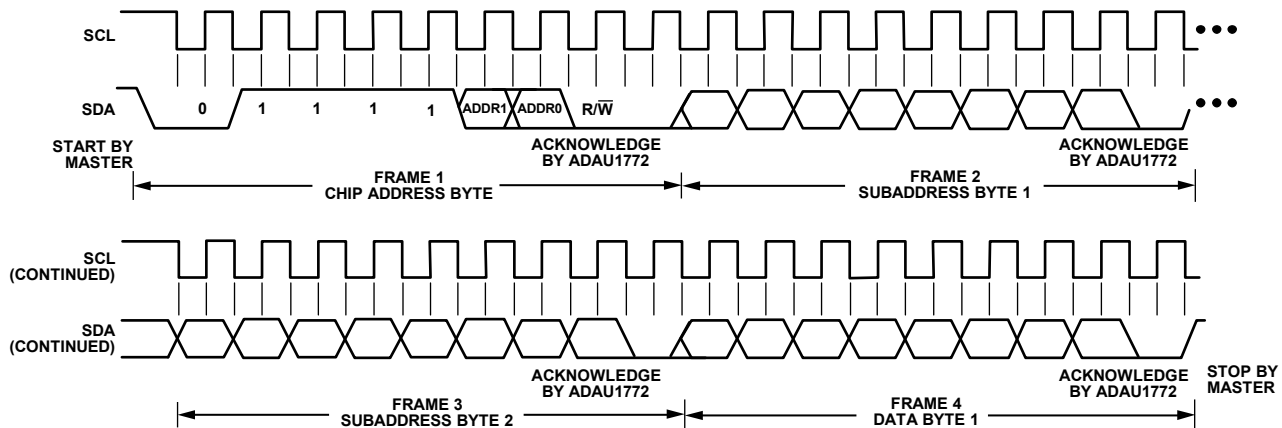


Figure 83. I²C Write to ADAU1772 Clocking

10804-069

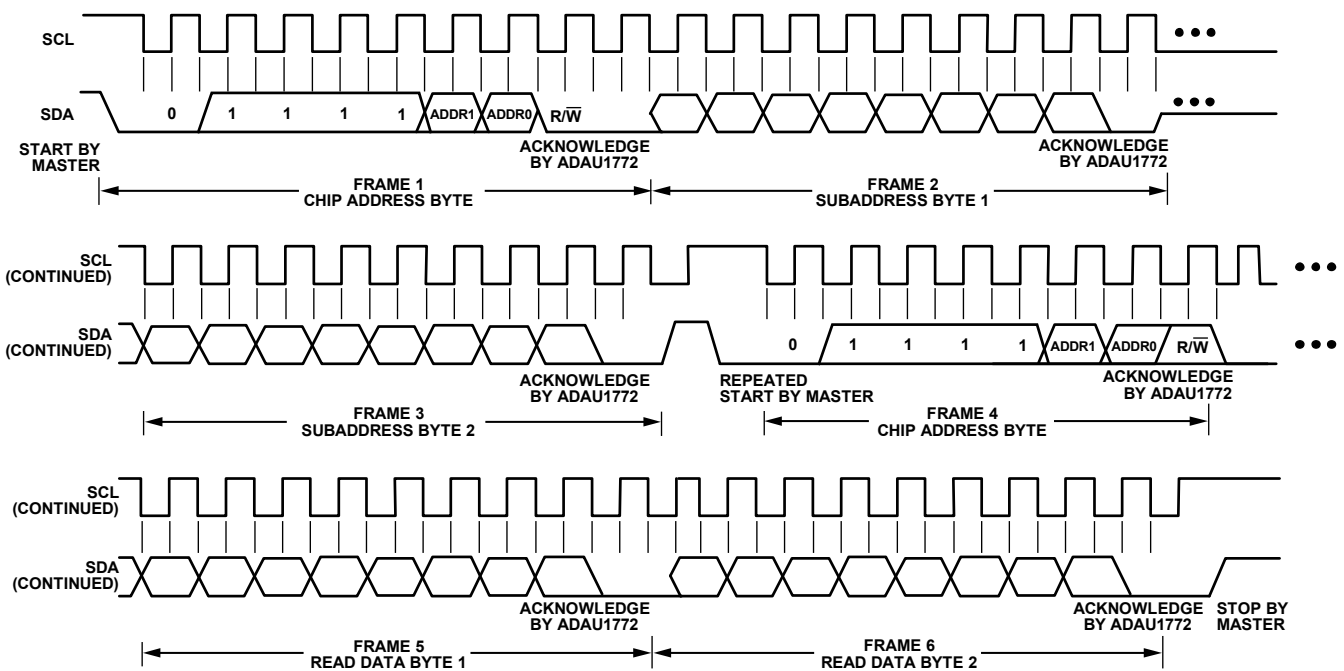


Figure 84. I²C Read from ADAU1772 Clocking

10804-069

I²C Read and Write Operations

Figure 85 shows the timing of a single-word write operation. Every ninth clock pulse, the ADAU1772 issues an acknowledge by pulling SDA low.

Figure 86 shows the timing of a burst mode write sequence. This figure shows an example where the target destination words are two bytes, such as the program memory. The ADAU1772 knows to increment its subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The timing of a single-word read operation is shown in Figure 87. Note that the first R/W bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the ADAU1772 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/W set to 1 (read). This causes the ADAU1772 SDA to reverse and begin driving data

back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1772.

Figure 88 shows the timing of a burst mode read sequence. This figure shows an example where the target read words are two bytes. The ADAU1772 increments its subaddress every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges may have a variety of word lengths, ranging from one to four bytes. The ADAU1772 always decodes the subaddress and sets the auto-increment circuit so that the address increments after the appropriate number of bytes.

Figure 85 to Figure 88 use the following abbreviations:

- S = start bit
- P = stop bit
- AM = acknowledge by master
- AS = acknowledge by slave

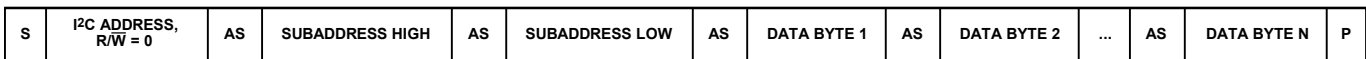


Figure 85. Single-Word I²C Write Format

10804-070



Figure 86. Burst Mode I²C Write Format

10804-071



Figure 87. Single-Word I²C Read Format

10804-072

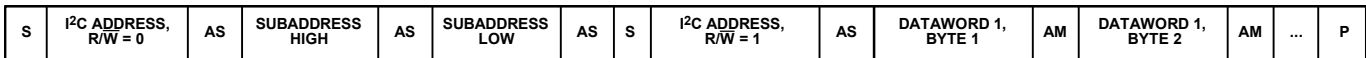


Figure 88. Burst Mode I²C Read Format

10804-073

SPI PORT

By default, the ADAU1772 is in I²C mode, but it can be put into SPI control mode by pulling SS low three times. This can be easily accomplished by issuing three SPI writes, which are in turn ignored by the ADAU1772. The next (fourth) SPI write is then latched into the SPI port.

The SPI port uses a 4-wire interface—consisting of SS, SCLK, MOSI, and MISO signals—and is always a slave port. The SS signal should go low at the beginning of a transaction and high at the end of a transaction. The SCLK signal latches MOSI on a low-to-high transition. MISO data is shifted out of the ADAU1772 on the falling edge of SCLK and should be clocked into a receiving device, such as a microcontroller, on the SCLK rising edge. The MOSI signal carries the serial input data, and the MISO signal is the serial output data. The MISO signal remains tristated until a read operation is requested. This allows other SPI-compatible peripherals to share the same readback line.

All SPI transactions have the same basic format shown in Table 23. A timing diagram is shown in Figure 89 and Figure 90. All data should be written MSB first. The ADAU1772 can only be taken out of SPI mode by pulling the PD pin low or by powering down the IC.

Read/Write

The first byte of an SPI transaction indicates whether the communication is a read or a write with the R/W bit. The LSB of this first byte determines whether the SPI transaction is a read (Logic Level 1) or a write (Logic Level 0).

Subaddress

The 16-bit subaddress word is decoded into a location in one of the memories or registers. This subaddress is the location of the appropriate memory location or register.

Data Bytes

The number of data bytes varies according to the register or memory being accessed. During a burst mode write, an initial subaddress is written followed by a continuous sequence of data for consecutive memory/register locations.

A sample timing diagram for a single-write SPI operation to the parameter RAM is shown in Figure 89. A sample timing diagram of a single-read SPI operation is shown in Figure 90. The MISO pin goes from tristate to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 2 contain the addresses and the R/W bit and subsequent bytes carry the data.

Table 23. Generic SPI Word Format

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 ¹ |
|--------------|--------------------------------|-------------------------------|--------|---------------------|
| 0000000, R/W | Register/memory address [15:8] | Register/memory address [7:0] | data | data |

¹ Continues to end of data.

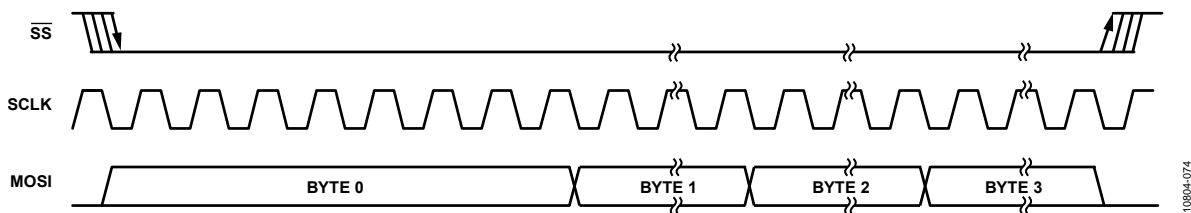


Figure 89. SPI Write to ADAU1772 Clocking (Single-Write Mode)

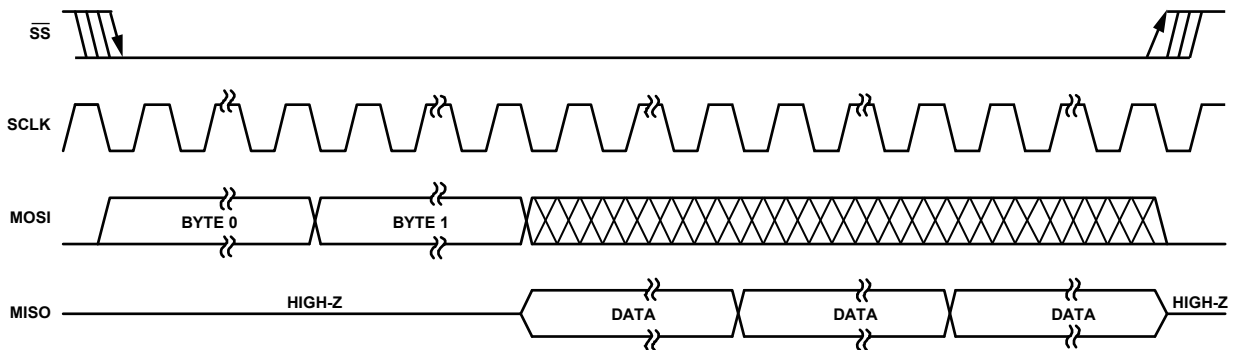


Figure 90. SPI Read from ADAU1772 Clocking (Single-Read Mode)

SELF-BOOT

The ADAU1772 boots up from an EEPROM over the I²C bus when the SELFBOOT pin is set high at power-up and the PD pin is set high. The state of the SELFBOOT pin is checked only when the ADAU1772 comes out of a reset via the PD pin, and the EEPROM is not used after a self-boot is complete. During booting, ensure that there is a stable DVDD in the system. The PD pin should remain high during the self-boot operation. The master SCL clock output from the ADAU1772 is derived from the input clock on XTALI/MCLKIN. A divide-by-64 circuit ensures that the SCL output frequency during the self-boot operation is never greater than 400 kHz for most input clock frequencies. With the external master clock to the ADAU1772 being between 12 MHz and 27 MHz, the SCL frequency ranges from 176 kHz to 422 kHz. If the self-boot EEPROM is not rated for operation above 400 kHz, be sure to use a master clock that is no faster than 25.6 MHz.

Table 25 shows the list of instructions that are possible during an ADAU1772 self-boot. The 0x01 and 0x05 instruction bytes are used to load the register, program, and parameter settings.

EEPROM Size

The self-boot circuit is compatible with an EEPROM that has a 2-byte address. For most EEPROM families, a 2-byte address is used on devices that are 32 kB or larger. The EEPROM must be set to Address 0x50. Examples of two compatible EEPROMs include Atmel AT24C32D and STMicroelectronics M24C32-F.

Table 24 lists the maximum necessary EEPROM size, assuming that there is 100% utilization of the program and parameters (both banks). There is inherently some overhead for instructions to control the self-boot procedure.

Table 24. Maximum EEPROM Size

| ADAU1772 Memory Blocks | Word Size (Bytes per Word) | Words | Total EEPROM Space Requirement (Bytes) |
|------------------------|----------------------------|--------------|--|
| Program | 2 | 32 | 64 |
| Bank 0 Parameters | 4 | 160 (32 × 5) | 640 |
| Bank 1 Parameters | 4 | 160 | 640 |
| Registers | 1 | 65 | 65 |
| Total Bytes | | | 1409 |

CRC

An 8-bit CRC validates the content of the EEPROM. This CRC is strong enough to detect single error bursts of up to eight bits in size.

The terminate self-boot instruction (0x00 instruction byte) must be followed by a CRC byte. The CRC is generated using all of the EEPROM bytes from Address 0x0000 to the last 0x00 instruction byte. The polynomial for the CRC is

$$x^8 + x^2 + x + 1$$

If the CRC is incorrect or if an unrecognized instruction byte is read during self-boot, the boot process is immediately stopped and restarted after a 250 ms delay (for a 12.288 MHz input clock). When SigmaStudio is used, the CRC byte is generated automatically when a configuration is downloaded to the EEPROM.

Delay

The delay instruction (0x02 instruction byte) delays by the 16-bit setting × 2048 clock cycles.

Boot Time

The time to self-boot the ADAU1772 from an EEPROM can be calculated using the following equation:

$$Boot\ Time = 64 / MCLK\ Frequency \times Total\ Bytes + Wait\ Time$$

The self-boot operation starts after 16,568 clock cycles are seen on the XTALI/MCLKIN pin after PD is set high. With a 12.288 MHz clock, this corresponds to approximately a 1.35 ms wait time from power-up. This delay ensures that the crystal used for generating the master clock has ramped up to a stable oscillation.

Table 25. EEPROM Self-Boot Instructions

| Instruction Byte ID | Instruction Byte Description | Following Bytes |
|---------------------|--|---|
| 0x00 | End self-boot | CRC |
| 0x01 | Write multibyte length minus two bytes, starting at target address | Length (high byte), length (low byte), address (high byte), address (low byte), data (0), data (1), ... data (length – 3) |
| 0x02 | Delays by the 16-bit setting × 2048 clock cycles | Delay (high byte), delay (low byte) |
| 0x03 | No operation | None |
| 0x04 | Wait for PLL lock | None |
| 0x05 | Write single byte to target address | Address (high byte), address (low byte), data |

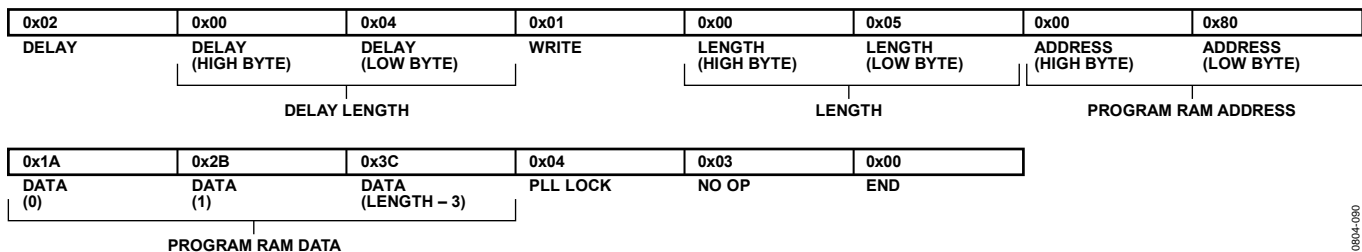


Figure 91. A List of Example Self-Boot EEPROM Instructions

MULTIPURPOSE PINS

The ADAU1772 has seven multipurpose (MP) pins that can be used for serial data I/O, clock outputs, and control in a system without a microcontroller. Each pin can be individually set to either its default or MP setting. The functions include push-button volume controls, enabling the compressors, parameter bank switching, DSP bypass mode, and muting the outputs.

The function of each of these pins is set in Register 0x0038 to Register 0x003E. By default, each pin is configured as an input.

Table 26. Multipurpose Pin Functions

| Pin No. | Default Pin Function | Secondary Pin Functions |
|---------|---------------------------------------|---|
| 31 | LRCLK | Multipurpose control inputs |
| 32 | BCLK | Multipurpose control inputs |
| 33 | DAC_SDATA | Multipurpose control inputs |
| 34 | MP1 acting as push-button volume up | ADC_SDATA0, PDM output, multipurpose control inputs |
| 35 | MP6 acting as push-button volume down | ADC_SDATA1, CLKOUT, multipurpose control inputs |
| 36 | DMIC2_3 | Multipurpose control inputs |
| 37 | DMIC0_1 | Multipurpose control inputs |

PUSH-BUTTON VOLUME CONTROLS

The ADC and DAC volume controls can be set up to be controlled with two push-buttons—one for volume up and one for volume down. The volume setting can either be changed with a click of the button or be ramped by holding the button. The volume settings change when the signal on the pin from the button goes from low to high.

When in push-button mode, the initial volume level is set with Bits PB_VOL_INIT_VAL. By default, MP1 acts as the push-button volume up and MP6 acts as the push-button volume down; however, any of the MPx pins can be set to act as the push-button up and push-button down volume controls.

When the ADC and/or DAC volumes are controlled with the push-buttons, the corresponding volume control registers no longer allow control of the volume from the control port.

Therefore, writing to these volume control registers has no effect on the codec volume level.

LIMITER COMPRESSION ENABLE

This function allows a user to enable limiter compression regardless of the signal level. Setting an MPx pin low when this function is enabled causes the limiter to compress the incoming signal by the minimum gain setting. When the MPx pin is released, the limiter resumes normal behavior.

PARAMETER BANK SWITCHING

An MPx pin can be used to switch the active parameter bank between Bank A and Bank B. When this setting is selected, Bank A is active when the pin is high and Bank B is active when the pin is low. Care should be taken to set the BANK_SL bits in the CORE_CONTROL register (Address 0x0009) to the default value of 0x00 before enabling MPx pin control over bank switching. Simultaneous control of bank switching by both register setting and MPx pin selection is not possible.

Bit ZERO_STATE selects whether the data memory of the codec is set to 0 during a bank switch. If the data is not set to 0 when a new set of filter coefficients is enabled via a bank switch, there may be a pop in the audio as the old data is circulated in the new filters.

MUTE

The MPx pins can be put into a mode to mute the ADCs or DACs. When in this mode, mute is enabled when an MPx pin is set low. The full combination of possible mutes for ADCs and DACs using MPx pins are set in Register 0x0038 to Register 0x003E.

DSP BYPASS MODE

When DSP bypass mode is enabled, a direct path from the ADC outputs to the DACs is set up to enable bypassing the core processing to listen to environmental sounds. This is useful for listening to someone speaking without having to remove the noise cancelling headphones. The DSP bypass path is enabled by setting an MPx pin low. Figure 92 shows the DSP bypass path disabled, and Figure 93 shows the DSP bypass path enabled by pressing the push-button switch. The DSP bypass feature works for both analog and digital microphone inputs.

DSP bypass is enabled when a switch connected to an MPx pin that is set to DSP bypass mode is closed and the MPx pin signal

is pulled low. Pressing and holding the switch closed enables the DSP bypass signal path as defined in the TALKTHRU register (Address 0x002A). The DAC volume control setting is switched from the default gain setting to the new TALKTHRU_GAINx register setting (Address 0x002B and Address 0x002C). DSP bypass is enabled only on ADC0 and ADC1. The DSP bypass signal path is from the output of ADCx to the input of the DAC(s).

When DSP bypass is enabled, the current DAC volume setting is ramped down to -95.625 dB and the DSP bypass volume setting is ramped up to avoid pops when switching paths.

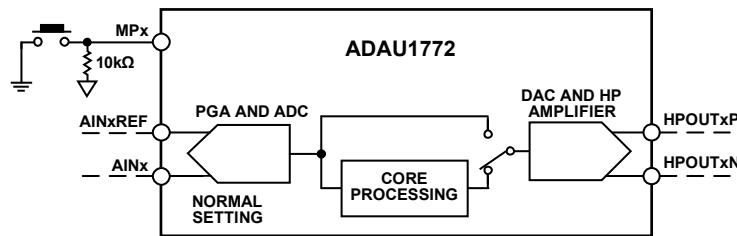


Figure 92. DSP Bypass Path Disabled

10804-076

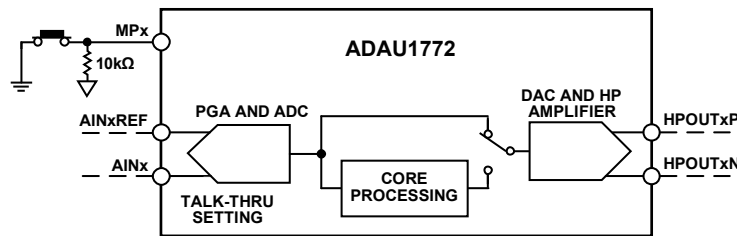


Figure 93. DSP Bypass Path Enabled

10804-077

SERIAL DATA INPUT/OUTPUT PORTS

The serial data input and output ports of the ADAU1772 can be set to accept or transmit data in a 2-channel format or in a 4-channel or 8-channel TDM stream to interface to external ADCs, DACs, DSPs, and SOCs. Data is processed in twos complement, MSB first format. The left-channel data field always precedes the right-channel data field in the 2-channel streams. In 8-channel TDM mode, the data channels are output sequentially, starting with the channel set by the ADC_SDATA0_ST and ADC_SDATA1_ST bits. The serial modes and the position of the data in the frame are set in the serial data port (SAI_0, SAI_1) and serial output control registers (SOUT_SOURCE_x_x, Address 0x0013 to Address 0x0016).

The serial data clocks do not need to be synchronous with the ADAU1772 master clock input, but the LRCLK and BCLK must be synchronous to each other. The LRCLK and BCLK pins are used to clock both the serial input and output ports. The ADAU1772 can be set to be either the master or the slave in a system. Because there is only one set of serial data clocks, the input and output ports must always both be either master or slave.

The serial data control registers allow control of the clock polarity and the data input modes. The valid data formats are I²S, left justified, right justified (24- or 16-bit), PCM, and TDM. In all modes except for the right justified modes, the serial port inputs an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they are truncated internally. The serial port can operate with an arbitrary number of BCLK transitions in each LRCLK frame. The LRCLK in TDM mode can be input to the ADAU1772 either as a 50% duty cycle clock or as a bit-wide pulse. Table 27 lists the modes in which the serial input/output port can function. When using low IOVDD (1.8 V) with a high

BCLK rate (12.288 MHz), a sample rate of 192 kHz, or a TDM8 mode operating at a sample rate of 48 kHz, it is recommended to use the high drive settings on the serial port pins. The high drive strength effectively speeds up the transition times of the waveforms, thereby improving the signal integrity of the clock and data lines. These can be set in the PAD_CONTROL4 register (Address 0x004C).

Table 27. Serial In/Out Port Master/Slave Mode Capabilities

| f _{SSD} | 2-Channel Modes (I ² S, Left Justified, Right Justified) | 4-Channel TDM | 8-Channel TDM |
|------------------|---|---------------|---------------|
| 48 kHz | Yes | Yes | Yes |
| 96 kHz | Yes | Yes | No |
| 192 kHz | Yes | No | No |

Table 28 describes the proper serial port settings for standard audio data formats. More information about the settings in this table can be found in the Serial Port Control 0 and Serial Port Control 1 registers (Address 0x0032 and Address 0x0033) descriptions.

TRISTATING UNUSED CHANNELS

Unused outputs can be tristated so that multiple ICs can drive a single TDM line. This function is available only when the serial ports of the ADAU1772 are operating in TDM mode. Channels that are inactive can be set in the SOUT_CONTROL0 register (Address 0x0034). The tristating of inactive channels is set in the SAI_1 register (Address 0x0033), which offers the option of tristating or driving the inactive channel.

In a 32-bit TDM frame with 24-bit data, the eight unused bits are tristated. Inactive channels are also tristated for the full frame.

Table 28. Serial Port Data Format Settings

| Format | LRCLK Polarity (LR_POL) | LRCLK Type (LR_MODE) | BCLK Polarity (BCLKEDGE) ¹ | MSB Position (SDATA_FMT) |
|---|-------------------------|----------------------|---------------------------------------|--------------------------|
| I ² S (Figure 94) | 0 | 0 | 0 | 00 |
| Left Justified (Figure 95) | 1 | 0 | 0 | 01 |
| Right Justified (Figure 96 and Figure 97) | 1 | 0 | 0 | 10 or 11 |
| TDM (Figure 98 and Figure 99) | 1 | 0 or 1 | 0 | 00 |
| PCM/DSP Short Frame Sync (Figure 100) | 1 | 1 | X | 00 |
| PCM/DSP Long Frame Sync (Figure 101) | 1 | 0 | X | 01 |

¹ X = don't care.

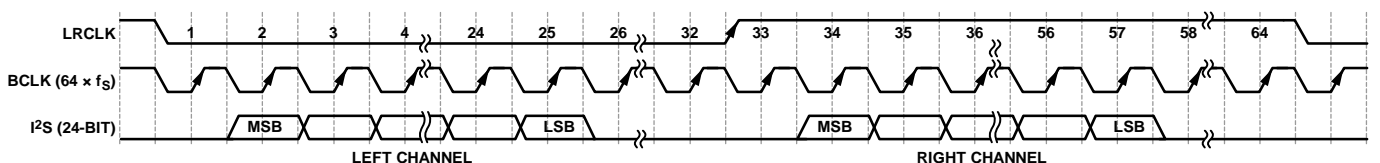


Figure 94. I²S Mode—16 Bits to 24 Bits per Channel

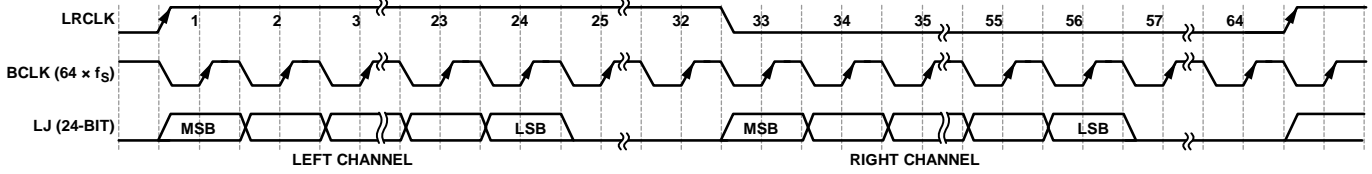


Figure 95. Left Justified Mode—16 Bits to 24 Bits per Channel

10804-079

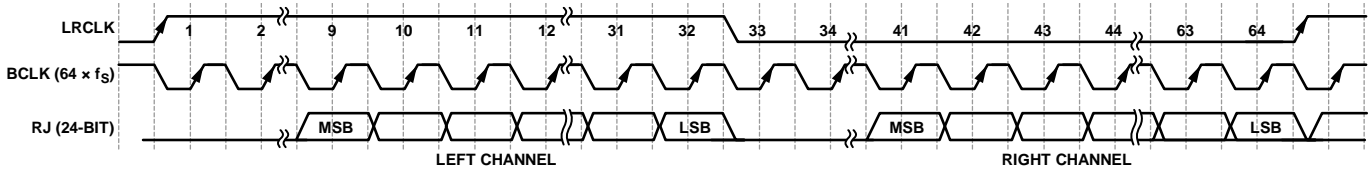


Figure 96. Right Justified Mode—24 Bits per Channel

10804-080

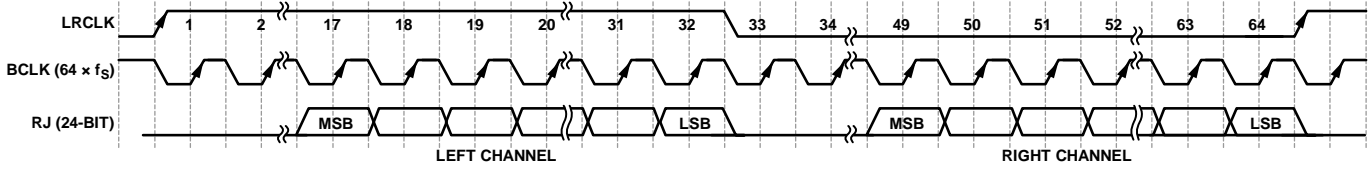


Figure 97. Right Justified Mode—16 Bits per Channel

10804-081

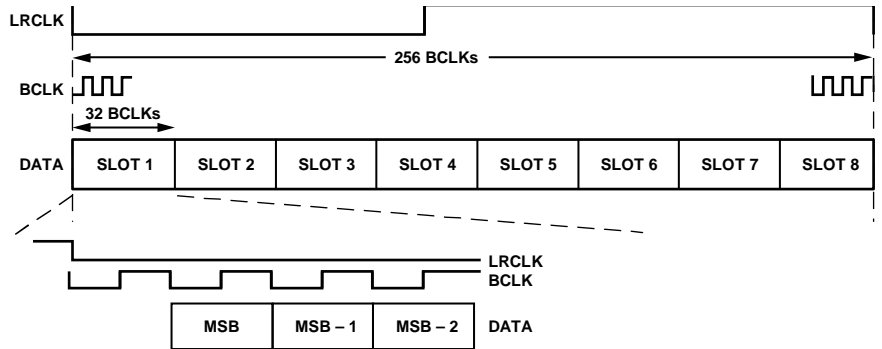


Figure 98. 8-Channel TDM Mode

10804-082

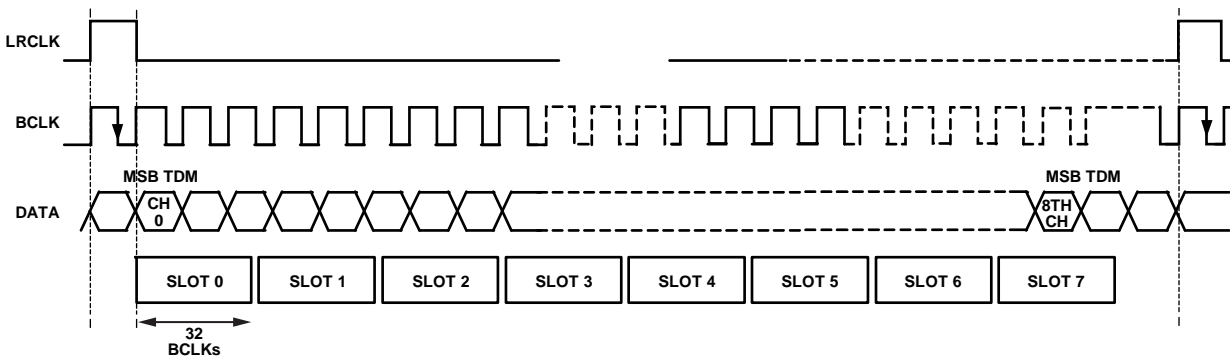


Figure 99. 8-Channel TDM Mode, Pulse LRCLK

10804-083

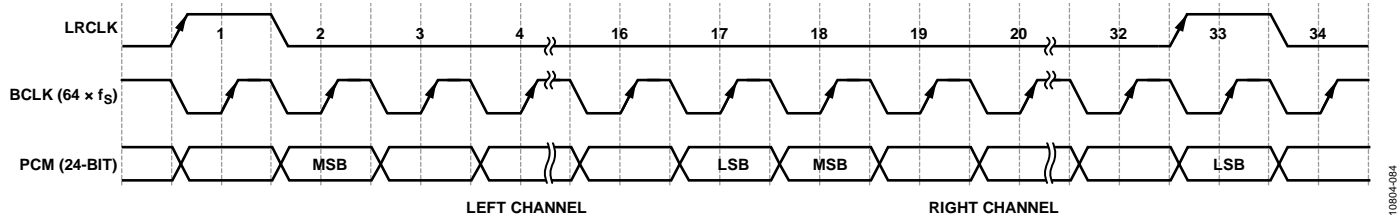


Figure 100. PCM/DSP Mode, 16 Bits per Channel, Short Frame Sync

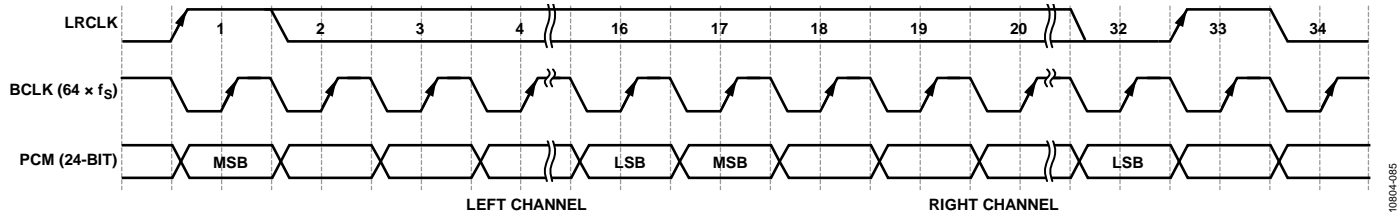


Figure 101. PCM/DSP Mode, 16 Bits per Channel, Long Frame Sync

10804-084

10804-085

APPLICATIONS INFORMATION

POWER SUPPLY BYPASS CAPACITORS

Each analog and digital power supply pin should be bypassed to its nearest appropriate ground pin with a single 0.1 μF capacitor. The connections to each side of the capacitor should be as short as possible, and the trace should be routed on a single layer with no vias. For maximum effectiveness, locate the capacitor equidistant from the power and ground pins or slightly closer to the power pin if equidistant placement is not possible. Thermal connections to the ground planes should be made on the far side of the capacitor.

Each supply signal on the board should also be bypassed with a single bulk capacitor (10 μF to 47 μF).

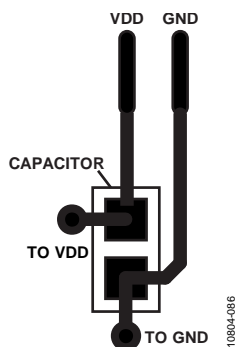


Figure 102. Recommended Power Supply Bypass Capacitor Layout

LAYOUT

Pin 24 is the AVDD supply for the headphone amplifiers. If the headphone amplifiers are enabled, the PCB trace to this pin should be wider than traces to other pins to increase the current carrying capacity. A wider trace should also be used for the headphone output lines.

GROUNDING

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.

EXPOSED PAD PCB DESIGN

The ADAU1772 has an exposed pad on the underside of the LFCSP. This pad is used to couple the package to the PCB for heat dissipation. When designing a board for the ADAU1772, special consideration should be given to the following:

- A copper layer equal in size to the exposed pad should be on all layers of the board, from top to bottom, and should connect somewhere to a dedicated copper board layer (see Figure 103).
- Vias should be placed to connect all layers of copper, allowing for efficient heat and energy conductivity. For an example, see Figure 104, which has nine vias arranged in a 3 \times 3 grid in the pad area.

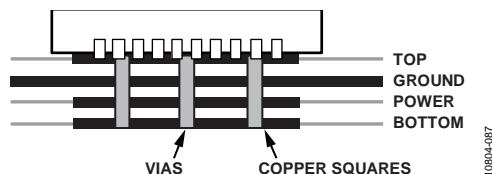


Figure 103. Exposed Pad Layout Example, Side View (Not to Scale)

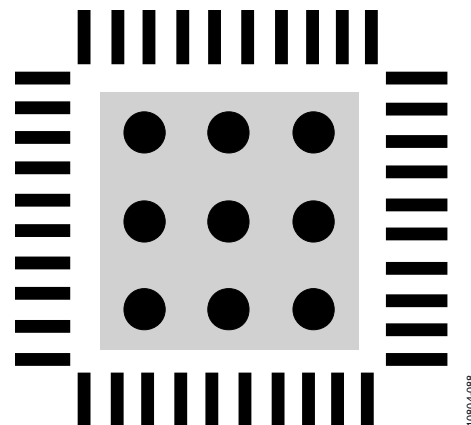


Figure 104. Exposed Pad Layout Example, Top View (Not to Scale)

REGISTER SUMMARY

Table 29. Low Latency Codec Register Summary

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW | | |
|--------|------------------|-------|--------------------|-----------|-------------|-------------------|---------------|--------------|---------------|---------------|-------------|-------------|------|----|
| 0x0000 | CLK_CONTROL | [7:0] | PLL_EN | RESERVED | SPK_FLT_DIS | XTAL_DIS | CLKSRC | CC_CDIV | CC_MDIV | COREN | 0x00 | RW | | |
| 0x0001 | PLL_CTRL0 | [7:0] | M_MSB | | | | | | | | | | 0x00 | RW |
| 0x0002 | PLL_CTRL1 | [7:0] | M_LSB | | | | | | | | | | 0x00 | RW |
| 0x0003 | PLL_CTRL2 | [7:0] | N_MSB | | | | | | | | | | 0x00 | RW |
| 0x0004 | PLL_CTRL3 | [7:0] | N_LSB | | | | | | | | | | 0x00 | RW |
| 0x0005 | PLL_CTRL4 | [7:0] | RESERVED | R | | | | X | | PLL_TYPE | 0x00 | RW | | |
| 0x0006 | PLL_CTRL5 | [7:0] | RESERVED | | | | | | | LOCK | 0x00 | R | | |
| 0x0007 | CLKOUT_SEL | [7:0] | RESERVED | | | | | CLKOUT_FREQ | | | | 0x00 | RW | |
| 0x0008 | REGULATOR | [7:0] | RESERVED | | | | | REG_PD | REGV | | | | 0x00 | RW |
| 0x0009 | CORE_CONTROL | [7:0] | ZERO_STATE | BANK_SL | | RESERVED | | CORE_FS | | CORE_RUN | 0x04 | RW | | |
| 0x000B | CORE_ENABLE | [7:0] | RESERVED | | | | | | | LIM_EN | DSP_CLK_EN | 0x03 | RW | |
| 0x000C | DBREG0 | [7:0] | DBVAL0 | | | | | | | | | | 0x00 | R |
| 0x000D | DBREG1 | [7:0] | DBVAL1 | | | | | | | | | | 0x00 | R |
| 0x000E | DBREG2 | [7:0] | DBVAL2 | | | | | | | | | | 0x00 | R |
| 0x000F | CORE_IN_MUX_0_1 | [7:0] | CORE_IN_MUX_SEL_1 | | | CORE_IN_MUX_SEL_0 | | | | | | | 0x10 | RW |
| 0x0010 | CORE_IN_MUX_2_3 | [7:0] | CORE_IN_MUX_SEL_3 | | | CORE_IN_MUX_SEL_2 | | | | | | | 0x32 | RW |
| 0x0011 | DAC_SOURCE_0_1 | [7:0] | DAC_SOURCE1 | | | DAC_SOURCE0 | | | | | | | 0x10 | RW |
| 0x0012 | PDM_SOURCE_0_1 | [7:0] | PDM_SOURCE1 | | | PDM_SOURCE0 | | | | | | | 0x32 | RW |
| 0x0013 | SOUT_SOURCE_0_1 | [7:0] | SOUT_SOURCE1 | | | SOUT_SOURCE0 | | | | | | | 0x54 | RW |
| 0x0014 | SOUT_SOURCE_2_3 | [7:0] | SOUT_SOURCE3 | | | SOUT_SOURCE2 | | | | | | | 0x76 | RW |
| 0x0015 | SOUT_SOURCE_4_5 | [7:0] | SOUT_SOURCE5 | | | SOUT_SOURCE4 | | | | | | | 0x54 | RW |
| 0x0016 | SOUT_SOURCE_6_7 | [7:0] | SOUT_SOURCE7 | | | SOUT_SOURCE6 | | | | | | | 0x76 | RW |
| 0x0017 | ADC_SDATA_CH | [7:0] | RESERVED | | | | ADC_SDATA1_ST | | ADC_SDATA0_ST | | | 0x04 | RW | |
| 0x0018 | ASRCO_SOURCE_0_1 | [7:0] | ASRC_OUT_SOURCE1 | | | ASRC_OUT_SOURCE0 | | | | | | | 0x10 | RW |
| 0x0019 | ASRCO_SOURCE_2_3 | [7:0] | ASRC_OUT_SOURCE3 | | | ASRC_OUT_SOURCE2 | | | | | | | 0x32 | RW |
| 0x001A | ASRC_MODE | [7:0] | RESERVED | | | | ASRC_IN_CH | | ASRC_OUT_EN | ASRC_IN_EN | | 0x00 | RW | |
| 0x001B | ADC_CONTROL0 | [7:0] | RESERVED | | RESERVED | ADC1_MUTE | ADC0_MUTE | RESERVED | | ADC_0_1_FS | | 0x19 | RW | |
| 0x001C | ADC_CONTROL1 | [7:0] | RESERVED | | RESERVED | ADC3_MUTE | ADC2_MUTE | RESERVED | | ADC_2_3_FS | | 0x19 | RW | |
| 0x001D | ADC_CONTROL2 | [7:0] | RESERVED | HP_0_1_EN | | DMIC_POL0 | DMIC_SW0 | DCM_0_1 | ADC_1_EN | ADC_0_EN | | 0x00 | RW | |
| 0x001E | ADC_CONTROL3 | [7:0] | RESERVED | HP_2_3_EN | | DMIC_POL1 | DMIC_SW1 | DCM_2_3 | ADC_3_EN | ADC_2_EN | | 0x00 | RW | |
| 0x001F | ADC0_VOLUME | [7:0] | ADC_0_VOL | | | | | | | | | | 0x00 | RW |
| 0x0020 | ADC1_VOLUME | [7:0] | ADC_1_VOL | | | | | | | | | | 0x00 | RW |
| 0x0021 | ADC2_VOLUME | [7:0] | ADC_2_VOL | | | | | | | | | | 0x00 | RW |
| 0x0022 | ADC3_VOLUME | [7:0] | ADC_3_VOL | | | | | | | | | | 0x00 | RW |
| 0x0023 | PGA_CONTROL_0 | [7:0] | PGA_EN0 | PGA_MUTE0 | PGA_GAIN0 | | | | | | | | 0x40 | RW |
| 0x0024 | PGA_CONTROL_1 | [7:0] | PGA_EN1 | PGA_MUTE1 | PGA_GAIN1 | | | | | | | | 0x40 | RW |
| 0x0025 | PGA_CONTROL_2 | [7:0] | PGA_EN2 | PGA_MUTE2 | PGA_GAIN2 | | | | | | | | 0x40 | RW |
| 0x0026 | PGA_CONTROL_3 | [7:0] | PGA_EN3 | PGA_MUTE3 | PGA_GAIN3 | | | | | | | | 0x40 | RW |
| 0x0027 | PGA_STEP_CONTROL | [7:0] | RESERVED | | | SLEW_RATE | | SLEW_PD3 | SLEW_PD2 | SLEW_PD1 | SLEW_PD0 | 0x00 | RW | |
| 0x0028 | PGA_10DB_BOOST | [7:0] | RESERVED | | | | | | PGA_3_BOOST | PGA_2_BOOST | PGA_1_BOOST | PGA_0_BOOST | 0x00 | RW |
| 0x0029 | POP_SUPPRESS | [7:0] | RESERVED | | HP_POP_DIS1 | HP_POP_DIS0 | PGA_POP_DIS3 | PGA_POP_DIS2 | PGA_POP_DIS1 | PGA_POP_DIS0 | 0x3F | RW | | |
| 0x002A | TALKTHRU | [7:0] | RESERVED | | | | | | | TALKTHRU_PATH | | 0x00 | RW | |
| 0x002B | TALKTHRU_GAIN0 | [7:0] | TALKTHRU_GAIN0_VAL | | | | | | | | | | 0x00 | RW |
| 0x002C | TALKTHRU_GAIN1 | [7:0] | TALKTHRU_GAIN1_VAL | | | | | | | | | | 0x00 | RW |
| 0x002D | MIC_BIAS | [7:0] | RESERVED | | MIC_EN1 | MIC_EN0 | RESERVED | RESERVED | MIC_GAIN1 | MIC_GAIN0 | 0x00 | RW | | |
| 0x002E | DAC_CONTROL1 | [7:0] | RESERVED | | DAC_POL | DAC1_MUTE | DAC0_MUTE | RESERVED | | DAC1_EN | DAC0_EN | 0x18 | RW | |
| 0x002F | DAC0_VOLUME | [7:0] | DAC_0_VOL | | | | | | | | | | 0x00 | RW |
| 0x0030 | DAC1_VOLUME | [7:0] | DAC_1_VOL | | | | | | | | | | 0x00 | RW |
| 0x0031 | OP_STAGE_MUTES | [7:0] | RESERVED | | | | HP_MUTE_R | | HP_MUTE_L | | | 0x0F | RW | |
| 0x0032 | SAL_0 | [7:0] | SDATA_FMT | | SAI | | SER_PORT_FS | | | | 0x00 | RW | | |
| 0x0033 | SAL_1 | [7:0] | TDM_TS | BCLK_TDMC | LR_MODE | LR_POL | SAI_MSB | BCLKRATE | BCLKEDGE | SAI_MS | 0x00 | RW | | |
| 0x0034 | SOUT_CONTROLO | [7:0] | TDM7_DIS | TDM6_DIS | TDM5_DIS | TDM4_DIS | TDM3_DIS | TDM2_DIS | TDM1_DIS | TDM0_DIS | 0x00 | RW | | |
| 0x0036 | PDM_OUT | [7:0] | RESERVED | | | PDM_CTRL | PDM_CH | | PDM_EN | | | 0x00 | RW | |
| 0x0037 | PDM_PATTERN | [7:0] | PATTERN | | | | | | | | | | 0x00 | RW |
| 0x0038 | MODE_MP0 | [7:0] | RESERVED | | | | MODE_MP0_VAL | | | | 0x00 | RW | | |
| 0x0039 | MODE_MP1 | [7:0] | RESERVED | | | | MODE_MP1_VAL | | | | 0x10 | RW | | |
| 0x003A | MODE_MP2 | [7:0] | RESERVED | | | | MODE_MP2_VAL | | | | 0x00 | RW | | |
| 0x003B | MODE_MP3 | [7:0] | RESERVED | | | | MODE_MP3_VAL | | | | 0x00 | RW | | |
| 0x003C | MODE_MP4 | [7:0] | RESERVED | | | | MODE_MP4_VAL | | | | 0x00 | RW | | |

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|--------|------------------|-------|-----------------|------------|-------------|--------------|-----------------|----------------|----------------|--------------|-------|----|
| 0x003D | MODE_MP5 | [7:0] | RESERVED | | | MODE_MP5_VAL | | | | | 0x00 | RW |
| 0x003E | MODE_MP6 | [7:0] | RESERVED | | | MODE_MP6_VAL | | | | | 0x11 | RW |
| 0x003F | PB_VOL_SET | [7:0] | PB_VOL_INIT_VAL | | | | HOLD | | | | 0x00 | RW |
| 0x0040 | PB_VOL_CONV | [7:0] | GAINSTEP | | RAMPSPEED | | PB_VOL_CONV_VAL | | | | 0x87 | RW |
| 0x0041 | DEBOUNCE_MODE | [7:0] | RESERVED | | | | DEBOUNCE | | | | 0x05 | RW |
| 0x0043 | OP_STAGE_CTRL | [7:0] | RESERVED | | HP_EN_R | HP_EN_L | HP_PDN_R | | HP_PDN_L | | 0x0F | RW |
| 0x0044 | DECIM_PWR_MODES | [7:0] | DEC_3_EN | DEC_2_EN | DEC_1_EN | DEC_0_EN | SINC_3_EN | SINC_2_EN | SINC_1_EN | SINC_0_EN | 0x00 | RW |
| 0x0045 | INTERP_PWR_MODES | [7:0] | RESERVED | | | | MOD_1_EN | MOD_0_EN | INT_1_EN | INT_0_EN | 0x00 | RW |
| 0x0046 | BIAS_CONTROL0 | [7:0] | HP_IBIAS | | AFE_IBIAS01 | | ADC_IBIAS23 | | ADC_IBIAS01 | | 0x00 | RW |
| 0x0047 | BIAS_CONTROL1 | [7:0] | RESERVED | CBIAS_DIS | AFE_IBIAS23 | | MIC_IBIAS | | DAC_IBIAS | | 0x00 | RW |
| 0x0048 | PAD_CONTROL0 | [7:0] | RESERVED | DMIC2_3_PU | DMIC0_1_PU | LRCLK_PU | BCLK_PU | ADC_SDATA1_PU | ADC_SDATA0_PU | DAC_SDATA_PU | 0x7F | RW |
| 0x0049 | PAD_CONTROL1 | [7:0] | RESERVED | | | SELFBOOT_PU | SCL_PU | SDA_PU | ADDR1_PU | ADDR0_PU | 0x1F | RW |
| 0x004A | PAD_CONTROL2 | [7:0] | RESERVED | DMIC2_3_PD | DMIC0_1_PD | LRCLK_PD | BCLK_PD | ADC_SDATA1_PD | ADC_SDATA0_PD | DAC_SDATA_PD | 0x00 | RW |
| 0x004B | PAD_CONTROL3 | [7:0] | RESERVED | | | SELFBOOT_PD | SCL_PD | SDA_PD | ADDR1_PD | ADDR0_PD | 0x00 | RW |
| 0x004C | PAD_CONTROL4 | [7:0] | RESERVED | RESERVED | RESERVED | LRCLK_DRV | BCLK_DRV | ADC_SDATA1_DRV | ADC_SDATA0_DRV | RESERVED | 0x00 | RW |
| 0x004D | PAD_CONTROL5 | [7:0] | RESERVED | | | RESERVED | SCL_DRV | SDA_DRV | RESERVED | RESERVED | 0x00 | RW |

REGISTER DETAILS

CLOCK CONTROL REGISTER

Address: 0x0000, Reset: 0x00, Name: CLK_CONTROL

This register is used to enable the internal clocks.

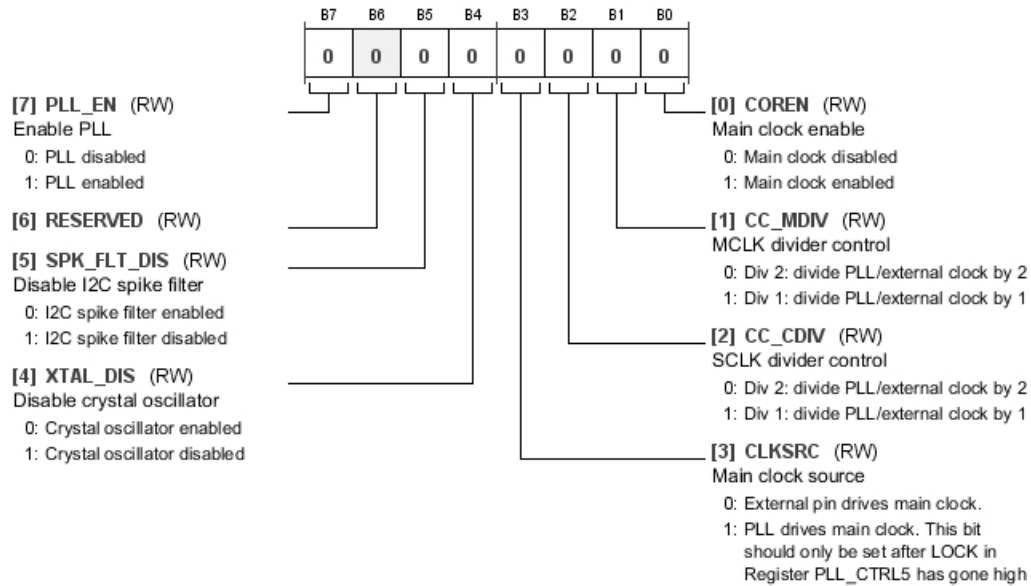


Table 30. Bit Descriptions for CLK_CONTROL

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-------------|----------|---|-------|--------|
| 7 | PLL_EN | 0 1 | Enable PLL. When this bit is set to 0, the PLL is powered down and the PLL output clock is disabled. The PLL should not be enabled until after all the PLL control settings (Register PLL_CTRL0 to Register PLL_CTRL5) have been set. The PLL clock output is active when both PLL_EN = 1 and COREN = 1. 0 PLL disabled 1 PLL enabled | 0x0 | RW |
| 5 | SPK_FLT_DIS | 0 1 | Disable I ² C spike filter. By default, the SDA and SCL inputs have a 50 ns spike suppression filter. When the control interface is in SPI mode, this filter is disabled regardless of this setting. 0 I ² C spike filter enabled 1 I ² C spike filter disabled | 0x0 | RW |
| 4 | XTAL_DIS | 0 1 | Disable crystal oscillator. 0 Crystal oscillator enabled 1 Crystal oscillator disabled | 0x0 | RW |
| 3 | CLKSRC | 0 1 | Main clock source. 0 External pin drives main clock. 1 PLL drives main clock. This bit should only be set after LOCK in Register PLL_CTRL5 has gone high. | 0x0 | RW |
| 2 | CC_CDIV | 0 1 | SCLK divider control. The core clock (SCLK) is used only by the core. It must run at 12.288 MHz. 0 Div 2: divide PLL/external clock by 2 1 Div 1: divide PLL/external clock by 1 | 0x0 | RW |
| 1 | CC_MDIV | 0 1 | MCLK divider control. The internal master clock (MCLK) of the IC is used by all digital logic except the core. It must run at 12.288 MHz. 0 Div 2: divide PLL/external clock by 2 1 Div 1: divide PLL/external clock by 1 | 0x0 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 0 | COREN | | Main clock enable. When COREN = 0, it is only possible to write to this register and the PLL control registers (PLL_CTRL0 to PLL_CTRL5). This control also enables the PLL clock. If using the PLL, do not set COREN = 1 until LOCK in Register PLL_CTRL5 is 1. Note that after COREN is enabled, writing to the parameters is disabled until setting DSP_CLK_EN in the CORE_ENABLE register. | 0x0 | RW |
| | | 0 | Main clock disabled | | |
| | | 1 | Main clock enabled | | |

PLL DENOMINATOR MSB REGISTER

Address: 0x0001, Reset: 0x00, Name: PLL_CTRL0

This register should only be written when PLL_EN = 0 in Register CLK_CONTROL.

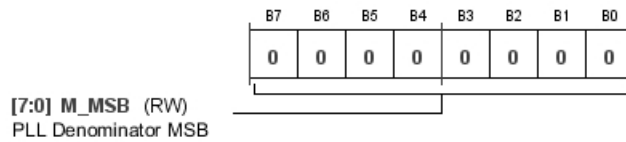


Table 31. Bit Descriptions for PLL_CTRL0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------|-------|--------|
| [7:0] | M_MSB | | PLL denominator MSB. | 0x00 | RW |

PLL DENOMINATOR LSB REGISTER

Address: 0x0002, Reset: 0x00, Name: PLL_CTRL1

This register should only be written when PLL_EN = 0 in Register CLK_CONTROL.

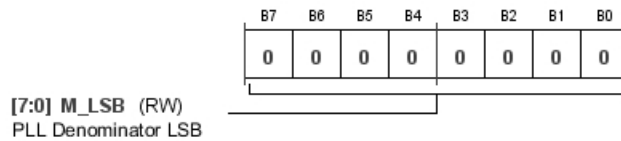


Table 32. Bit Descriptions for PLL_CTRL1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------|-------|--------|
| [7:0] | M_LSB | | PLL denominator LSB. | 0x00 | RW |

PLL NUMERATOR MSB REGISTER

Address: 0x0003, Reset: 0x00, Name: PLL_CTRL2

This register should only be written when PLL_EN = 0 in Register CLK_CONTROL.

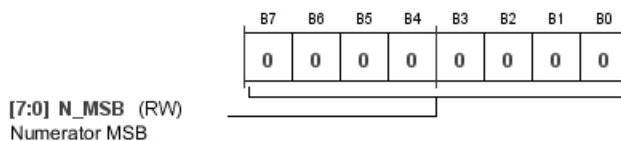


Table 33. Bit Descriptions for PLL_CTRL2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|--------------------|-------|--------|
| [7:0] | N_MSB | | PLL numerator MSB. | 0x00 | RW |

PLL NUMERATOR LSB REGISTER

Address: 0x0004, Reset: 0x00, Name: PLL_CTRL3

This register should only be written when PLL_EN = 0 in Register CLK_CONTROL.

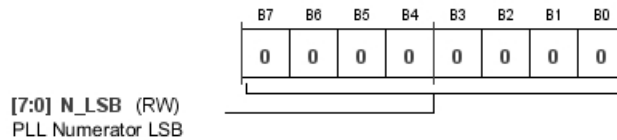


Table 34. Bit Descriptions for PLL_CTRL3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|--------------------|-------|--------|
| [7:0] | N_LSB | | PLL numerator LSB. | 0x00 | RW |

PLL INTEGER SETTING REGISTER

Address: 0x0005, Reset: 0x00, Name: PLL_CTRL4

This register should only be written when PLL_EN = 0 in Register CLK_CONTROL.

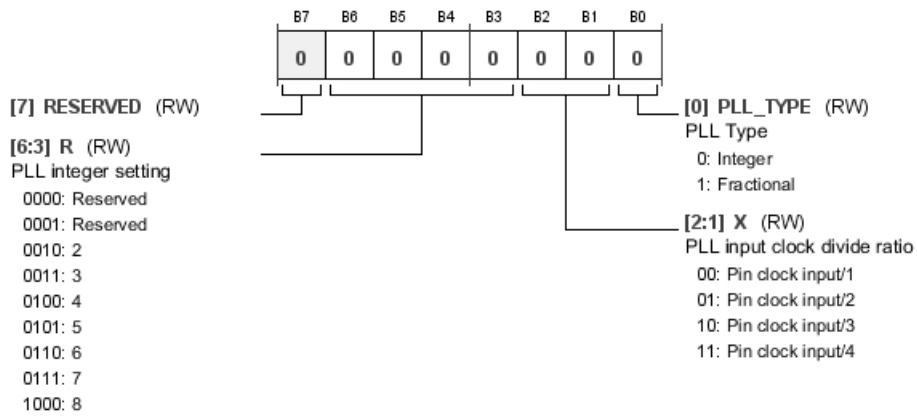


Table 35. Bit Descriptions for PLL_CTRL4

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|----------------------|-------|--------|
| [6:3] | R | | PLL integer setting. | 0x0 | RW |
| | | 0000 | Reserved | | |
| | | 0001 | Reserved | | |
| | | 0010 | 2 | | |
| | | 0011 | 3 | | |
| | | 0100 | 4 | | |
| | | 0101 | 5 | | |
| | | 0110 | 6 | | |
| | | 0111 | 7 | | |
| | | 1000 | 8 | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------------------|---|-------|--------|
| [2:1] | X | 00 01 10 11 | PLL input clock divide ratio. Pin clock input/1 Pin clock input/2 Pin clock input/3 Pin clock input/4 | 0x0 | RW |
| 0 | PLL_TYPE | 0 1 | PLL type. Integer Fractional | 0x0 | RW |

PLL LOCK FLAG REGISTER

Address: 0x0006, Reset: 0x00, Name: PLL_CTRL5

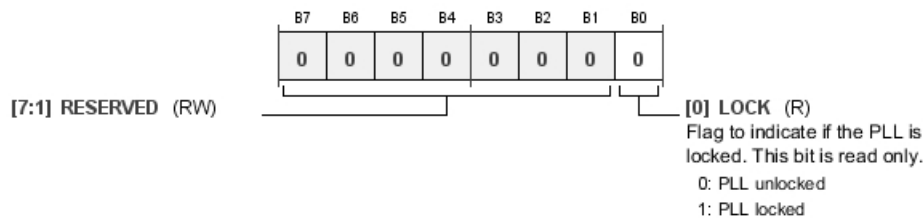


Table 36. Bit Descriptions for PLL_CTRL5

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 0 | LOCK | 0 1 | Flag to indicate if the PLL is locked. This bit is read only. PLL unlocked PLL locked | 0x0 | R |

CLKOUT SETTING SELECTION REGISTER

Address: 0x0007, Reset: 0x00, Name: CLKOUT_SEL

When Pin ADC_SDATA1/CLKOUT/MP6 is set to clock output mode, the frequency of the output clock is set here. CLKOUT can be used to provide a master clock to another IC, the clock for digital microphones, or as the clock for the PDM output stream. The 12 MHz/24 MHz setting is used when clocking another IC, 3 MHz/6 MHz for PDMOUT, and 1.5 MHz/3 MHz when clocking digital microphones. The CLKOUT frequency is derived from the master clock frequency, which is assumed to (and always should) be 12.288 MHz. The 12.288 MHz and 24.576 MHz output modes are not functional if PDM is enabled (Register PDM_OUT, Bits[1:0]).

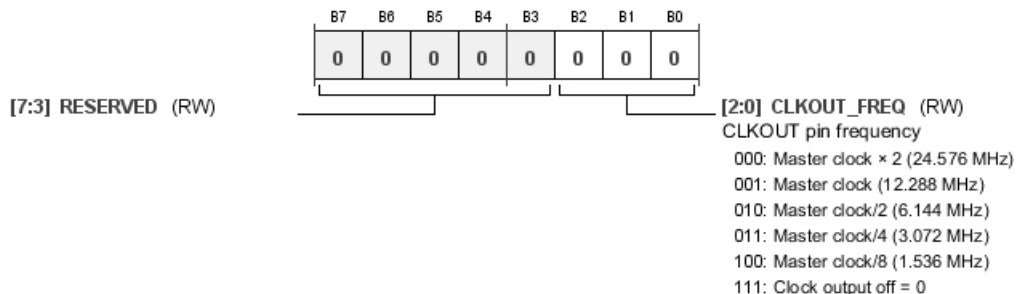


Table 37. Bit Descriptions for CLKOUT_SEL

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------|-------------------------------|-------|--------|
| [2:0] | CLKOUT_FREQ | | CLKOUT pin frequency. | 0x0 | RW |
| | | 000 | Master clock × 2 (24.576 MHz) | | |
| | | 001 | Master clock (12.288 MHz) | | |
| | | 010 | Master clock/2 (6.144 MHz) | | |
| | | 011 | Master clock/4 (3.072 MHz) | | |
| | | 100 | Master clock/8 (1.536 MHz) | | |
| | | 111 | Clock output off = 0 | | |

REGULATOR CONTROL REGISTER

Address: 0x0008, Reset: 0x00, Name: REGULATOR

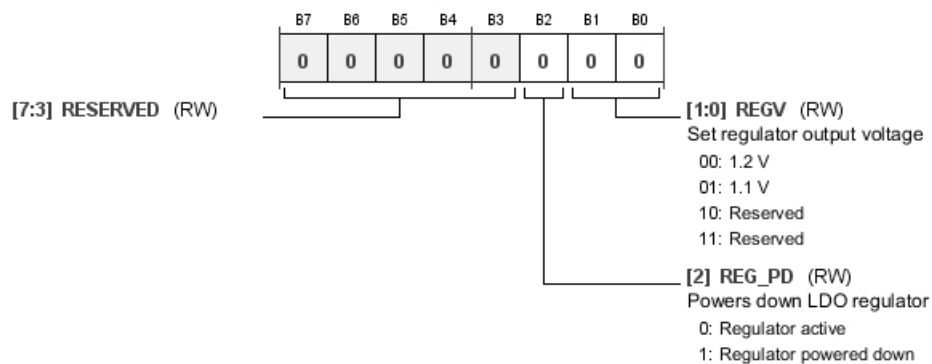


Table 38. Bit Descriptions for REGULATOR

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|-------------------------------|-------|--------|
| 2 | REG_PD | | Powers down LDO regulator. | 0x0 | RW |
| | | 0 | Regulator active | | |
| | | 1 | Regulator powered down | | |
| [1:0] | REGV | | Set regulator output voltage. | 0x0 | RW |
| | | 00 | 1.2 V | | |
| | | 01 | 1.1 V | | |
| | | 10 | Reserved | | |
| | | 11 | Reserved | | |

CORE CONTROL REGISTER

Address: 0x0009, Reset: 0x04, Name: CORE_CONTROL

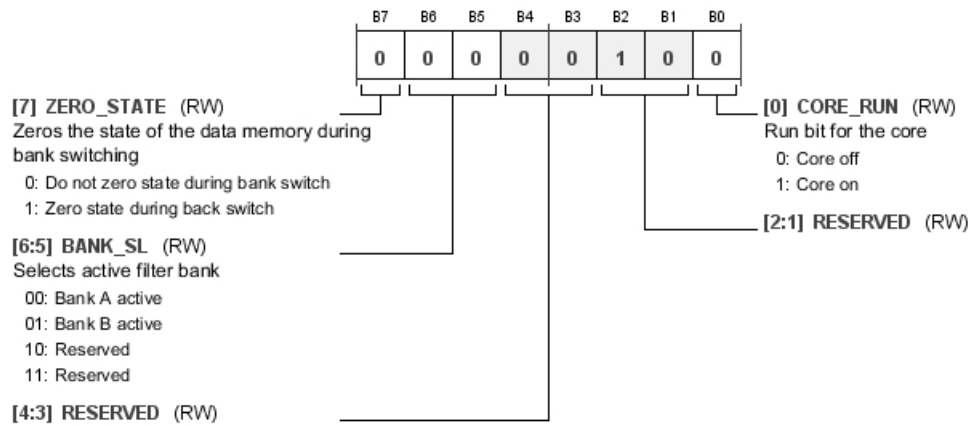


Table 39. Bit Descriptions for CORE_CONTROL

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------------------|---|-------|--------|
| 7 | ZERO_STATE | 0 1 | Zeroes the state of the data memory during bank switching. When switching active parameter banks between two settings, zeroing the state of the bank prevents the new filter settings from being active on old data that is recirculating in filters. Zeroing the state may prevent filter instability or unwanted noises upon bank switching. Do not zero state during bank switch Zero state during back switch | 0x0 | RW |
| [6:5] | BANK_SL | 00 01 10 11 | Selects active filter bank. Bank A active Bank B active Reserved Reserved | 0x0 | RW |
| [2:1] | CORE_FS | 00 01 10 11 | This bit sets the core sample rate. This setting should not be changed while the core is running. CORE_RUN must be set to 0 for this setting to be updated. Reserved 96 kHz 192 kHz Reserved | | |
| 0 | CORE_RUN | 0 1 | Run bit for the core. This bit should only be enabled when the program and parameters are loaded and the sample rate settings have been set. CORE_RUN starts and stops the core at the beginning of the program. Core off Core on | 0x0 | RW |

FILTER ENGINE AND LIMITER CONTROL REGISTER

Address: 0x000B, Reset: 0x03, Name: CORE_ENABLE

Disabling the limiter only disables the attack operation. The decay operation is always active, so a limiter can be safely disabled while it performs gain adjustments.

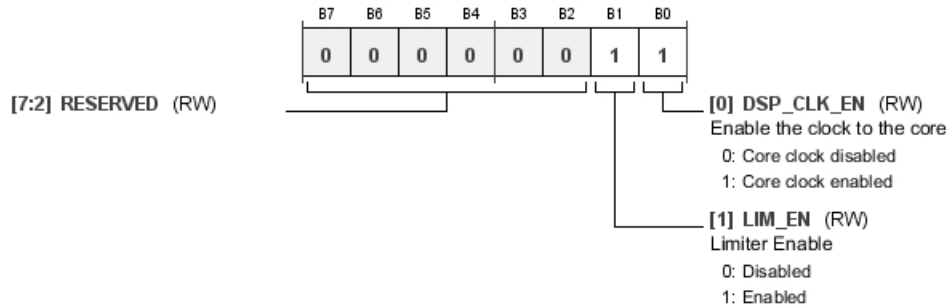


Table 40. Bit Descriptions for CORE_ENABLE

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|------------|----------|--|-------|--------|
| 1 | LIM_EN | 0 1 | Limiter enable. When the limiter function is disabled, a fixed max gain setting is applied to instructions using the limiters. 0 Disabled 1 Enabled | 0x1 | RW |
| 0 | DSP_CLK_EN | 0 1 | Enable the clock to the core. Directly controls the clock to the core. It should be set to 0 when the chip is used in a codec-only configuration, in which the core is not used. Writing to any of the biquad coefficient registers (Parameter Memory Address 0x0E0 to Address 0x2BF) is blocked until this bit is 1. This bit should not be used to start or stop the core while it is running, because it would immediately start or stop the core clock and not allow the program to finish. Instead, use CORE_RUN in Register CORE_CONTROL to start or stop the core. 0 Core clock disabled 1 Core clock enabled | 0x1 | RW |

DB VALUE REGISTER 0 READ

Address: 0x000C, Reset: 0x00, Name: DBREG0

The core can write data to this register, and the data is automatically converted to a level in dB. The most common usage is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG0 register.

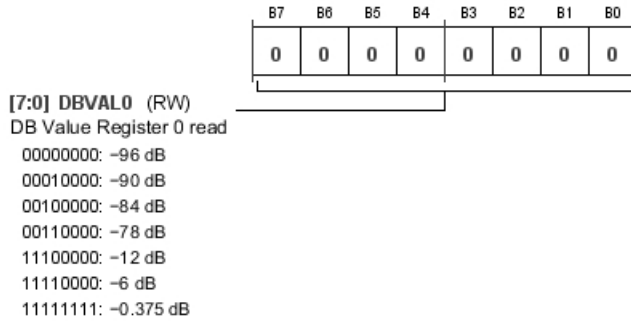


Table 41. Bit Descriptions for DBREG0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|--|---|-------|--------|
| [7:0] | DBVAL0 | 00000000 00010000 00100000 00110000 11100000 11110000 11111111 | DB Value Register 0 read. -96 dB -90 dB -84 dB -78 dB -12 dB -6 dB -0.375 dB | 0x00 | R |

DB VALUE REGISTER 1 READ

Address: 0x000D, Reset: 0x00, Name: DBREG1

The core can write data to this register, and the data is automatically converted to a level in dB. The most common usage is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG1 register.

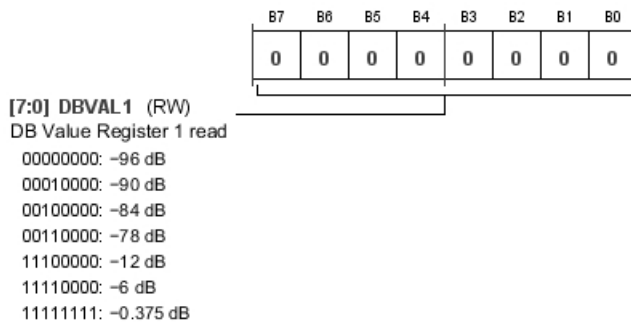


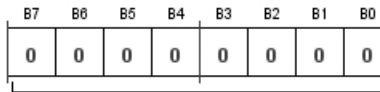
Table 42. Bit Descriptions for DBREG1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|---------------------------|-------|--------|
| [7:0] | DBVAL1 | | DB Value Register 1 read. | 0x00 | R |
| | | 00000000 | -96 dB | | |
| | | 00010000 | -90 dB | | |
| | | 00100000 | -84 dB | | |
| | | 00110000 | -78 dB | | |
| | | 11100000 | -12 dB | | |
| | | 11110000 | -6 dB | | |
| | | 11111111 | -0.375 dB | | |

DB VALUE REGISTER 2 READ

Address: 0x000E, Reset: 0x00, Name: DBREG2

The core can write data to this register, and the data is automatically converted to a level in dB. The most common usage is to determine the rms value of a signal by taking the absolute value, and then performing low-pass filtering and moving the result to the DBREG2 register.



[7:0] DBVAL2 (RW)

DB Value Register 2 read

00000000: -96 dB

00010000: -90 dB

00100000: -84 dB

00110000: -78 dB

11100000: -12 dB

11110000: -6 dB

11111111: -0.375 dB

Table 43. Bit Descriptions for DBREG2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|---------------------------|-------|--------|
| [7:0] | DBVAL2 | | DB Value Register 2 read. | 0x00 | R |
| | | 00000000 | -96 dB | | |
| | | 00010000 | -90 dB | | |
| | | 00100000 | -84 dB | | |
| | | 00110000 | -78 dB | | |
| | | 11100000 | -12 dB | | |
| | | 11110000 | -6 dB | | |
| | | 11111111 | -0.375 dB | | |

CORE CHANNEL 0/CORE CHANNEL 1 INPUT SELECT REGISTER

Address: 0x000F, Reset: 0x10, Name: CORE_IN_MUX_0_1

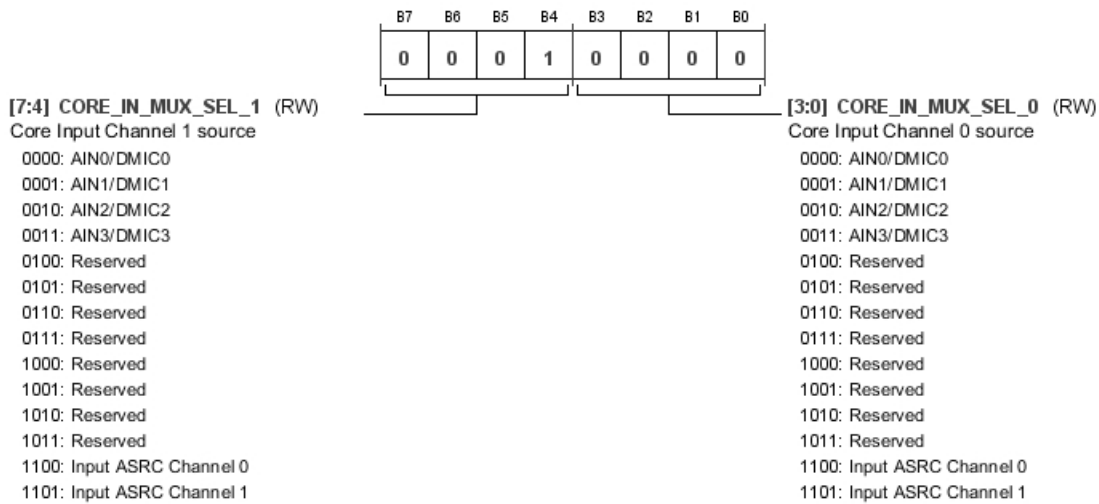


Table 44. Bit Descriptions for CORE_IN_MUX_0_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------------|--|--|-------|--------|
| [7:4] | CORE_IN_MUX_SEL_1 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | Core Input Channel 1 source. AIN0/DMIC0 AIN1/DMIC1 AIN2/DMIC2 AIN3/DMIC3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x1 | RW |
| [3:0] | CORE_IN_MUX_SEL_0 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | Core Input Channel 0 source. AIN0/DMIC0 AIN1/DMIC1 AIN2/DMIC2 AIN3/DMIC3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x0 | RW |

CORE CHANNEL 2/CORE CHANNEL 3 INPUT SELECT REGISTER

Address: 0x0010, Reset: 0x32, Name: CORE_IN_MUX_2_3

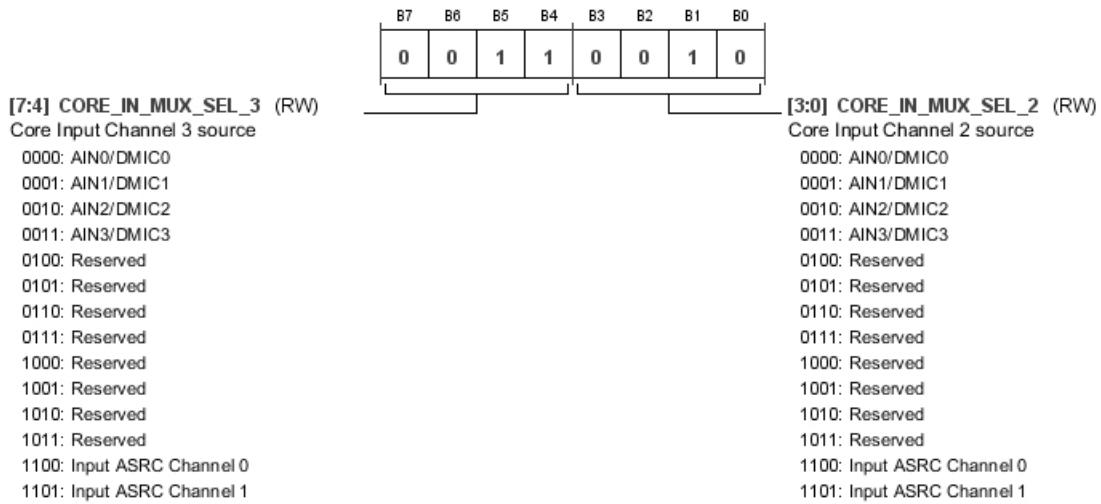


Table 45. Bit Descriptions for CORE_IN_MUX_2_3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------------|--|--|-------|--------|
| [7:4] | CORE_IN_MUX_SEL_3 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | Core Input Channel 3 source. AIN0/DMIC0 AIN1/DMIC1 AIN2/DMIC2 AIN3/DMIC3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x3 | RW |
| [3:0] | CORE_IN_MUX_SEL_2 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | Core Input Channel 2 source. AIN0/DMIC0 AIN1/DMIC1 AIN2/DMIC2 AIN3/DMIC3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x2 | RW |

DAC INPUT SELECT REGISTER

Address: 0x0011, Reset: 0x10, Name: DAC_SOURCE_0_1

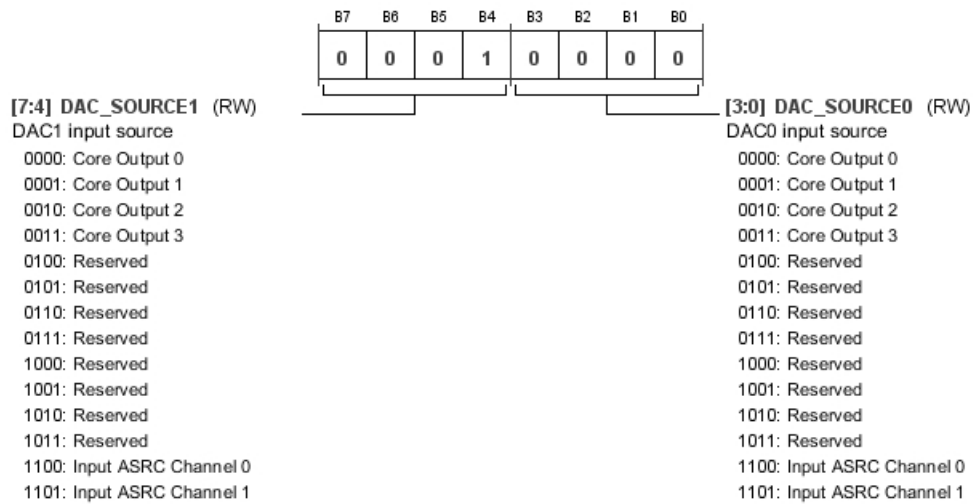


Table 46. Bit Descriptions for DAC_SOURCE_0_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|--|--|-------|--------|
| [7:4] | DAC_SOURCE1 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | DAC1 input source. This setting should not be changed while the core is running. CORE_RUN must be set to 0 for this setting to be updated. Core Output 0 Core Output 1 Core Output 2 Core Output 3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x1 | RW |
| [3:0] | DAC_SOURCE0 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | DAC0 input source. This setting should not be changed while the core is running. CORE_RUN must be set to 0 for this setting to be updated. Core Output 0 Core Output 1 Core Output 2 Core Output 3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x0 | RW |

PDM MODULATOR INPUT SELECT REGISTER

Address: 0x0012, Reset: 0x32, Name: PDM_SOURCE_0_1

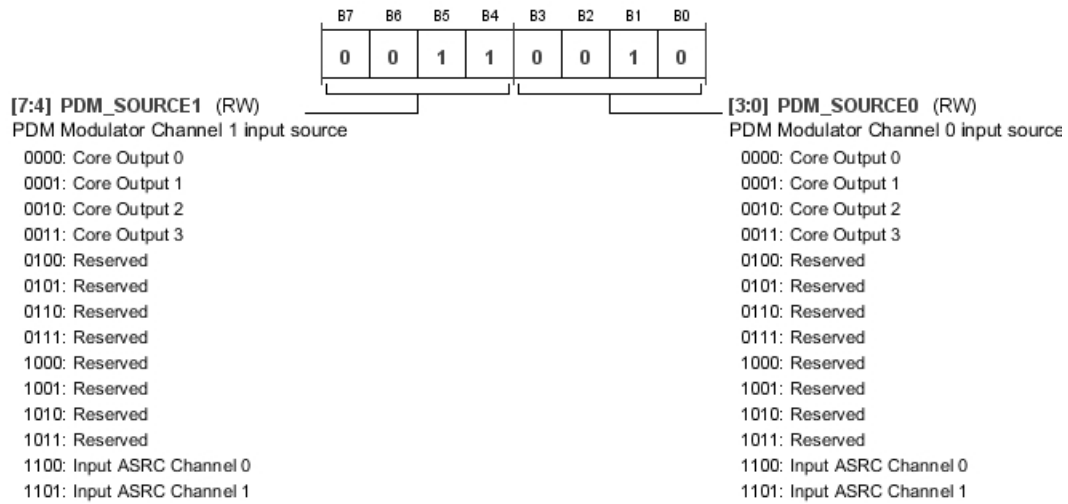


Table 47. Bit Descriptions for PDM_SOURCE_0_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|--|---|-------|--------|
| [7:4] | PDM_SOURCE1 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | PDM Modulator Channel 1 input source. Core Output 0 Core Output 1 Core Output 2 Core Output 3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x3 | RW |
| [3:0] | PDM_SOURCE0 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 | PDM Modulator Channel 0 input source. Core Output 0 Core Output 1 Core Output 2 Core Output 3 Reserved Reserved Reserved Reserved Reserved Reserved Reserved Input ASRC Channel 0 Input ASRC Channel 1 | 0x2 | RW |

SERIAL DATA OUTPUT 0/SERIAL DATA OUTPUT 1 INPUT SELECT REGISTER

Address: 0x0013, Reset: 0x54, Name: SOUT_SOURCE_0_1

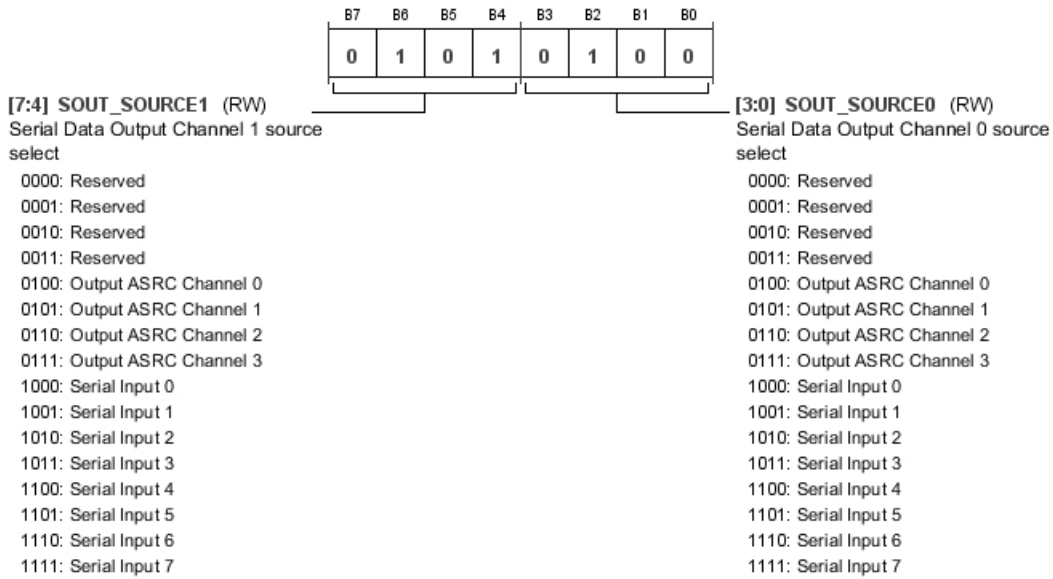


Table 48. Bit Descriptions for SOUT_SOURCE_0_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|--|---|-------|--------|
| [7:4] | SOUT_SOURCE1 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 | Serial Data Output Channel 1 source select. Reserved Reserved Reserved Reserved Output ASRC Channel 0 Output ASRC Channel 1 Output ASRC Channel 2 Output ASRC Channel 3 Serial Input 0 Serial Input 1 Serial Input 2 Serial Input 3 Serial Input 4 Serial Input 5 Serial Input 6 Serial Input 7 | 0x5 | RW |
| [3:0] | SOUT_SOURCE0 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 | Serial Data Output Channel 0 source select. Reserved Reserved Reserved Reserved Output ASRC Channel 0 Output ASRC Channel 1 Output ASRC Channel 2 Output ASRC Channel 3 Serial Input 0 Serial Input 1 Serial Input 2 | 0x4 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|----------------|-------|--------|
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |

SERIAL DATA OUTPUT 2/SERIAL DATA OUTPUT 3 INPUT SELECT REGISTER

Address: 0x0014, Reset: 0x76, Name: SOUT_SOURCE_2_3

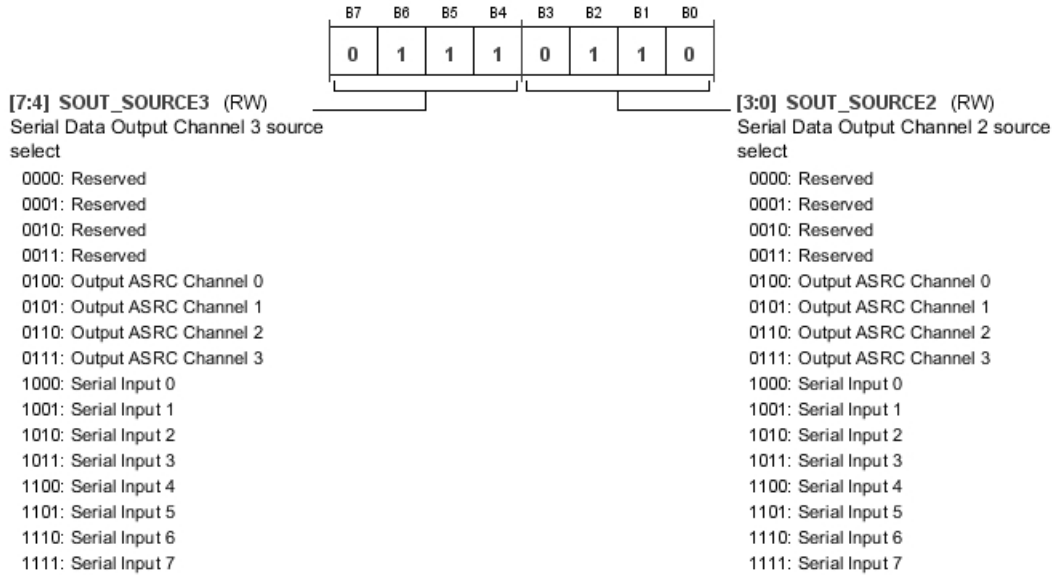


Table 49. Bit Descriptions for SOUT_SOURCE_2_3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [7:4] | SOUT_SOURCE3 | | Serial Data Output Channel 3 source select. | 0x7 | RW |
| | | 0000 | Reserved | | |
| | | 0001 | Reserved | | |
| | | 0010 | Reserved | | |
| | | 0011 | Reserved | | |
| | | 0100 | Output ASRC Channel 0 | | |
| | | 0101 | Output ASRC Channel 1 | | |
| | | 0110 | Output ASRC Channel 2 | | |
| | | 0111 | Output ASRC Channel 3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |
| [3:0] | SOUT_SOURCE2 | | Serial Data Output Channel 2 source select. | 0x6 | RW |
| | | 0000 | Reserved | | |
| | | 0001 | Reserved | | |
| | | 0010 | Reserved | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-----------------------|-------|--------|
| | | 0011 | Reserved | | |
| | | 0100 | Output ASRC Channel 0 | | |
| | | 0101 | Output ASRC Channel 1 | | |
| | | 0110 | Output ASRC Channel 2 | | |
| | | 0111 | Output ASRC Channel 3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |

SERIAL DATA OUTPUT 4/SERIAL DATA OUTPUT 5 INPUT SELECT REGISTER

Address: 0x0015, Reset: 0x54, Name: SOUT_SOURCE_4_5

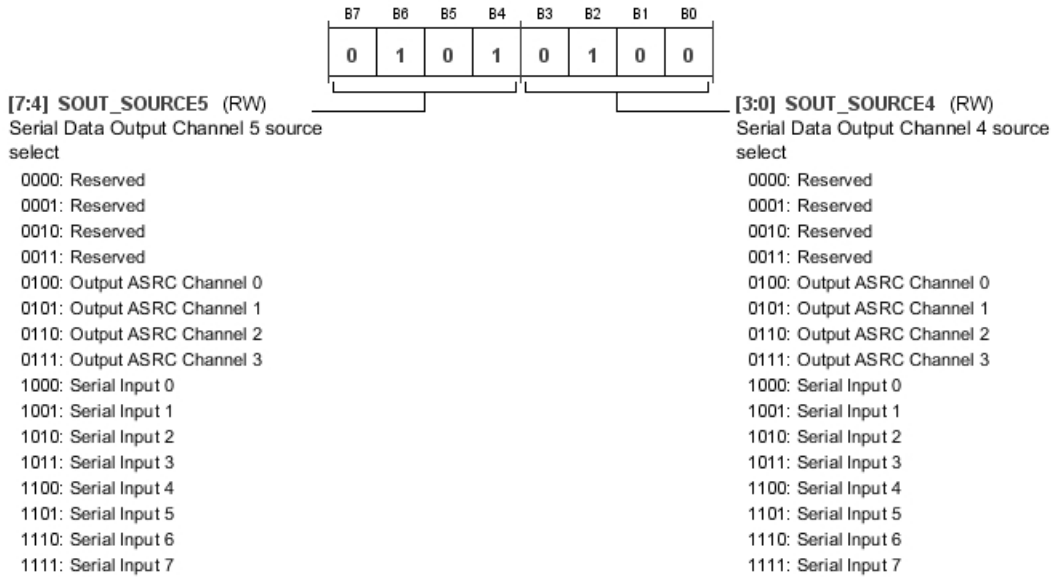


Table 50. Bit Descriptions for SOUT_SOURCE_4_5

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [7:4] | SOUT_SOURCE5 | | Serial Data Output Channel 5 source select. | 0x5 | RW |
| | | 0000 | Reserved | | |
| | | 0001 | Reserved | | |
| | | 0010 | Reserved | | |
| | | 0011 | Reserved | | |
| | | 0100 | Output ASRC Channel 0 | | |
| | | 0101 | Output ASRC Channel 1 | | |
| | | 0110 | Output ASRC Channel 2 | | |
| | | 0111 | Output ASRC Channel 3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|--|---|-------|--------|
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |
| [3:0] | SOUT_SOURCE4 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 | Serial Data Output Channel 4 source select. Reserved Reserved Reserved Reserved Output ASRC Channel 0 Output ASRC Channel 1 Output ASRC Channel 2 Output ASRC Channel 3 Serial Input 0 Serial Input 1 Serial Input 2 Serial Input 3 Serial Input 4 Serial Input 5 Serial Input 6 Serial Input 7 | 0x4 | RW |

SERIAL DATA OUTPUT 6/SERIAL DATA OUTPUT 7 INPUT SELECT REGISTER

Address: 0x0016, Reset: 0x76, Name: SOUT_SOURCE_6_7

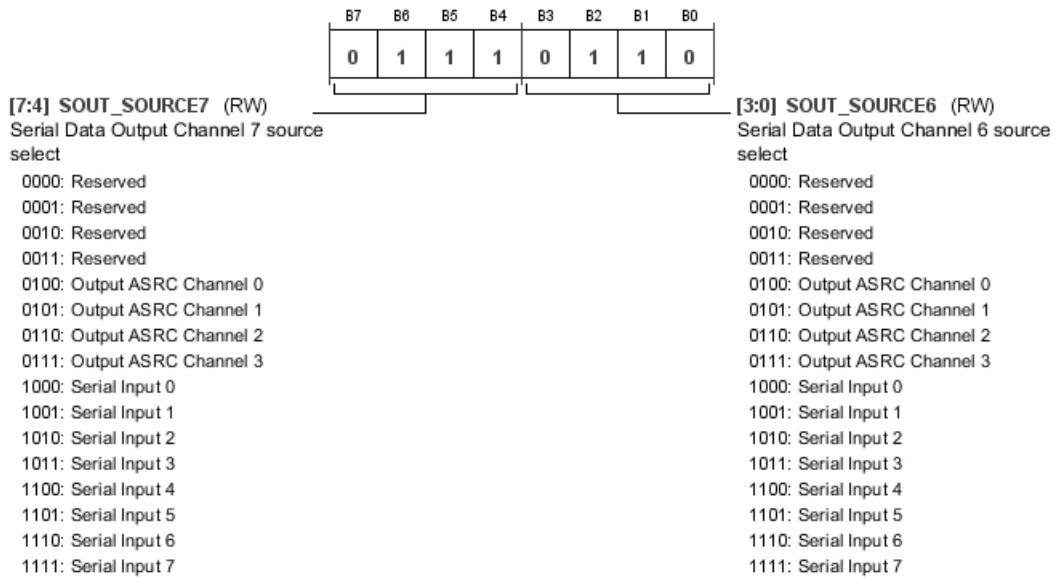


Table 51. Bit Descriptions for SOUT_SOURCE_6_7

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|------------------------------|---|-------|--------|
| [7:4] | SOUT_SOURCE7 | 0000 0001 0010 0011 | Serial Data Output Channel 7 source select. Reserved Reserved Reserved Reserved | 0x7 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| | | 0100 | Output ASRC Channel 0 | | |
| | | 0101 | Output ASRC Channel 1 | | |
| | | 0110 | Output ASRC Channel 2 | | |
| | | 0111 | Output ASRC Channel 3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |
| [3:0] | SOUT_SOURCE6 | | Serial Data Output Channel 6 source select. | 0x6 | RW |
| | | 0000 | Reserved | | |
| | | 0001 | Reserved | | |
| | | 0010 | Reserved | | |
| | | 0011 | Reserved | | |
| | | 0100 | Output ASRC Channel 0 | | |
| | | 0101 | Output ASRC Channel 1 | | |
| | | 0110 | Output ASRC Channel 2 | | |
| | | 0111 | Output ASRC Channel 3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |

ADC_SDATA0/ADC_SDATA1 CHANNEL SELECT REGISTER

Address: 0x0017, Reset: 0x04, Name: ADC_SDATA_CH

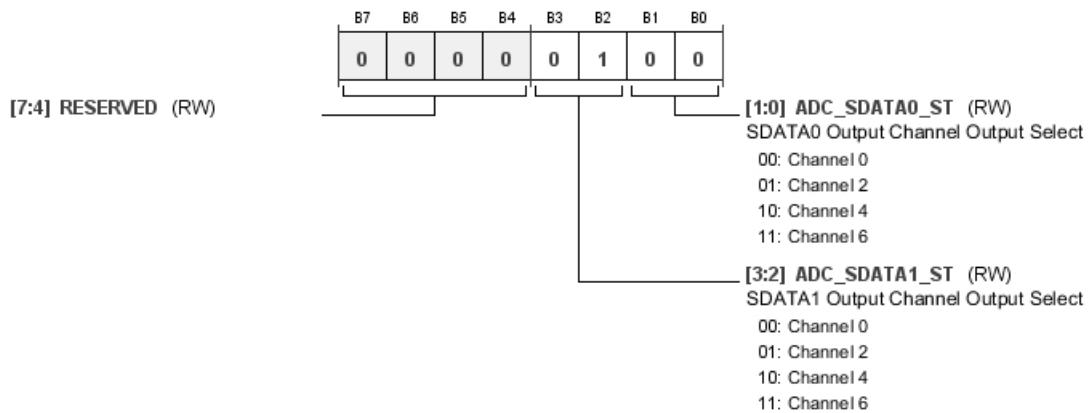


Table 52. Bit Descriptions for ADC_SDATA_CH

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------------------|--|-------|--------|
| [3:2] | ADC_SDATA1_ST | 00 01 10 11 | SDATA1 output channel output select. Selects the output channel at which ADC_SDATA1 starts to output data. The output port sequentially outputs data following this start channel according to the setting of Bit SAI. Channel 0 Channel 2 Channel 4 Channel 6 | 0x1 | RW |
| [1:0] | ADC_SDATA0_ST | 00 01 10 11 | SDATA0 output channel output select. Selects the output channel at which ADC_SDATA0 starts to output data. The output port sequentially outputs data following this start channel according to the setting of Bit SAI. Channel 0 Channel 2 Channel 4 Channel 6 | 0x0 | RW |

OUTPUT ASRC0/OUTPUT ASRC1 SOURCE REGISTER

Address: 0x0018, Reset: 0x10, Name: ASRCO_SOURCE_0_1

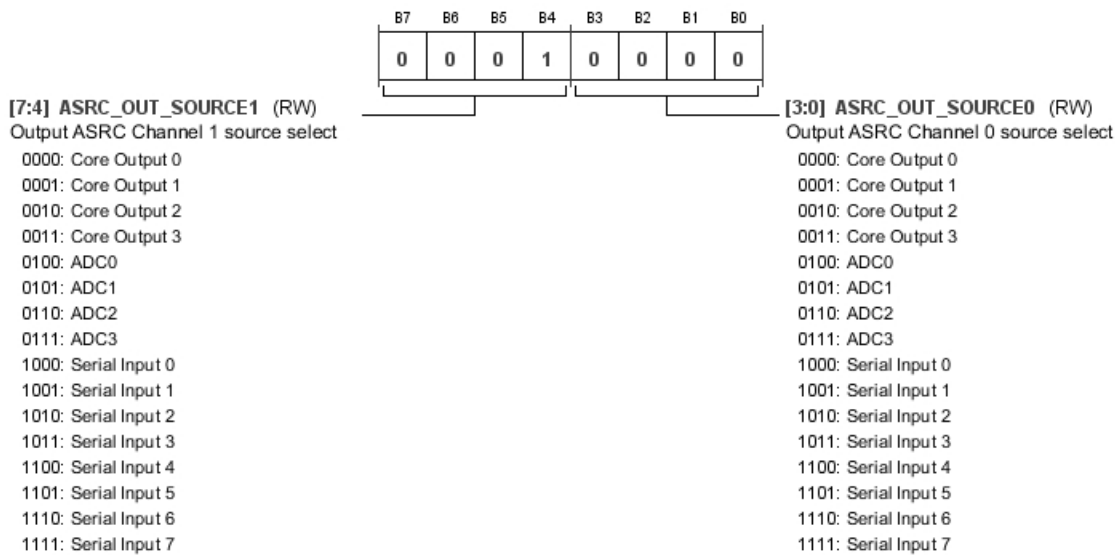


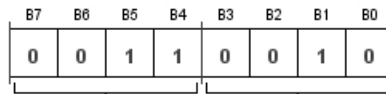
Table 53. Bit Descriptions for ASRCO_SOURCE_0_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------------|--|--|-------|--------|
| [7:4] | ASRC_OUT_SOURCE1 | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 | Output ASRC Channel 1 source select. Core Output 0 Core Output 1 Core Output 2 Core Output 3 ADC0 ADC1 ADC2 ADC3 Serial Input 0 Serial Input 1 Serial Input 2 | 0x1 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------------|----------|--------------------------------------|-------|--------|
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |
| [3:0] | ASRC_OUT_SOURCE0 | | Output ASRC Channel 0 source select. | 0x0 | RW |
| | | 0000 | Core Output 0 | | |
| | | 0001 | Core Output 1 | | |
| | | 0010 | Core Output 2 | | |
| | | 0011 | Core Output 3 | | |
| | | 0100 | ADC0 | | |
| | | 0101 | ADC1 | | |
| | | 0110 | ADC2 | | |
| | | 0111 | ADC3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |

OUTPUT ASRC2/OUTPUT ASRC3 SOURCE REGISTER

Address: 0x0019, Reset: 0x32, Name: ASRCO_SOURCE_2_3



[7:4] ASRC_OUT_SOURCE3 (RW)
 Output ASRC Channel 3 source select

- 0000: Core Output 0
- 0001: Core Output 1
- 0010: Core Output 2
- 0011: Core Output 3
- 0100: ADC0
- 0101: ADC1
- 0110: ADC2
- 0111: ADC3
- 1000: Serial Input 0
- 1001: Serial Input 1
- 1010: Serial Input 2
- 1011: Serial Input 3
- 1100: Serial Input 4
- 1101: Serial Input 5
- 1110: Serial Input 6
- 1111: Serial Input 7

[3:0] ASRC_OUT_SOURCE2 (RW)
 Output ASRC Channel 2 source select

- 0000: Core Output 0
- 0001: Core Output 1
- 0010: Core Output 2
- 0011: Core Output 3
- 0100: ADC0
- 0101: ADC1
- 0110: ADC2
- 0111: ADC3
- 1000: Serial Input 0
- 1001: Serial Input 1
- 1010: Serial Input 2
- 1011: Serial Input 3
- 1100: Serial Input 4
- 1101: Serial Input 5
- 1110: Serial Input 6
- 1111: Serial Input 7

Table 54. Bit Descriptions for ASRCO_SOURCE_2_3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------------|----------|--------------------------------------|-------|--------|
| [7:4] | ASRC_OUT_SOURCE3 | | Output ASRC Channel 3 source select. | 0x3 | RW |
| | | 0000 | Core Output 0 | | |
| | | 0001 | Core Output 1 | | |
| | | 0010 | Core Output 2 | | |
| | | 0011 | Core Output 3 | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------------|----------|----------------|-------|--------|
| | | 0100 | ADC0 | | |
| | | 0101 | ADC1 | | |
| | | 0110 | ADC2 | | |
| | | 0111 | ADC3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |
| [3:0] | ASRC_OUT_SOURCE2 | 0000 | Core Output 0 | 0x2 | RW |
| | | 0001 | Core Output 1 | | |
| | | 0010 | Core Output 2 | | |
| | | 0011 | Core Output 3 | | |
| | | 0100 | ADC0 | | |
| | | 0101 | ADC1 | | |
| | | 0110 | ADC2 | | |
| | | 0111 | ADC3 | | |
| | | 1000 | Serial Input 0 | | |
| | | 1001 | Serial Input 1 | | |
| | | 1010 | Serial Input 2 | | |
| | | 1011 | Serial Input 3 | | |
| | | 1100 | Serial Input 4 | | |
| | | 1101 | Serial Input 5 | | |
| | | 1110 | Serial Input 6 | | |
| | | 1111 | Serial Input 7 | | |

INPUT ASRC CHANNEL SELECT REGISTER

Address: 0x001A, Reset: 0x00, Name: ASRC_MODE

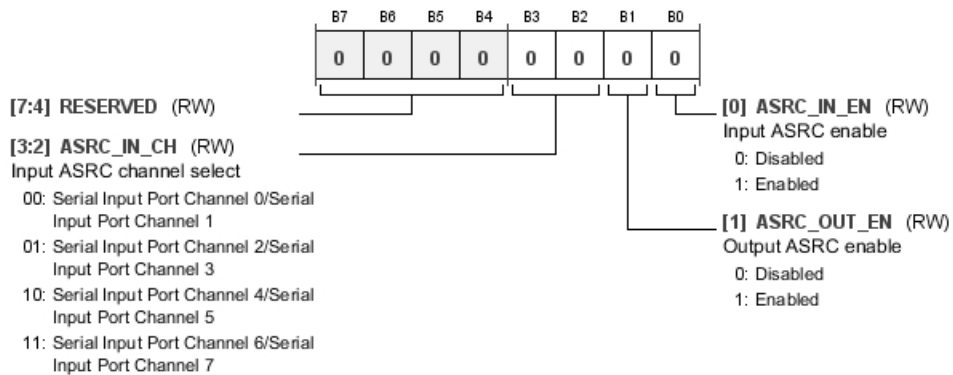


Table 55. Bit Descriptions for ASRC_MODE

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------|---|-------|--------|
| [3:2] | ASRC_IN_CH | 00 | Serial Input Port Channel 0/Serial Input Port Channel 1 | 0x0 | RW |
| | | 01 | Serial Input Port Channel 2/Serial Input Port Channel 3 | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-------------|----------|---|-------|--------|
| | | 10 | Serial Input Port Channel 4/Serial Input Port Channel 5 | | |
| | | 11 | Serial Input Port Channel 6/Serial Input Port Channel 7 | | |
| 1 | ASRC_OUT_EN | 0 1 | Output ASRC enable. Disabled Enabled | 0x0 | RW |
| 0 | ASRC_IN_EN | 0 1 | Input ASRC enable. Disabled Enabled | 0x0 | RW |

ADC0/ADC1 CONTROL 0 REGISTER

Address: 0x001B, Reset: 0x19, Name: ADC_CONTROL0

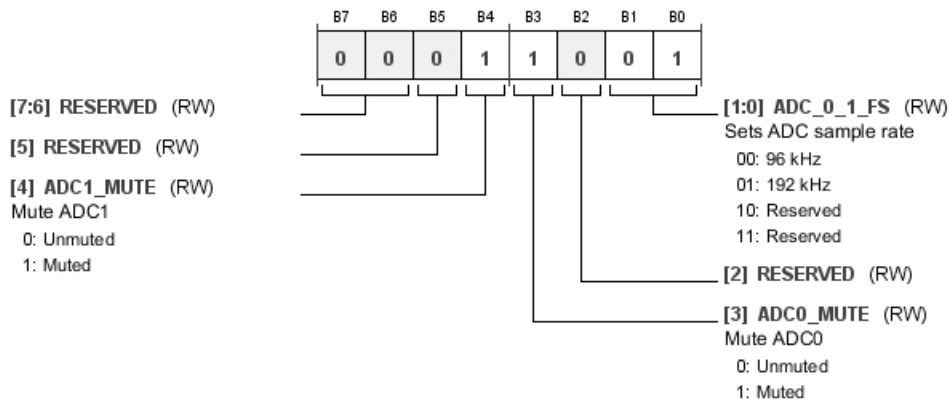


Table 56. Bit Descriptions for ADC_CONTROL0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------------------|---|-------|--------|
| 4 | ADC1_MUTE | 0 1 | Mute ADC1. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. Unmuted Muted | 0x1 | RW |
| 3 | ADC0_MUTE | 0 1 | Mute ADC0. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. Unmuted Muted | 0x1 | RW |
| [1:0] | ADC_0_1_FS | 00 01 10 11 | Sets ADC sample rate. 96 kHz 192 kHz Reserved Reserved | 0x1 | RW |

ADC2/ADC3 CONTROL 0 REGISTER

Address: 0x001C, Reset: 0x19, Name: ADC_CONTROL1

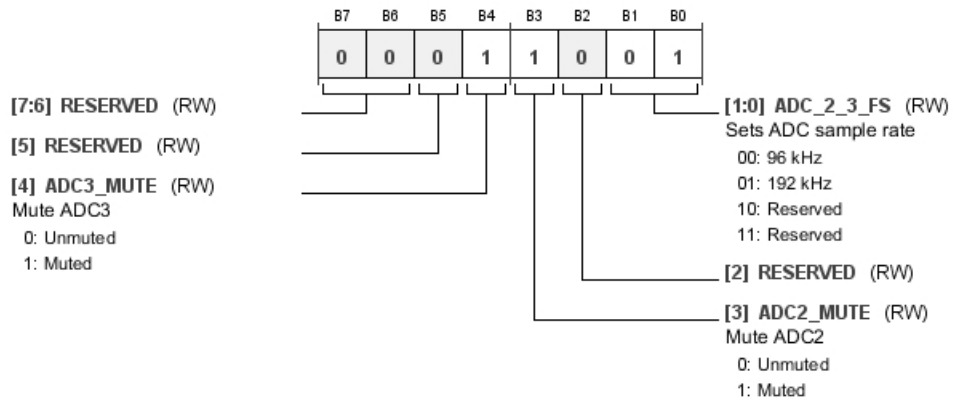


Table 57. Bit Descriptions for ADC_CONTROL1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|------------|----------------------|---|-------|--------|
| 4 | ADC3_MUTE | 0 1 | Mute ADC3. Unmuted Muted | 0x1 | RW |
| 3 | ADC2_MUTE | 0 1 | Mute ADC2. Muting is accomplished by setting the volume control to maximum attenuation. This bit has no effect if volume control is bypassed. Unmuted Muted | 0x1 | RW |
| [1:0] | ADC_2_3_FS | 00 01 10 11 | Sets ADC sample rate. 96 kHz 192 kHz Reserved Reserved | 0x1 | RW |

ADC0/ADC1 CONTROL 1 REGISTER

Address: 0x001D, Reset: 0x00, Name: ADC_CONTROL2

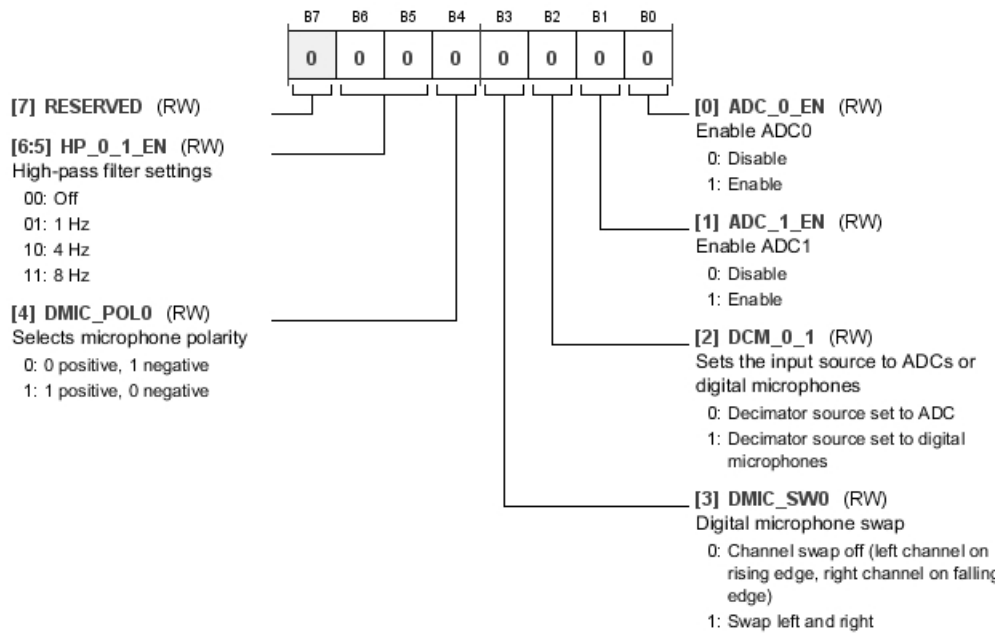


Table 58. Bit Descriptions for ADC_CONTROL2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------|--|-------|--------|
| [6:5] | HP_0_1_EN | 00 01 10 11 | High-pass filter settings. Off 1 Hz 4 Hz 8 Hz | 0x0 | RW |
| 4 | DMIC_POLO | 0 1 | Selects microphone polarity. 0 positive, 1 negative 1 positive, 0 negative | 0x0 | RW |
| 3 | DMIC_SW0 | 0 1 | Digital microphone swap. Channel swap off (left channel on rising edge, right channel on falling edge) Swap left and right | 0x0 | RW |
| 2 | DCM_0_1 | 0 1 | Sets the input source to ADCs or digital microphones. Decimator source set to ADC Decimator source set to digital microphones | 0x0 | RW |
| 1 | ADC_1_EN | 0 1 | Enable ADC1. This bit must be set in conjunction with the SINC_1_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. Disable Enable | 0x0 | RW |
| 0 | ADC_0_EN | 0 1 | Enable ADC0. This bit must be set in conjunction with the SINC_0_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. Disable Enable | 0x0 | RW |

ADC2/ADC3 CONTROL 1 REGISTER

Address: 0x001E, Reset: 0x00, Name: ADC_CONTROL3

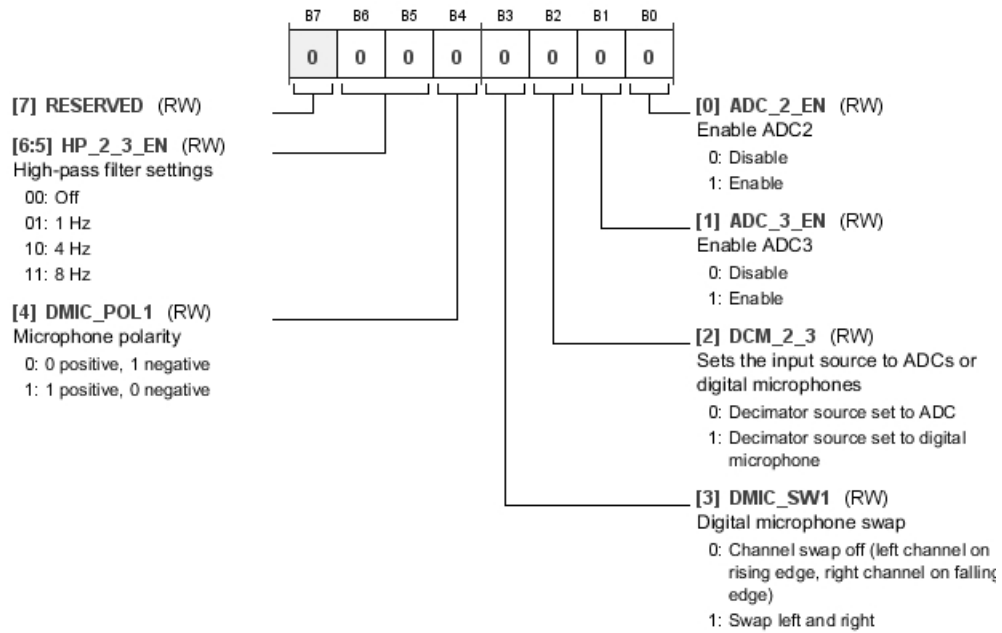


Table 59. Bit Descriptions for ADC_CONTROL3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------|--|-------|--------|
| [6:5] | HP_2_3_EN | 00 01 10 11 | High-pass filter settings. Off 1 Hz 4 Hz 8 Hz | 0x0 | RW |
| 4 | DMIC_POL1 | 0 1 | Microphone polarity. 0 positive, 1 negative 1 positive, 0 negative | 0x0 | RW |
| 3 | DMIC_SW1 | 0 1 | Digital microphone swap. Channel swap off (left channel on rising edge, right channel on falling edge) Swap left and right | 0x0 | RW |
| 2 | DCM_2_3 | 0 1 | Sets the input source to ADCs or digital microphones. Decimator source set to ADC Decimator source set to digital microphone | 0x0 | RW |
| 1 | ADC_3_EN | 0 1 | Enable ADC3. This bit must be set in conjunction with the SINC_3_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. Disable Enable | 0x0 | RW |
| 0 | ADC_2_EN | 0 1 | Enable ADC2. This bit must be set in conjunction with the SINC_2_EN bit in the DECIM_PWR_MODES register to fully enable or disable the ADC. Disable Enable | 0x0 | RW |

ADC0 VOLUME CONTROL REGISTER

Address: 0x001F, Reset: 0x00, Name: ADC0_VOLUME

When SINC_0_EN is set, the volume starts to ramp from -95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/fs, where there are 256 steps between 0 dB and -95.625 dB. For example, with fs = 192 kHz, the volume ramps from -95.625 dB to 0 dB in 21 ms.

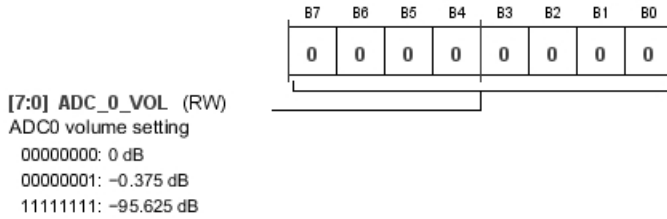


Table 60. Bit Descriptions for ADC0_VOLUME

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | ADC_0_VOL | 00000000 00000001 11111111 | ADC0 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

ADC1 VOLUME CONTROL REGISTER

Address: 0x0020, Reset: 0x00, Name: ADC1_VOLUME

When SINC_1_EN is set, the volume starts to ramp from -95.625 dB to the value in this register. The volume ramp time is (number of steps) × 16/fs, where there are 256 steps between 0 dB and -95.625 dB. For example, with fs = 192 kHz, the volume ramps from -95.625 dB to 0 dB in 21 ms.

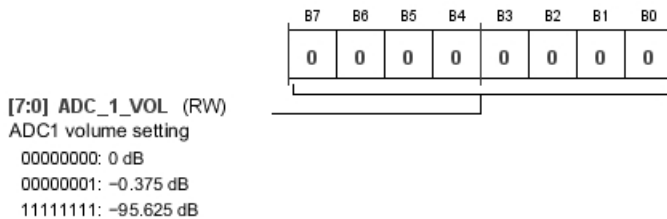
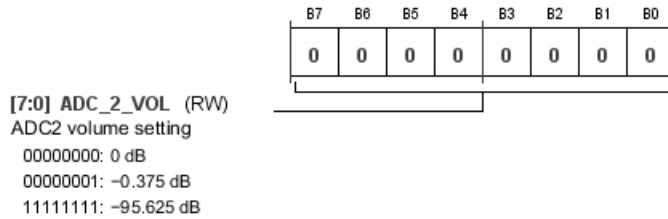


Table 61. Bit Descriptions for ADC1_VOLUME

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | ADC_1_VOL | 00000000 00000001 11111111 | ADC1 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

ADC2 VOLUME CONTROL REGISTER**Address: 0x0021, Reset: 0x00, Name: ADC2_VOLUME**

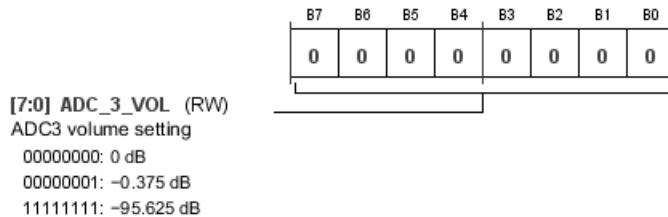
When SINC_2_EN is set, the volume starts to ramp from -95.625 dB to the value in this register. The volume ramp time is (number of steps) $\times 16/f_s$, where there are 256 steps between 0 dB and -95.625 dB. For example, with $f_s = 192$ kHz, the volume ramps from -95.625 dB to 0 dB in 21 ms.

**Table 62. Bit Descriptions for ADC2_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | ADC_2_VOL | 00000000 00000001 11111111 | ADC2 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

ADC3 VOLUME CONTROL REGISTER**Address: 0x0022, Reset: 0x00, Name: ADC3_VOLUME**

When SINC_3_EN is set, the volume starts to ramp from -95.625 dB to the value in this register. The volume ramp time is (number of steps) $\times 16/f_s$, where there are 256 steps between 0 dB and -95.625 dB. For example, with $f_s = 192$ kHz, the volume ramps from -95.625 dB to 0 dB in 21 ms.

**Table 63. Bit Descriptions for ADC3_VOLUME**

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | ADC_3_VOL | 00000000 00000001 11111111 | ADC3 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

PGA CONTROL 0 REGISTER

Address: 0x0023, Reset: 0x40, Name: PGA_CONTROL_0

This register controls the PGA connected to AIN0.

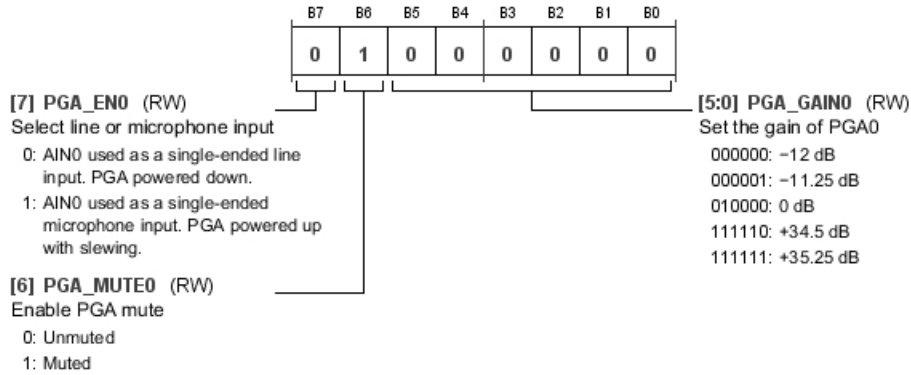


Table 64. Bit Descriptions for PGA_CONTROL_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|--|--|-------|--------|
| 7 | PGA_EN0 | 0 1 | Select line or microphone input. Note that the PGA inverts the signal going through it. 0 AIN0 used as a single-ended line input. PGA powered down. 1 AIN0 used as a single-ended microphone input. PGA powered up with slewing. | 0x0 | RW |
| 6 | PGA_MUTE0 | 0 1 | Enable PGA mute. When PGA is muted, PGA_GAIN0 is ignored. 0 Unmuted 1 Muted | 0x1 | RW |
| [5:0] | PGA_GAIN0 | 000000 000001 010000 111110 111111 | Set the gain of PGA0. -12 dB -11.25 dB 0 dB +34.5 dB +35.25 dB | 0x0 | RW |

PGA CONTROL 1 REGISTER

Address: 0x0024, Reset: 0x40, Name: PGA_CONTROL_1

This register controls the PGA connected to AIN1.

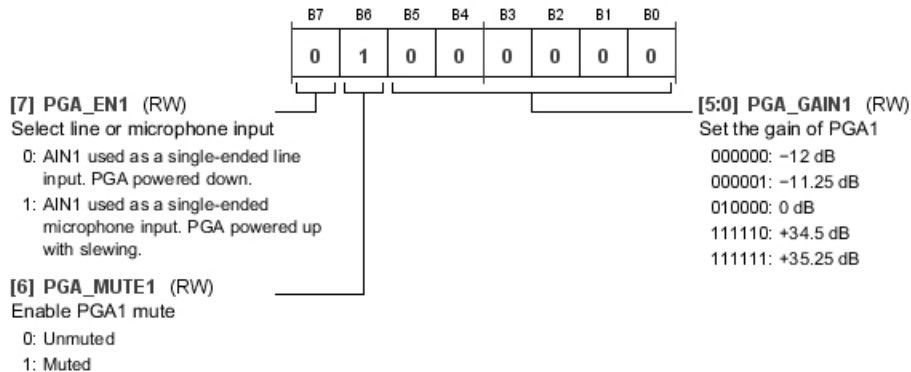


Table 65. Bit Descriptions for PGA_CONTROL_1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|--|--|-------|--------|
| 7 | PGA_EN1 | 0 1 | Select line or microphone input. Note that the PGA inverts the signal going through it. 0 AIN1 used as a single-ended line input. PGA powered down. 1 AIN1 used as a single-ended microphone input. PGA powered up with slewing. | 0x0 | RW |
| 6 | PGA_MUTE1 | 0 1 | Enable PGA1 mute. When PGA is muted, PGA_GAIN1 is ignored. 0 Unmuted 1 Muted | 0x1 | RW |
| [5:0] | PGA_GAIN1 | 000000 000001 010000 111110 111111 | Set the gain of PGA1. –12 dB –11.25 dB 0 dB +34.5 dB +35.25 dB | 0x0 | RW |

PGA CONTROL 2 REGISTER

Address: 0x0025, Reset: 0x40, Name: PGA_CONTROL_2

This register controls the PGA connected to AIN2.

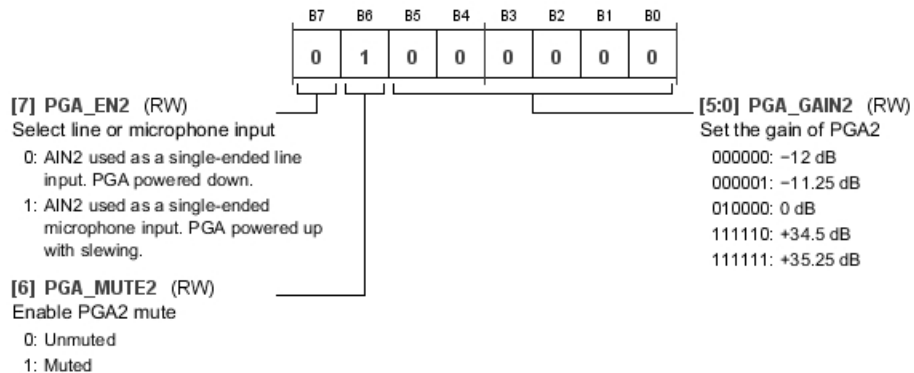


Table 66. Bit Descriptions for PGA_CONTROL_2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|--|--|-------|--------|
| 7 | PGA_EN2 | 0 1 | Select line or microphone input. Note that the PGA inverts the signal going through it. 0 AIN2 used as a single-ended line input. PGA powered down. 1 AIN2 used as a single-ended microphone input. PGA powered up with slewing. | 0x0 | RW |
| 6 | PGA_MUTE2 | 0 1 | Enable PGA2 mute. When PGA is muted, PGA_GAIN2 is ignored. 0 Unmuted 1 Muted | 0x1 | RW |
| [5:0] | PGA_GAIN2 | 000000 000001 010000 111110 111111 | Set the gain of PGA2. –12 dB –11.25 dB 0 dB +34.5 dB +35.25 dB | 0x0 | RW |

PGA CONTROL 3 REGISTER

Address: 0x0026, Reset: 0x40, Name: PGA_CONTROL_3

This register controls the PGA connected to AIN3.

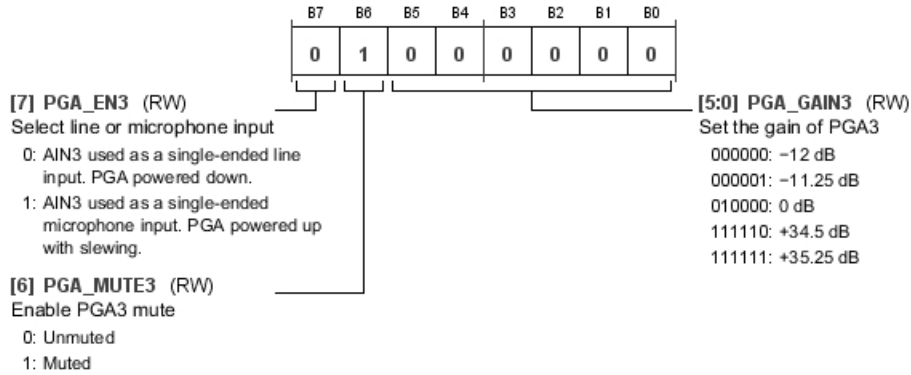


Table 67. Bit Descriptions for PGA_CONTROL_3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|--|--|-------|--------|
| 7 | PGA_EN3 | 0 1 | Select line or microphone input. Note that the PGA inverts the signal going through it. AIN3 used as a single-ended line input. PGA powered down. AIN3 used as a single-ended microphone input. PGA powered up with slewing. | 0x0 | RW |
| 6 | PGA_MUTE3 | 0 1 | Enable PGA3 mute. When PGA is muted, PGA_GAIN3 is ignored. Unmuted Muted | 0x1 | RW |
| [5:0] | PGA_GAIN3 | 000000 000001 010000 111110 111111 | Set the gain of PGA3. -12 dB -11.25 dB 0 dB +34.5 dB +35.25 dB | 0x0 | RW |

PGA SLEW CONTROL REGISTER

Address: 0x0027, Reset: 0x00, Name: PGA_STEP_CONTROL

If PGA slew is disabled with the SLEW_PDx controls, the SLEW_RATE parameter is ignored for that PGA block.

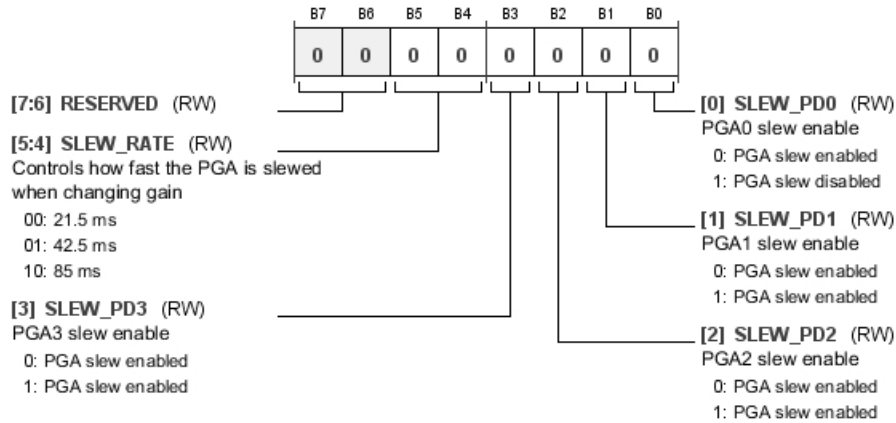


Table 68. Bit Descriptions for PGA_STEP_CONTROL

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------|--|-------|--------|
| [5:4] | SLEW_RATE | 00 01 10 | Controls how fast the PGA is slewed when changing gain. 21.5 ms 42.5 ms 85 ms | 0x0 | RW |
| 3 | SLEW_PD3 | 0 1 | PGA3 slew disable. PGA slew enabled PGA slew disabled | 0x0 | RW |
| 2 | SLEW_PD2 | 0 1 | PGA2 slew disable. PGA slew enabled PGA slew disabled | 0x0 | RW |
| 1 | SLEW_PD1 | 0 1 | PGA1 slew disable. PGA slew enabled PGA slew disabled | 0x0 | RW |
| 0 | SLEW_PD0 | 0 1 | PGA0 slew disable. PGA slew enabled PGA slew disabled | 0x0 | RW |

PGA 10 dB GAIN BOOST REGISTER

Address: 0x0028, Reset: 0x00, Name: PGA_10DB_BOOST

Each PGA can have an additional +10 dB gain added, making the PGA gain range -2 dB to +46 dB.

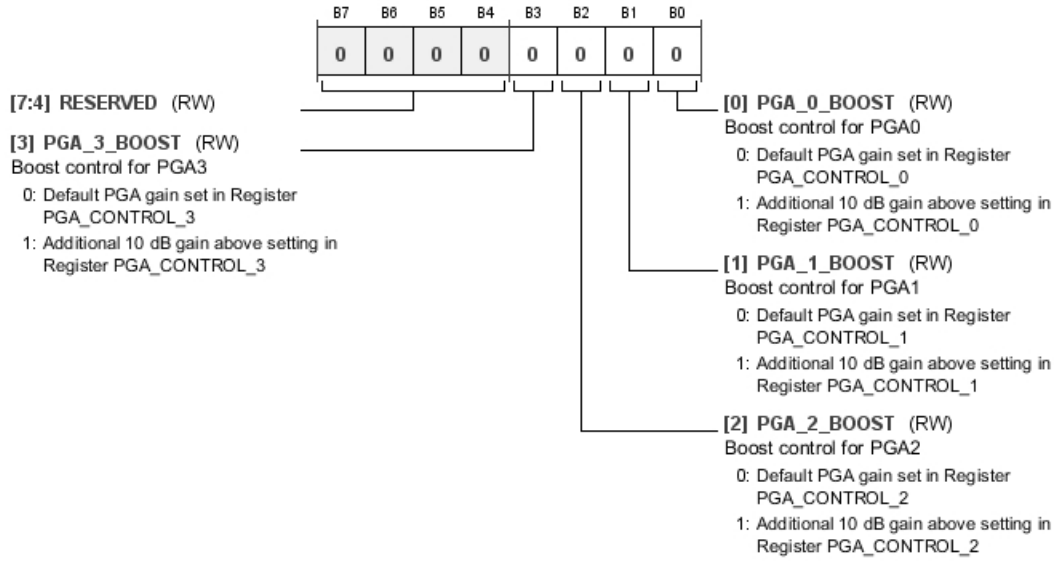


Table 69. Bit Descriptions for PGA_10DB_BOOST

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-------------|----------|--|-------|--------|
| 3 | PGA_3_BOOST | 0 1 | Boost control for PGA3. Default PGA gain set in Register PGA_CONTROL_3 Additional 10 dB gain above setting in Register PGA_CONTROL_3 | 0x0 | RW |
| 2 | PGA_2_BOOST | 0 1 | Boost control for PGA2. Default PGA gain set in Register PGA_CONTROL_2 Additional 10 dB gain above setting in Register PGA_CONTROL_2 | 0x0 | RW |
| 1 | PGA_1_BOOST | 0 1 | Boost control for PGA1. Default PGA gain set in Register PGA_CONTROL_1 Additional 10 dB gain above setting in Register PGA_CONTROL_1 | 0x0 | RW |
| 0 | PGA_0_BOOST | 0 1 | Boost control for PGA0. Default PGA gain set in Register PGA_CONTROL_0 Additional 10 dB gain above setting in Register PGA_CONTROL_0 | 0x0 | RW |

INPUT AND OUTPUT CAPACITOR CHARGING REGISTER

Address: 0x0029, Reset: 0x3F, Name: POP_SUPPRESS

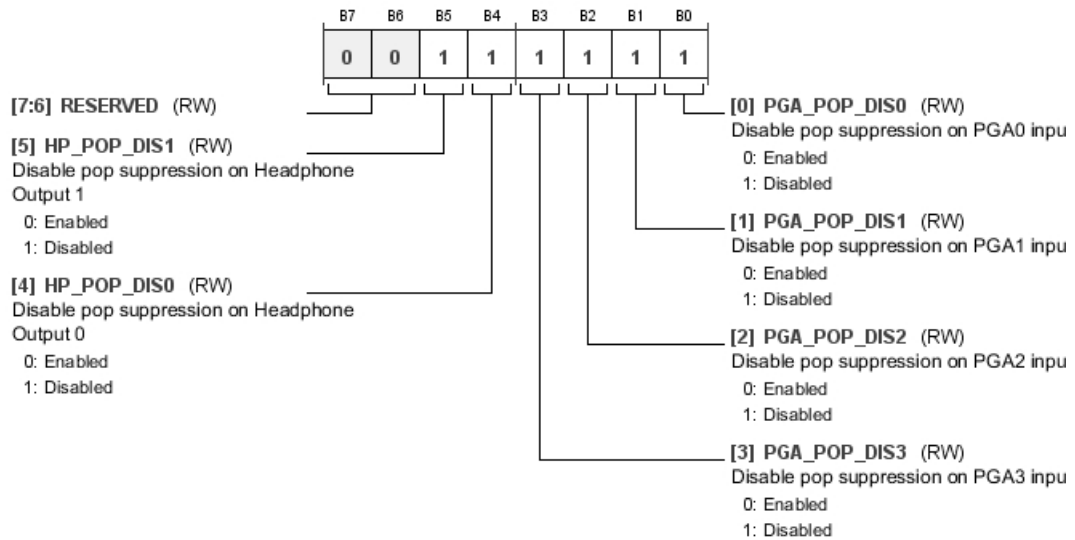


Table 70. Bit Descriptions for POP_SUPPRESS

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|--------------|----------|---|-------|--------|
| 5 | HP_POP_DIS1 | 0 1 | Disable pop suppression on Headphone Output 1. Enabled Disabled | 0x1 | RW |
| 4 | HP_POP_DIS0 | 0 1 | Disable pop suppression on Headphone Output 0. Enabled Disabled | 0x1 | RW |
| 3 | PGA_POP_DIS3 | 0 1 | Disable pop suppression on PGA3 input. Enabled Disabled | 0x1 | RW |
| 2 | PGA_POP_DIS2 | 0 1 | Disable pop suppression on PGA2 input. Enabled Disabled | 0x1 | RW |
| 1 | PGA_POP_DIS1 | 0 1 | Disable pop suppression on PGA1 input. Enabled Disabled | 0x1 | RW |
| 0 | PGA_POP_DIS0 | 0 1 | Disable pop suppression on PGA0 input. Enabled Disabled | 0x1 | RW |

DSP BYPASS PATH REGISTER

Address: 0x002A, Reset: 0x00, Name: TALKTHRU

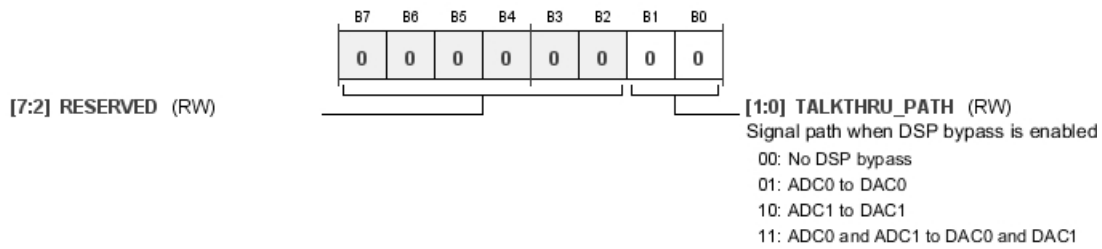


Table 71. Bit Descriptions for TALKTHRU

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|---------------|----------------------|--|-------|--------|
| [1:0] | TALKTHRU_PATH | 00 01 10 11 | Signal path when DSP bypass is enabled. No DSP bypass ADC0 to DAC0 ADC1 to DAC1 ADC0 and ADC1 to DAC0 and DAC1 | 0x0 | RW |

DSP BYPASS GAIN FOR PGA0 REGISTER

Address: 0x002B, Reset: 0x00, Name: TALKTHRU_GAIN0

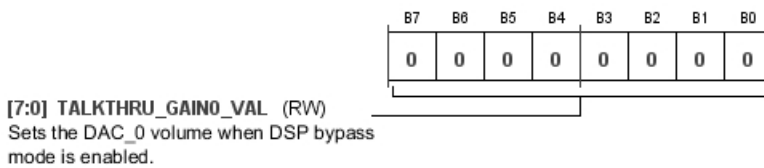


Table 72. Bit Descriptions for TALKTHRU_GAIN0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------------|----------|---|-------|--------|
| [7:0] | TALKTHRU_GAIN0_VAL | | Sets the DAC0 volume when DSP bypass mode is enabled. | 0x00 | RW |

DSP BYPASS GAIN FOR PGA1 REGISTER

Address: 0x002C, Reset: 0x00, Name: TALKTHRU_GAIN1

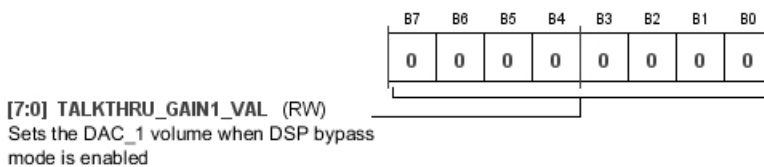


Table 73. Bit Descriptions for TALKTHRU_GAIN1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------------|----------|---|-------|--------|
| [7:0] | TALKTHRU_GAIN1_VAL | | Sets the DAC1 volume when DSP bypass mode is enabled. | 0x00 | RW |

MIC_BIAS0_1 CONTROL REGISTER

Address: 0x002D, Reset: 0x00, Name: MIC_BIAS

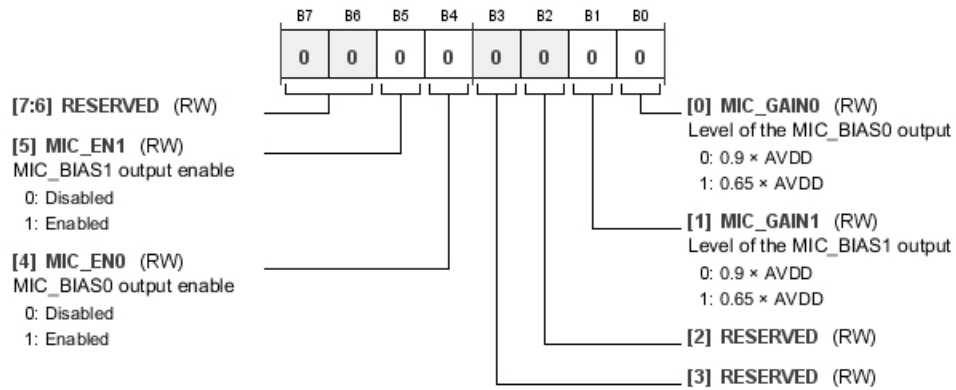


Table 74. Bit Descriptions for MIC_BIAS

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------|----------|--|-------|--------|
| 5 | MIC_EN1 | 0 1 | MICBIAS1 output enable. Disabled Enabled | 0x0 | RW |
| 4 | MIC_EN0 | 0 1 | MICBIAS0 output enable. Disabled Enabled | 0x0 | RW |
| 1 | MIC_GAIN1 | 0 1 | Level of the MICBIAS1 output. 0.9 × AVDD 0.65 × AVDD | 0x0 | RW |
| 0 | MIC_GAIN0 | 0 1 | Level of the MICBIAS0 output. 0.9 × AVDD 0.65 × AVDD | 0x0 | RW |

DAC CONTROL REGISTER

Address: 0x002E, Reset: 0x18, Name: DAC_CONTROL1

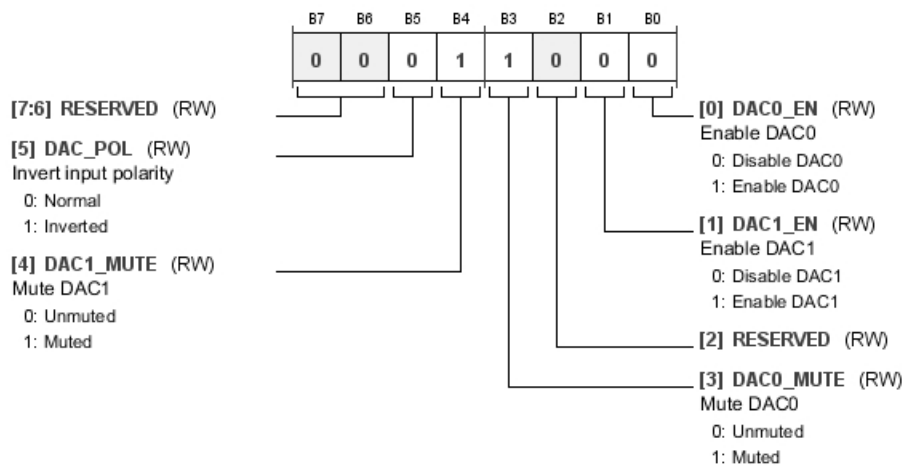
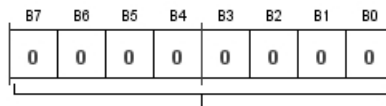


Table 75. Bit Descriptions for DAC_CONTROL1

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------|----------|--|-------|--------|
| 5 | DAC_POL | 0 1 | Invert input polarity. Normal Inverted | 0x0 | RW |
| 4 | DAC1_MUTE | 0 1 | Mute DAC1. Unmuted Muted | 0x1 | RW |
| 3 | DAC0_MUTE | 0 1 | Mute DAC0. Unmuted Muted | 0x1 | RW |
| 1 | DAC1_EN | 0 1 | Enable DAC1. Disable DAC1 Enable DAC1 | 0x0 | RW |
| 0 | DAC0_EN | 0 1 | Enable DAC0. Disable DAC0 Enable DAC0 | 0x0 | RW |

DAC0 VOLUME CONTROL REGISTER

Address: 0x002F, Reset: 0x00, Name: DAC0_VOLUME



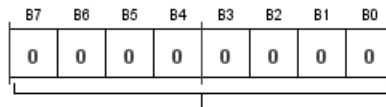
[7:0] DAC_0_VOL (RW)
 DAC0 volume setting
 00000000: 0 dB
 00000001: -0.375 dB
 11111111: -95.625 dB

Table 76. Bit Descriptions for DAC0_VOLUME

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | DAC_0_VOL | 00000000 00000001 11111111 | DAC0 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

DAC1 VOLUME CONTROL REGISTER

Address: 0x0030, Reset: 0x00, Name: DAC1_VOLUME



[7:0] DAC_1_VOL (RW)
 DAC1 volume setting
 00000000: 0 dB
 00000001: -0.375 dB
 11111111: -95.625 dB

Table 77. Bit Descriptions for DAC1_VOLUME

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------------------|---|-------|--------|
| [7:0] | DAC_1_VOL | 00000000 00000001 11111111 | DAC1 volume setting. 0 dB -0.375 dB -95.625 dB | 0x00 | RW |

HEADPHONE OUTPUT MUTES REGISTER

Address: 0x0031, Reset: 0x0F, Name: OP_STAGE_MUTES

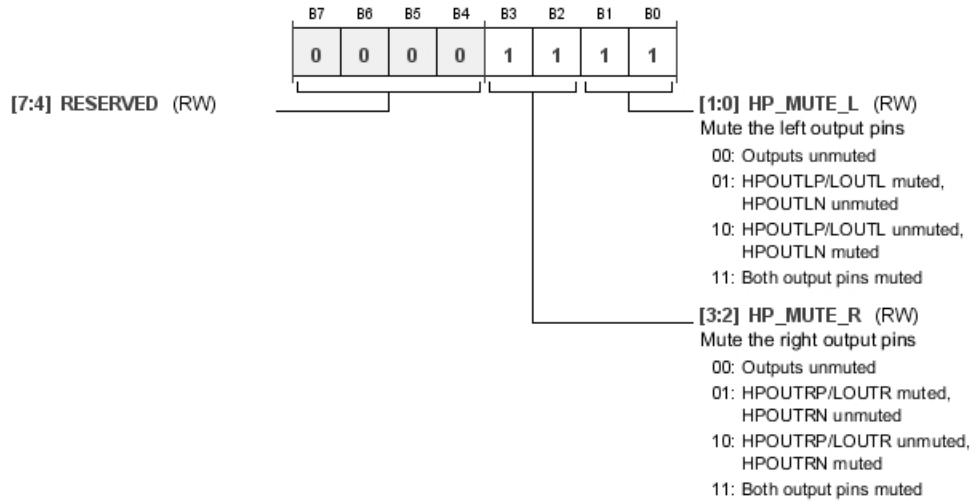


Table 78. Bit Descriptions for OP_STAGE_MUTES

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------|----------------------|---|-------|--------|
| [3:2] | HP_MUTE_R | 00 01 10 11 | Mute the right output pins. When a pin is muted, it can be used as a common-mode output. Outputs unmuted HPOUTRP/LOUTRP muted, HPOUTRN/LOUTRN unmuted HPOUTRP/LOUTRP unmuted, HPOUTRN/LOUTRN muted Both output pins muted | 0x3 | RW |
| [1:0] | HP_MUTE_L | 00 01 10 11 | Mute the left output pins. When a pin is muted, it can be used as a common-mode output. Outputs unmuted HPOUTLP/LOUTLP muted, HPOUTLN/LOUTLN unmuted HPOUTLP/LOUTLP unmuted, HPOUTLN/LOUTLN muted Both output pins muted | 0x3 | RW |

SERIAL PORT CONTROL 0 REGISTER

Address: 0x0032, Reset: 0x00, Name: SAI_0

Using 16-bit serial I/O limits device performance.

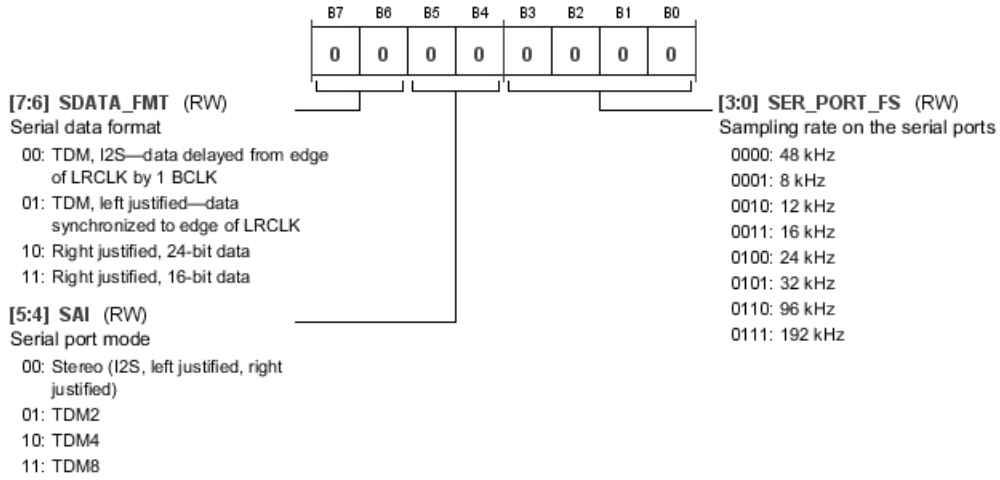


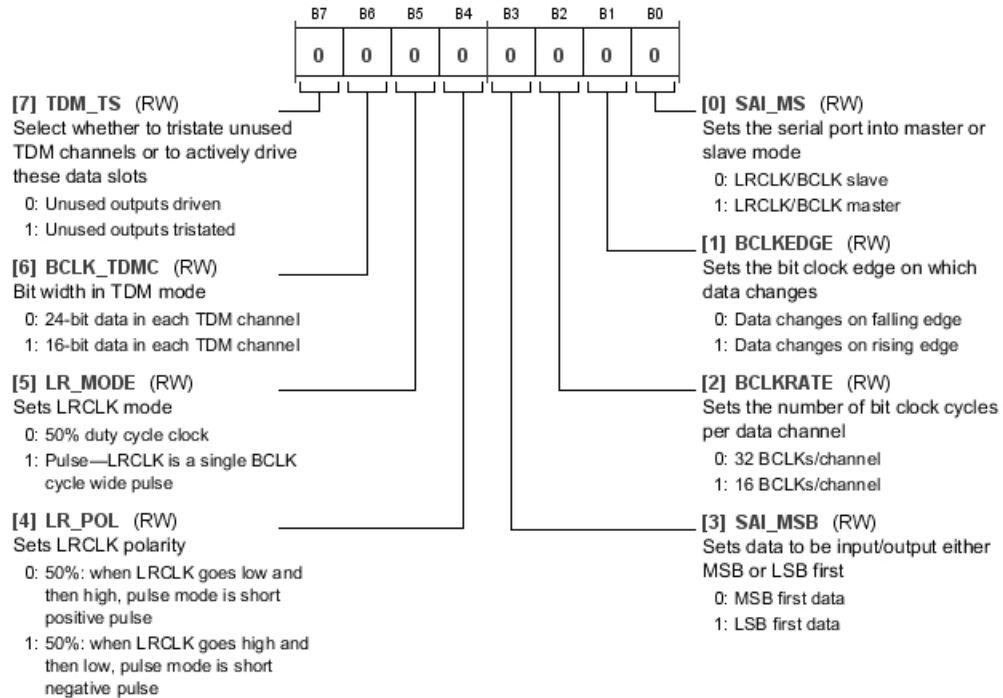
Table 79. Bit Descriptions for SAI_0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|--|--|-------|--------|
| [7:6] | SDATA_FMT | 00 01 10 11 | Serial data format. TDM, I ² S—data delayed from edge of LRCLK by 1 BCLK cycle TDM, left justified—data synchronized to edge of LRCLK Right justified, 24-bit data Right justified, 16-bit data | 0x0 | RW |
| [5:4] | SAI | 00 01 10 11 | Serial port mode. Stereo (I ² S, left justified, right justified) TDM2 TDM4 TDM8 | 0x0 | RW |
| [3:0] | SER_PORT_FS | 0000 0001 0010 0011 0100 0101 0110 0111 | Sampling rate on the serial ports. 48 kHz 8 kHz 12 kHz 16 kHz 24 kHz 32 kHz 96 kHz 192 kHz | 0x0 | RW |

SERIAL PORT CONTROL 1 REGISTER

Address: 0x0033, Reset: 0x00, Name: SAI_1

Using 16-bit serial I/O limits device performance.

**Table 80. Bit Descriptions for SAI_1**

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------|----------|---|-------|--------|
| 7 | TDM_TS | | Select whether to tristate unused TDM channels or to actively drive these data slots. | 0x0 | RW |
| | | 0 | Unused outputs driven | | |
| | | 1 | Unused outputs tristated | | |
| 6 | BCLK_TDMC | | Bit width in TDM mode. | 0x0 | RW |
| | | 0 | 24-bit data in each TDM channel | | |
| | | 1 | 16-bit data in each TDM channel | | |
| 5 | LR_MODE | | Sets LRCLK mode. | 0x0 | RW |
| | | 0 | 50% duty cycle clock | | |
| | | 1 | Pulse—LRCLK is a single BCLK cycle wide pulse | | |
| 4 | LR_POL | | Sets LRCLK polarity. | 0x0 | RW |
| | | 0 | 50%: when LRCLK goes low and then high, pulse mode is short positive pulse | | |
| | | 1 | 50%: when LRCLK goes high and then low, pulse mode is short negative pulse | | |
| 3 | SAI_MSB | | Sets data to be input/output either MSB or LSB first. | 0x0 | RW |
| | | 0 | MSB first data | | |
| | | 1 | LSB first data | | |
| 2 | BCLKRATE | | Sets the number of bit clock cycles per data channel. | 0x0 | RW |
| | | 0 | 32 BCLK cycles/channel | | |
| | | 1 | 16 BCLK cycles/channel | | |
| 1 | BCLKEDGE | | Sets the bit clock edge on which data changes. | 0x0 | RW |
| | | 0 | Data changes on falling edge | | |
| | | 1 | Data changes on rising edge | | |
| 0 | SAI_MS | | Sets the serial port into master or slave mode. | 0x0 | RW |
| | | 0 | LRCLK/BCLK slave | | |
| | | 1 | LRCLK/BCLK master | | |

TDM OUTPUT CHANNEL DISABLE REGISTER

Address: 0x0034, Reset: 0x00, Name: SOUT_CONTROL0

This register is for use only in TDM mode.

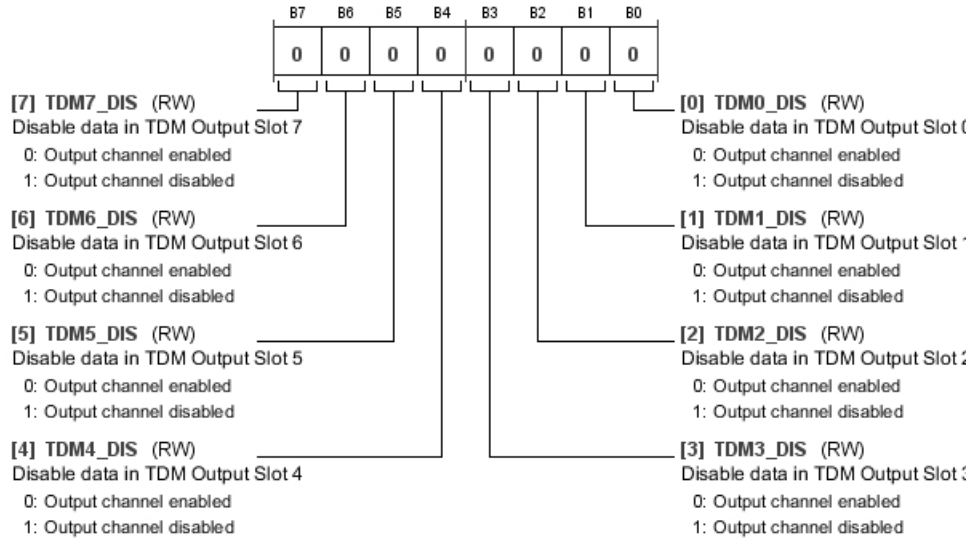


Table 81. Bit Descriptions for SOUT_CONTROL0

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 7 | TDM7_DIS | 0 1 | Disable data in TDM Output Slot 7. Output channel enabled Output channel disabled | 0x0 | RW |
| 6 | TDM6_DIS | 0 1 | Disable data in TDM Output Slot 6. Output channel enabled Output channel disabled | 0x0 | RW |
| 5 | TDM5_DIS | 0 1 | Disable data in TDM Output Slot 5. Output channel enabled Output channel disabled | 0x0 | RW |
| 4 | TDM4_DIS | 0 1 | Disable data in TDM Output Slot 4. Output channel enabled Output channel disabled | 0x0 | RW |
| 3 | TDM3_DIS | 0 1 | Disable data in TDM Output Slot 3. Output channel enabled Output channel disabled | 0x0 | RW |
| 2 | TDM2_DIS | 0 1 | Disable data in TDM Output Slot 2. Output channel enabled Output channel disabled | 0x0 | RW |
| 1 | TDM1_DIS | 0 1 | Disable data in TDM Output Slot 1. Output channel enabled Output channel disabled | 0x0 | RW |
| 0 | TDM0_DIS | 0 1 | Disable data in TDM Output Slot 0. Output channel enabled Output channel disabled | 0x0 | RW |

PDM ENABLE REGISTER

Address: 0x0036, Reset: 0x00, Name: PDM_OUT

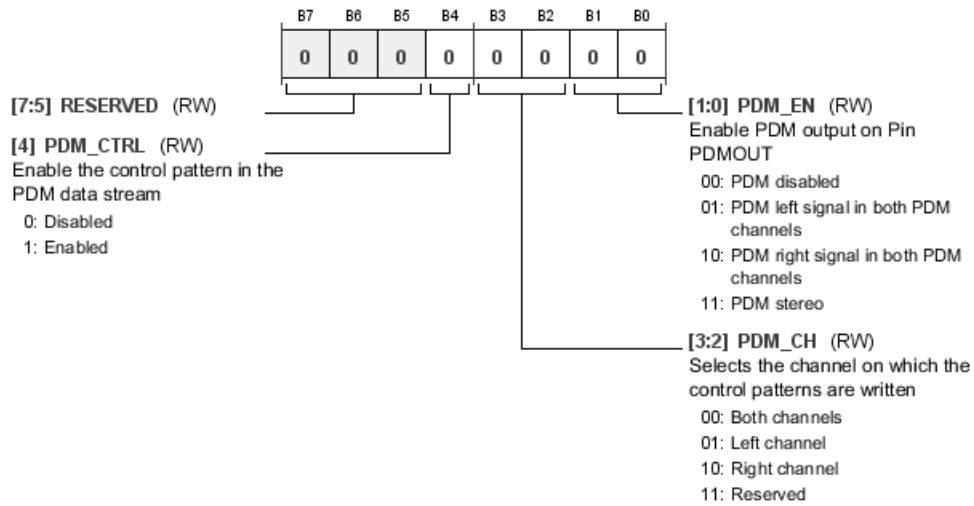


Table 82. Bit Descriptions for PDM_OUT

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------------------|--|-------|--------|
| 4 | PDM_CTRL | 0 1 | Enable the control pattern in the PDM data stream. Disabled Enabled | 0x0 | RW |
| [3:2] | PDM_CH | 00 01 10 11 | Selects the channel on which the control patterns are written. These control bits should not be changed while the PDM channel is operating and transmitting audio. Both channels Left channel Right channel Reserved | 0x0 | RW |
| [1:0] | PDM_EN | 00 01 10 11 | Enable PDM output on Pin PDMOUT. PDM disabled PDM left signal in both PDM channels PDM right signal in both PDM channels PDM stereo | 0x0 | RW |

PDM PATTERN SETTING REGISTER

Address: 0x0037, Reset: 0x00, Name: PDM_PATTERN

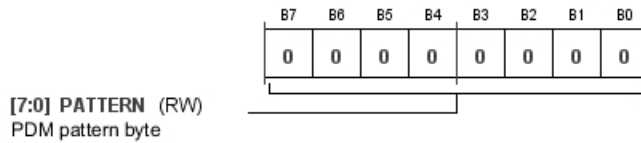


Table 83. Bit Descriptions for PDM_PATTERN

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------|---|-------|--------|
| [7:0] | PATTERN | | PDM pattern byte. The PDM pattern byte should not be changed while the PDM channel is operating and transmitting the pattern. | 0x00 | RW |

MP0 FUNCTION SETTING REGISTER

Address: 0x0038, Reset: 0x00, Name: MODE_MP0

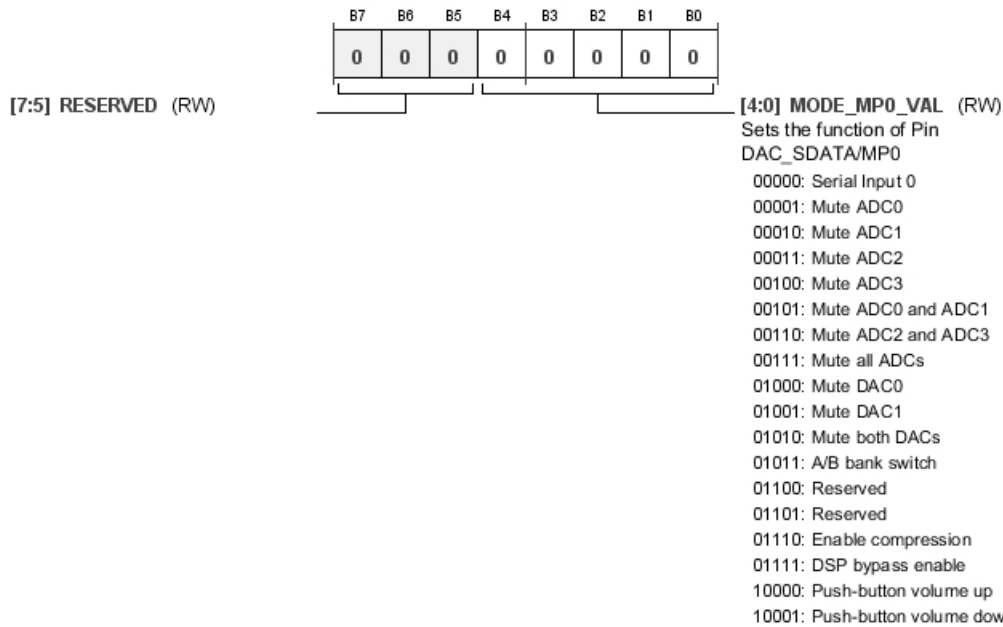


Table 84. Bit Descriptions for MODE_MP0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [4:0] | MODE_MP0_VAL | | Sets the function of Pin DAC_SDATA/MP0. | 0x00 | RW |
| | | 00000 | Serial Input 0 | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------------------|-------|--------|
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |

MP1 FUNCTION SETTING REGISTER

Address: 0x0039, Reset: 0x10, Name: MODE_MP1

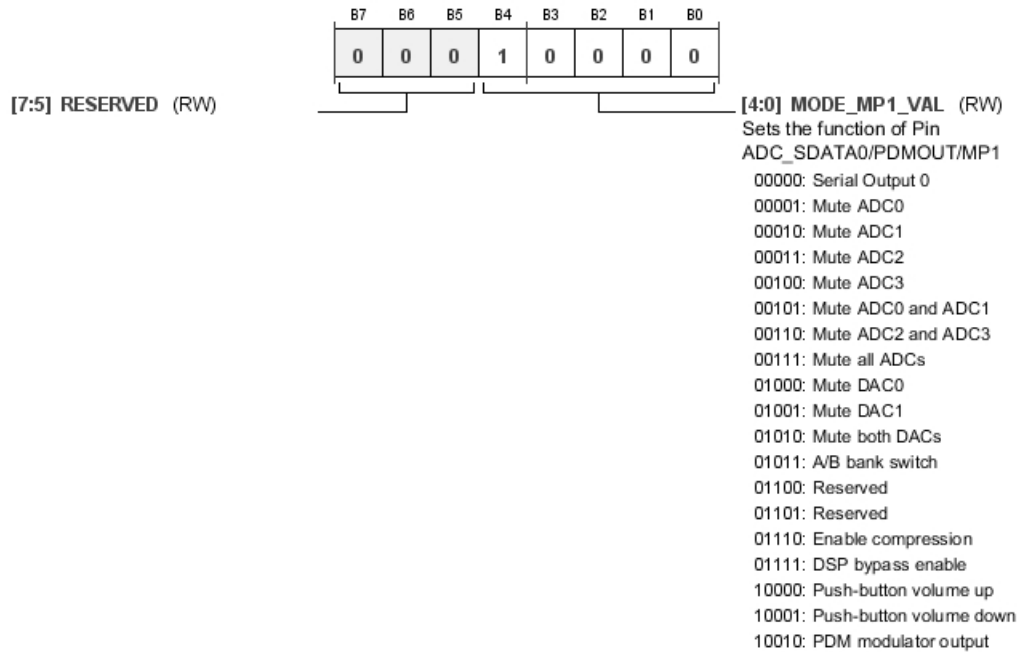


Table 85. Bit Descriptions for MODE_MP1

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [4:0] | MODE_MP1_VAL | | Sets the function of Pin ADC_SDATA0/PDMOUT/MP1. | 0x10 | RW |
| | | 00000 | Serial Output 0 | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------------------|-------|--------|
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |
| | | 10010 | PDM modulator output | | |

MP2 FUNCTION SETTING REGISTER

Address: 0x003A, Reset: 0x00, Name: MODE_MP2

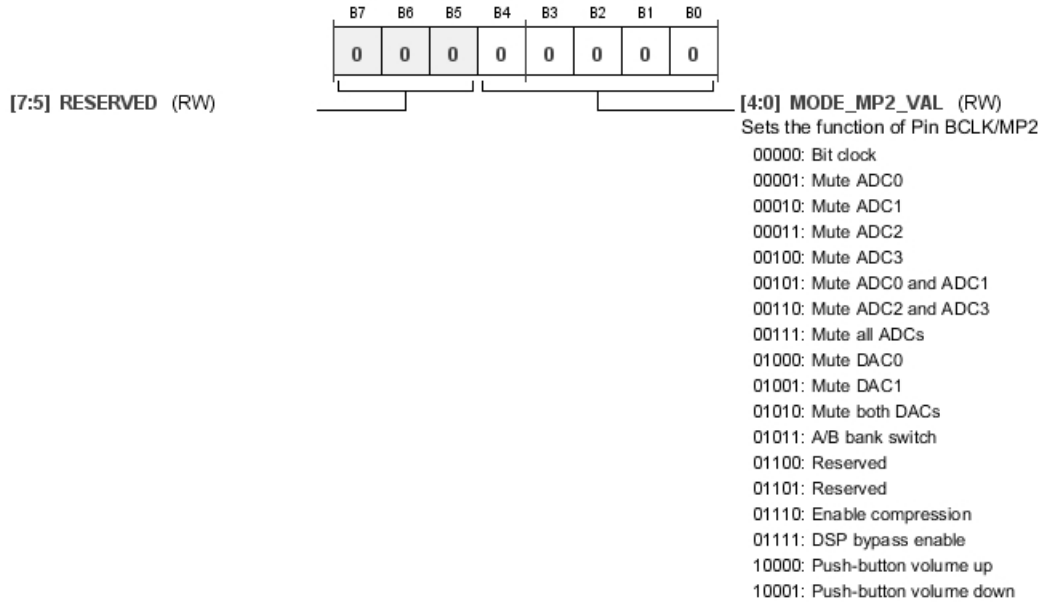


Table 86. Bit Descriptions for MODE_MP2

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|------------------------------------|-------|--------|
| [4:0] | MODE_MP2_VAL | | Sets the function of Pin BCLK/MP2. | 0x00 | RW |
| | | 00000 | Bit clock | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |

MP3 FUNCTION SETTING REGISTER

Address: 0x003B, Reset: 0x00, Name: MODE_MP3

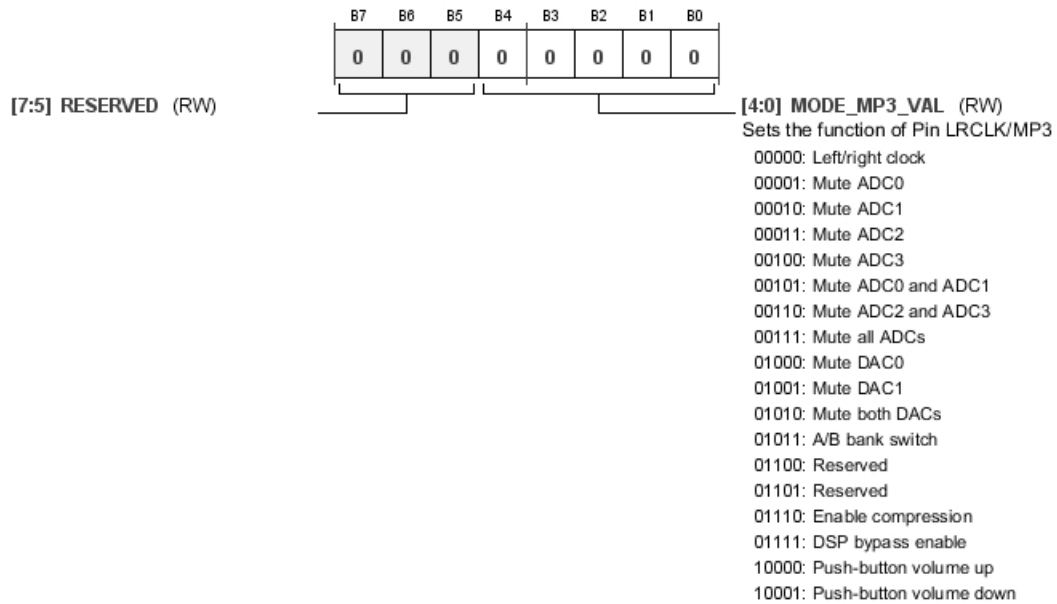


Table 87. Bit Descriptions for MODE_MP3

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|-------------------------------------|-------|--------|
| [4:0] | MODE_MP3_VAL | | Sets the function of Pin LRCLK/MP3. | 0x00 | RW |
| | | 00000 | Left/right clock | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |

MP4 FUNCTION SETTING REGISTER

Address: 0x003C, Reset: 0x00, Name: MODE_MP4

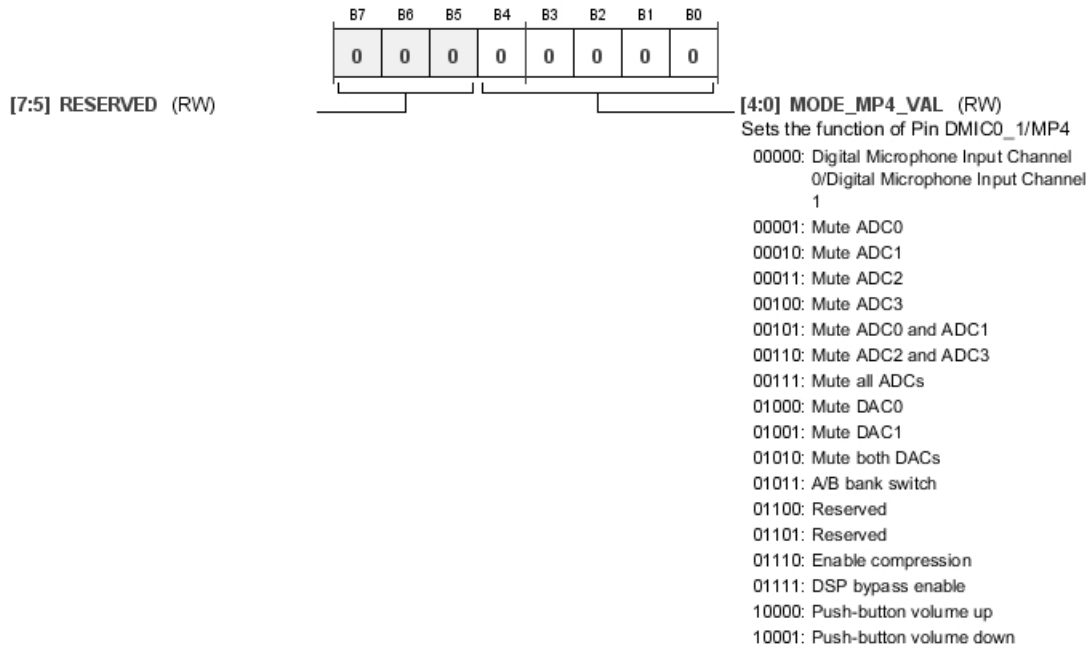
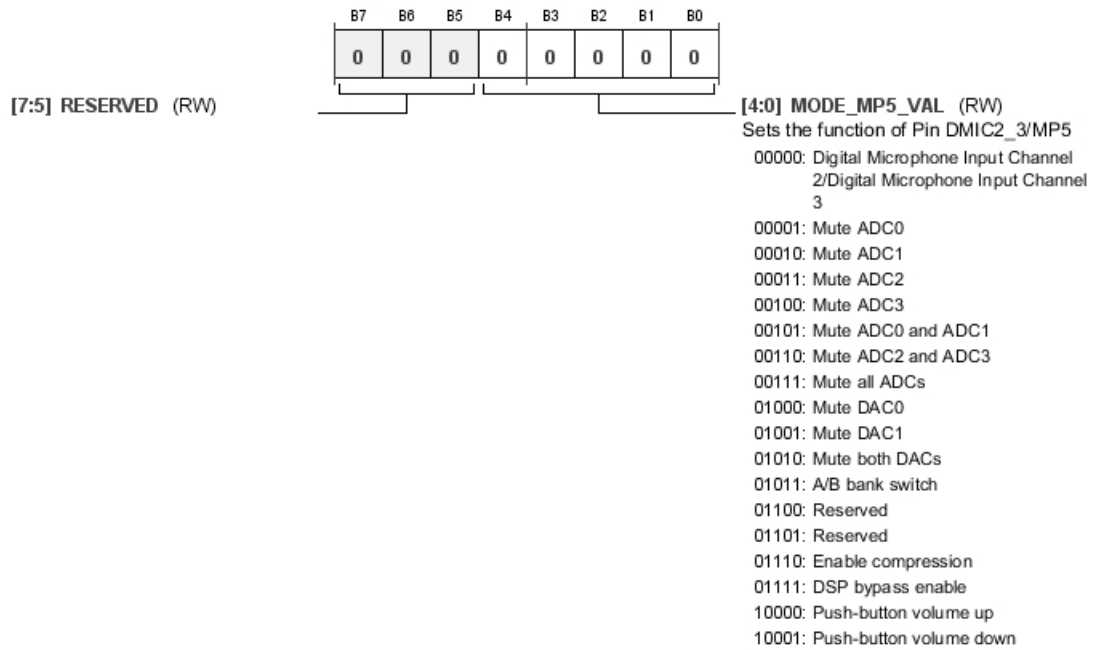


Table 88. Bit Descriptions for MODE_MP4

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [4:0] | MODE_MP4_VAL | | Sets the function of Pin DMIC0_1/MP4. | 0x00 | RW |
| | | 00000 | Digital Microphone Input Channel 0/Digital Microphone Input Channel 1 | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |

MP5 FUNCTION SETTING REGISTER

Address: 0x003D, Reset: 0x00, Name: MODE_MP5

**Table 89. Bit Descriptions for MODE_MP5**

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [4:0] | MODE_MP5_VAL | | Sets the function of Pin DMIC2_3/MP5. | 0x00 | RW |
| | | 00000 | Digital Microphone Input Channel 2/Digital Microphone Input Channel 3 | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |

MP6 FUNCTION SETTING REGISTER

Address: 0x003E, Reset: 0x11, Name: MODE_MP6

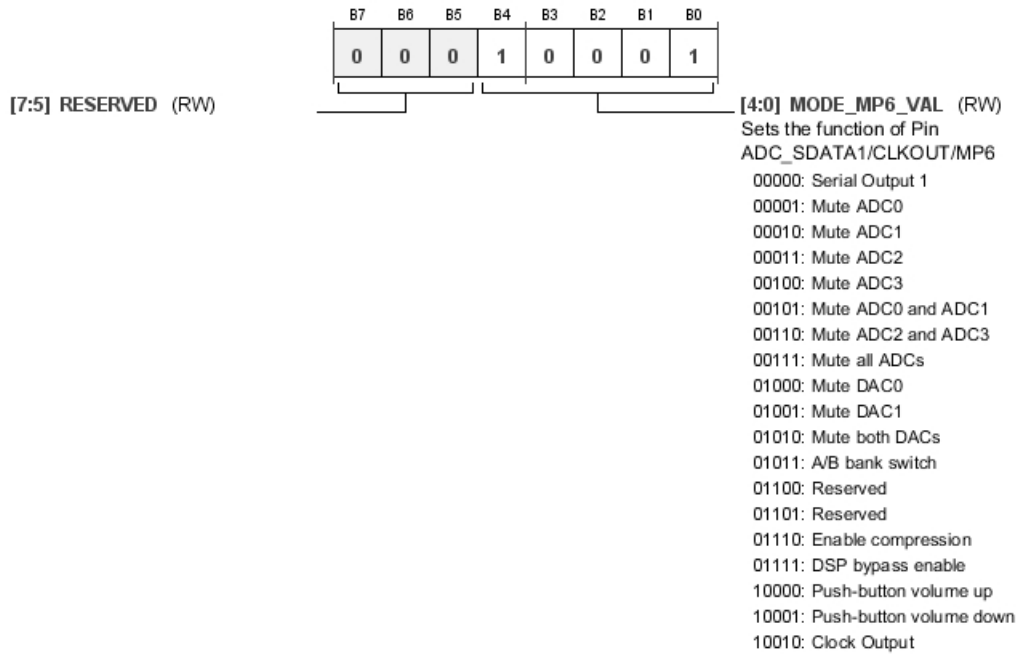


Table 90. Bit Descriptions for MODE_MP6

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|--------------|----------|---|-------|--------|
| [4:0] | MODE_MP6_VAL | | Sets the function of Pin ADC_SDATA1/CLKOUT/MP6. | 0x11 | RW |
| | | 00000 | Serial Output 1 | | |
| | | 00001 | Mute ADC0 | | |
| | | 00010 | Mute ADC1 | | |
| | | 00011 | Mute ADC2 | | |
| | | 00100 | Mute ADC3 | | |
| | | 00101 | Mute ADC0 and ADC1 | | |
| | | 00110 | Mute ADC2 and ADC3 | | |
| | | 00111 | Mute all ADCs | | |
| | | 01000 | Mute DAC0 | | |
| | | 01001 | Mute DAC1 | | |
| | | 01010 | Mute both DACs | | |
| | | 01011 | A/B bank switch | | |
| | | 01100 | Reserved | | |
| | | 01101 | Reserved | | |
| | | 01110 | Enable compression | | |
| | | 01111 | DSP bypass enable | | |
| | | 10000 | Push-button volume up | | |
| | | 10001 | Push-button volume down | | |
| | | 10010 | Clock output | | |

PUSH-BUTTON VOLUME SETTINGS REGISTER

Address: 0x003F, Reset: 0x00, Name: PB_VOL_SET

This register must be written before Bits PB_VOL_CONV_VAL are set to something other than the default value. Otherwise, the push-button volume control is initialized to -96 dB.

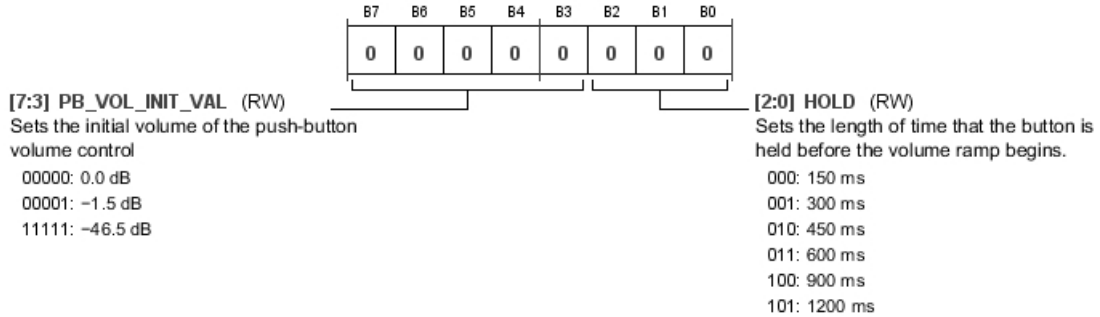


Table 91. Bit Descriptions for PB_VOL_SET

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------------|--|--|-------|--------|
| [7:3] | PB_VOL_INIT_VAL | 00000 00001 11111 | Sets the initial volume of the push-button volume control. Each increment of this register attenuates the level by 1.5 dB, from 0 dB to -46.5 dB. 0.0 dB -1.5 dB -46.5 dB | 0x00 | RW |
| [2:0] | HOLD | 000 001 010 011 100 101 | Sets the length of time that the button is held before the volume ramp begins. 150 ms 300 ms 450 ms 600 ms 900 ms 1200 ms | 0x0 | RW |

PUSH-BUTTON VOLUME CONTROL ASSIGNMENT REGISTER

Address: 0x0040, Reset: 0x87, Name: PB_VOL_CONV

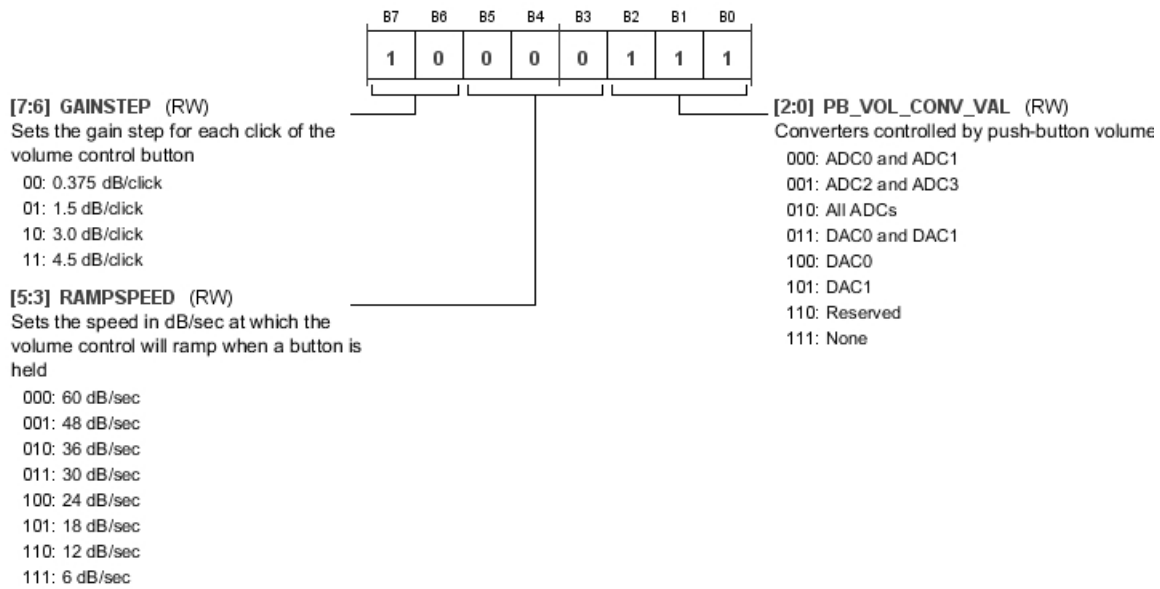


Table 92. Bit Descriptions for PB_VOL_CONV

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-----------------|--|--|-------|--------|
| [7:6] | GAINSTEP | 00 01 10 11 | Sets the gain step for each press of the volume control button. 0.375 dB/press 1.5 dB/press 3.0 dB/press 4.5 dB/press | 0x2 | RW |
| [5:3] | RAMPSPEED | 000 001 010 011 100 101 110 111 | Sets the speed in dB/sec at which the volume control ramps when a button is pressed. 60 dB/sec 48 dB/sec 36 dB/sec 30 dB/sec 24 dB/sec 18 dB/sec 12 dB/sec 6 dB/sec | 0x0 | RW |
| [2:0] | PB_VOL_CONV_VAL | 000 001 010 011 100 101 110 111 | Converters controlled by push-button volume. The push-button volume control is enabled when these bits are set to something other than the default setting (111). When set to 111, the push-button volume is disabled and the converter volumes are set by the ADCx_VOLUME and DACx_VOLUME registers. ADC0 and ADC1 ADC2 and ADC3 All ADCs DAC0 and DAC1 DAC0 DAC1 Reserved None (default) | 0x7 | RW |

DEBOUNCE MODES REGISTER

Address: 0x0041, Reset: 0x05, Name: DEBOUNCE_MODE

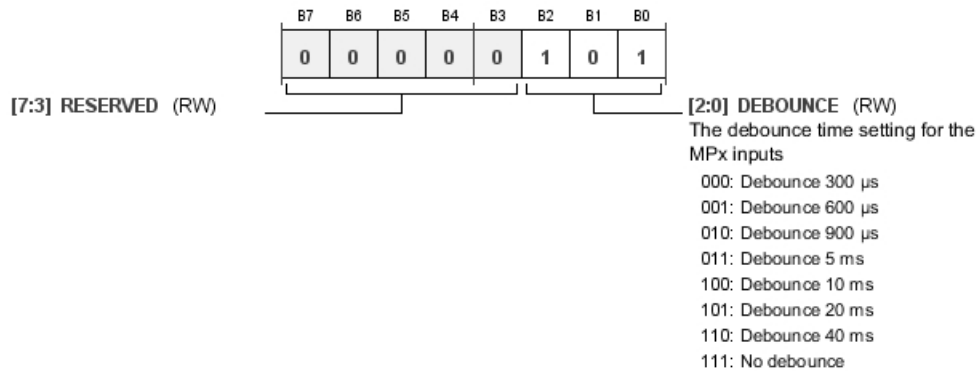


Table 93. Bit Descriptions for DEBOUNCE_MODE

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|--|---|-------|--------|
| [2:0] | DEBOUNCE | 000 001 010 011 100 101 110 111 | The debounce time setting for the MPx inputs. Debounce 300 μ s Debounce 600 μ s Debounce 900 μ s Debounce 5 ms Debounce 10 ms Debounce 20 ms Debounce 40 ms No debounce | 0x5 | RW |

HEADPHONE LINE OUTPUT SELECT REGISTER

Address: 0x0043, Reset: 0x0F, Name: OP_STAGE_CTRL

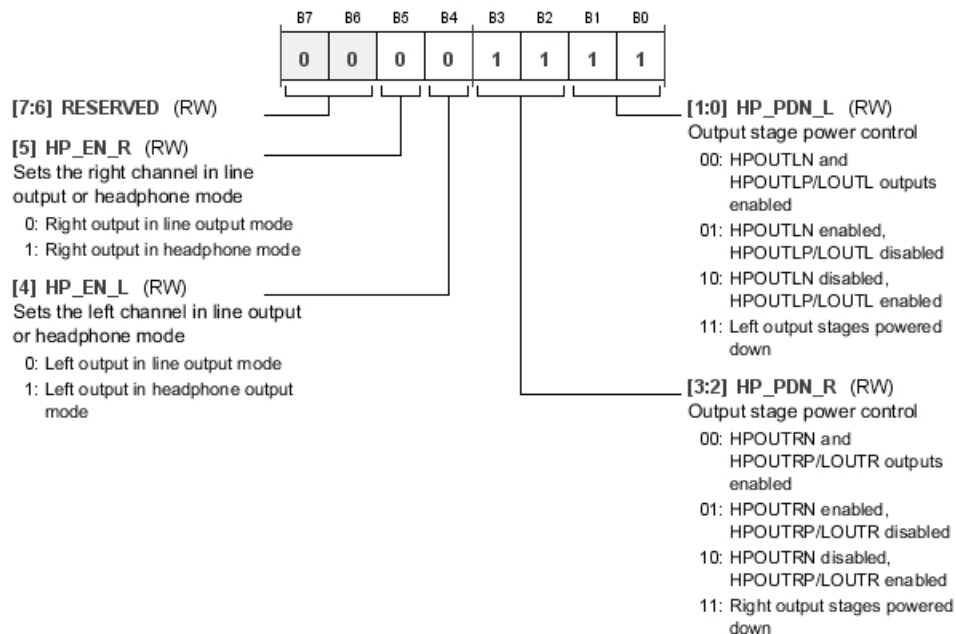


Table 94. Bit Descriptions for OP_STAGE_CTRL

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|----------|----------------------|--|-------|--------|
| 5 | HP_EN_R | 0 1 | Sets the right channel in line output or headphone mode. Right output in line output mode Right output in headphone mode | 0x0 | RW |
| 4 | HP_EN_L | 0 1 | Sets the left channel in line output or headphone mode. Left output in line output mode Left output in headphone output mode | 0x0 | RW |
| [3:2] | HP_PDN_R | 00 01 10 11 | Output stage power control. Powers down the right output stage, regardless of whether the device is in line output or headphone mode. After enabling the headphone output, wait at least 6 ms before unmuting the headphone output by setting HP_MUTE_R in the OP_STAGE_MUTES register to 00. HPOUTRN/LOUTRN and HPOUTRP/LOUTRP outputs enabled HPOUTRN/LOUTRN enabled, HPOUTRP/LOUTRP disabled HPOUTRN/LOUTRN disabled, HPOUTRP/LOUTRP enabled Right output stages powered down | 0x3 | RW |
| [1:0] | HP_PDN_L | 00 01 10 11 | Output stage power control. Powers down the left output stage, regardless of whether the device is in line output or headphone mode. After enabling the headphone output, wait at least 6 ms before unmuting the headphone output by setting HP_MUTE_L in the OP_STAGE_MUTES register to 00. HPOUTLN/LOUTLN and HPOUTLP/LOUTLP outputs enabled HPOUTLN/LOUTLN enabled, HPOUTLP/LOUTLP disabled HPOUTLN/LOUTLN disabled, HPOUTLP/LOUTLP enabled Left output stages powered down | 0x3 | RW |

DECIMATOR POWER CONTROL REGISTER

Address: 0x0044, Reset: 0x00, Name: DECIM_PWR_MODES

These bits enable clocks to the digital filters and ASRC decimator filters of the ADCs. These bits must be enabled for all channels that will be used in the design. To use the ADCs, these SINC_x_EN bits must be enabled along with the appropriate ADC_x_EN bits in the ADC_CONTROL2 and ADC_CONTROL3 registers. If the digital microphone inputs are used, the SINC_x_EN bits can be set without setting ADC_x_EN.

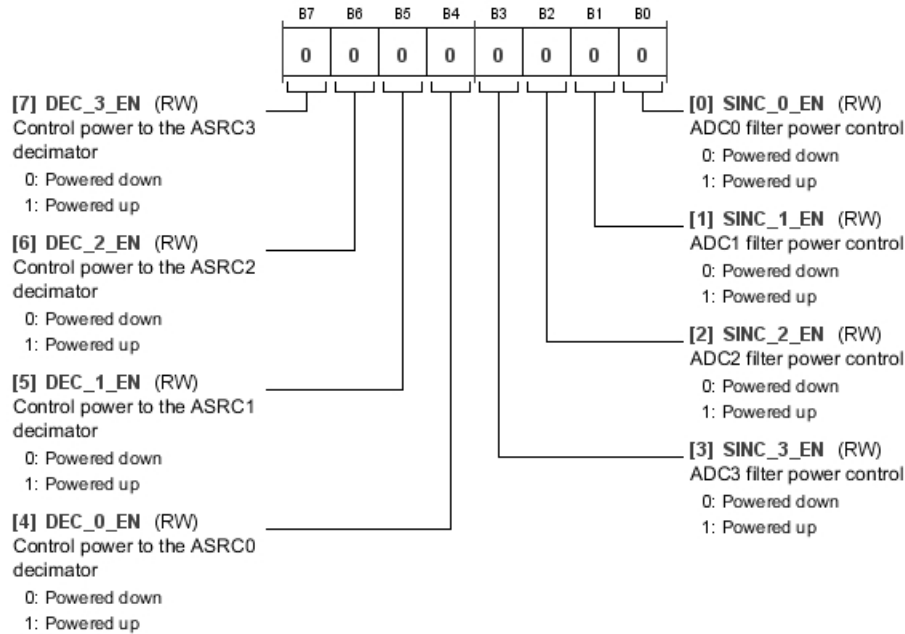


Table 95. Bit Descriptions for DECIM_PWR_MODES

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------|----------|---|-------|--------|
| 7 | DEC_3_EN | 0 1 | Control power to the ASRC3 decimator. Powered down Powered up | 0x0 | RW |
| 6 | DEC_2_EN | 0 1 | Control power to the ASRC2 decimator. Powered down Powered up | 0x0 | RW |
| 5 | DEC_1_EN | 0 1 | Control power to the ASRC1 decimator. Powered down Powered up | 0x0 | RW |
| 4 | DEC_0_EN | 0 1 | Control power to the ASRC0 decimator. Powered down Powered up | 0x0 | RW |
| 3 | SINC_3_EN | 0 1 | ADC3 filter power control. Powered down Powered up | 0x0 | RW |
| 2 | SINC_2_EN | 0 1 | ADC2 filter power control. Powered down Powered up | 0x0 | RW |
| 1 | SINC_1_EN | 0 1 | ADC1 filter power control. Powered down Powered up | 0x0 | RW |
| 0 | SINC_0_EN | 0 1 | ADC0 filter power control. Powered down Powered up | 0x0 | RW |

ASRC INTERPOLATOR AND DAC MODULATOR POWER CONTROL REGISTER

Address: 0x0045, Reset: 0x00, Name: INTERP_PWR_MODES

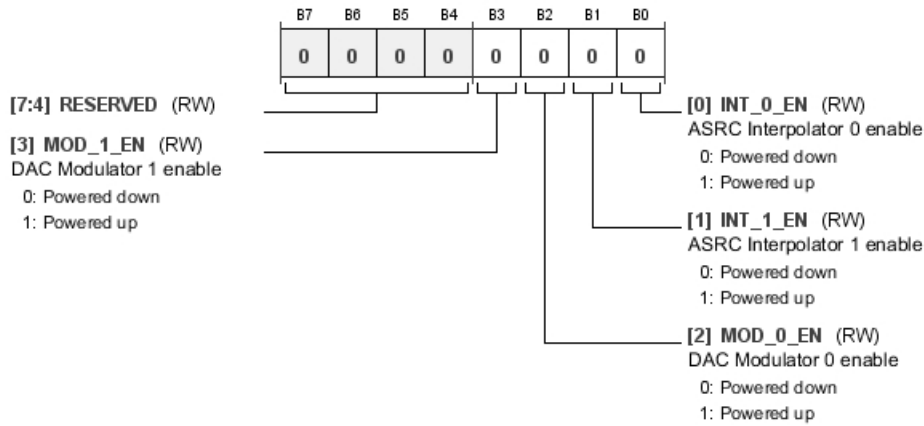


Table 96. Bit Descriptions for INTERP_PWR_MODES

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---|-------|--------|
| 3 | MOD_1_EN | 0 1 | DAC Modulator 1 enable. Powered down Powered up | 0x0 | RW |
| 2 | MOD_0_EN | 0 1 | DAC Modulator 0 enable. Powered down Powered up | 0x0 | RW |
| 1 | INT_1_EN | 0 1 | ASRC Interpolator 1 enable. Powered down Powered up | 0x0 | RW |
| 0 | INT_0_EN | 0 1 | ASRC Interpolator 0 enable. Powered down Powered up | 0x0 | RW |

ANALOG BIAS CONTROL 0 REGISTER

Address: 0x0046, Reset: 0x00, Name: BIAS_CONTROL0

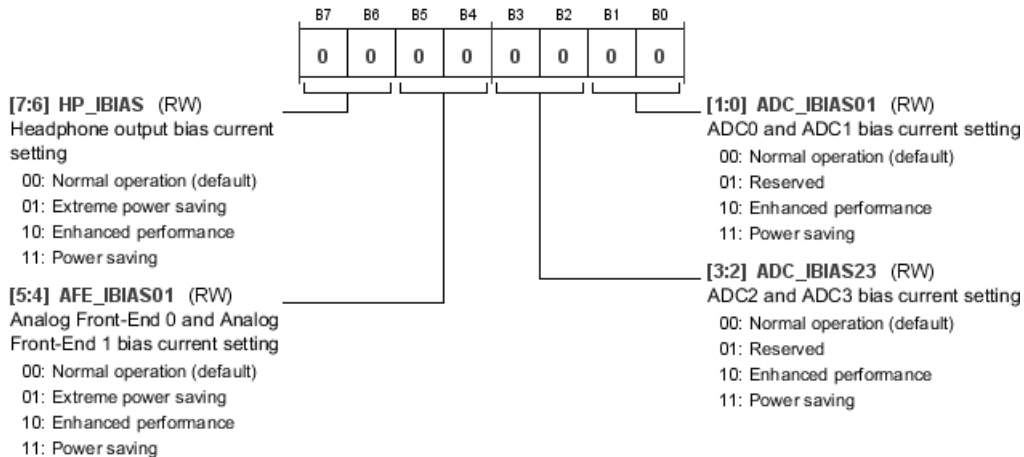


Table 97. Bit Descriptions for BIAS_CONTROL0

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------------------|--|-------|--------|
| [7:6] | HP_IBIAS | 00 01 10 11 | Headphone output bias current setting. Higher bias currents result in higher performance. Normal operation (default) Extreme power saving Enhanced performance Power saving | 0x0 | RW |
| [5:4] | AFE_IBIAS01 | 00 01 10 11 | Analog Front-End 0 and Analog Front-End 1 bias current setting. Higher bias currents result in higher performance. Normal operation (default) Extreme power saving Enhanced performance Power saving | 0x0 | RW |
| [3:2] | ADC_IBIAS23 | 00 01 10 11 | ADC2 and ADC3 bias current setting. Higher bias currents result in higher performance. Normal operation (default) Reserved Enhanced performance Power saving | 0x0 | RW |
| [1:0] | ADC_IBIAS01 | 00 01 10 11 | ADC0 and ADC1 bias current setting. Higher bias currents result in higher performance. Normal operation (default) Reserved Enhanced performance Power saving | 0x0 | RW |

ANALOG BIAS CONTROL 1 REGISTER

Address: 0x0047, Reset: 0x00, Name: BIAS_CONTROL1

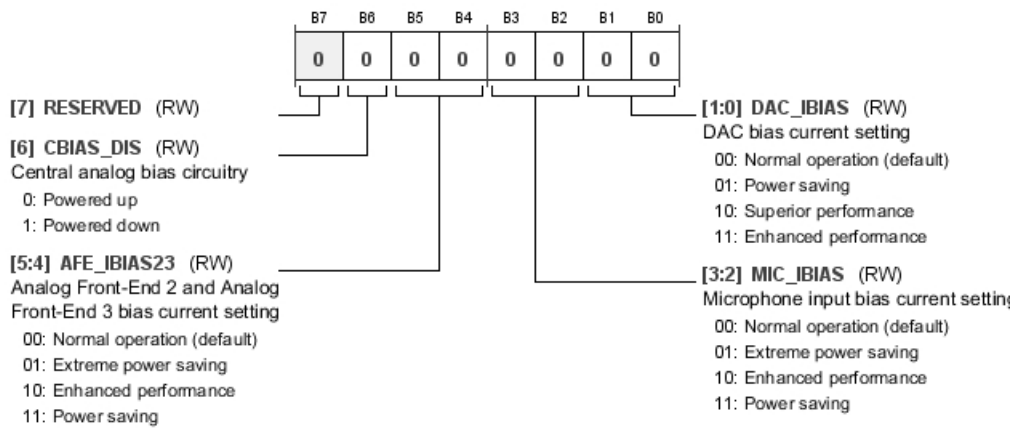


Table 98. Bit Descriptions for BIAS_CONTROL1

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-----------|----------|---|-------|--------|
| 6 | CBIAS_DIS | 0 1 | Central analog bias circuitry. Higher bias currents result in higher performance. Powered up Powered down | 0x0 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|-------|-------------|----------------------|--|-------|--------|
| [5:4] | AFE_IBIAS23 | 00 01 10 11 | Analog Front-End 2 and Analog Front-End 3 bias current setting. Higher bias currents result in higher performance. Normal operation (default) Extreme power saving Enhanced performance Power saving | 0x0 | RW |
| [3:2] | MIC_IBIAS | 00 01 10 11 | Microphone input bias current setting. Higher bias currents result in higher performance. Normal operation (default) Extreme power saving Enhanced performance Power saving | 0x0 | RW |
| [1:0] | DAC_IBIAS | 00 01 10 11 | DAC bias current setting. Higher bias currents result in higher performance. Normal operation (default) Power saving Superior performance Enhanced performance | 0x0 | RW |

DIGITAL PIN PULL-UP CONTROL 0 REGISTER

Address: 0x0048, Reset: 0x7E, Name: PAD_CONTROLO

Controls the behavior of the pad. Possible to enable pull-up.

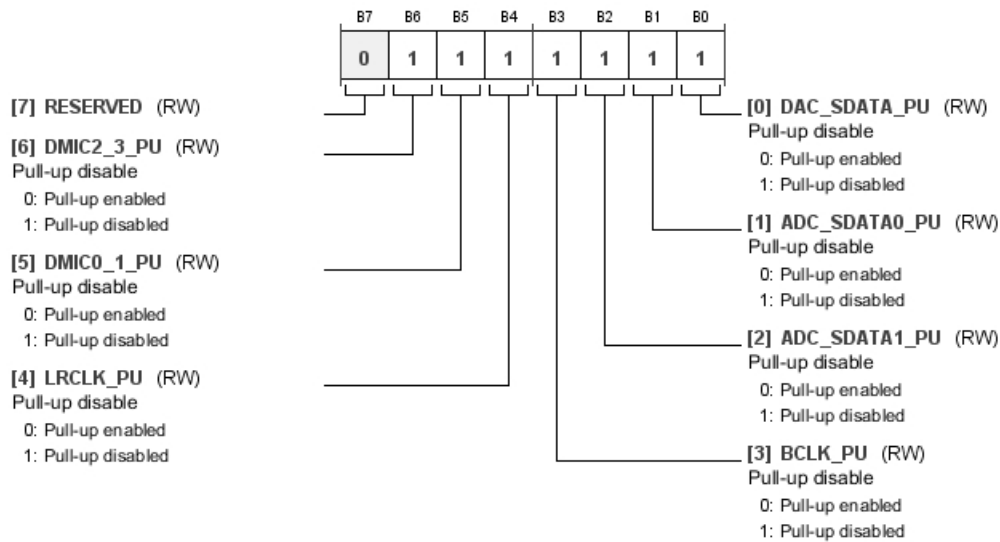


Table 99. Bit Descriptions for PAD_CONTROLO

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|------------|----------|---|-------|--------|
| 6 | DMIC2_3_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 5 | DMIC0_1_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 4 | LRCLK_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|---------------|----------|---|-------|--------|
| 3 | BCLK_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 2 | ADC_SDATA1_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 1 | ADC_SDATA0_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 0 | DAC_SDATA_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |

DIGITAL PIN PULL-UP CONTROL 1 REGISTER

Address: 0x0049, Reset: 0x1F, Name: PAD_CONTROL1

Controls the behavior of the pad. Possible to enable pull-up.

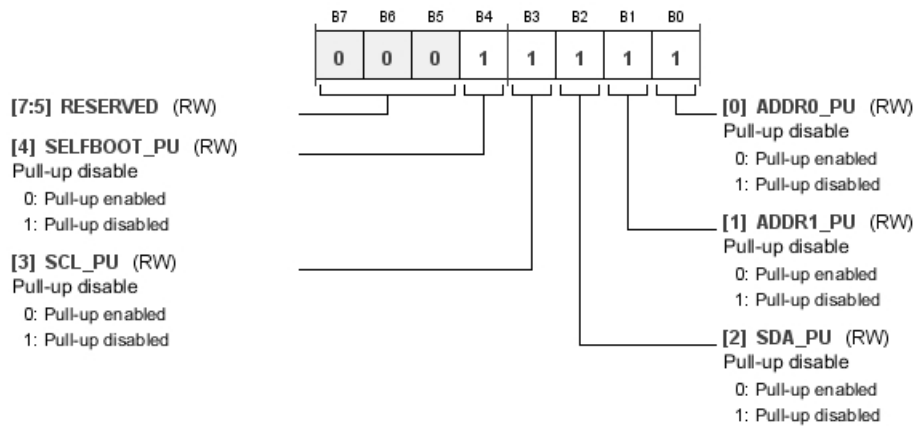


Table 100. Bit Descriptions for PAD_CONTROL1

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-------------|----------|---|-------|--------|
| 4 | SELFBOOT_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 3 | SCL_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 2 | SDA_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 1 | ADDR1_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |
| 0 | ADDR0_PU | 0 1 | Pull-up disable. Pull-up enabled Pull-up disabled | 0x1 | RW |

DIGITAL PIN PULL-DOWN CONTROL 0 REGISTER

Address: 0x004A, Reset: 0x00, Name: PAD_CONTROL2

Controls the behavior of the pad. Possible to enable pull-down.

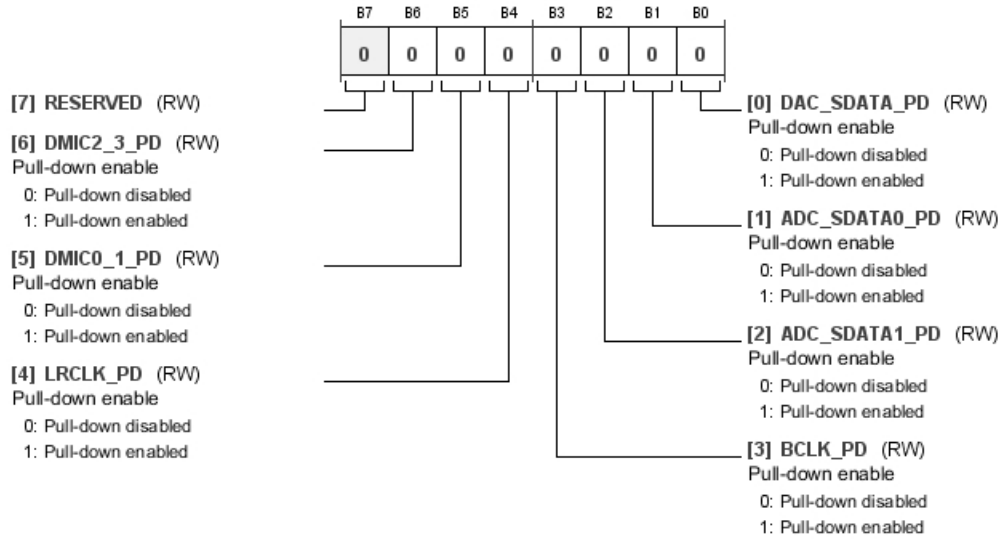


Table 101. Bit Descriptions for PAD_CONTROL2

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|---------------|----------|--|-------|--------|
| 6 | DMIC2_3_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 5 | DMIC0_1_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 4 | LRCLK_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 3 | BCLK_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 2 | ADC_SDATA1_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 1 | ADC_SDATA0_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 0 | DAC_SDATA_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |

DIGITAL PIN PULL-DOWN CONTROL 1 REGISTER

Address: 0x004B, Reset: 0x00, Name: PAD_CONTROL3

Controls the behavior of the pad. Possible to enable pull-down.

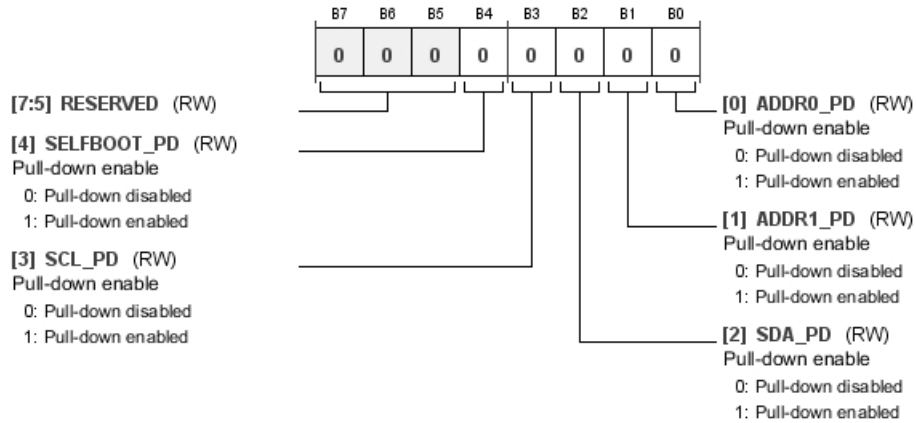


Table 102. Bit Descriptions for PAD_CONTROL3

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|-------------|----------|--|-------|--------|
| 4 | SELFBOOT_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 3 | SCL_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 2 | SDA_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 1 | ADDR1_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |
| 0 | ADDR0_PD | 0 1 | Pull-down enable. Pull-down disabled Pull-down enabled | 0x0 | RW |

DIGITAL PIN DRIVE STRENGTH CONTROL 0 REGISTER

Address: 0x004C, Reset: 0x00, Name: PAD_CONTROL4

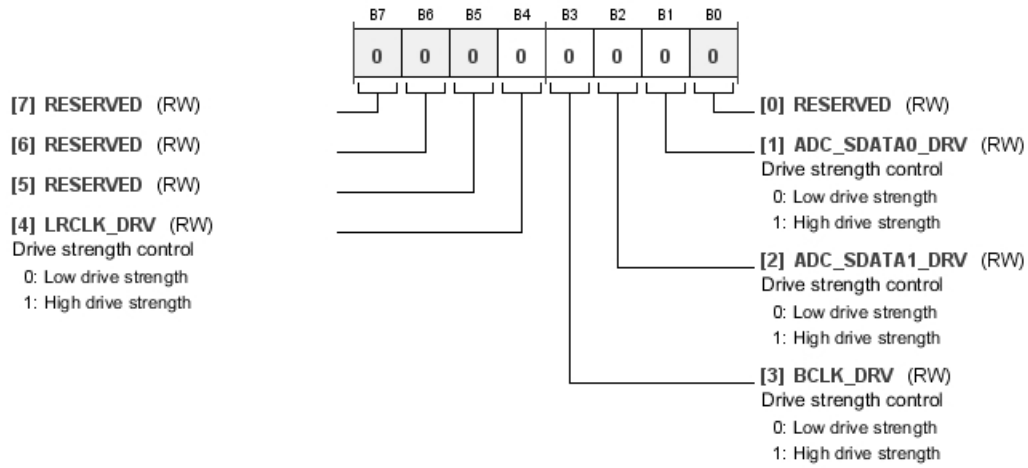


Table 103. Bit Descriptions for PAD_CONTROL4

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------------|----------|--|-------|--------|
| 4 | LRCLK_DRV | 0 1 | Drive strength control. Low drive strength High drive strength | 0x0 | RW |
| 3 | BCLK_DRV | 0 1 | Drive strength control. Low drive strength High drive strength | 0x0 | RW |
| 2 | ADC_SDATA1_DRV | 0 1 | Drive strength control. Low drive strength High drive strength | 0x0 | RW |
| 1 | ADC_SDATA0_DRV | 0 1 | Drive strength control. Low drive strength High drive strength | 0x0 | RW |

DIGITAL PIN DRIVE STRENGTH CONTROL 1 REGISTER

Address: 0x004D, Reset: 0x00, Name: PAD_CONTROL5

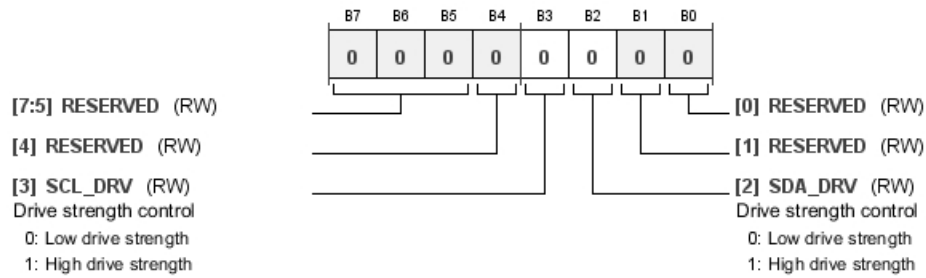
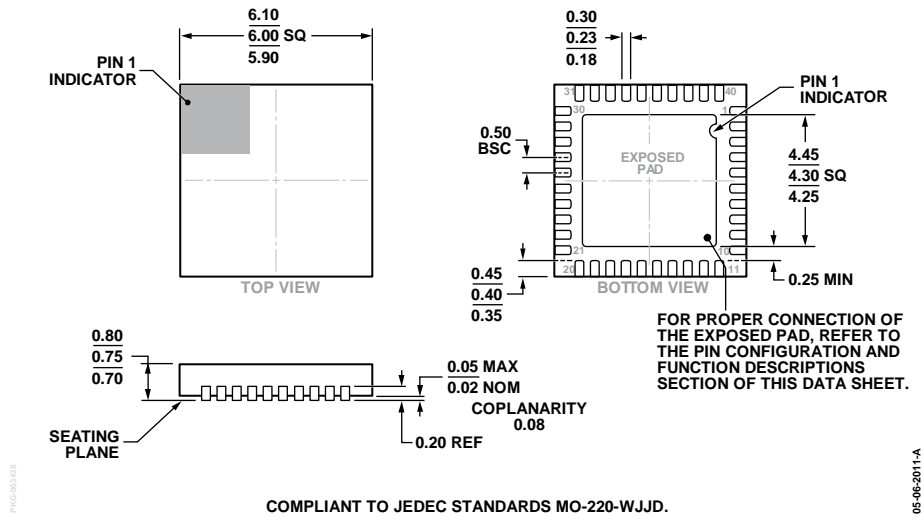


Table 104. Bit Descriptions for PAD_CONTROL5

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|---------------------|-------|--------|
| 3 | SCL_DRV | 0 | Low drive strength | 0x0 | RW |
| | | 1 | High drive strength | | |
| 2 | SDA_DRV | 0 | Low drive strength | 0x0 | RW |
| | | 1 | High drive strength | | |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD.
 Figure 105. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 6 mm × 6 mm Body, Very Very Thin Quad
 (CP-40-10)
 Dimension shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADAU1772BCPZ | -40°C to +85°C | 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-40-10 |
| ADAU1772BCPZ-R7 | -40°C to +85°C | 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 7" Tape and Reel | CP-40-10 |
| ADAU1772BCPZ-RL | -40°C to +85°C | 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ], 13" Tape and Reel | CP-40-10 |
| EVAL-ADAU1772Z | | Evaluation Board | |

¹ Z = RoHS Compliant Part.

NOTES