Rail-to-Rail, Very Fast, 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparators

ADCMP600/ADCMP601/ADCMP602

FEATURES

- Fully specified rail to rail at V_{CC} = 2.5 V to 5.5 V
- Input common-mode voltage from −0.2 V to V_{CC} + 0.2 V
- Low glitch CMOS-/TTL-compatible output stage
- 3.5 ns propagation delay
- 10 mW at 3.3 V
- Shutdown pin
- Single-pin control for programmable hysteresis and latch
- Power supply rejection > 50 dB
- Improved replacement for MAX999
- −40°C to +125°C operation

APPLICATIONS

- High speed instrumentation
- Clock and data signal restoration
- Logic level shifting or translation
- Pulse spectroscopy
- High speed line receivers
- Threshold detection
- Peak and zero-crossing detectors
- High speed trigger circuitry
- Pulse-width modulators
- Current/voltage-controlled oscillators
- Automatic test equipment (ATE)

FUNCTIONAL BLOCK DIAGRAM

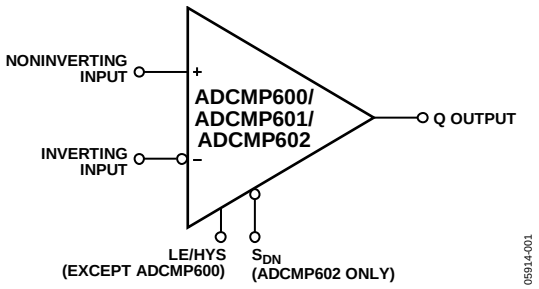

Figure 1.

GENERAL DESCRIPTION

The ADCMP600, ADCMP601, and ADCMP602 are very fast comparators fabricated on XFCB2, an Analog Devices, Inc. proprietary process. These comparators are exceptionally versatile and easy to use. Features include an input range from GND − 0.5 V to V_{CC} + 0.2 V, low noise, TTL-/CMOS-compatible output drivers, and latch inputs with adjustable hysteresis and/or shutdown inputs.

The device offers 5 ns propagation delay with 10 mV overdrive on 3 mA typical supply current.

A flexible power supply scheme allows the devices to operate with a single +2.5 V positive supply and a −0.5 V to +2.8 V input signal range up to a +5.5 V positive supply with a −0.5 V to +5.8 V input signal range. Split input/output supplies with no sequencing restrictions on the ADCMP602 support a wide input signal range while still allowing independent output swing control and power savings.

The TTL-/CMOS-compatible output stage is designed to drive up to 5 pF with full timing specs and to degrade in a graceful and linear fashion as additional capacitance is added. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. Latch and programmable hysteresis features are also provided with a unique single-pin control option.

The ADCMP600 is available in 5-lead SC70 and SOT-23 packages, the ADCMP601 is available in a 6-lead SC70 package, and the ADCMP602 is available in an 8-lead MSOP package.

Rev. A

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REVISION HISTORY

1/11—Rev. 0 to Rev. A

Changed V_{EE} Pin to GND ... Throughout
Changes to Common-Mode Dispersion Conditions ... 4
Changes to Figure 15 and Figure 16 ... 9
Changes to Comparator Hysteresis Section ... 12
Updated Outline Dimensions ... 14
Changes to Ordering Guide ... 15

10/06—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CCI} = V_{CCO} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CC} = 2.5 V to 5.5 V	−0.5		V_{CC} + 0.2	V
Common-Mode Range		V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2	V
Differential Voltage		V_{CC} = 2.5 V to 5.5 V			V_{CC} + 0.8	V
Offset Voltage	V_{OS}		−5.0	±2	+5.0	mV
Bias Current	I_P, I_N		−5.0	±2	+5.0	µA
Offset Current			−2.0		+2.0	µA
Capacitance	C_P, C_N			1		pF
Resistance, Differential Mode		−0.1 V to V_{CC}	200	700		kΩ
Resistance, Common Mode		−0.5 V to V_{CC} + 0.5 V	100	350		kΩ
Active Gain	A_V			85		dB
Common-Mode Rejection Ratio	CMRR	V_{CCI} = 2.5 V, V_{CCO} = 2.5 V, V_{CM} = −0.2 V to +2.7 V	50			dB
		V_{CCI} = 2.5 V, V_{CCO} = 5.5 V	50			dB
Hysteresis (ADCMP600)				2		mV
Hysteresis (ADCMP601/ADCMP602)		R_{HYS} = ∞		0.1		mV
LATCH ENABLE PIN CHARACTERISTICS (ADCMP601/ADCMP602 Only)						
V_{IH}		Hysteresis is shut off	2.0		V_{CC}	V
V_{IL}		Latch mode guaranteed	−0.2	+0.4	+0.8	V
I_{IH}		V_{IH} = V_{CC}	−6		+6	µA
I_{OL}		V_{IL} = 0.4 V	−0.1		+0.1	mA
HYSTERESIS MODE AND TIMING (ADCMP601/ADCMP602 Only)						
Hysteresis Mode Bias Voltage		Current −1 µA	1.145	1.25	1.35	V
Resistor Value		Hysteresis = 120 mV	65	80	120	kΩ
Hysteresis Current		Hysteresis = 120 mV	−18	−12	−7	µA
Latch Setup Time	t_S	V_{OD} = 50 mV		−2		ns
Latch Hold Time	t_H	V_{OD} = 50 mV		2.6		ns
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 50 mV		27		ns
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 50 mV		21		ns
SHUTDOWN PIN CHARACTERISTICS (ADCMP602 Only)						
V_{IH}		Comparator is operating	2.0		V_{CCO}	V
V_{IL}		Shutdown guaranteed	−0.2	+0.4	+0.6	V
I_{IH}		V_{IH} = V_{CC}	−6		6	µA
I_{OL}		V_{IL} = 0 V		−100		µA
Sleep Time	t_{SD}	I_{CCO} < 500 µA		20		ns
Wake-Up Time	t_H	V_{OD} = 100 mV, output valid		50		ns
DC OUTPUT CHARACTERISTICS		V_{CCO} = 2.5 V to 5.5 V				
Output Voltage High Level	V_{OH}	I_{OH} = 8 mA, V_{CCO} = 2.5 V	V_{CC} − 0.4			V
Output Voltage Low Level	V_{OL}	I_{OL} = 8 mA, V_{CCO} = 2.5 V			0.4	V
Output Voltage High Level at −40°C	V_{OH}	I_{OH} = 6 mA, V_{CCO} = 2.5 V	V_{CC} − 0.4			V
Output Voltage Low Level at− 40°C	V_{OL}	I_{OL} = 6 mA, V_{CCO} = 2.5 V			0.4	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AC PERFORMANCE[1]						
Rise Time /Fall Time	t_R t_F	10% to 90%, V_{CCO} = 2.5 V		2.2		ns
		10% to 90%, V_{CCO} = 5.5 V		4		ns
Propagation Delay	t_{PD}	V_{OD} = 50 mV, V_{CCO} = 2.5 V		3.5		ns
		V_{OD} = 50 mV, V_{CCO} = 5.5 V		4.3		ns
		V_{OD} = 10 mV, V_{CCO} = 2.5 V		5		ns
Propagation Delay Skew—Rising to Falling Transition		V_{CCO} = 2.5 V to 5.5 V V_{OD} = 50 mV		500		ps
Overdrive Dispersion		10 mV < V_{OD} < 125 mV		1.2		ns
Common-Mode Dispersion		−0.2 V < V_{CM} < V_{CCI} + 0.2 V V_{OD} = 50 mV		200		ps
Minimum Pulse Width	PW_{MIN}	V_{CCI} = V_{CCO} = 2.5 V PW_{OUT} = 90% of PW_{IN}		3		ns
		V_{CCI} = V_{CCO} = 5.5 V PW_{OUT} = 90% of PW_{IN}		4.5		ns
POWER SUPPLY						
Input Supply Voltage Range	V_{CCI}		2.5		5.5	V
Output Supply Voltage Range	V_{CCO}		2.5		5.5	V
Positive Supply Differential (ADCMP602 Only)	$V_{CCI} - V_{CCO}$	Operating	−3.0		+3.0	V
	$V_{CCI} - V_{CCO}$	Nonoperating	−5.5		+5.5	V
Positive Supply Current (ADCMP600/ADCMP601)	I_{VCC}	V_{CC} = 2.5 V		3	3.5	mA
		V_{CC} = 5.5 V		3.5	4.0	
Input Section Supply Current (ADCMP602 Only)	I_{VCCI}	V_{CCI} = 2.5 V		0.9	1.4	mA
		V_{CCI} = 5.5 V		1.2	2.0	mA
Output Section Supply Current (ADCMP602 Only)	I_{VCCO}	V_{CCO} = 2.5 V		1.45	3.0	mA
		V_{CCO} = 5.5 V		2.1	3.5	mA
Power Dissipation	P_D	V_{CC} = 2.5 V		7	9	mW
	P_D	V_{CC} = 5.5 V		20	23	mW
Power Supply Rejection Ratio	PSRR	V_{CCI} = 2.5 V to 5 V	−50			dB
Shutdown Mode I_{CCI} (ADCMP602 Only)		V_{CC} = 2.5 V		240	400	µA
Shutdown Mode I_{CCO} (ADCMP602 Only)		V_{CC} =2.5 V			30	µA

[1] V_{IN} = 100 mV square input at 50 MHz, V_{CM} = 0 V, CL = 5 pF, V_{CCI} = V_{CCO} =2.5 V, unless otherwise noted.

TIMING INFORMATION

Figure 2 illustrates the ADCMP600/ADCMP601/ADCMP602 latch timing relationships. Table 2 provides definitions of the terms shown in Figure 2.

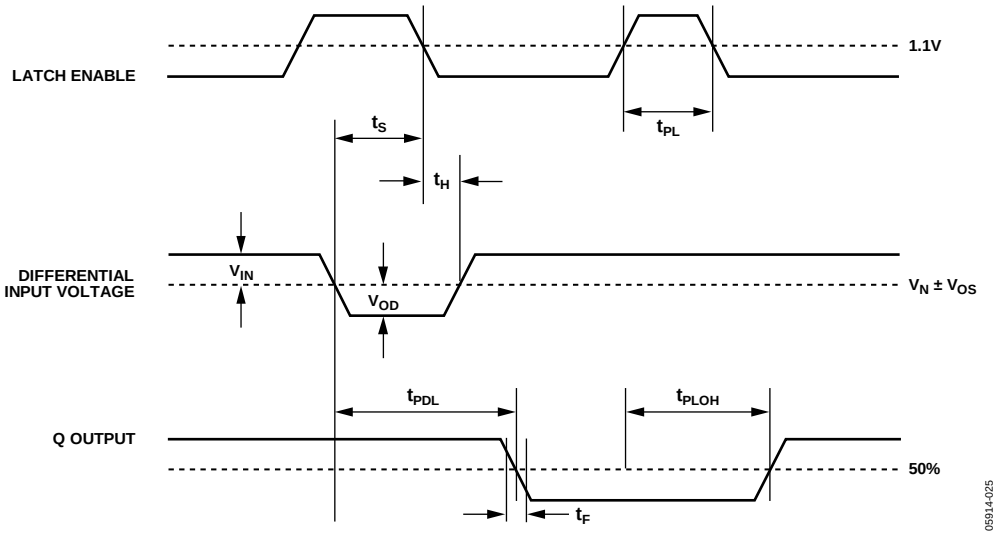


Figure 2. System Timing Diagram

Table 2. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_A and V_B.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltages	
Input Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Output Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
Positive Supply Differential ($V_{CCI} - V_{CCO}$)	−6.0 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CCI} + 0.5 V
Differential Input Voltage	±(V_{CCI} + 0.5 V)
Maximum Input/Output Current	±50 mA
Shutdown Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Latch/Hysteresis Control Pin	
Applied Voltage (HYS to GND)	−0.5 V to V_{CCO} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Temperature	
Operating Temperature, Ambient	−40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	Unit
ADCMP600 SC70 5-Lead	426	°C/W
ADCMP600 SOT-23 5-Lead	302	°C/W
ADCMP601 SC70 6-Lead	426	°C/W
ADCMP602 MSOP 5-Lead	130	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

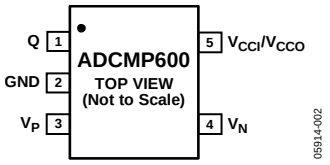


Figure 3. ADCMP600 Pin Configuration

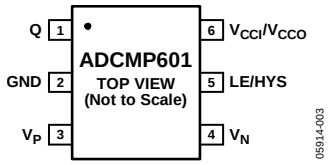


Figure 4. ADCMP601 Pin Configuration

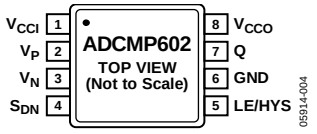


Figure 5. ADCMP602 Pin Configuration

Table 5. ADCMP600 (SOT-23-5 and SC70-5) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N.
2	GND	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	V_{CCI}/V_{CCO}	Input Section Supply/Output Section Supply. Shared pin.

Table 6. ADCMP601 (SC70-6) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, if the comparator is in compare mode.
2	GND	Negative Supply Voltage.
3	V_P	Noninverting Analog Input.
4	V_N	Inverting Analog Input.
5	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis adjustment; drive low to latch.
6	V_{CCI}/V_{CCO}	Input Section Supply/Output Section Supply. Shared pin.

Table 7. ADCMP602 (MSOP-8) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CCI}	Input Section Supply.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	S_{DN}	Shutdown. Drive this pin low to shut down the device.
5	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis adjustment; drive low to latch.
6	GND	Negative Supply Voltage.
7	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, if the comparator is in compare mode.
8	V_{CCO}	Output Section Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 2.5$ V, $T_A = 25°C$, unless otherwise noted.

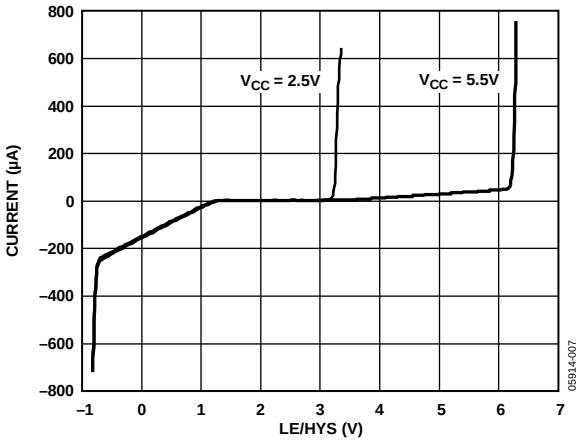


Figure 6. LE/HYS Pin I/V Characteristics

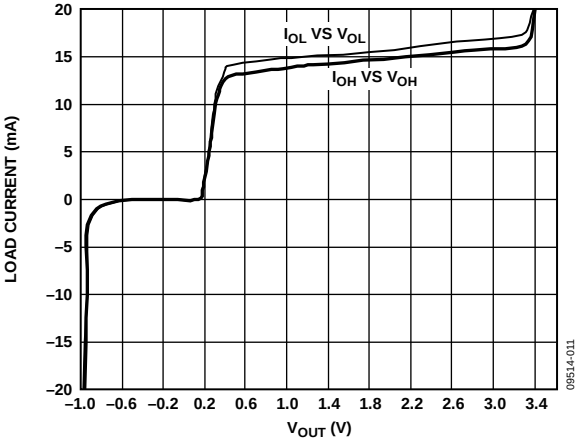


Figure 9. V_{OH}/V_{OL} vs. Current Load

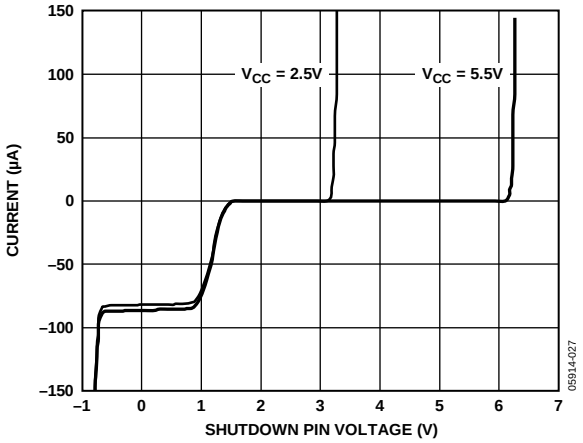


Figure 7. S_{DN} Pin I/V Characteristics

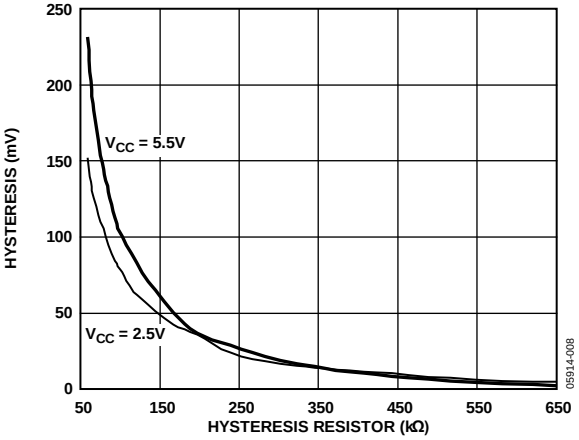


Figure 10. Hysteresis vs. R_{HYS} Control Resistor

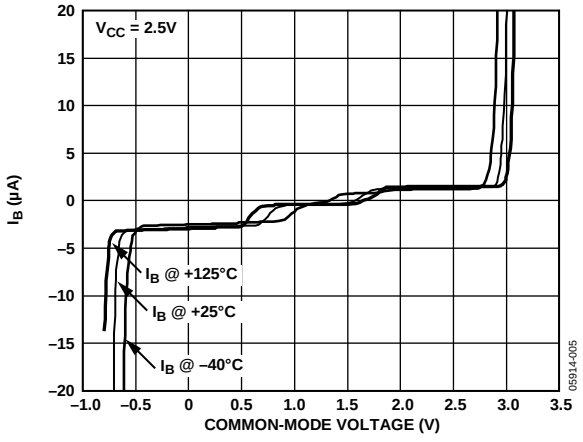


Figure 8. Input Bias Current vs. Input Common Mode

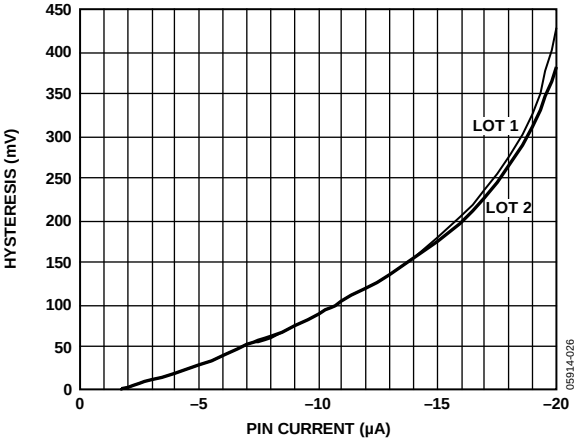


Figure 11. Hysteresis vs. Pin Current

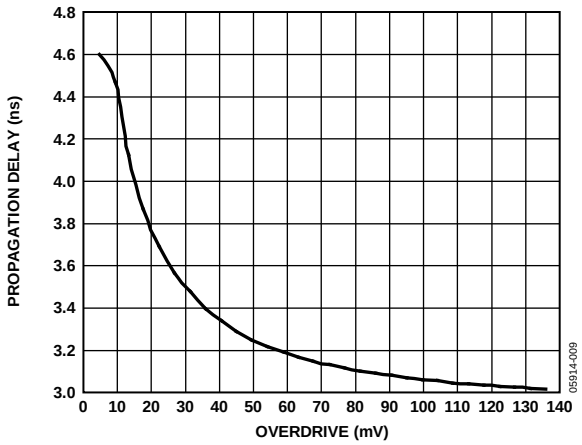


Figure 12. Propagation Delay vs. Input Overdrive at V_{CC} = 2.5 V

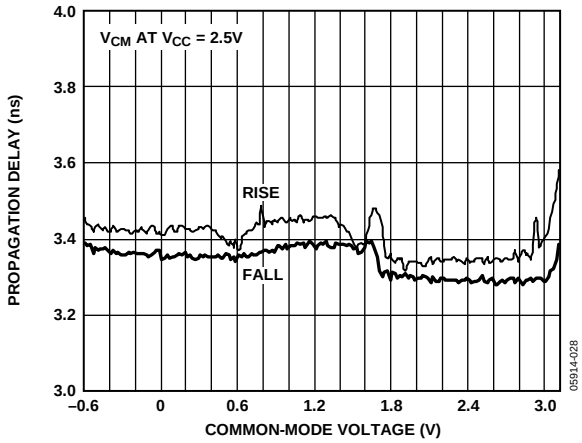


Figure 13. Propagation Delay vs. Input Common-Mode Voltage at V_{CC} = 2.5 V

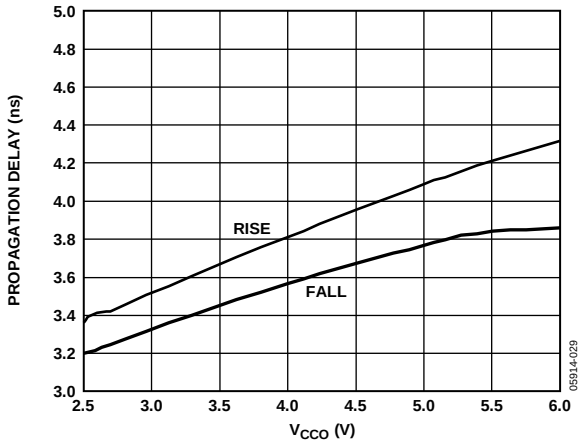


Figure 14. Propagation Delay vs. V_{CCO}

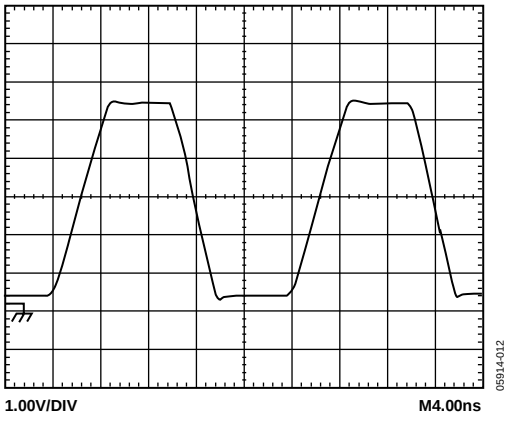


Figure 15. 50 MHz Output Waveform V_{CC} = 5.5 V

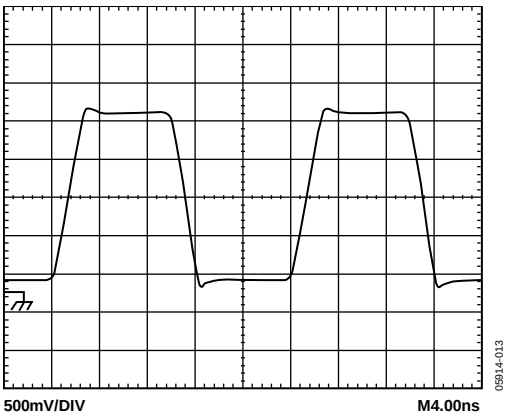


Figure16. 50 MHz Output Waveforms @ 2.5 V

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP600/ADCMP601/ADCMP602 comparators are very high speed devices. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Multiple high quality 0.01 µF bypass capacitors should be placed as close as possible to each of the V_{CCI} and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. At least one of these should be placed to provide a physically short return path for output currents flowing back from ground to the V_{CC} pin. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

If the package allows and the input and output supplies have been connected separately such that $V_{CCI} \neq V_{CCO}$, care should be taken to bypass each of these supplies separately to the GND plane. A bypass capacitor should never be connected between them. It is recommended that the GND plane separate the V_{CCI} and V_{CCO} planes when the circuit board layout is designed to minimize coupling between the two supplies and to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation such that $V_{CCI} = V_{CCO}$, coupling between the two supplies is unavoidable; however, careful board placement can help keep output return currents away from the inputs.

TTL-/CMOS-COMPATIBLE OUTPUT STAGE

Specified propagation delay performance can be achieved only by keeping the capacitive load at or below the specified minimums. The outputs of the devices are designed to directly drive one Schottky TTL or three low power Schottky TTL loads or the equivalent. For large fan outputs, buses, or transmission lines, use an appropriate buffer to maintain the excellent speed and stability of the comparator.

With the rated 5 pF load capacitance applied, more than half of the total device propagation delay is output stage slew time, even at 2.5 V V_{CC}. Because of this, the total prop delay decreases as V_{CCO} decreases, and instability in the power supply may appear as excess delay dispersion.

This delay is measured to the 50% point for the supply in use; therefore, the fastest times are observed with the V_{CC} supply at 2.5 V, and larger values are observed when driving loads that switch at other levels.

When duty cycle accuracy is critical, the logic being driven should switch at 50% of V_{CC} and load capacitance should be minimized. When in doubt, it is best to power V_{CCO} or the entire device from the logic supply and rely on the input PSRR and CMRR to reject noise.

Overdrive and input slew rate dispersions are not significantly affected by output loading and V_{CC} variations.

The TTL-/CMOS-compatible output stage is shown in the simplified schematic diagram (Figure 17). Because of its inherent symmetry and generally good behavior, this output stage is readily adaptable for driving various filters and other unusual loads.

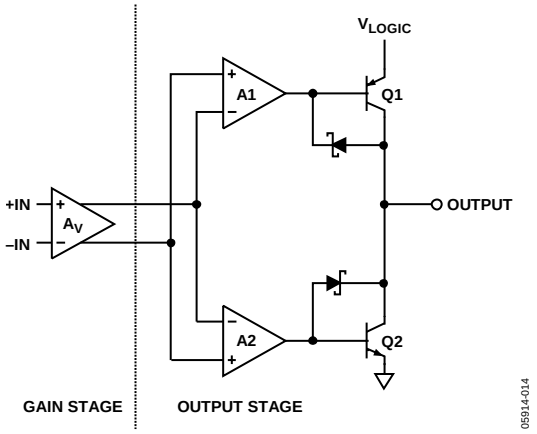


Figure 17. Simplified Schematic Diagram of TTL-/CMOS-Compatible Output Stage

USING/DISABLING THE LATCH FEATURE

The latch input is designed for maximum versatility. It can safely be left floating for fixed hysteresis or be tied to V_{CC} to remove the hysteresis, or it can be driven low by any standard TTL/CMOS device as a high speed latch.

In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately 7000 Ω. This allows the comparator hysteresis to be easily and accurately controlled by either a resistor or an inexpensive CMOS DAC.

Hysteresis control and latch mode can be used together if an open drain, an open collector, or a three-state driver is connected parallel to the hysteresis control resistor or current source.

Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V regardless of V_{CC}.

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Large discontinuities along input and output transmission lines can also limit the specified pulse-width dispersion performance. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals; higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP600/ADCMP601/ADCMP602 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (that is, how far or how fast the input signal exceeds the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 18 and Figure 19).

The device dispersion is typically < 2 ns as the overdrive varies from 10 mV to 125 mV. This specification applies to both positive and negative signals because the device has very closely matched delays both positive-going and negative-going inputs.

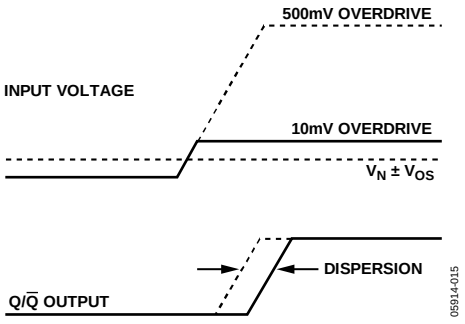


Figure 18. Propagation Delay—Overdrive Dispersion

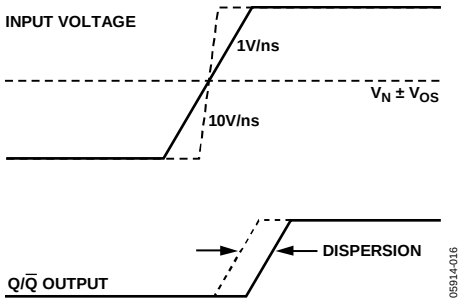


Figure 19. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. Figure 20 shows the transfer function for a comparator with hysteresis. As the input voltage approaches the threshold (0.0 V, in this example) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_H/2$, and the new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the new threshold, $-V_H/2$, is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0.0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

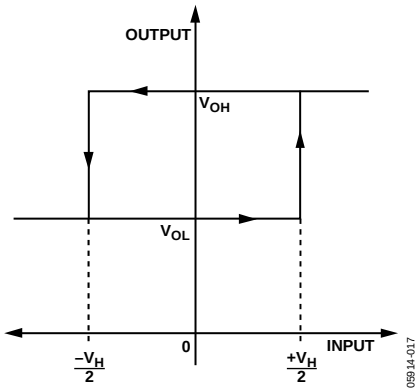


Figure 20. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and induce oscillation in some cases.

These ADCMP600 features a fixed hysteresis of approximately 2 mV. The ADCMP601 and ADCMP602 comparators offer a programmable Hysteresis feature that can significantly improve accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND, varies the amount of hysteresis in a predictable, stable manner.

Leaving the LE/HYS pin disconnected results in a fixed hysteresis of 2 mV; driving this pin high removes hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 21 illustrates the amount of hysteresis applied as a function of the external resistor value, and Figure 11 illustrates hysteresis as a function of the current.

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of 7 kΩ. The bias voltage changes ± 20% throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the HYS pin because it impairs the latch function and often degrades the jitter performance of the device. As described in the Using/Disabling the Latch Feature section, hysteresis control need not compromise the latch function.

CROSSOVER BIAS POINT

In both op amps and comparators, rail-to-rail inputs of this type have a dual front-end design. Certain devices are active near the V_{CC} rail and others are active near the GND rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CC}/2$, the direction of the bias current reverses and the measured offset voltages and currents change.

The ADCMP600/ADCMP601/ADCMP602 comparators slightly elaborate on this scheme. Crossover points can be found at approximately 0.8 V and 1.6 V.

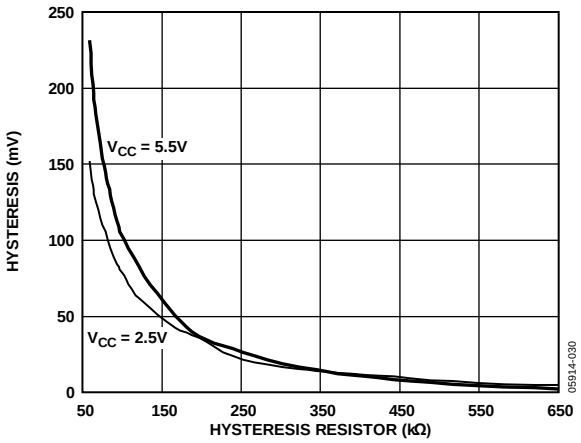


Figure 21. Hysteresis vs. R_{HYS} Control Resistor

MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PC Board design practice, as discussed in the Optimizing Performance section, these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chattering seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation is observed. This oscillation is due to the high gain bandwidth of the comparator in combination with feedback parasitics in the package and PC board. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

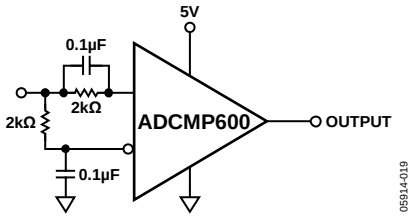


Figure 22. Self-Biased, 50% Slicer

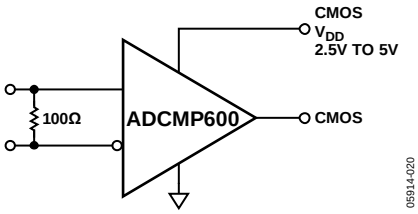


Figure 23. LVDS-to-CMOS Receiver

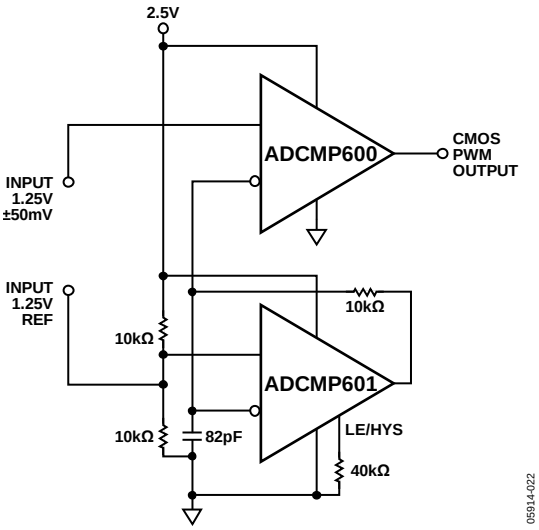


Figure 25. Oscillator and Pulse-Width Modulator

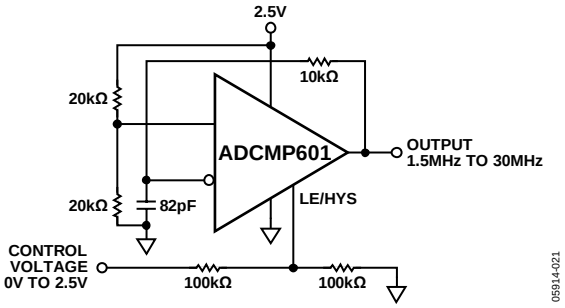


Figure 24. Voltage-Controlled Oscillator

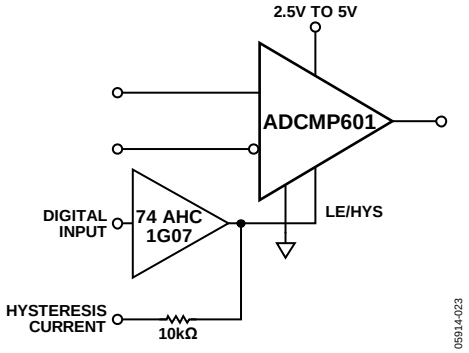
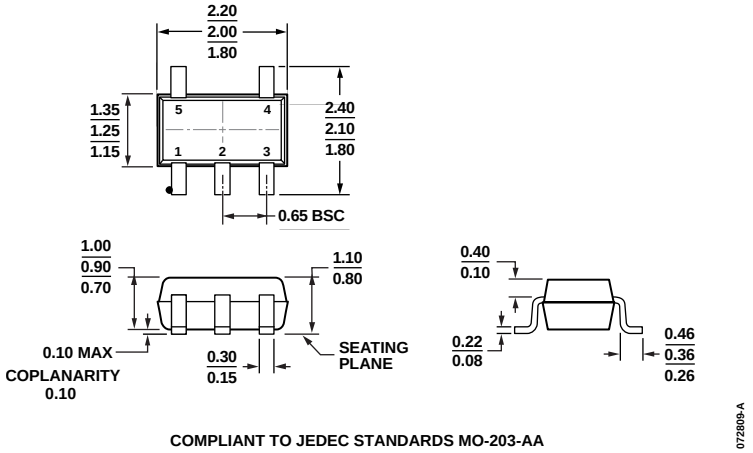


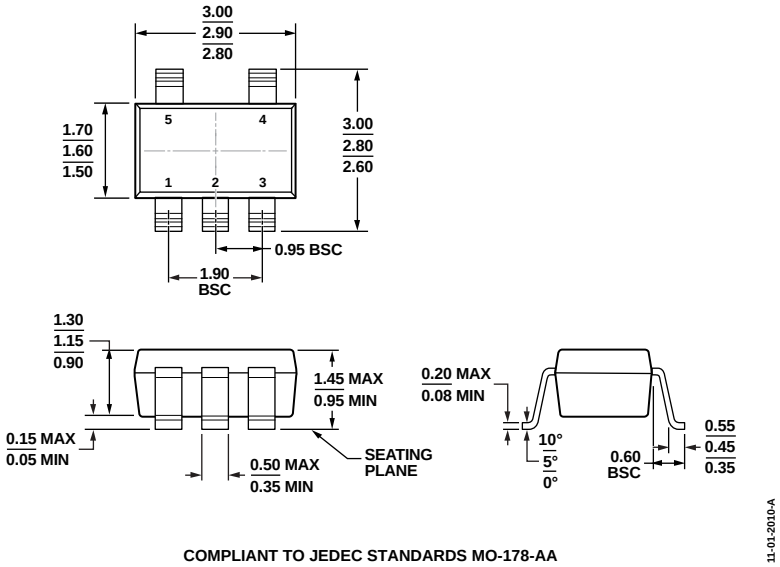
Figure 26. Hysteresis Adjustment with Latch

OUTLINE DIMENSIONS



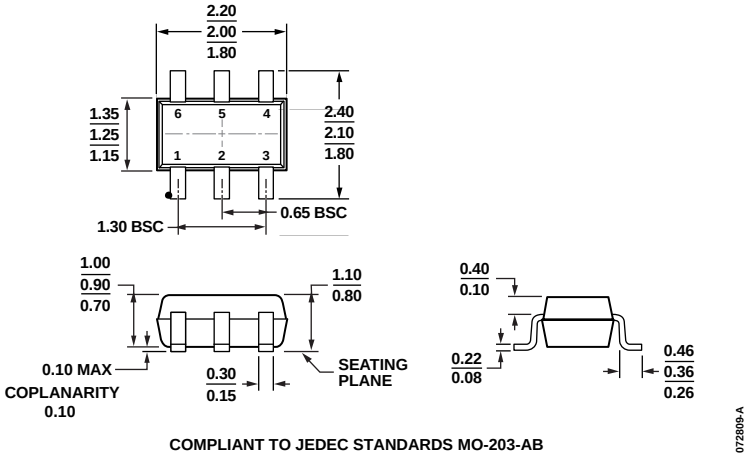
COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 27. 5-Lead Thin Shrink Small Outline Transistor Package (SC70)
(KS-5)
Dimensions shown in millimeters



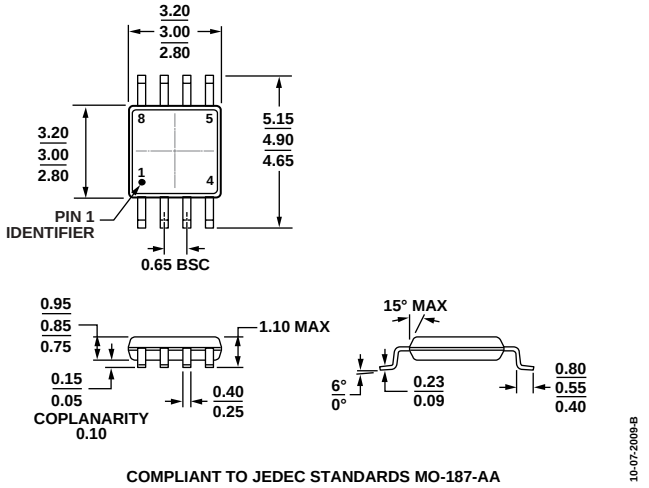
COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 28. 5-Lead Small Outline Transistor Package (SOT-23)
(RJ-5)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 29. 6-Lead Thin Shrink Small Outline Transistor Package (SC70)
(KS-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 30. 8-Lead Mini Small Outline Package (MSOP)
(RM-8)
Dimensions shown in millimeters