Rail-to-Rail, Fast, Low Power 2.5 V to 5.5 V, Single-Supply TTL/CMOS Comparator

Data Sheet **ADCMP609**

FEATURES

Fully specified rail-to-rail at V_{CC} = 2.5 V to 5.5 V
Input common-mode voltage from −0.2 V to V_{CC} + 0.2 V
Low glitch TTL-/CMOS-compatible output stage
40 ns propagation delay
Low power 1 mW at 2.5 V
Shutdown pin
Programmable hysteresis
Power supply rejection > 60 dB
−40°C to +125°C operation

APPLICATIONS

High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current/voltage controlled oscillators

FUNCTIONAL BLOCK DIAGRAM

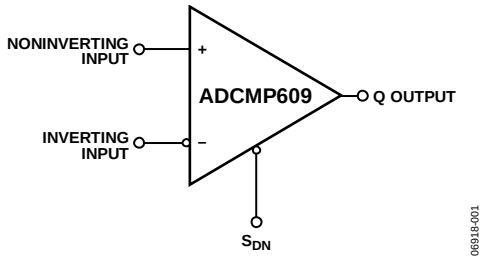

Figure 1.

GENERAL DESCRIPTION

The ADCMP609 is a fast comparator fabricated on XFCB2, an Analog Devices, Inc., proprietary process. These comparators are exceptionally versatile and easy to use. Features include an input range from V_{EE} − 0.2 V to V_{CC} + 0.2 V, low noise, TTL-/CMOS-compatible output drivers, and adjustable hysteresis and/or shutdown inputs.

The device offers 40 ns propagation delay driving a 15 pF load with 10 mV overdrive on 500 µA typical supply current.

A flexible power supply scheme allows the devices to operate with a single +2.5 V positive supply and a −0.2 V to +3.0 V input signal range up to a +5.5 V positive supply with a −0.2 V to +5.7 V input signal range.

The TTL-/CMOS-compatible output stage is designed to drive up to 15 pF with full rated timing specifications and to degrade in a graceful and linear fashion as additional capacitance is added. The input stage of the comparator offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. A programmable hysteresis feature is also provided.

The ADCMP609, available in an 8-lead MSOP package, features a shutdown pin and hysteresis control.

Rev. C **Document Feedback**

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8/08—Rev. 0 to Rev. A

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7/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5 V, T_A = −40°C to +125°C; typical value is T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Voltage Range	V_P, V_N	V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2 V	V
Common-Mode Range		V_{CC} = 2.5 V to 5.5 V	−0.2		V_{CC} + 0.2 V	V
Differential Voltage		V_{CC} = 2.5 V to 5.5 V			V_{CC}	V
Offset Voltage	V_{OS}		−5.0	±3	+5.0	mV
Bias Current	I_P, I_N		−0.4		+0.4	µA
Offset Current			−1.0		+1.0	µA
Capacitance	C_P, C_N			1		pF
Resistance, Differential Mode		−0.5 V to V_{CC} + 0.5 V	200		7000	kΩ
Resistance, Common Mode		−0.5 V to V_{CC} + 0.5 V	100		4000	kΩ
Active Gain	A_V			80		dB
Common-Mode Rejection Ratio	CMRR	V_{CC} = 2.5 V	50			dB
		V_{CM} = −0.2 V to +2.7 V				
		V_{CC} = 5.5 V	50			dB
Hysteresis		R_{HYS} = ∞		0.1		mV
HYSTERESIS MODE AND TIMING						
Hysteresis Mode Bias Voltage		Current − 1 µA	1.145	1.25	1.35	V
Minimum Resistor Value		Hysteresis = 120 mV	30		120	kΩ
SHUTDOWN PIN CHARACTERISTICS[1]						
V_{IH}		Comparator is operating	2.0		V_{CC}	V
V_{IL}		Shutdown guaranteed	−0.2	+0.4	+0.4	V
I_{IH}		V_{IH} = V_{CC}	−6		+6	µA
Sleep Time	t_{SD}	I_{CC} < 100 µA		300		ns
Wake-Up Time	t_H	V_{PP} = 10 mV, output valid		150		ns
DC OUTPUT CHARACTERISTICS		V_{CC} = 2.5 V to 5.5 V				
Output Voltage High Level	V_{OH}	I_{OH} = 0.8 mA, V_{CC} = 2.5 V	V_{CC} − 0.4			V
Output Voltage Low Level	V_{OL}	I_{OL} = 0.8 mA, V_{CC} = 2.5 V			0.4	V
AC PERFORMANCE[2]		V_{CC} = 2.5 V to 5.5 V				
Rise Time/Fall Time	t_R/t_F	10% to 90%, V_{CC} = 2.5 V		25 to 50		ns
		10% to 90%, V_{CC} = 5.5 V		45 to 75		ns
Propagation Delay	t_{PD}	V_{OD} = 10 mV, V_{CC} = 2.5 V		30 to 50		ns
		V_{OD} = 50 mV, V_{CC} = 5.5 V		35 to 60		ns
Propagation Delay Skew, Rising to Falling Transition		V_{CC} = 2.5 V		4.5		ns
		V_{CC} = 5.5 V		8		ns
Propagation Delay Skew, Q to $\overline{Q}$		V_{CC} = 2.5 V		3		ns
		V_{CC} = 5.5 V		4		ns
Overdrive Dispersion		10 mV < V_{OD} < 125 mV		12		ns
Common-Mode Dispersion		−0.2 V < V_{CM} < V_{CC} + 0.2 V		1.5		ns
POWER SUPPLY						
Supply Voltage Range	V_{CC}		2.5		5.5	V
Positive Supply Current	I_{VCC}	V_{CC} = 2.5 V		550	650	µA
		V_{CC} = 5.5 V		800	1100	µA
Power Dissipation	P_D	V_{CC} = 2.5 V		1.4	1.7	mW
		V_{CC} = 5.5 V		4.5	7	mW
Power Supply Rejection Ratio	PSRR	V_{CC} = 2.5 V to 5.5 V	−50			dB
Shutdown Current	I_{SD}	V_{CC} = 2.5 V to 5.5 V		150	260	µA

[1] The output is a high impedance mode when the device is in shutdown mode. Note that this feature is to be used with care since the enable/disable time is much longer than with a true tristate output.

[2] V_{IN} = 100 mV square input at 1 MHz, V_{CM} = 0 V, C_L = 15 pF, V_{CCI} = 2.5 V, unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages	
Supply Voltage (V_{CC} to Ground)	−0.5 V to +6.0 V
Supply Differential	−6.0 V to +6.0 V
Input Voltages	
Input Voltage	−0.5 V to V_{CC} + 0.5 V
Differential Input Voltage	±(V_{CC} + 0.5 V)
Maximum Input/Output Current	±50 mA
Shutdown Pin	
Applied Voltage (S_{DN} to Ground)	−0.5 V to V_{CC} + 0.5 V
Maximum Input/Output Current	±50 mA
Hysteresis Control Pin	
Applied Voltage (HYS to Ground)	−0.5 V to V_{CC} + 0.5 V
Maximum Input/Output Current	±50 mA
Output Current	±50 mA
Operating Temperature	
Ambient Temperature Range	−40°C to +125°C
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3.

Package Type	θ_{JA}[1]	Unit
ADCMP609 8-Lead MSOP	130	°C/W

[1] Measurement in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

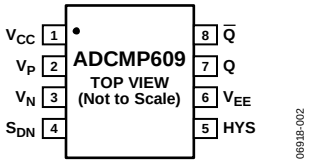

Figure 2. ADCMP609 Pin Configuration

Table 4. ADCMP609 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{CC}	V_{CC} Supply.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	S_{DN}	Shutdown. Drive this pin low to shut down the device.
5	HYS	Hysteresis Control. Bias with resistor or current source for hysteresis.
6	V_{EE}	Negative Supply Voltage.
7	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input (V_P) is greater than the analog voltage at the inverting input (V_N), provided the comparator is in compare mode.
8	$\overline{Q}$	Inverting Output. $\overline{Q}$ is at logic low if the analog voltage at the noninverting input (V_P) is greater than the analog voltage at the inverting input (V_N), provided the comparator is in compare mode.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 2.5 V, T_A = 25°C, unless otherwise noted.

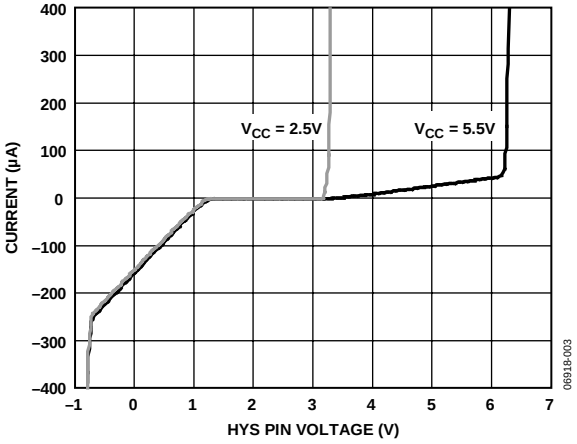

Figure 3. HYS Pin Current (µA) vs. Voltage (V)

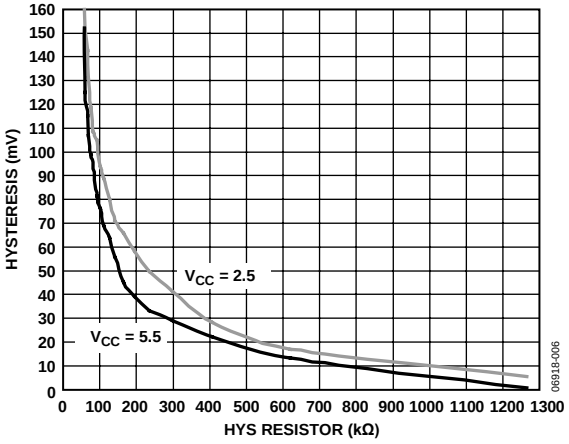

Figure 6. Hysteresis vs. HYS Resistor

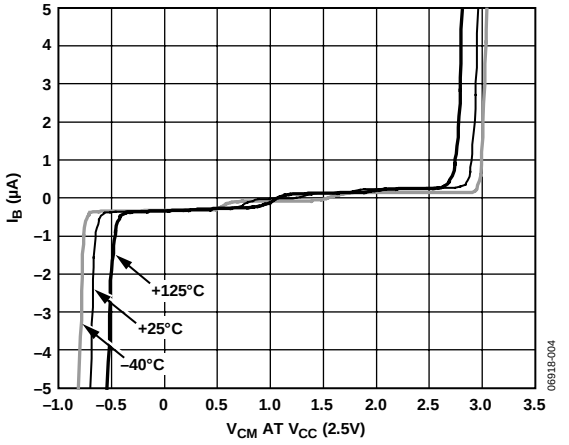

Figure 4. Input Bias Current vs. Input Common-Mode Voltage (V)

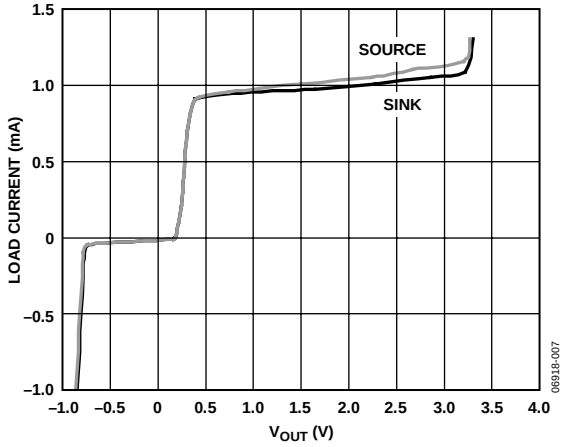

Figure 7. Load Current vs. V_{OH}/V_{OL}

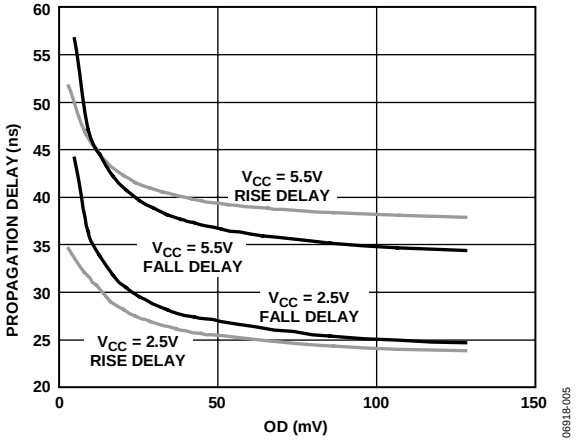

Figure 5. Propagation Delay vs. Input Overdrive at V_{CC} = 2.5 V and 5.5 V

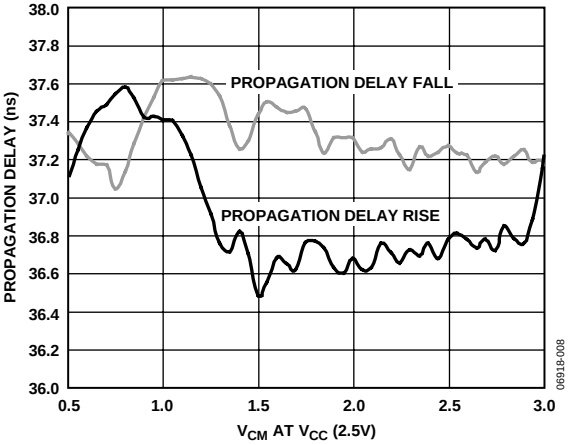

Figure 8. Propagation Delay vs. Input Common-Mode Voltage (V)

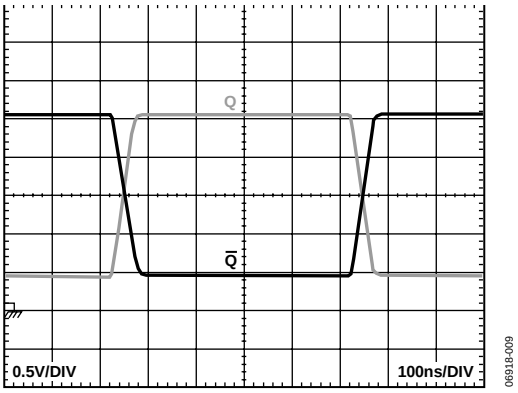

Figure 9. 1 MHz Output Voltage Waveform at V_{CC} = 2.5 V

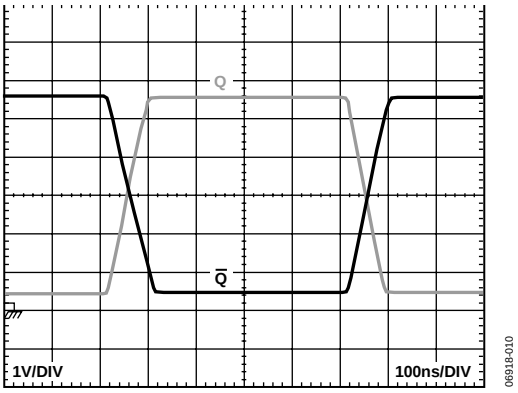

Figure 10. 1 MHz Output Voltage Waveform at V_{CC} = 5.5 V

APPLICATIONS INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP609 comparator is a high speed device. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane (V_{CC}) and the ground plane. Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Place a 0.1 µF bypass capacitor as close as possible to each V_{CC} supply pin. The capacitor should be connected to the ground plane with redundant vias placed to provide a physically short return path for output currents flowing back from ground to the V_{CC} pin. Carefully select high frequency bypass capacitors for minimum inductance and effective series resistance (ESR). Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

TTL-/CMOS-COMPATIBLE OUTPUT STAGE

To achieve specified propagation delay performance, keep the capacitive load at or below the specified minimums. The outputs of the ADCMP609 are designed to directly drive one Schottky TTL or three low power Schottky TTL loads (or an equivalent). For large fan outputs, buses, or transmission lines, use an appropriate buffer to maintain the excellent speed and stability of the comparator.

With the rated 15 pF load capacitance applied, more than half of the total device propagation delay is output stage slew time. Because of this, the total propagation delay decreases as V_{CC} decreases, and instability in the power supply may appear as excess delay dispersion.

Delay is measured to the 50% point for whatever supply is in use; therefore, the fastest times are observed with the V_{CC} supply at 2.5 V, and larger values are observed when driving loads that switch at other levels.

Overdrive and input slew rate dispersions are not significantly affected by output loading and V_{CC} variations.

The TTL-/CMOS-compatible output stage is shown in the simplified schematic diagram (Figure 11). Because of its inherent symmetry and generally good behavior, this output stage is readily adaptable for driving various filters and other unusual loads.

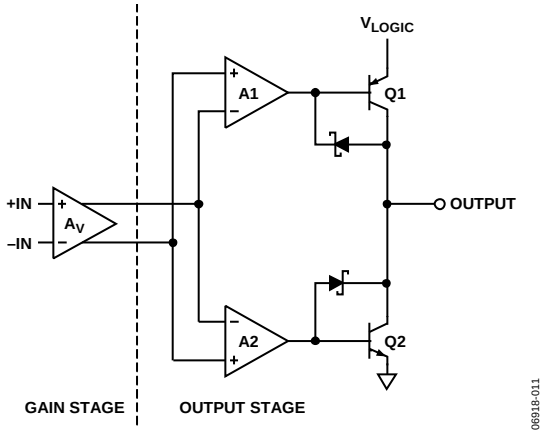

Figure 11. Simplified Schematic Diagram of TTL-/CMOS-Compatible Output Stage

OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, common power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, therefore degrading the overall response. Higher impedances encourage undesired coupling.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP609 comparator is designed to reduce propagation delay dispersion over a wide input overdrive range of 10 mV to V_{CC} − 1 V. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate, which is how far or how fast the input signal exceeds the switching threshold.

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is the variation in propagation delay as the input overdrive conditions are changed (see Figure 12 and Figure 13).

ADCMP609 dispersion is typically <12 ns as the overdrive varies from 10 mV to 125 mV. This specification applies to both positive and negative signals because the device has very closely matched delays for both positive-going and negative-going inputs, and very low output skews. Note that for repeatable dispersion measurements the actual device offset is added to the overdrive.

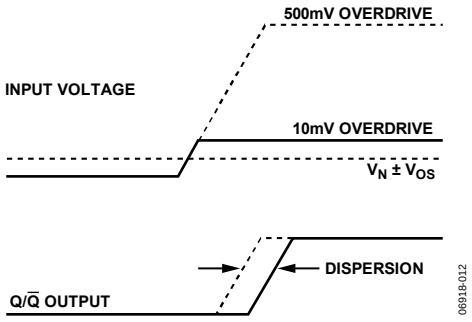

Figure 12. Propagation Delay—Overdrive Dispersion

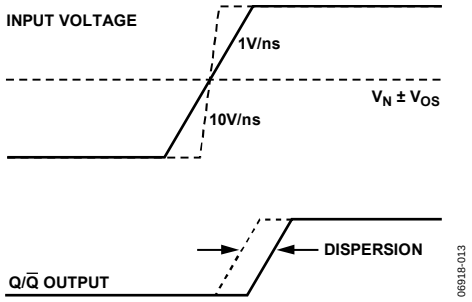

Figure 13. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 14. As the input voltage approaches the threshold (0.0 V, in Figure 14) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold, $-V_H/2$, is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0.0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

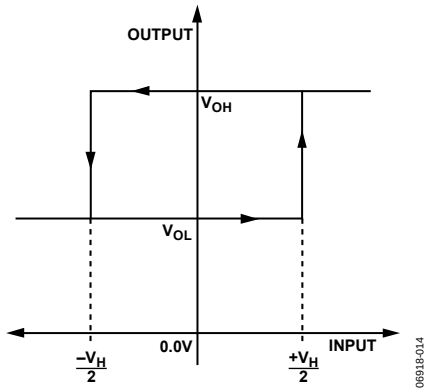

Figure 14. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and can even induce oscillation in some cases.

The ADCMP609 comparator offers a programmable hysteresis feature that significantly improves accuracy and stability. Connecting an external pull-down resistor or a current source from the HYS pin to ground varies the amount of hysteresis in a predictable, stable manner. Leaving the HYS pin disconnected or driving it high removes the hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 15 illustrates the amount of hysteresis applied as a function of the external resistor value.

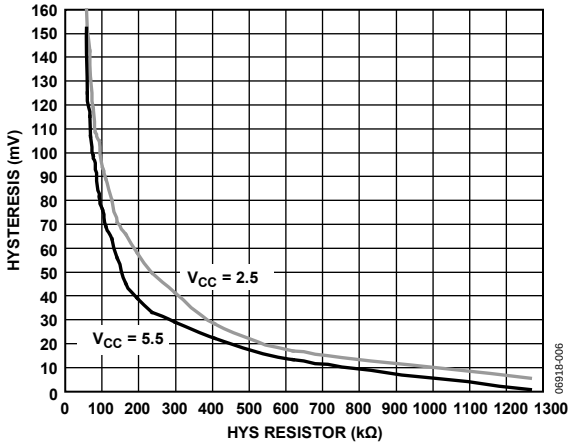

Figure 15. Hysteresis vs. HYS Resistor

The HYS pin appears as a 1.25 V bias voltage seen through a series resistance of 7 kΩ ± 20% throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the HYS pin because it impairs the latch function and often degrades the jitter performance of the device.

With the pin driven low, hysteresis may become large, but in this device, the effect is not reliable or intended as a latch function.

CROSSOVER BIAS POINT

Rail-to-rail inputs of this type, in both op amps and comparators, have a dual front-end design. Certain devices are active near the V_{CC} rail, and others are active near the V_{EE} rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $V_{CC}/2$, the direction of the bias current reverses and there are changes in measured offset voltages and currents.

The ADCMP609 slightly elaborates on this scheme. The crossover points are at approximately 0.8 V and 1.6 V.

MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PCB design practice (as discussed in the Optimizing Performance section), these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chatter seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation may be encountered. These oscillations are due to the high gain bandwidth of the comparator in combination with feedback through parasitics in the package and PCB. In many applications, chatter is not harmful.

TYPICAL APPLICATIONS CIRCUITS

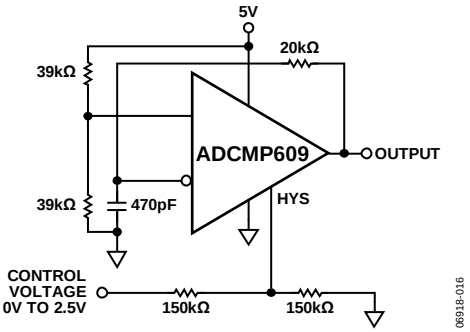

Figure 16. Voltage Controlled Oscillator

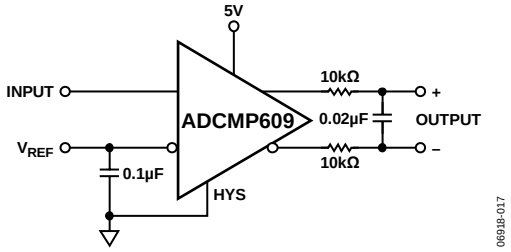

Figure 17. Duty Cycle to Differential Voltage Converter

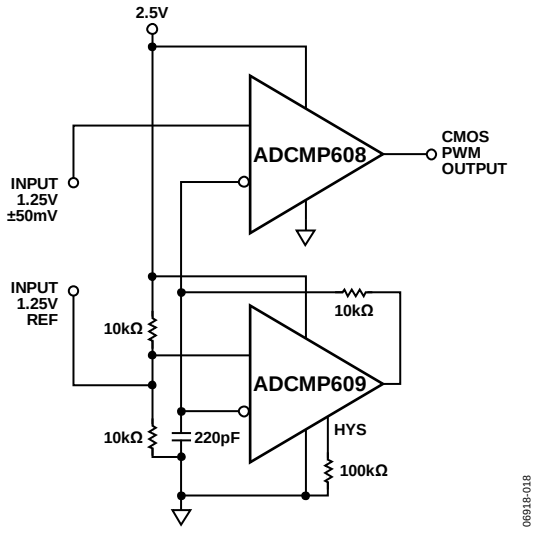

Figure 18. Oscillator and Pulse-Width Modulator