Evaluating the ADG1408L 4 Ω R_{ON}, 8-Channel *i*CMOS Multiplexer with 1.2 V and 1.8 V JEDEC Logic Compliance

FEATURES

- Single inline headers provide flexibility for the field programmable gate array (FPGA) or microcontroller 1.2 V or 1.8 V logic input signals
- Surface-mount device (SMD) pin resistor or capacitor sockets available for the addition of passive components
- SMB connector sockets provide flexibility for the input and output signals

EVALUATION KIT CONTENTS

- EVAL-ADG1408LEBZ evaluation board

DOCUMENTS NEEDED

- ADG1408L data sheet
- EVAL-ADG1408LEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±15 V for dual supply
  - 12 V for single supply
  - ±5 V for dual supply
- Optional digital logic supply (V_L)
  - 1.1 V to 1.3 V for 1.2 V logic
  - 1.65 V to 1.95 V for 1.8 V logic
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG1408LEBZ is the evaluation board for the ADG1408L. The ADG1408L contains an eight channel multiplexer. The ADG1408L switches one of eight inputs to a common output, as determined by the 3-bit binary address lines, A0, A1, and A2. The enable pin (EN) is used to enable or disable the device. When disabled, all channels are switched off. When enabled, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

An external V_L supply pin provides logic control flexibility for lower logic controls. The ADG1408L is both 1.2 V and 1.8 V JEDEC standard compliant.

Figure 1 shows the EVAL-ADG1408LEBZ in a typical evaluation setup. The EVAL-ADG1408LEBZ is located in the center of the evaluation board, and wire screw terminals are provided to connect each source and drain pin. Three screw terminals are used to power the device, and an external pin provides users with a defined digital logic supply voltage. Alternatively, the digital logic supply voltage can be supplied from a 5-pin header.

Full specifications on the ADG1408L are available in the ADG1408L data sheet available from Analog Devices, Inc., and must be consulted in conjunction with this user guide when using the EVAL-ADG1408LEBZ.

TABLE OF CONTENTS

REVISION HISTORY

5/2023—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

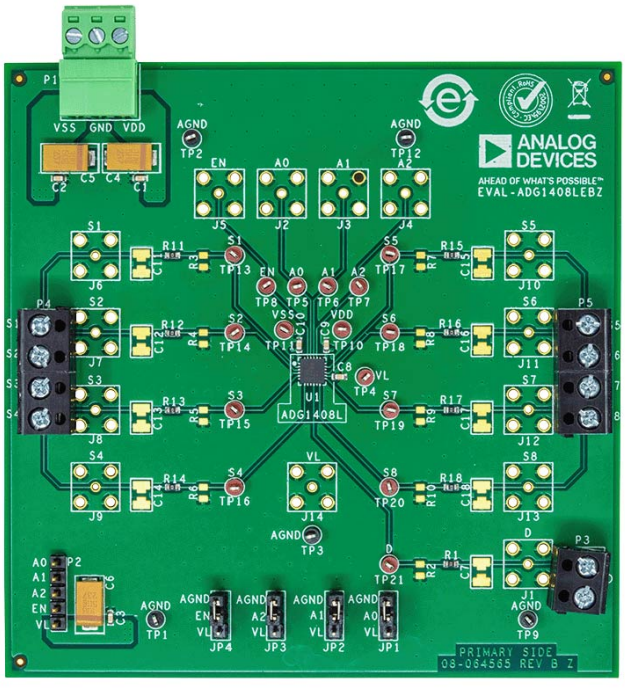

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Figure 1. EVAL-ADG1408LEBZ Evaluation Board Photograph

EVALUATION BOARD HARDWARE

POWER SUPPLY

Connector P1 provides access to the supply pins on the ADG1408L. VDD, AGND, and VSS on the P1 terminal block link to the appropriate pins on the ADG1408L. For dual-supply voltages, the EVAL-ADG1408LEBZ can be powered at ±15 V or ±5 V. For single-supply voltages, the GND and VSS terminals must be connected and power the EVAL-ADG1408LEBZ with 12 V. Additionally, 1.1 V to 1.95 V is supplied to the V_L pin of the ADG1408L.

LINK HEADERS

The EVAL-ADG1408LEBZ provides several link options that must be set for the required operating conditions before using.

Table 1 describes the positioning of the links necessary for controlling the EVAL-ADG1408LEBZ via the link headers. The functions of these link options are described in detail in Table 2.

Table 1. Link Header Descriptions

Link	Position	Description
JP1 to JP4	A	VL
	B	AGND

Table 2. Link Header Functions

Link	Function
JP1 to JP4	This link selects the source of the Ax voltage supplied to the ADG1408L. Position A selects VL from P2. Position B selects 0 V or AGND.

SMB CONNECTORS

The parallel interface of the ADG1408L is controlled manually using the link headers of JP1 to JP4, or it can be accessed using the Subminiature Version B (SMB) connectors, J2 to J5. To use the SMB connectors, remove the link headers of JP1 to JP4.

INPUT SIGNALS

Provided in the EVAL-ADG1408LEBZ are screw connectors, P3, P4, and P5 to connect to both the source and drain pins of the ADG1408L. Additional SMB connector pads are available if extra connections are required.

Each trace on the source and drain side includes two sets of 0603 pads, which can place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads can create a simple RC filter.

EVALUATION BOARD SCHEMATIC AND ARTWORK

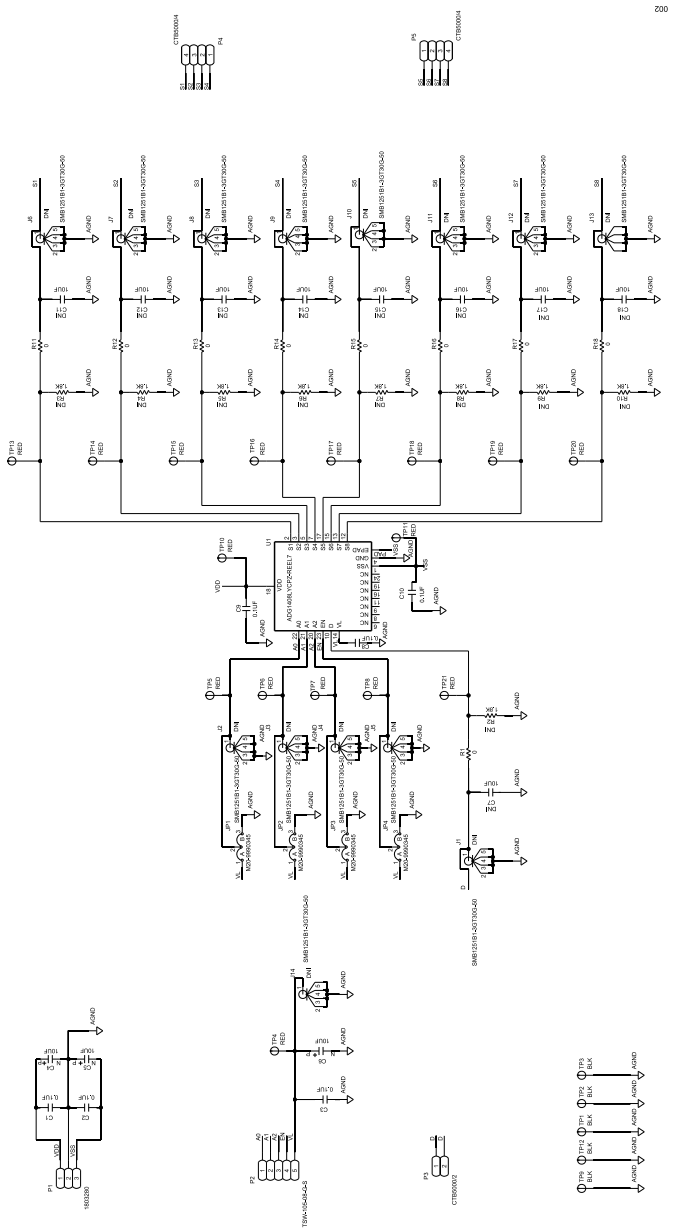

Figure 2. EVAL-ADG1408LEBZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

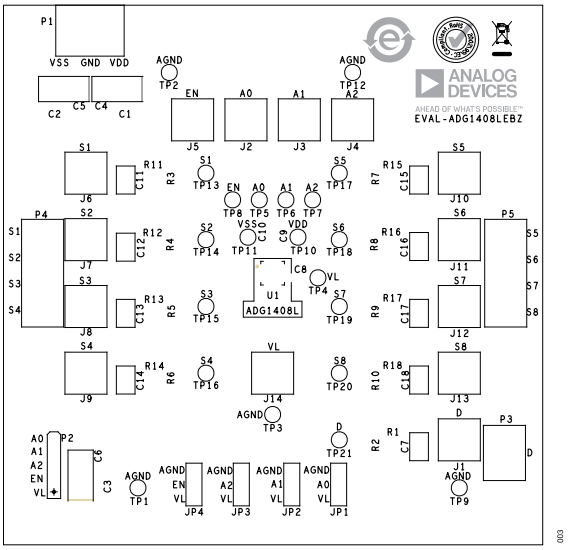

Figure 3. EVAL-ADG1408LEBZ Silkscreen

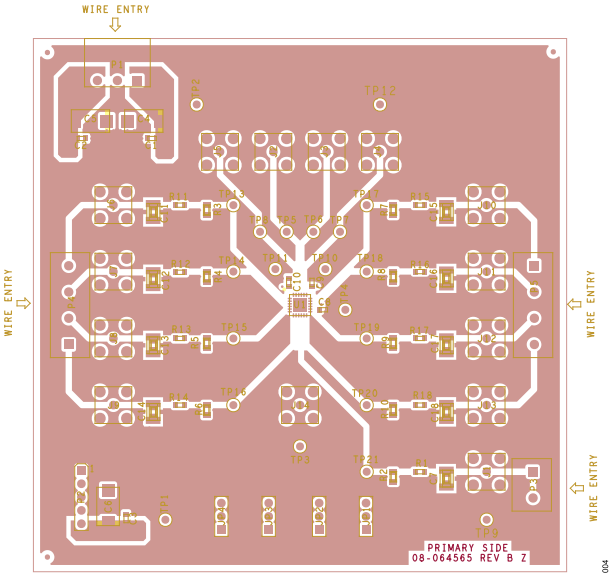

Figure 4. EVAL-ADG1408LEBZ Top Layer

EVALUATION BOARD SCHEMATIC AND ARTWORK

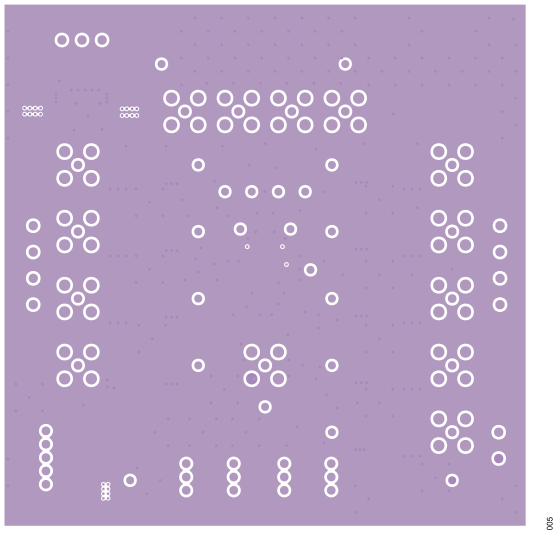

Figure 5. EVAL-ADG1408LEBZ Layer 2

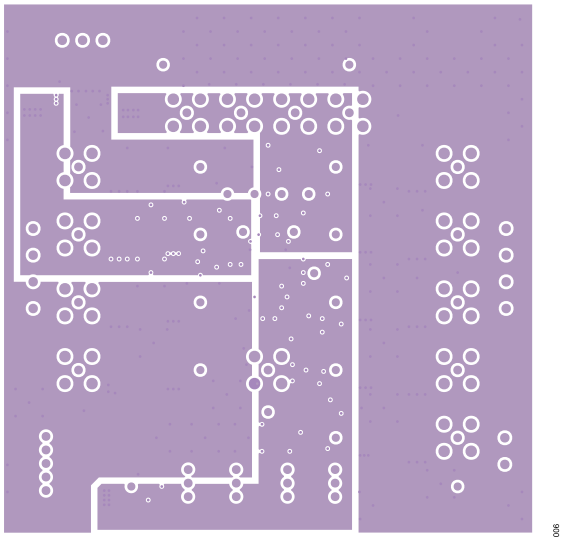

Figure 6. EVAL-ADG1408LEBZ Layer 3

EVALUATION BOARD SCHEMATIC AND ARTWORK

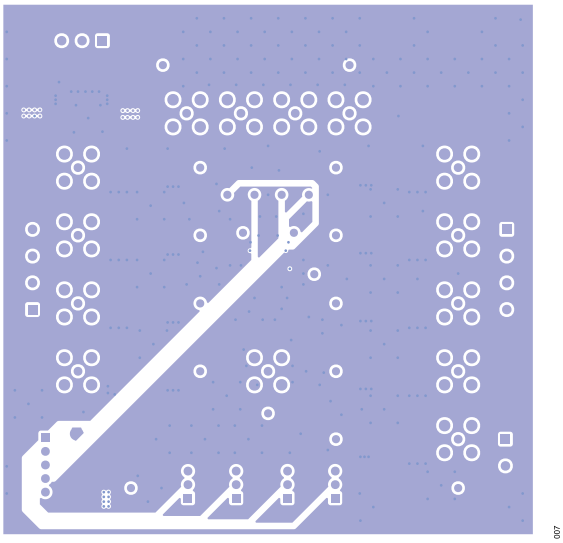

Figure 7. EVAL-ADG1408LEBZ Bottom Layer