Data Sheet

ADG7421F

Low Voltage Fault Protection and Detection, 12 Ω R_{ON}, Dual SPST Switch

FEATURES

- Overvoltage fault protection up to ±60 V on S1 and S2 pins
- Power-off protection up to ±60 V on S1 and S2 pins
- Overvoltage detection on S1 and S2 pins
- Known state output without digital inputs present
- Low on resistance: 12 Ω typical
- Ultraflat, on resistance: 0.005 Ω typical
- Low fault detection threshold voltage: 0.1 V typical
- 3 kV HBM ESD rating
- Latch-up immune under any circumstance
- ±1.8 V to ±2.5 V dual supply operation
- 1.8 V to 5.5 V single-supply operation
- 10-Lead, 3 mm × 2 mm LFCSP

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

COMPANION PRODUCTS

- ADCs: AD7124-4, AD7124-8
- Linear Regulator: ADP162
- Additional companion products on the ADG7421F product page

FUNCTIONAL BLOCK DIAGRAM

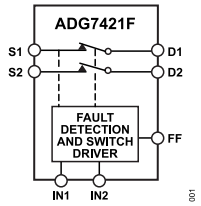

Figure 1.

GENERAL DESCRIPTION

The ADG7421F is a low voltage, dual single-pole/single-throw (SPST), low on-resistance switch that features overvoltage protection, power-off protection, and overvoltage detection on the source pins.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. When powered, if the analog input signal levels on the Sx pins exceed V_{DD} or V_{SS} by a threshold voltage, V_T, the switch automatically turns off and the digital FF (fault flag) pin drops to a logic low to indicate a fault.

Input signal levels up to +60 V or −60 V relative to ground are blocked, in both the powered and unpowered condition. The switches turn on with a Logic 1 input and conducts equally well in both directions with an analog signal range of V_{SS} + 0.1 V to V_{DD} − 0.55 V for a 5 V single supply. The digital input is compatible with 1.8 V logic inputs over the full operating supply range.

The ADG7421F is ideal for providing overvoltage protection for small signals such as resistance temperature device (RTD) inputs (see Figure 56) and thermocouple inputs (see Figure 55). The ability to protect against high voltages up to ±60 V coupled with a low voltage supply can enable complete low voltage input stages for industrial applications.

PRODUCT HIGHLIGHTS

1. Pin S1 and Pin S2 are protected against voltages greater than the supply rails, up to ±60 V in both powered and unpowered states.
2. Overvoltage detection with digital output indicates operating state of switches.
3. Trench isolation guards against latch-up.
4. The ADG7421F can operate from a dual supply range of ±1.8 V to ±2.5 V or a single-supply range of 1.8 V to 5.5 V.

Rev. 0

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REVISION HISTORY

7/2021—Revision 0: Initial Version

SPECIFICATIONS

Table 1. Operating Supply Voltages

Parameter	Min	Typ	Max	Unit
SUPPLY VOLTAGE				
Dual	±1.8		±2.5	V
Single	1.8		5.5	V

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 4.5 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} + 0.1 to V_{DD} − 0.55			V	
On Resistance, R_{ON}	12			Ω typ	Source voltage (V_S) = 0.1 V to 3.95 V, source current (I_S) = 10 mA
	15	19	23	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.005			Ω typ	V_S = 0.1 V to 3.95 V, I_S = 10 mA
	0.03	0.05	0.1	Ω max	
On Resistance Matching, $R_{MATCH(ON)}$	0.01			Ω typ	V_S = 0.1 V to 3.95 V, I_S = 10 mA
	0.2	0.5	0.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 4.5 V to 1 V, drain voltage (V_D) = 1 V to 4.5 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 4.5 V to 1 V, V_D = 1 V to 4.5 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
Channel On Leakage, I_D (On), I_S (On)	±0.05			nA typ	V_S = V_D = 1 V to 4.5 V
	±0.3	±1.5	±15	nA max	
			±4.0	nA max	−40°C to +105°C
FAULT					
Threshold Voltage, V_T	0.1			V typ	
Source Leakage Current, I_S					
With Overvoltage			±120	µA typ	V_{DD} = 5.5 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±100	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±60 V
Drain Leakage Current, I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 5.5 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
	±0.3	±2.5	±30	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, INx = 0 V
	±0.3	±2.5	±30	nA max	
Power Supplies Floating			±11	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, INx = 0 V
DIGITAL INPUTS/OUTPUTS					
Input Voltage High, V_{INH}			1.3	V min	
Input Voltage Low, V_{INL}			0.8	V max	
Input Low or High Current, I_{INL} or I_{INH}	0.7			µA typ	Input voltage (V_{IN}) = 0 V or V_{DD}
			1	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	

SPECIFICATIONS

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Output Voltage Low, V_{OL}	0.4			V max	Fault flag current (I_{FF}) = 2 mA
DYNAMIC CHARACTERISTICS					
On Time, t_{ON}	4.2			µs typ	Load resistance (R_L) = 300 Ω, load capacitance (C_L) = 35 pF, V_S = 3 V
	5.2	5.3	5.3	µs max	
Off Time, t_{OFF}	150			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V
	180	180	180	ns max	
Break-Before-Make Time Delay, t_D	3.5			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V
			2.8	µs min	
Overvoltage Response Time, $t_{RESPONSE}$					
Positive	1.2			µs typ	R_L = 1 kΩ, C_L = 5 pF
	1.5	1.6	1.6	µs max	
Negative	1.5			µs typ	Pull-up resistor (R_{PULLUP}) = 1 kΩ, C_L = 5 pF
	1.8	1.9	2	µs max	
Overvoltage Recovery Time, $t_{RECOVERY}$	7.6			µs typ	R_L = 1 kΩ, C_L = 5 pF
	9.5	10	10.3	µs max	
Interrupt Flag Response Time, $t_{DIGRESP}$	500			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, pull-up voltage (V_{PULL_UP}) = 5 V
	650	650	650	ns max	
Interrupt Flag Recovery Time, t_{DIGREC}	1.2			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 5 V
	1.5	1.5	1.5	µs max	
Charge Injection, Q_{INJ}	−45			pC typ	V_S = 2.5 V, source resistor (R_S) = 0 Ω, C_L = 1 nF
Off Isolation	−65			dB typ	R_L = 50 Ω, C_L = 5 pF, frequency (f) = 1 MHz
Channel to Channel Crosstalk	−68			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Total Harmonic Distortion Plus Noise, THD + N	−101			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 20 Hz to 20 kHz
	0.009			% typ	
Total Harmonic Distortion, THD	−132			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 1 kHz
	−125			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 20 kHz
	−112			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 100 kHz
−3 dB Bandwidth	580			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.92			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Source Off Capacitance, C_S (Off)	11			pF typ	V_S = 2.5 V, f = 1 MHz
Drain Off Capacitance, C_D (Off)	11			pF typ	V_S = 2.5 V, f = 1 MHz
Drain On Capacitance and Source On Capacitance, C_D (On) and C_S (On)	13			pF typ	V_S = 2.5 V, f = 1 MHz
Drain On Capacitance and Source On Capacitance Flatness, C_{DFLAT} (On) and C_{SFLAT} (On)	1.6			pF typ	V_S = 0.1 V to 3.95 V, f = 1 MHz
Capacitance Matching, C_{MATCH} (On)	0.2			pF typ	V_S = 0.1 V to 3.95 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V, V_{SS} = 0 V, GND = 0 V, digital inputs = V_{DD} or GND
Normal Mode					
Positive Supply Current, I_{DD}	850			µA typ	
	1100		1100	µA max	
GND Current, I_{GND}	745			µA typ	
	950		950	µA max	
Negative Supply Current, I_{SS}	105			µA typ	
	150		150	µA max	
Fault Mode					V_S = ±60 V

SPECIFICATIONS

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_{DD}	850			µA typ	
	1100		1100	µA max	
I_{GND}	630			µA typ	
	850		850	µA max	
I_{SS}	200			µA typ	
	270		270	µA max	

3 V SINGLE SUPPLY

V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V and GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 2.7 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} + 0.1 to V_{DD} − 0.25			V	
R_{ON}	12			Ω typ	V_S = 0.1 V to 2.45 V, I_S = 10 mA
	15	19	23	Ω max	
$R_{FLAT (ON)}$	0.005			Ω typ	V_S = 0.1 V to 2.45 V, I_S = 10 mA
	0.03	0.05	0.1	Ω max	
$R_{MATCH(ON)}$	0.01			Ω typ	V_S = 0.1 V to 2.45 V, I_S = 10 mA
	0.2	0.5	0.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
I_S (Off)	±0.05			nA typ	V_S = 3.3 V to 1 V, V_D = 1 V to 3.3 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = 3.3 V to 1 V, V_D = 1 V to 3.3 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = V_D = 1 V to 3.3 V
	±0.3	±1.5	±15	nA max	
			±4.0	nA max	−40°C to +105°C
FAULT					
V_T	0.1			V typ	
I_S					
With Overvoltage			±120	µA typ	V_{DD} = 3.6 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±100	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±60 V
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 3.6 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
	±0.3	±2.5	±30	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, INx = 0 V
	±0.3	±2.5	±30	nA max	
Power Supplies Floating			±11	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, INx = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.3	V min	
V_{INL}			0.5	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or V_{DD}

SPECIFICATIONS

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
			1	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	4			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
	4.8	5	5	µs max	
t_{OFF}	170			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
	200	200	210	ns max	
t_D	3.4			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
			2.7	µs min	
$t_{RESPONSE}$					
Positive	1.4			µs typ	R_L = 1 kΩ, C_L = 5 pF
	1.7	1.8	1.9	µs max	
Negative	1.7			µs typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF
	2.1	2.3	2.4	µs max	
$t_{RECOVERY}$	7.8			µs typ	R_L = 1 kΩ, C_L = 5 pF
	9.7	10.2	10.5	µs max	
$t_{DIGRESP}$	450			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 3 V
	550	550	550	ns max	
t_{DIGREC}	1.1			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 3 V
	1.4	1.4	1.4	µs max	
Q_{INJ}	−40			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−64			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−68			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	−97			dB	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 20 Hz to 20 kHz
	0.0013			%	
THD	−130			dB	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 1 kHz
	−126			dB	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 20 kHz
	−117			dB	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 100 kHz
−3 dB Bandwidth	570			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.92			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	12			pF typ	V_S = 1.5 V, f = 1 MHz
C_D (Off)	12.5			pF typ	V_S = 1.5 V, f = 1 MHz
CD (On), CS (On)	13.5			pF typ	V_S = 1.5 V, f = 1 MHz
C_{DFLAT} (On), C_{SFLAT} (On)	1.3			pF typ	V_S = 0.1 V to 2.45 V, f = 1 MHz
C_{MATCH} (On)	0.2			pF typ	V_S = 0.1 V to 2.45 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V, V_{SS} = 0 V, GND = 0 V, digital inputs = GND or V_{DD}
Normal Mode					
I_{DD}	630			µA typ	
	850		850	µA max	
I_{GND}	530			µA typ	
	750		750	µA max	
I_{SS}	90			µA typ	
	140		140	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	630			µA typ	
	850		850	µA max	
I_{GND}	420			µA typ	

SPECIFICATIONS

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
I_{SS}	600		600	µA max	
	180			µA typ	
	250		250	µA max	

1.8 V SINGLE SUPPLY

V_{DD} = 1.8 V ± 5%, V_{SS} = 0 V and GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 1.71 V, V_{SS} = 0 V
Analog Signal Range	V_{SS} + 0.1 to V_{DD} − 0.1			V	
R_{ON}	12			Ω typ	V_S = 0.1 V to 1.61 V, I_S = 10 mA
	15	19	23	Ω max	
$R_{FLAT (ON)}$	0.005			Ω typ	V_S = 0.1 V to 1.61 V, I_S = 10 mA
	0.03	0.05	0.1	Ω max	
$R_{MATCH (ON)}$	0.01				V_S = 0.1 V to 1.61 V, I_S = 10 mA
	0.2	0.5	0.7		
LEAKAGE CURRENTS					V_{DD} = 1.95 V, V_{SS} = 0 V
I_S (Off)	±0.05			nA typ	V_S = 0.6 V to 1.65 V, V_D = 1.65 V to 0.6 V
	±0.2	±1.0	±14.0	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = 0.6 V to 1.65 V, V_D = 1.65 V to 0.6 V
	±0.2	±1.0	±14.0	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = 0.6 V to 1.65 V, V_D = 1.65 V to 0.6 V
	±0.3	±1.5	±15.0	nA max	
			±4.0	nA max	−40°C to +105°C
FAULT					
V_T	0.1			V typ	
I_S					
With Overvoltage			±120	µA typ	V_{DD} = 1.95 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±100	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±60 V
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 1.95 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V
	±0.3	±2.5	±30	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, INx = 0 V
	±0.3	±2.5	±30	nA max	
Power Supplies Floating			±11	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, INx = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.07	V min	
V_{INL}			0.5	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or 5 V
			1	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA

SPECIFICATIONS

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS					
t_{ON}	4.7			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
	6.3	7.3	7.3	µs max	
t_{OFF}	250			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
	360	380	400	ns max	
t_D	3.9			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
			2.9	ns min	
$t_{RESPONSE}$					
Positive	1.7			µs typ	R_L = 1 kΩ, C_L = 5 pF
	2.1	2.2	2.4	µs max	
Negative	2			µs typ	R_{PULLUP} = 1 kΩ, C_L = 5 pF
	2.5	2.6	2.8	µs max	
$t_{RECOVERY}$	9			µs typ	R_L = 1 kΩ, C_L = 5 pF
	14	18.4	18.4	µs max	
$t_{DIGRESP}$	400			ns typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 1.8 V
	450	500	500	ns max	
t_{DIGREC}	1			µs typ	R_{PULLUP} = 1 kΩ, C_L = 12 pF, V_{PULL_UP} = 1.8 V
	1.2	1.3	1.3	µs max	
Q_{INJ}	−25			pC typ	V_S = 0.9 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−68			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	−97			dB typ	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 20 Hz to 20 kHz
	0.0012			% typ	
THD	−130			dB typ	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 1 kHz
	−121			dB typ	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 20 kHz
	−110			dB typ	R_L = 10 kΩ, V_S = 1.5 V p-p, f = 100 kHz
−3 dB Bandwidth	550			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.92			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	13			pF typ	V_S = 1 V, f = 1 MHz
C_D (Off)	14			pF typ	V_S = 1 V, f = 1 MHz
C_D (On), C_S (On)	14			pF typ	V_S = 1 V, f = 1 MHz
C_{SFLAT}(On), C_{DFLAT}(On)	0.8			pF typ	V_S = 0.1 V to 1.61 V, f = 1 MHz
C_{MATCH}(On)	0.2			pF typ	V_S = 0.1 V to 1.61 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 1.95 V, V_{SS} = 0 V, GND = 0 V, digital inputs = GND or V_{DD}
Normal Mode					
I_{DD}	480			µA typ	
	700		700	µA max	
I_{GND}	400			µA typ	
	600		600	µA max	
I_{SS}	80			µA typ	
	125		125	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	520			µA typ	
	800		800	µA max	
I_{GND}	320			µA typ	
	550		550	µA max	
I_{SS}	175			µA typ	

SPECIFICATIONS

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	245		245	µA max	

±2.5 V DUAL SUPPLY

V_{DD} = 2.5 V ± 10%, V_{SS} = −2.5 V ± 10%, and GND = 0 V, unless otherwise noted.

Table 5.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 2.25 V, V_{SS} = −2.25 V
Analog Signal Range	V_{SS} + 0.1 to V_{DD} − 0.35			V	
R_{ON}	12			Ω typ	V_S = −2.15 V to +1.9 V, I_S = 10 mA
	15	19	23	max	
$R_{FLAT (ON)}$	0.005			Ω typ	V_S = −2.15 V to +1.9 V, I_S = 10 mA
	0.03	0.05	0.1	Ω max	
$R_{MATCH (ON)}$	0.01			Ω typ	V_S = −2.15 V to +1.9 V, I_S = 10 mA
	0.2	0.5	0.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = 2.75 V, V_{SS} = −2.75 V
I_S (Off)	±0.05			nA typ	V_S = +2.25 V to −2.25 V, V_D = −2.25 V to +2.25 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (Off)	±0.05			nA typ	V_S = +2.25 V to −2.25 V, V_D = −2.25 V to +2.25 V
	±0.2	±1.0	±14	nA max	
			±3.5	nA max	−40°C to +105°C
I_D (On), I_S (On)	±0.05			nA typ	V_S = V_D = −2.25 V, or V_S = V_D = 2.25 V
	±0.3	±1.5	±15	nA max	
			±4.0	nA max	−40°C to +105°C
FAULT (ON Sx PINS)					
V_T	0.1			V typ	
I_S					
With Overvoltage			±120	µA typ	V_{DD} = 2.75 V, V_{SS} = −2.75 V, GND = 0 V, V_S = ±60 V
Power Supplies Grounded or Floating			±100	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±60 V
I_D					
With Overvoltage	±0.1			nA typ	V_{DD} = 2.75 V, V_{SS} = −2.75 V, GND = 0 V, V_S = ±60 V
	±0.3	±2.5	±30	nA max	
Power Supplies Grounded	±0.1			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±60 V, INx = 0 V
	±0.3	±2.5	±30	nA max	
Power Supplies Floating			±11	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±60 V, INx = 0 V
DIGITAL INPUTS/OUTPUTS					
V_{INH}			1.07	V min	
V_{INL}			0.5	V max	
I_{INL} or I_{INH}	0.7			µA typ	V_{IN} = 0 V or 5 V
			1	µA max	
C_{IN}	5			pF typ	
V_{OL}	0.4			V max	I_{FF} = 2 mA
DYNAMIC CHARACTERISTICS					
t_{ON}	5.5			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V

SPECIFICATIONS

Table 5.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
	6.7	6.8	6.8	µs max	
t_{OFF}	130			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
	170	170	170	ns max	
t_D	4.9			µs typ	R_L = 300 Ω, C_L = 35 pF, V_S = 1.5 V
			4	µs min	
$t_{RESPONSE}$					
Positive	1.3			µs typ	R_L = 1 kΩ, C_L = 5 pF
	1.5	1.6	1.7	µs max	
Negative	2			µs typ	R_L = 1 kΩ, C_L = 5 pF
	2.4	2.6	2.7	µs max	
$t_{RECOVERY}$	7.4			µs typ	R_L = 1 kΩ, C_L = 5 pF
	9.5	9.9	10.1	µs max	
$t_{DIGRESP}$	500			ns typ	R_{PULLUP} = 1 kΩ, C_L = 10 pF, V_{PULL_UP} = 2.5 V
	550	550	600	ns max	
t_{DIGREC}	800			ns typ	R_{PULLUP} = 1 kΩ, C_L = 10 pF, V_{PULL_UP} = 2.5 V
	1.0	1.0	1.0	µs max	
Q_{INJ}	−50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
THD + N	−101			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 20 Hz to 20 kHz
	0.009			% typ	
THD	−133			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f =1 kHz
	−131			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 20 kHz
	−114			dB typ	R_L = 10 kΩ, V_S = 3 V p-p, f = 100 kHz
−3 dB Bandwidth	590			MHz typ	R_L = 50 Ω, C_L = 5 pF
Insertion Loss	−0.92			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
Channel to Channel Crosstalk	−68			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz
C_S (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
CD (On), C_S (On)	13			pF typ	V_S = 0 V, f = 1 MHz
C_{SFLAT} (On), C_{DFLAT} (On)	1.2			pF typ	V_S = −2.15 V to +1.9 V, f = 1 MHz
C_{MATCH} (On)	0.2			pF typ	V_S = −2.15 V to +1.9 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 2.75 V, V_{SS} = −2.75 V, GND = 0 V, digital inputs = GND or V_{DD}
Normal Mode					
I_{DD}	580			µA typ	
	850		850	A max	
I_{GND}	480			µA typ	
	700		700	µA max	
I_{SS}	100			µA typ	
	150		150	µA max	
Fault Mode					V_S = ±60 V
I_{DD}	630			µA typ	
	850		850	A max	
I_{GND}	405			µA typ	
	600		600	µA max	
I_{SS}	210			µA typ	
	290		290	µA max	

SPECIFICATIONS

CONTINUOUS CURRENT PER CHANNEL, SX OR DX, TWO CHANNELS ON

Table 6.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					
θ_{JA} = 170°C/W	80	56	38	mA max	V_S = analog signal range[1]

[1] The analog signal range for each supply range is given in Table 2 to Table 5.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Value
V_{DD} to V_{SS}	7 V
V_{DD} to GND	−0.3 V to +7 V
V_{SS} to GND	−3.5 V to +0.3 V
Sx to GND	−60 V to +60 V
Sx to V_{DD} or V_{SS}	67 V
Sx to Dx	67 V
Dx[1]	V_{SS} − 0.7 V to V_{DD} + 0.7 V or 30 mA, whichever occurs first
Digital Inputs	GND − 0.7 V to +6 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pin	255 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pin	Data + 15%[2]
Fault Trip Frequency[3]	1 kHz
Digital Output	GND − 0.7 V to +6 V or 30 mA, whichever occurs first
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb-Free	As per JEDEC J-STD-020

1 Overvoltages at the D1 and D2 pins are clamped by internal diodes. Limit current to the maximum ratings given.

2 See Table 6.

3 Each fault trip causes a short duration peak current. Limit the fault trip frequency to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 8. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-10-16	170	58.2	°C/W

1 Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADG7421F

Table 9. ADG7421F, 10-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM[1]	±3	2
FICDM	±1.250	C3

1 This is the HBM for the input/output port to supplies, the input/output port to input/output port, and for all other pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

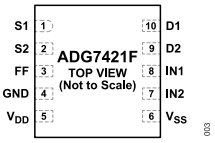


Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	S1	Overvoltage Protected Source Terminal. The S1 pin can be an input or an output.
2	S2	Overvoltage Protected Source Terminal. The S2 pin can be an input or an output.
3	FF	Fault Flag Digital Output. The FF pin is an open-drain output that requires an external pull-up resistor. This digital output pulls low when a fault condition occurs on either the S1 or S2 input.
4	GND	Ground (0 V) Reference.
5	V_{DD}	Most Positive Power Supply Potential.
6	V_{SS}	Most Negative Power Supply Potential.
7	IN2	Logic Control Input.
8	IN1	Logic Control Input.
9	D2	Drain Terminal. The D2 pin can be an input or an output.
10	D1	Drain Terminal. The D1 pin can be an input or an output.

TYPICAL PERFORMANCE CHARACTERISTICS

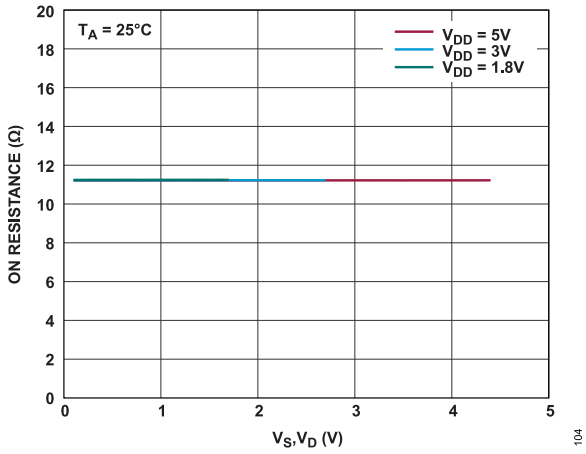


Figure 3. On Resistance as a Function of V_S, V_D (Single Supply)

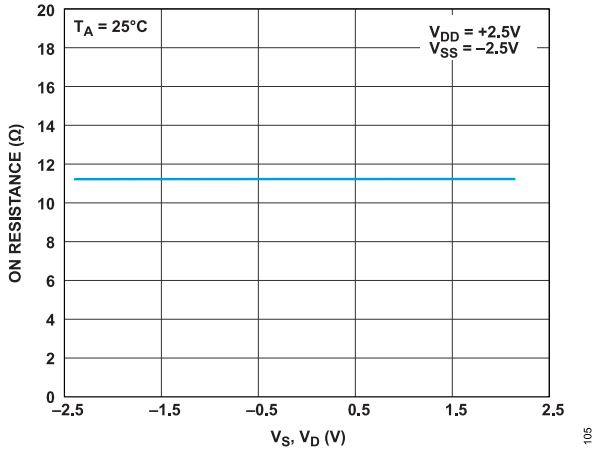


Figure 4. On Resistance as a Function of V_S, V_D (2.5 V Dual Supply)

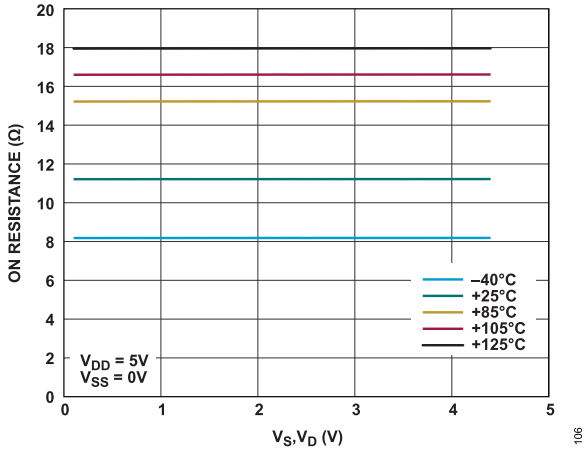


Figure 5. On Resistance as a Function of V_S, V_D for Different Temperatures, 5 V Single Supply

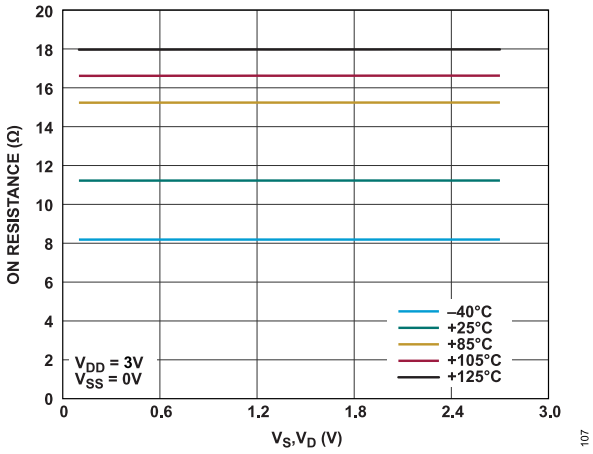


Figure 6. On Resistance as a Function of V_S, V_D for Different Temperatures, 3 V Single Supply

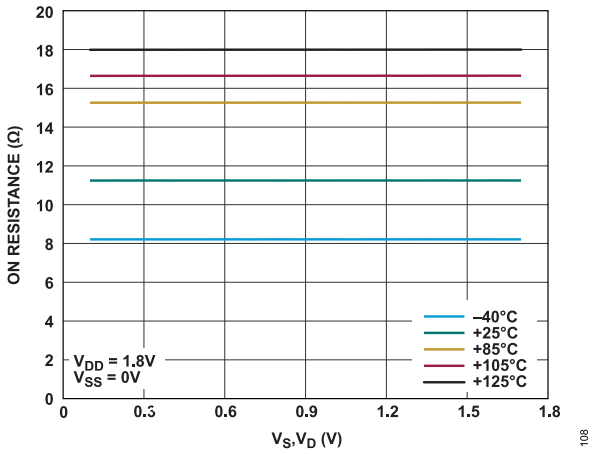


Figure 7. On Resistance as a Function of V_S, V_D for Different Temperatures, 1.8 V Single Supply

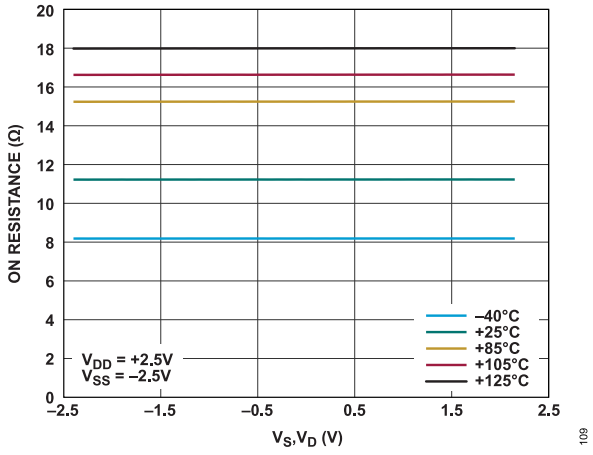


Figure 8. On Resistance as a Function of V_S, V_D for Different Temperatures, 2.5 V Dual Supply

TYPICAL PERFORMANCE CHARACTERISTICS

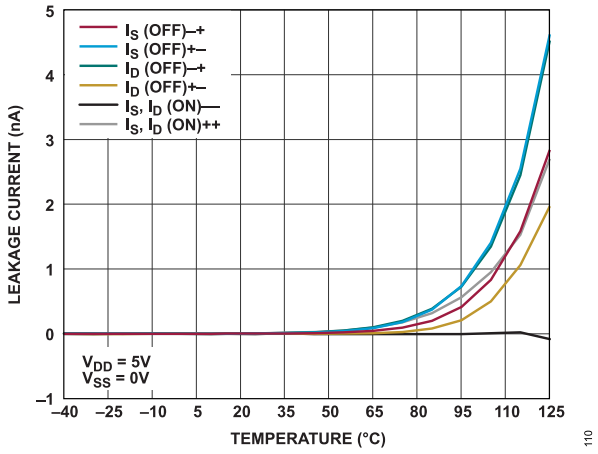


Figure 9. Leakage Current vs. Temperature, 5 V Single Supply

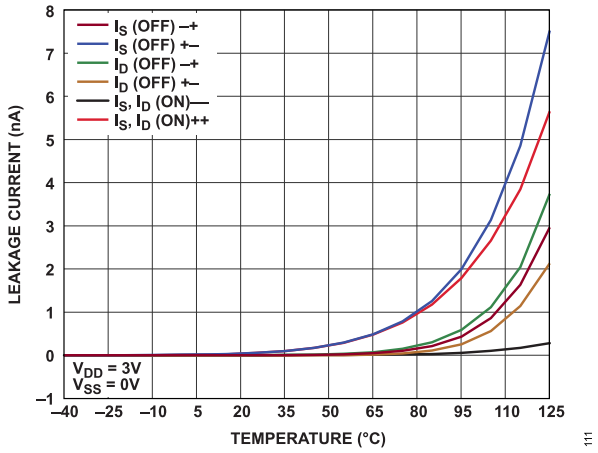


Figure 10. Leakage Current vs. Temperature, 3 V Single Supply

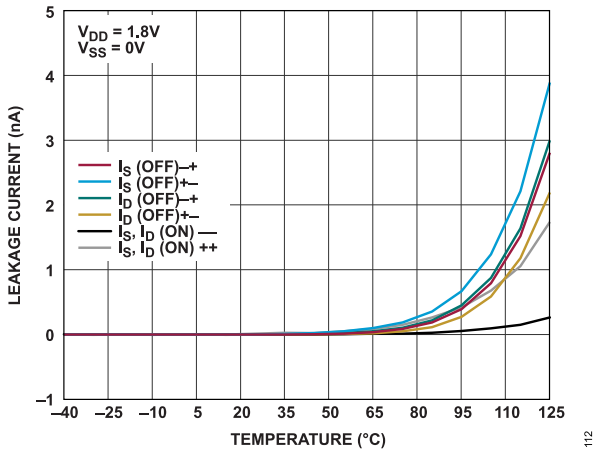


Figure 11. Leakage Current vs. Temperature, 1.8 V Single Supply

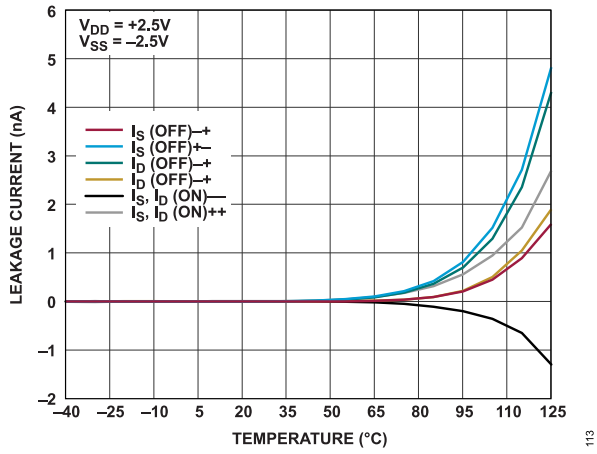


Figure 12. Leakage Current vs. Temperature, 2.5 V Dual Supply

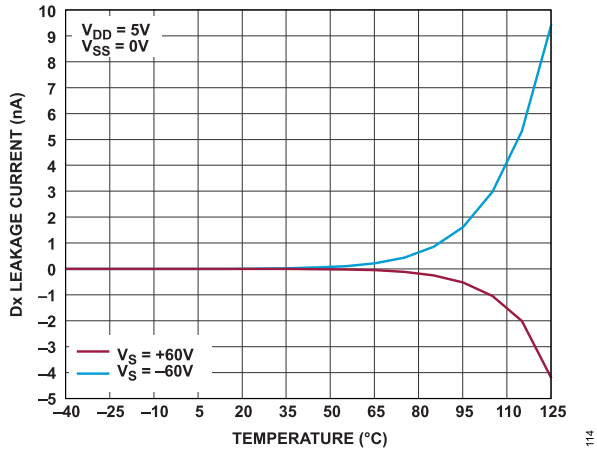


Figure 13. Dx Leakage Current vs. Temperature During Overvoltage, 5 V Single Supply

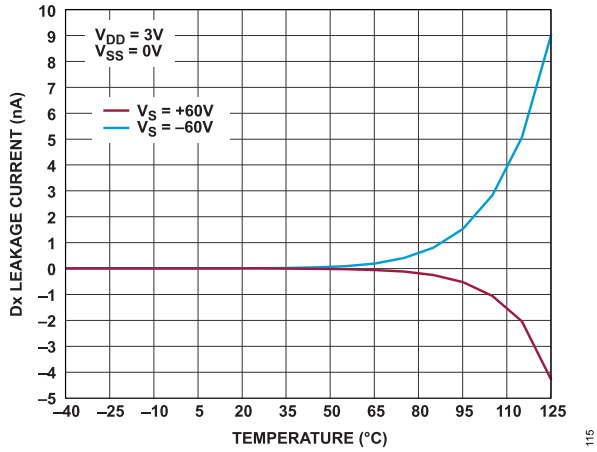


Figure 14. Dx Leakage Current vs. Temperature During Overvoltage, 3 V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

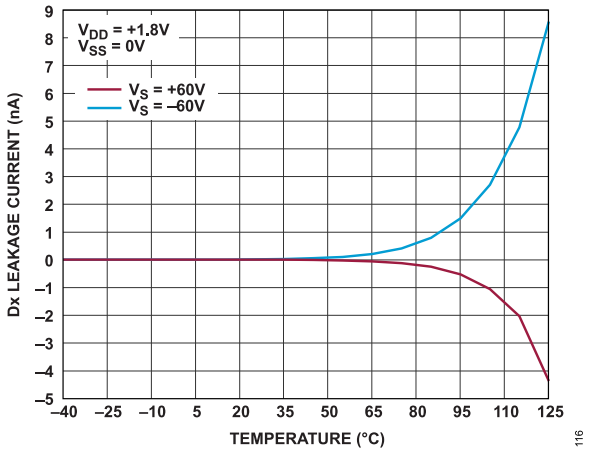


Figure 15. Dx Leakage Current vs. Temperature During Overvoltage, 1.8 V Single Supply

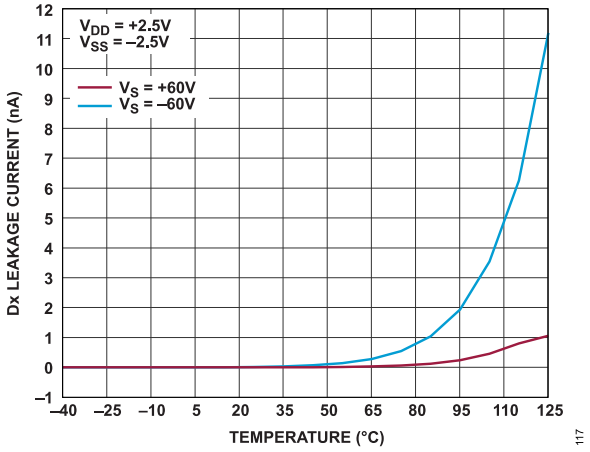


Figure 16. Dx Leakage Current vs. Temperature During Overvoltage, 2.5 V Dual Supply

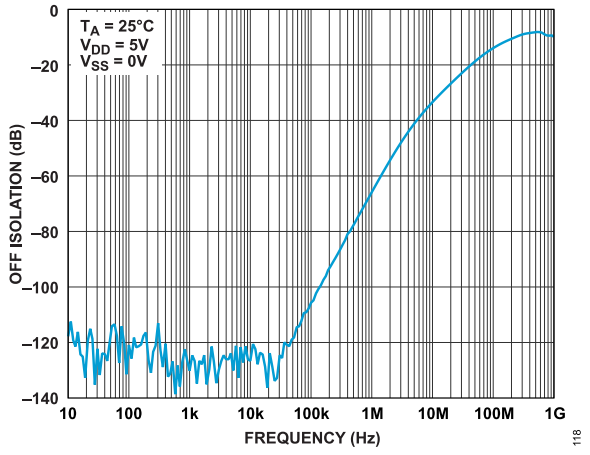


Figure 17. Off Isolation vs. Frequency, 5 V Single Supply

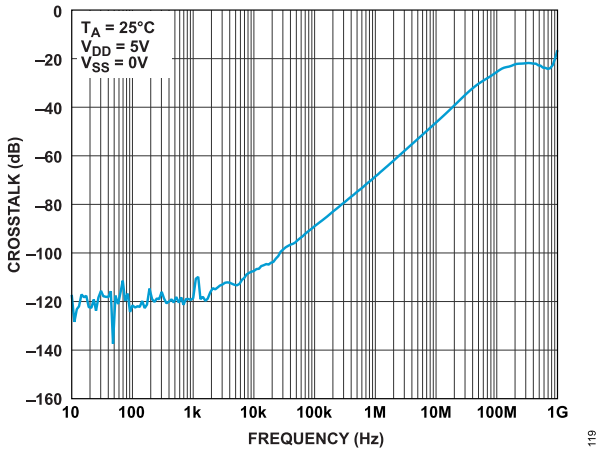


Figure 18. Crosstalk vs. Frequency, 5 V Single Supply

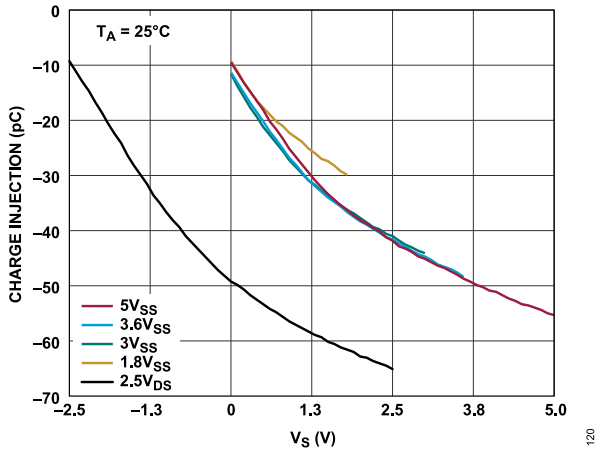


Figure 19. Charge Injection vs. V_S

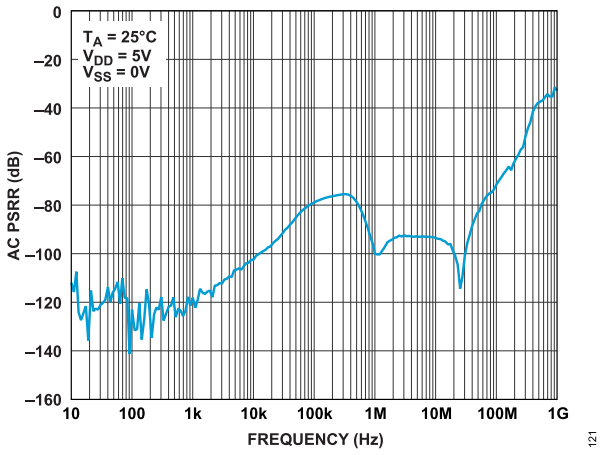


Figure 20. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, 5 V Single Supply

TYPICAL PERFORMANCE CHARACTERISTICS

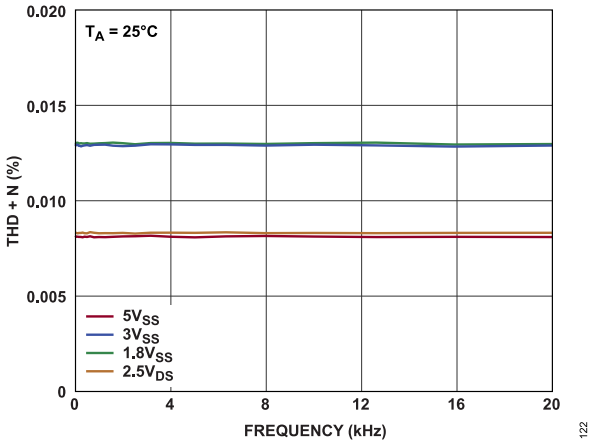


Figure 21. THD + N vs. Frequency

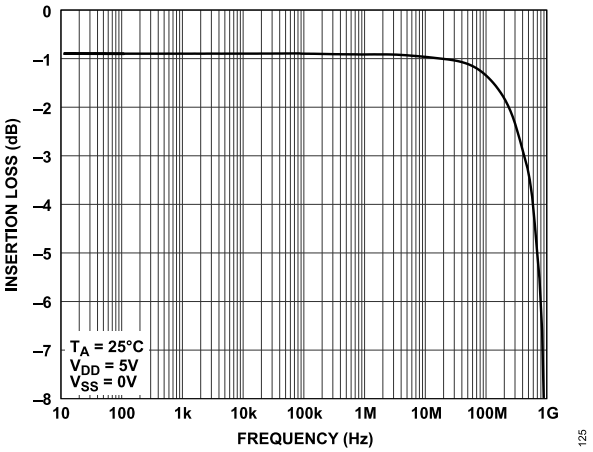


Figure 24. Insertion Loss vs. Frequency

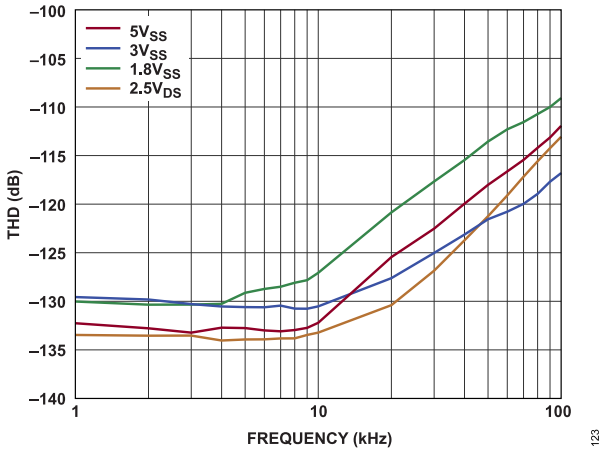


Figure 22. THD vs. Frequency

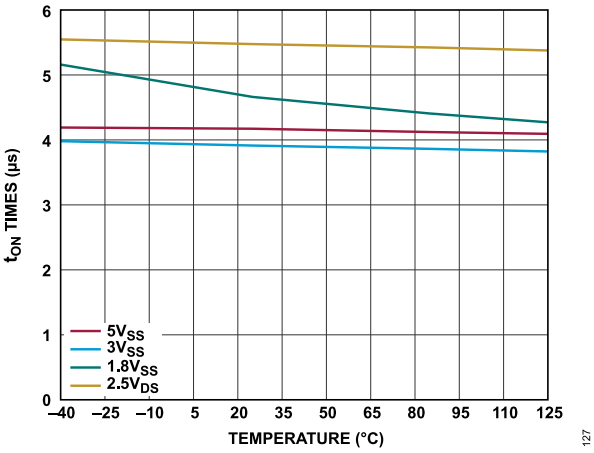


Figure 25. t_{ON} Times vs. Temperature for Various Supplies

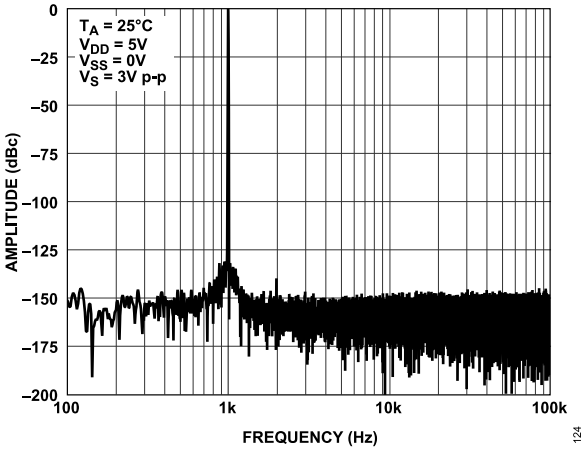


Figure 23. THD FFT

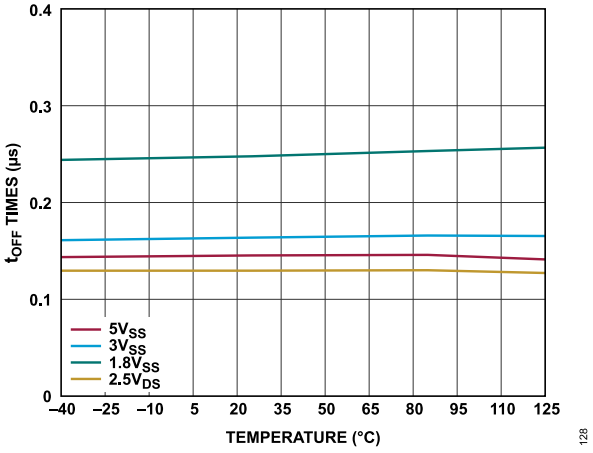


Figure 26. t_{OFF} Times vs. Temperature for Various Supplies

TYPICAL PERFORMANCE CHARACTERISTICS

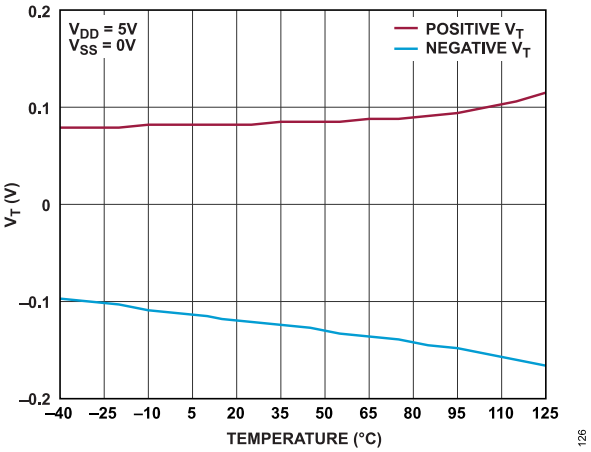


Figure 27. V_T vs. Temperature, 5 V Single Supply

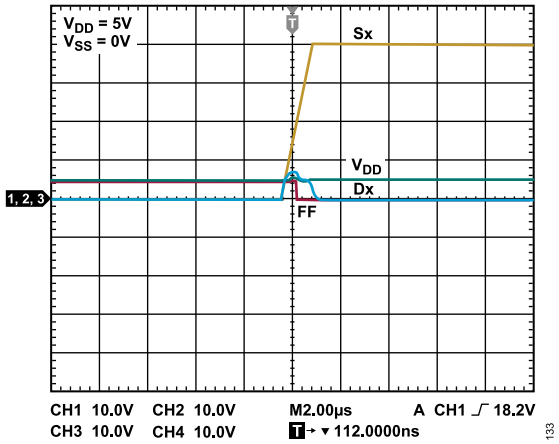


Figure 30. Drain Output Response to Positive Overvoltage

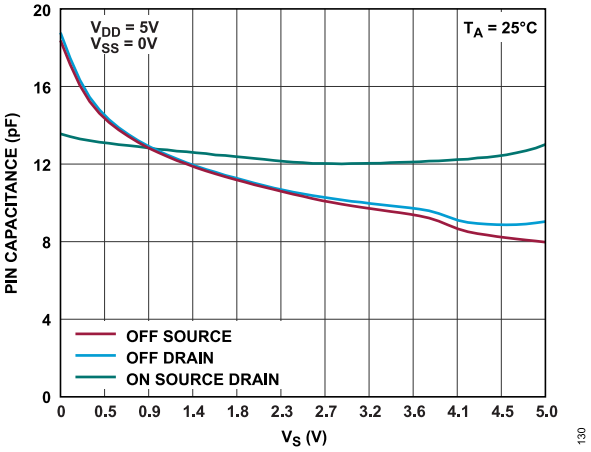


Figure 28. Pin Capacitance vs. V_S

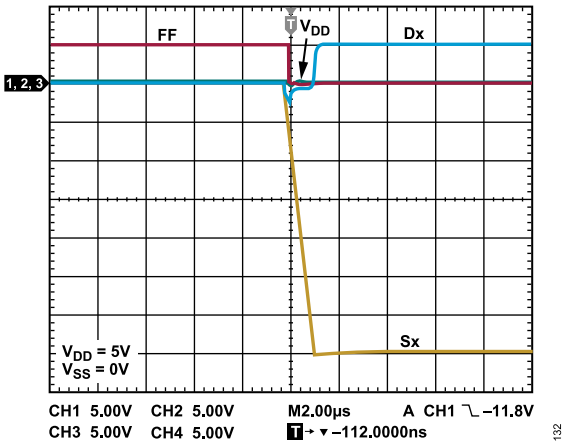


Figure 31. Drain Output Response to Negative Overvoltage

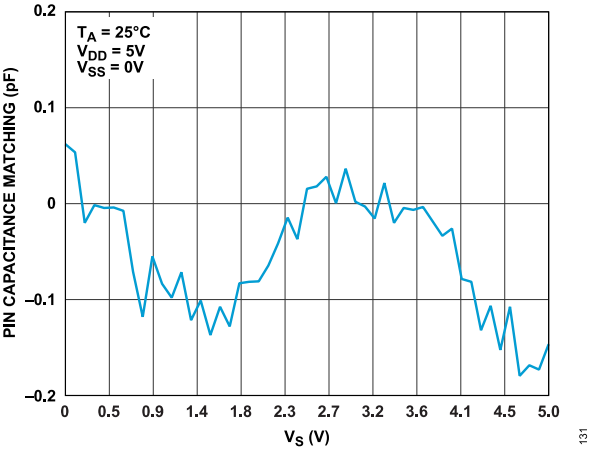


Figure 29. Pin Capacitance Matching vs. V_S

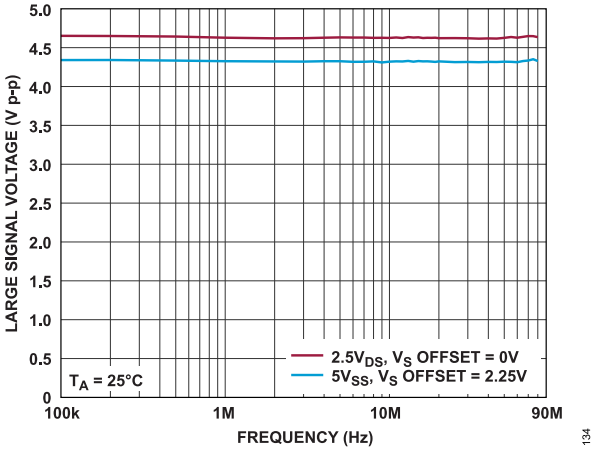


Figure 32. Large Voltage Signal Voltage vs. Frequency

TEST CIRCUITS

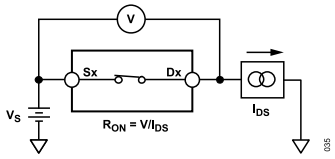


Figure 33. On Resistance (I_{DS} Is the Drain to Source Current)

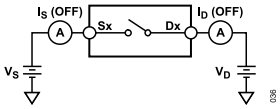


Figure 34. Off Leakage

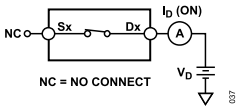


Figure 35. On Leakage

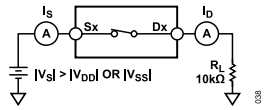


Figure 36. Switch Overvoltage Leakage

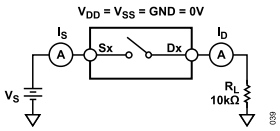


Figure 37. Switch Unpowered Leakage

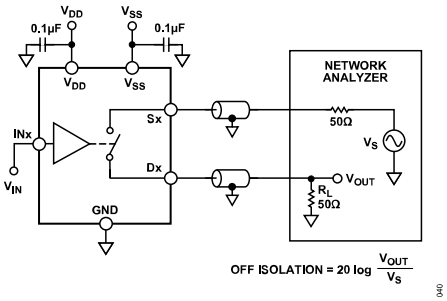
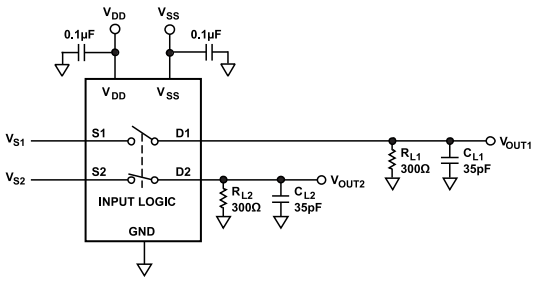


Figure 38. Off Isolation (V_{OUT} Is the Output Voltage)



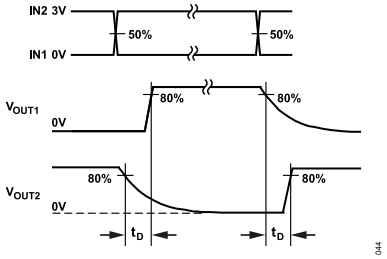


Figure 42. Break-Before-Make Time Delay, t_D

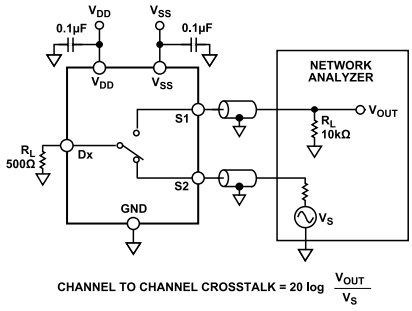


Figure 39. Channel to Channel Crosstalk

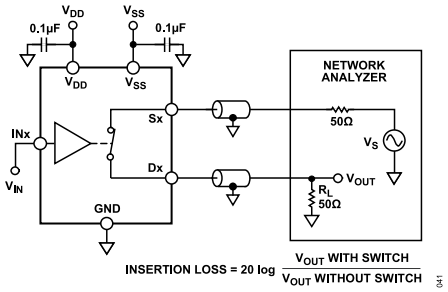


Figure 40. Bandwidth

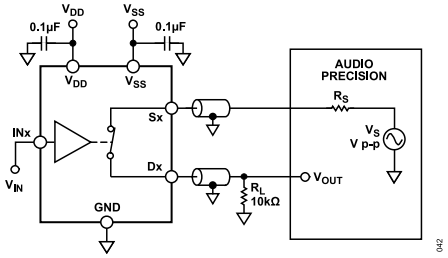


Figure 41. THD + N

TEST CIRCUITS

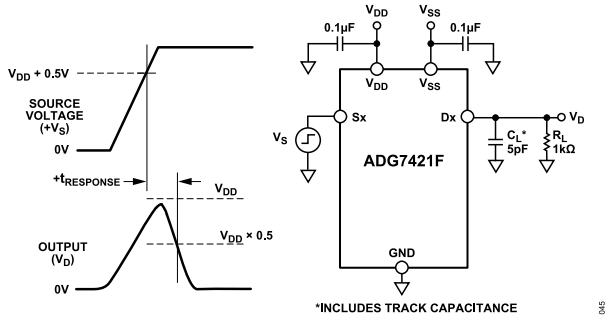


Figure 43. Overvoltage Response Time, $t_{RESPONSE}$

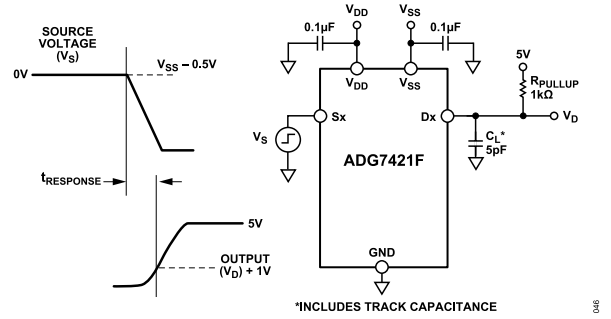


Figure 44. Negative Overvoltage Response Time, Single-Supply, $t_{RESPONSE}$

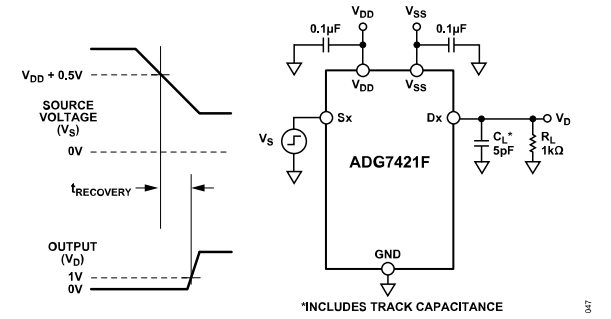


Figure 45. Overvoltage Recovery Time, $t_{RECOVERY}$

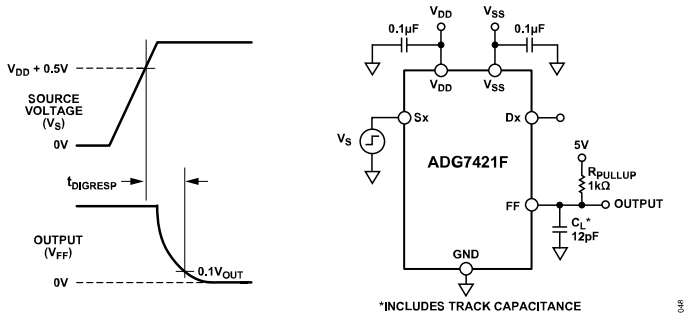


Figure 46. Interrupt Flag Response Time, $t_{DIGRESP}$ (V_{FF} Is the Fault Flag Voltage)

TEST CIRCUITS

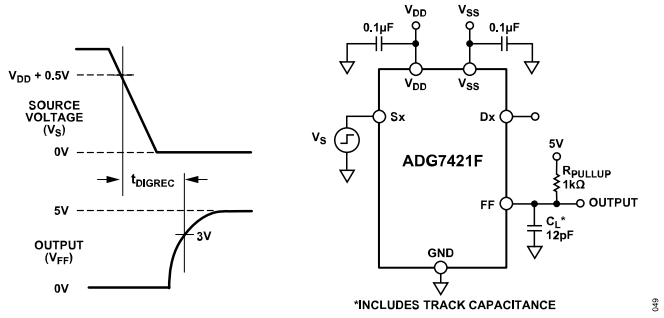


Figure 47. Interrupt Flag Recovery Time, t_{DIGREC}

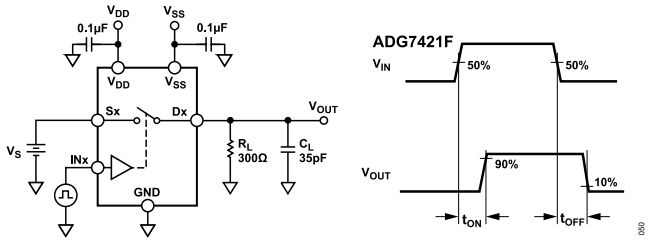


Figure 48. Switching Times, t_{ON} and t_{OFF}

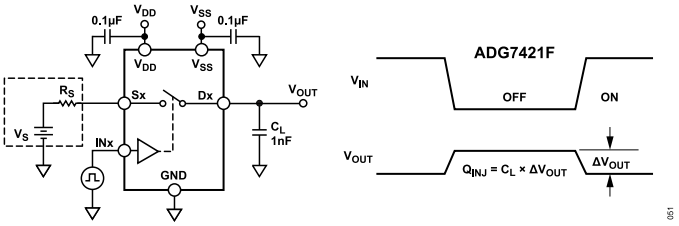


Figure 49. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on the Dx pins and the Sx pins, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

$R_{FLAT\ (ON)}$

$R_{FLAT\ (ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch Dx pin capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch Sx pin capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON}

t_{ON} represents the delay between applying the digital control input and the output switching on (see Figure 48).

t_{OFF}

t_{OFF} represents the delay between applying the digital control input and the output switching off (see Figure 48).

$t_{DIGRESP}$

$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}

t_{DIGREC} is the time required for the FF pin to return high, measured with respect to voltage on the Sx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$

$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RECOVERY}$

$t_{RECOVERY}$ represents the delay between an overvoltage on the Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

−3 dB Bandwidth

−3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

TERMINOLOGY

THD + N

THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

V_T

V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 27).

THEORY OF OPERATION

SWITCH ARCHITECTURE

The ADG7421F consists of two switch channels of N channel diffused metal-oxide semiconductor (DMOS) transistors. This construction provides excellent R_{ON} performance in a small area. The ADG7421F operates as a standard switch when input signals within the analog signal range are applied. For example, the on resistance is 12 Ω typically, and the INx pins control when the switches open or close.

Additional internal circuitry enables the switches to detect overvoltage inputs by comparing the voltage on both the S1 and S2 pins with the V_{DD} and V_{SS} pins. A signal is considered overvoltage when the signal exceeds the supply voltages by V_T. V_T is typically 0.1 V but can change over temperature. See Figure 27 to see the change in V_T with the operating temperature.

When an overvoltage condition is detected on either the S1 or S2 pins, the switch automatically opens regardless of the digital logic state (INx). The S1 to D1 and S2 to D2 pins become high impedance and ensure that no current flows through the switches. In Figure 30, the voltage on the Dx pin follows the voltage on the Sx pins until the main channel switch turns off completely, and the drain voltage discharges through the load. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the Dx pins.

The maximum voltage that can be applied to any source input is +60 V or −60 V. During overvoltage conditions, the leakage current into and out of the Sx pins is 120 µA typical and only 30 nA maximum for the Dx pins. This limit protects the switches and connected circuitry from overstresses and restricts the current drawn from the signal source.

ESD Performance

The ADG7421F has an ESD rating of 3 kV for the HBM.

The Dx pins have ESD protection diodes to the rails and the voltage at these pins must not exceed the supply voltage. The Sx pins have specialized ESD protection that allows the signal voltage to reach ±60 V regardless of the supply voltage level. See Figure 50 for the switch channel overview.

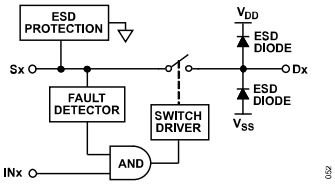


Figure 50. Switch Channel and Control Function

Trench Isolation

In the ADG7421F, an insulating oxide layer (trench) is placed between the N channel DMOS (NDMOS) and the P channel DMOS (PDMOS) transistors in the circuit. Parasitic junctions that occur between the transistors in the junction isolated switches are eliminated, and the result is a switch that is latch-up immune under all circumstances. These devices pass the JESD78D latch-up test.

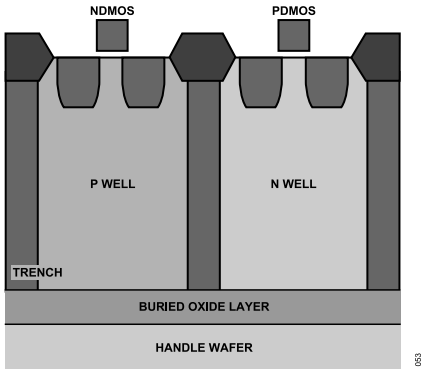


Figure 51. Trench Isolation

OVERVOLTAGE FAULT PROTECTION

When the voltage at the Sx inputs exceeds V_{DD} or V_{SS} by V_T, the switches turn off or, if the device is unpowered, the switches remain off. Both switch inputs remain high impedance regardless of the digital input state or the load resistance, and the output acts as a virtual open circuit. Signal levels up to +60 V and −60 V are blocked in both the powered and unpowered condition.

Power-On Protection

To activate the switches, the three following conditions must be met:

- The minimum supply operating conditions in Table 1.
- The input signal must be within the analog signal range.
- The digital logic control input, INx, is on.

When the switches are on, signal levels within the analog signal range are passed.

When the voltage on either of the Sx pins exceeds V_{DD} or V_{SS} by V_T, the switches respond by turning off. The absolute input voltage limits are −60 V and +60 V. The switches remain off until the V_S voltage at the Sx pins returns to within the analog signal range.

When powered by the 5 V single supply, the positive overvoltage response time ($t_{RESPONSE}$) is typically 1.2 µs, and $t_{RECOVERY}$ is 7.6 µs. These values vary with different supply voltage and output load conditions.

Exceeding ±60 V on either the Sx inputs may damage the ESD protection circuitry on the ADG7421F.

Power-Off Protection

When no power supplies are present, the switches remain in an off state and the switch inputs are high impedance. This state

THEORY OF OPERATION

ensures that no current flows and prevents damage to the switches or downstream circuitry. The switch outputs are open circuit.

The switches remain off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A 0 V GND reference must always be present to ensure proper operation. Signal levels of up to ±60 V are blocked when the switches are powered off.

Overvoltage Interrupt Flag

The voltages on the Sx inputs of the ADG7421F are continuously monitored, and the open-drain output pin, FF, indicates the fault state.

The voltage on the FF pin indicates if either of the Sx input pins is experiencing a fault condition. The FF pin is an open-drain output that requires an external pull-up resistor. The output of the FF pin is high impedance when both the Sx pins are within the normal operating range. If the voltage of either Sx pin exceeds the supply voltage (V_{DD} or V_{SS}) by V_T, the FF output provides a low impedance path to GND.

APPLICATIONS INFORMATION

The ADG7421F overvoltage protected switches provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments where overvoltage signals can be present, and the system must remain operational after an overvoltage occurs.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required on both V_{DD} and V_{SS} to GND.

The ADG7421F can operate with bipolar supplies between ±1.8 V and ±2.5 V. Note that the V_{DD} and V_{SS} supplies do not have to be symmetrical, but the supply voltage range must not exceed 5.5 V. The ADG7421F can also operate with single supplies between 1.8 V and 5.5 V with V_{SS} connected to GND.

The ADG7421F is fully specified at the +5 V, +3 V , +1.8 V, and ±2.5 V supply ranges.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a unipolar power solution is shown in Figure 52. The ADP162 ultralow quiescent current, 150 mA, CMOS linear regulator generates a positive supply rail for the ADG7421F amplifier and/or a precision converter in a typical signal chain.

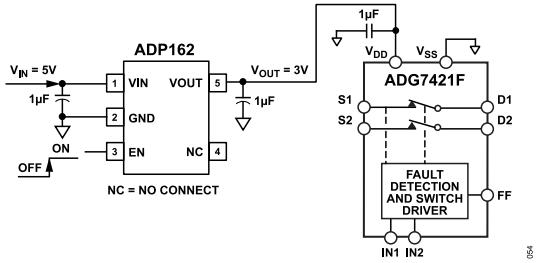


Figure 52. Power Solution

POWER SUPPLY SEQUENCING PROTECTION

When the device is off, the switch channels remain open and the signals from −60 V to +60 V can be applied without damaging the device. The switch channels only close when the supplies are connected, a suitable digital control signal is placed on the INx pin, and the signal is within the normal operating range. Note that placing the ADG7421F between external connectors and sensitive components offers protection in systems where a signal is presented to the S1 or S2 pin before the supply voltages are available.

SIGNAL RANGE

The ADG7421F switches have overvoltage detection circuitry on the S1 and S2 pins that compares the voltage levels with V_{DD} and V_{SS}. To protect downstream circuitry from overvoltages, supply the ADG7421F with voltages that match the intended signal range. The ADG7421F uses an NDMOS only architecture, and to achieve a near rail-to-rail signal range, an internal charge pump is used. The internal charge pump frequency is 20 MHz. A signal that exceeds the supply rail by V_T is then blocked. This signal block offers protection to both the device and any downstream circuitry. To avoid any false trips, the analog signal range is reduced slightly inside the supply voltages, V_{DD} and V_{SS}. Table 11 shows the signal range for the specified voltage supply ranges.

Table 11. Signal Range for Specified Voltage Supply Ranges

Power Supply	Signal Range
5 V Single Supply	V_{SS} + 0.1 V to V_{DD} – 0.55 V
3 V Single Supply	V_{SS} + 0.1 V to V_{DD} – 0.25 V
1.8 V Single Supply	V_{SS} + 0.1 V to V_{DD} – 0.1 V
2.5 V Dual Supply	V_{SS} + 0.1 V to V_{DD} – 0.35 V

INTELLIGENT FAULT DETECTION

The ADG7421F digital output pin (FF) can interface with a microprocessor or control system and be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which the device connects.

The control system can use the digital interrupt to start a variety of actions, such as the following:

- Initiating investigation into the source of the overvoltage fault
- Shutting down critical systems in response to the overvoltage
- Data recorders marking data during these events as unreliable or out of specification

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG7421F powers on and that all input voltages are within the normal operating range before initiating operation. The FF pin is an open drain that requires an external pull-up resistor, typically 1 kΩ, which allows signals to be combined into a single interrupt for larger modules that contain multiple devices.

SHORT DURATION FAULT CURRENT

When a fault voltage is present on either S1 or S2, the switch channel opens within typically 1.2 µs. During this short duration, the internal diodes on the drain side of the switch, shown in Figure 53, starts to clamp the voltage on the Dx pins until the switch is fully open. These internal diodes shunt the majority of the short duration current to the power supply. As the voltage on the Dx pin stabilizes, there may be some residual current allowed to flow from the ADG7421F into a connected device.

Figure 54 is a measurement of the current that flows out of the ADG7421F and into external diodes. The external diodes in Figure 53 are used to represent the internal ESD protection diodes that are usually present on the input of a downstream device in a signal chain (for example, an ADC or an amplifier).

APPLICATIONS INFORMATION

Before the switch opens, the majority of the short duration fault current that flows during a fault event flows through the internal diodes to the supplies (shown in Figure 53 as I_1). The remaining current, I_2 (approximately 20 mA), flows out of the switch drain pin and through the succeeding external diodes that represent the next device in the signal chain.

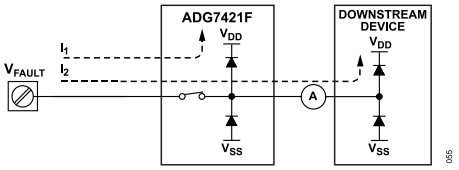


Figure 53. Fault Current Test Circuit

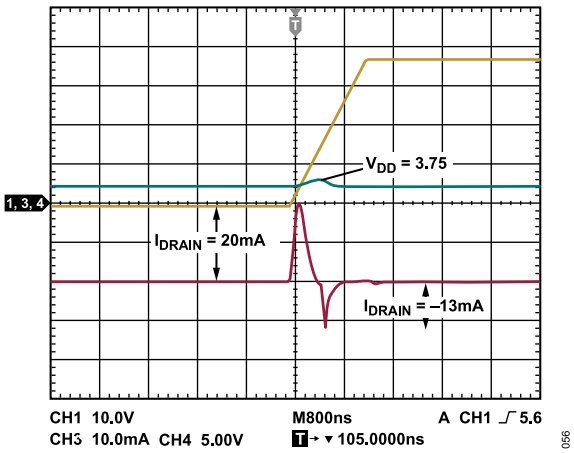


Figure 54. Fault Current Measurement

Depending on the nature of the fault and the power supply setup, the short duration current that flows through the internal diodes on the ADG7421F may cause a variation on supply voltage. If this variation is an issue, use larger decoupling capacitors (10 µF) on the supply to stabilize V_{DD} and V_{SS}.

THERMOCOUPLE INPUT PROTECTION

Figure 55 shows a typical configuration to protect thermocouple inputs to the AD7124-4. The signal from a thermocouple is small. Therefore, the thermocouple voltage must be suitably biased to stay within the specified signal range of the ADG7421F. The AD7124-4 includes an internal bias voltage generator to set the bias voltage to $AV_{DD}/2$, which is available on any input channel. For a dual supply solution, the thermocouple voltages can be centered around ground.

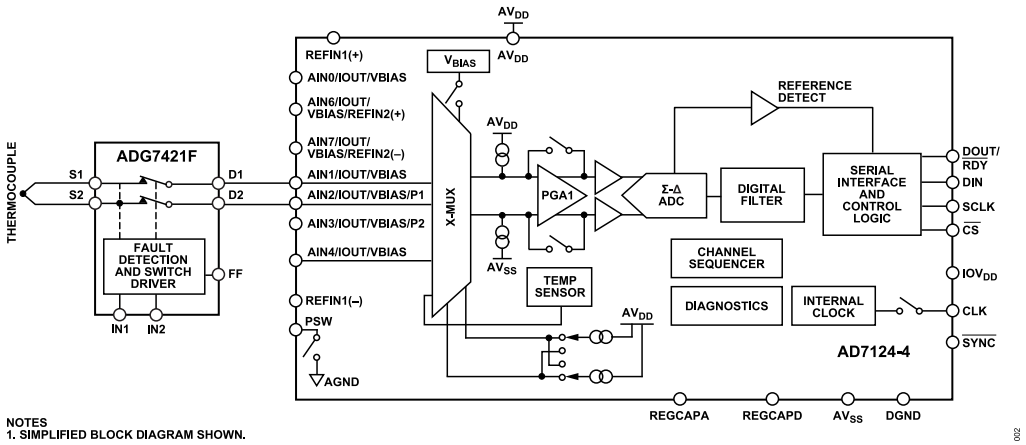


Figure 55. Thermocouple Input Configuration

APPLICATIONS INFORMATION

RTD INPUT PROTECTION

The ADG7421F can be used to protect the inputs for 2-, 3-, or 4-wire RTD configurations. Figure 56 shows one possible configuration diagram to protect a 4-wire RTD input to the AD7124-4 ADC. For 4-wire RTD configurations, two ADG7421F devices are required to protect the four system input nodes accessible by the user.

In this configuration, the voltage developed across the RTD device is sensed by the two ADC input channels, AIN1 and AIN2. These ADC input channels are connected to the external environment through two channels of the ADG7421F to provide protection against overvoltages up to ±60 V.

The excitation current required for the RTD is provided by the AD7124-4 on the AIN0/IOUT/VBIAS pin. The excitation current flows from AIN0/IOUT/VBIAS through one ADG7421F channel, through the RTD device, through a second ADG7421F channel, and finally to GND via the reference resistor, R_{REF}, and the headroom resistor, $R_{HEADROOM}$. The reference resistor in this setup is used to provide a ratiometric measurement. This reference resistor generates the ADC reference voltage from the excitation current so that any variation in excitation current does not affect the accuracy of the measurement.

The headroom resistor is required because the reference input buffers on the ADC may require some headroom and the switch is not fully rail to rail.

For more information on thermocouple and RTD measurements using the AD7124-4 ADC, see the AD7124-4 data sheet.

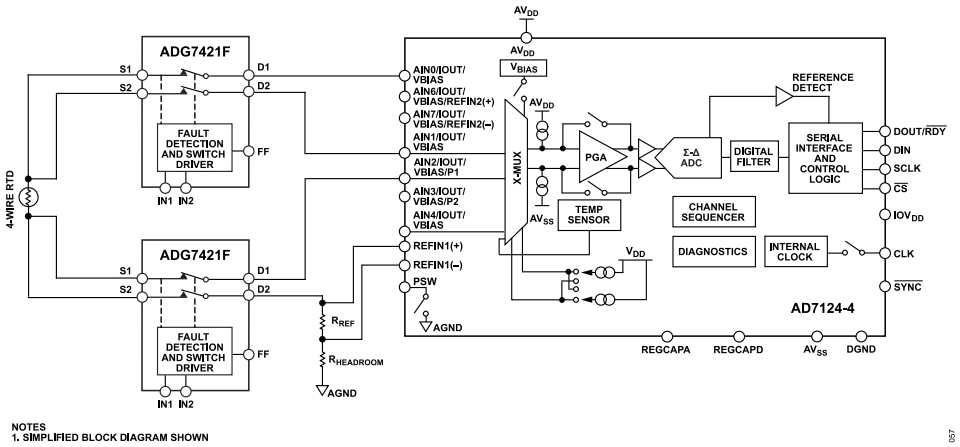


Figure 56. RTD Input Configuration

APPLICATIONS INFORMATION

SWITCHES IN A KNOWN STATE

If no digital inputs are present on the switch control lines (INx), the switches remain in an off state, which prevents unwanted signals passing through the switches.

HIGH VOLTAGE SUPPRESSION

To achieve protection from high voltage transients, such as IEC 61000-4-2 ESD, IEC 61000-4-4 electrical fast transient (EFT), and IEC61000-4-5 surge, implement the circuit shown in Figure 57 by using a discrete resistors and a transient voltage suppression (TVS) device.

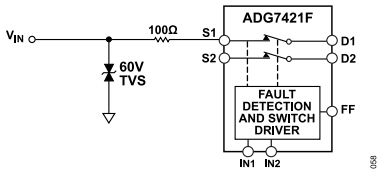


Figure 57. High Voltage Transient Protection

Table 12 details the results achieved by using the discrete protection circuit shown in Figure 57. To replicate the harshest environments, the surge test was performed by striking the Sx pins directly through a 40 Ω resistor and a 0.5 µF capacitor coupling network. The EFT test was performed by zapping the Sx pins directly without any capacitive coupling through cables.

Table 12. High Voltage Transient Protection

IEC 61000-4 Transient	Protection Level (kV)
ESD (Contact)	±8
EFT	±4
Surge	±1