CMOS Low Power Dual 2:1 Mux/Demux USB 2.0 (480 Mbps)/USB 1.1 (12 Mbps)

FEATURES

USB 2.0 (480 Mbps) and USB 1.1 (12 Mbps) signal switching compliant
Tiny 10-lead 1.3 mm × 1.6 mm mini LFCSP package and 12-lead 3 mm × 3 mm LFCSP package
2.7 V to 3.6 V single-supply operation
Typical power consumption: <0.1 µW
RoHS compliant

APPLICATIONS

USB 2.0 signal switching circuits
Cellular phones
PDAs
MP3 players
Battery-powered systems
Headphone switching
Audio and video signal routing
Communications systems

FUNCTIONAL BLOCK DIAGRAM

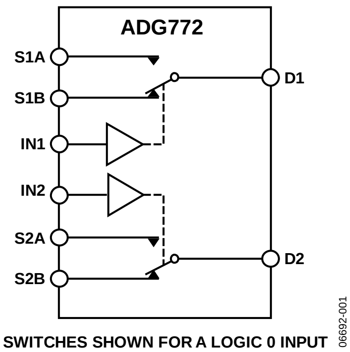

Figure 1.

GENERAL DESCRIPTION

The ADG772 is a low voltage CMOS device that contains two independently selectable single-pole, double throw (SPDT) switches. It is designed as a general-purpose switch and can be used for routing both USB 1.1 and USB 2.0 signals.

This device offers a data rate of 1260 Mbps, making the device suitable for high frequency data switching. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG772 exhibits break-before-make switching action.

The ADG772 is available in a 12-lead LFCSP and a 10-lead mini LFCSP. These packages make the ADG772 the ideal solution for space-constrained applications.

PRODUCT HIGHLIGHTS

1. 1.6 mm × 1.3 mm mini LFCSP package.
2. USB 1.1 (12 Mbps) and USB 2.0 (480 Mbps) compliant.
3. Single 2.7 V to 3.6 V operation.
4. 1.8 V logic compatible.
5. RoHS compliant.

Rev. C
Document Feedback

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8/07—Revision 0: Initial Version

Specifications

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	6.7		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_{DS} = 10 mA; see Figure 21
		8.8	Ω max	
On-Resistance Match	0.04		Ω typ	V_{DD} = 2.7 V, V_S = 1.5 V, I_{DS} = 10 mA
Between Channels (ΔR_{ON})		0.2	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	3.3		Ω typ	V_{DD} = 2.7 V, V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		3.6	Ω max	
LEAKAGE CURRENTS				V_{DD} = 3.6 V
Source Off Leakage I_S (Off)	±0.2		nA typ	V_S = 0.6 V/3.3 V, V_D = 3.3 V/0.6 V; see Figure 22
Channel On Leakage I_D, I_S (On)	±0.2		nA typ	V_S = V_D = 0.6 V or 3.3 V; see Figure 23
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.35	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[1]				
t_{ON}	9		ns typ	R_L = 50 Ω, C_L = 35 pF
	12.5	13.5	ns max	V_S = 2 V; see Figure 24
t_{OFF}	6		ns typ	R_L = 50 Ω, C_L = 35 pF
	9.5	10	ns max	V_S = 2 V; see Figure 24
Propagation Delay	250		ps typ	R_L = 50 Ω, C_L = 35 pF
Propagation Delay Skew, t_{SKEW}	20		ps typ	R_L = 50 Ω, C_L = 35 pF
Break-Before-Make Time Delay (t_{BBM})	5		ns typ	R_L = 50 Ω, C_L = 35 pF
	3.4	2.9	ns min	V_{S1} = V_{S2} = 2 V; see Figure 25
Charge Injection	0.5		pC typ	V_D = 1.25 V, R_S = 0 Ω, C_L = 1 nF; see Figure 26
Off Isolation	73		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
Channel-to-Channel Crosstalk	−90		dB typ	S1A to S2A/S1B to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
	−80		dB typ	S1A to S1B/S2A to S2B; R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
−3 dB Bandwidth	630		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
Data Rate	1260		Mbps typ	R_L = 50 Ω, C_L = 5 pF; see Figure 30
C_S (Off)	2.4		pF typ	
C_D, C_S (On)	6.9		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.6 V
I_{DD}	0.006		µA typ	Digital inputs = 0 V or 3.6 V
		1	µA max	

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4.6 V
Analog Inputs,[1] Digital Inputs	−0.3 V to V_{DD} + 0.3 V or 10 mA, whichever occurs first
Peak Current, Pin S1A, Pin S2A, Pin D1, or Pin D2	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, Pin S1A, Pin S2A, Pin D1, or Pin D2	30 mA
Operating Temperature Industrial Range (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (4-Layer Board)	
10-Lead Mini LFCSP	131.6°C/W
12-Lead LFCSP	61°C/W
Pb-Free Temperature, Soldering, IR Reflow	
Peak Temperature	260(+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at the IN1, IN2, S1A, S2A, D1, or D2 pin are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

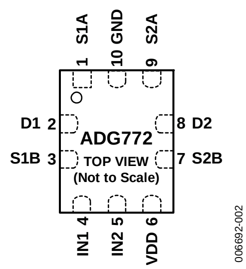
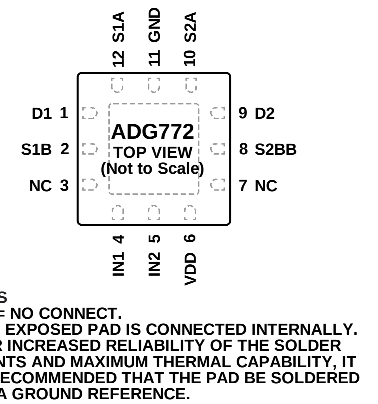


Figure 2. 10-Lead Mini LFCSP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO A GROUND REFERENCE.

Figure 3. 12-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.			
10-Lead Mini LFCSP	**12-Lead LFCSP**	**Mnemonic**	**Description**
1	12	S1A	Source Terminal. Can be an input or an output.
2	1	D1	Drain Terminal. Can be an input or an output.
3	2	S1B	Source Terminal. Can be an input or an output.
4	4	IN1	Logic Control Input. This pin controls Switch S1A and Switch S1B to D1.
5	5	IN2	Login Control Input. This pin controls Switch S2A and Switch S2B to D2.
6	6	VDD	Most Positive Power Supply Potential.
7	8	S2B	Source Terminal. Can be an input or an output.
8	9	D2	Drain Terminal. Can be an input or an output.
9	10	S2A	Source Terminal. Can be an input or an output.
10	11	GND	Ground (0 V) Reference.
Not applicable	3, 7	NC	No Connect.
Not applicable	13	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to a ground reference.

TRUTH TABLE

Table 4.

Logic (IN1 or IN2)	Switch A (S1A or S2A)	Switch B (S1B or S2B)
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

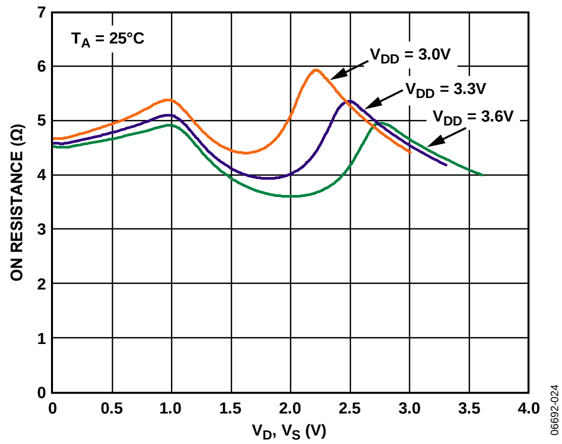


Figure 4. On Resistance vs. V_D, V_S; V_{DD} = 3.3 V ± 0.3 V

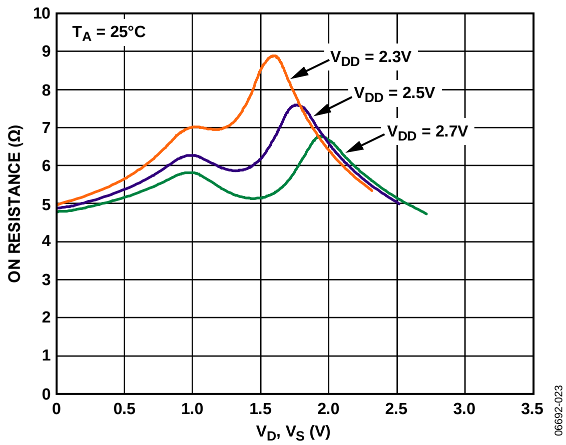


Figure 5. On Resistance vs. V_D, V_S; V_{DD} = 2.5 V ± 0.2 V

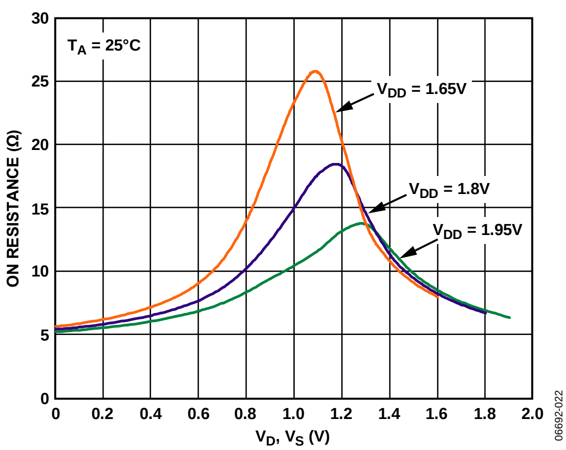


Figure 6. On Resistance vs. V_D, V_S; V_{DD} = 1.8 V ± 0.15 V

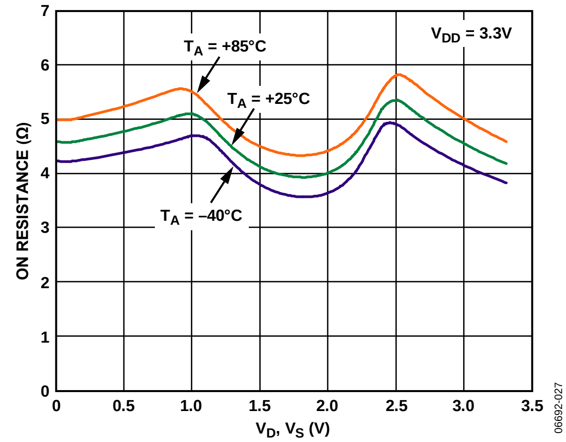


Figure 7. On Resistance vs. V_D, V_S for Different Temperatures; V_{DD} = 3.3 V

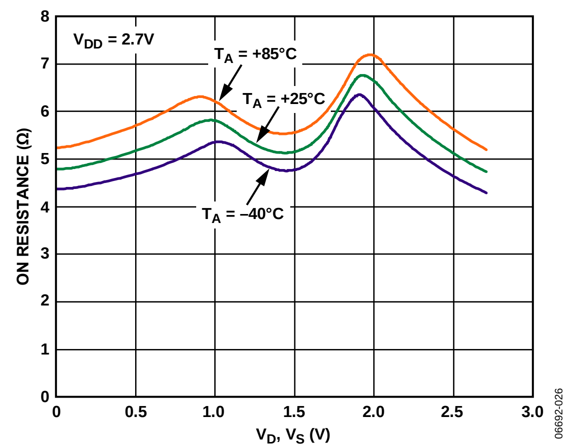


Figure 8. On Resistance vs. V_D, V_S for Different Temperatures; V_{DD} = 2.7 V

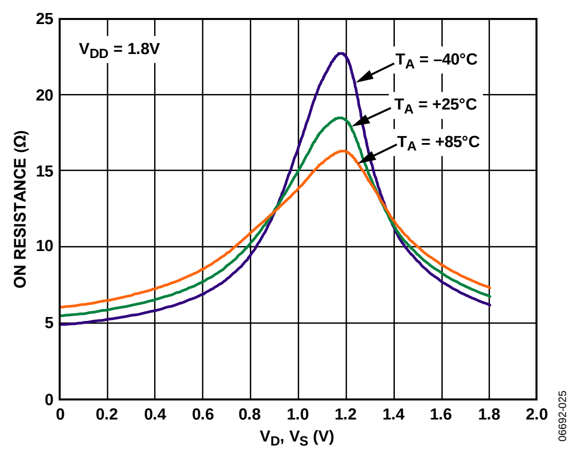


Figure 9. On Resistance vs. V_D, V_S for Different Temperatures; V_{DD} = 1.8 V

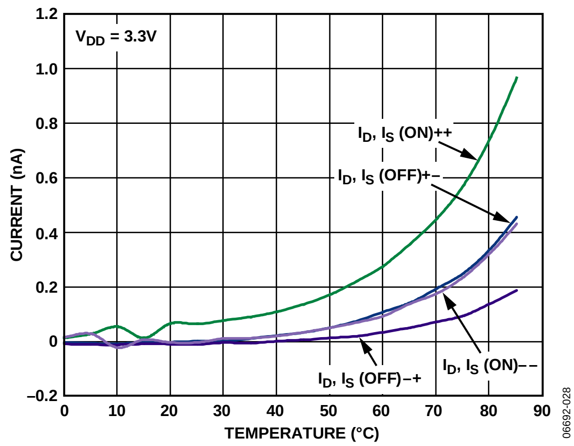


Figure 10. Leakage Current vs. Temperature; V_{DD} = 3.3 V

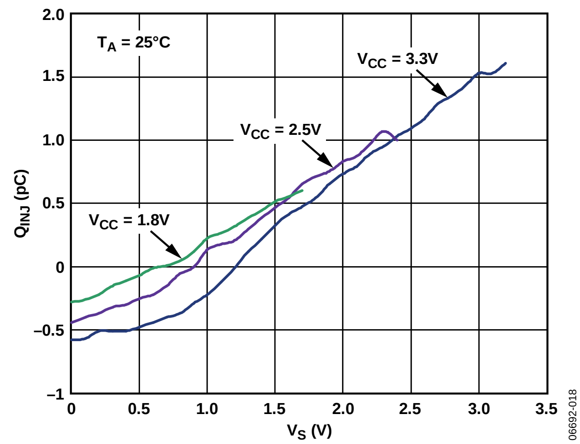


Figure 13. Charge Injection vs. Source Voltage

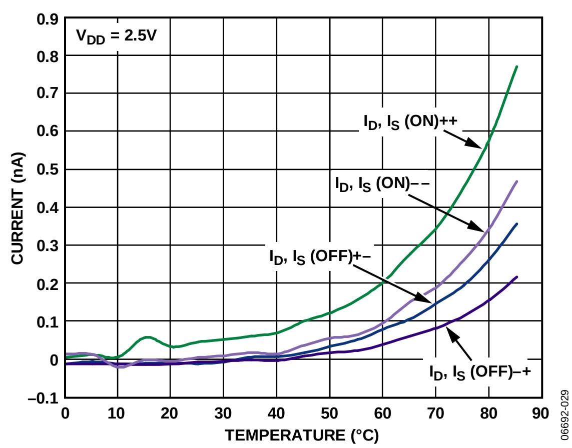


Figure 11. Leakage Current vs. Temperature; V_{DD} = 2.5 V

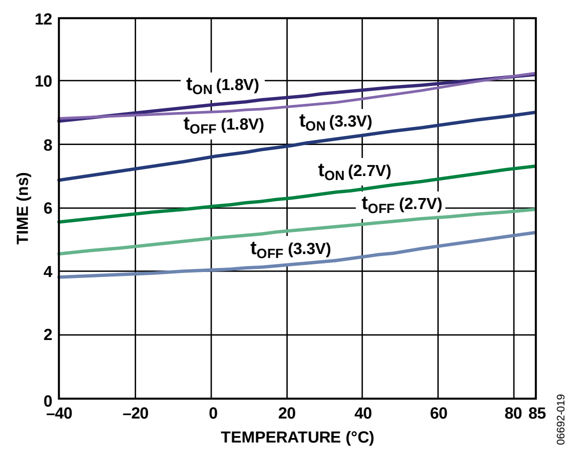


Figure 14. t_{ON}/t_{OFF} Times vs. Temperature

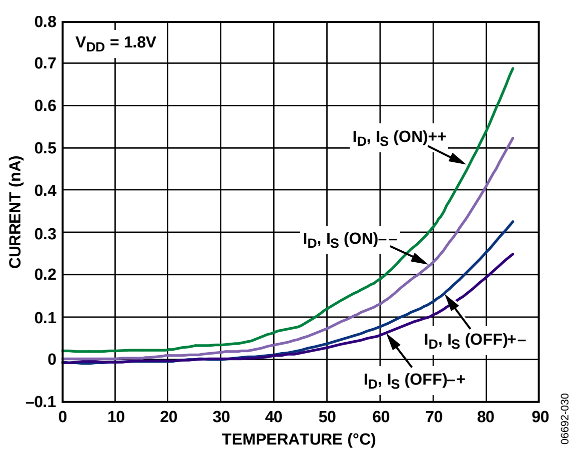


Figure 12. Leakage Current vs. Temperature; V_{DD} = 1.8 V

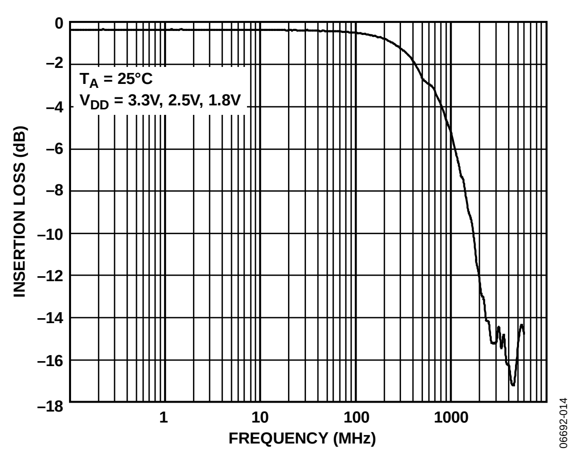


Figure 15. Bandwidth

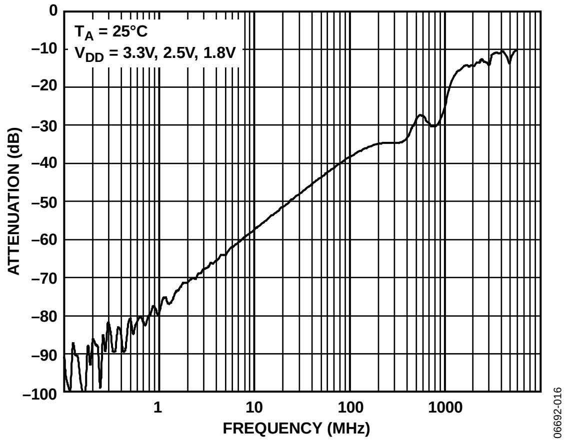


Figure 16. Off Isolation vs. Frequency

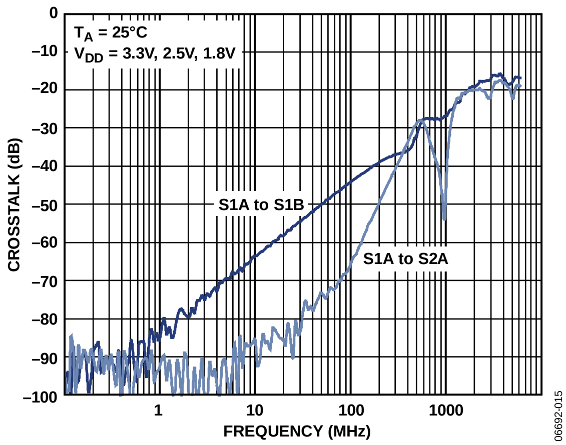


Figure 17. Crosstalk vs. Frequency

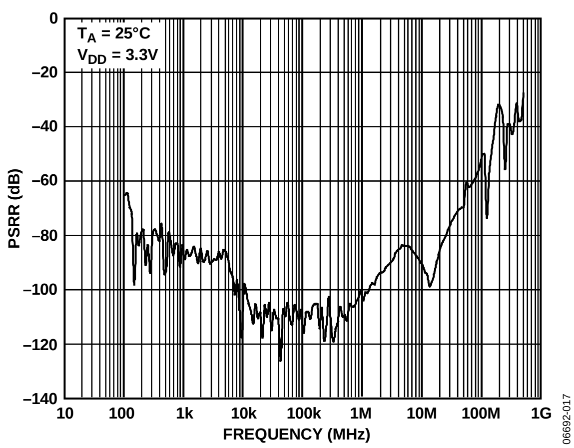


Figure 18. PSRR vs. Frequency

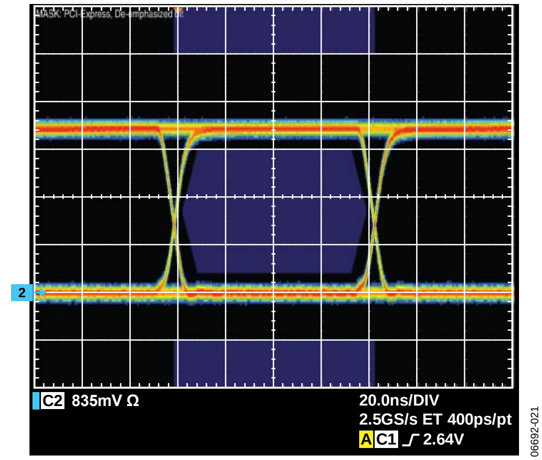


Figure 19. USB 1.1 Eye Diagram

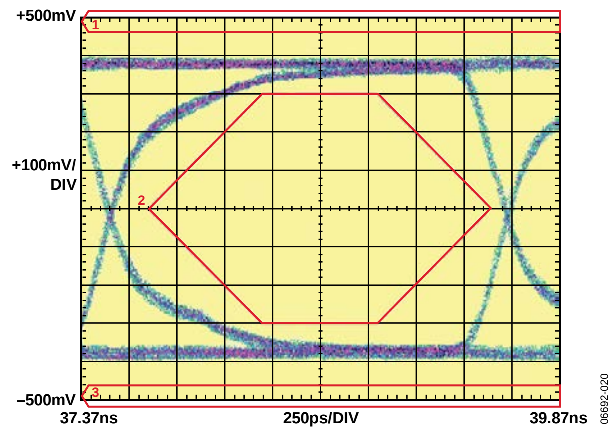


Figure 20. USB 2.0 Eye Diagram

TEST CIRCUITS

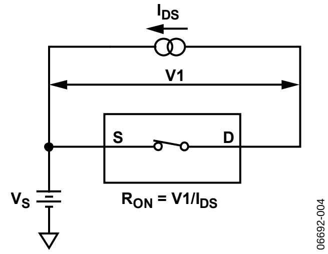


Figure 21. On Resistance

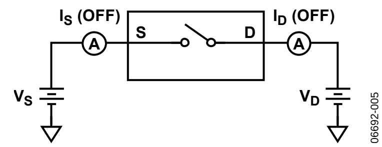


Figure 22. Off Leakage

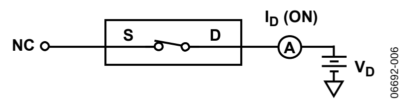


Figure 23. On Leakage

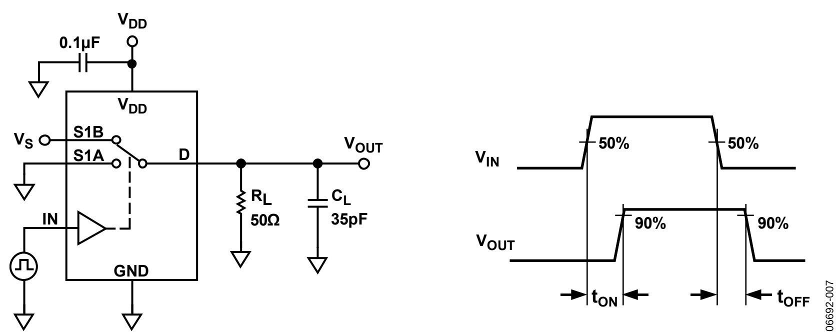


Figure 24. Switching Times, t_{ON}, t_{OFF}

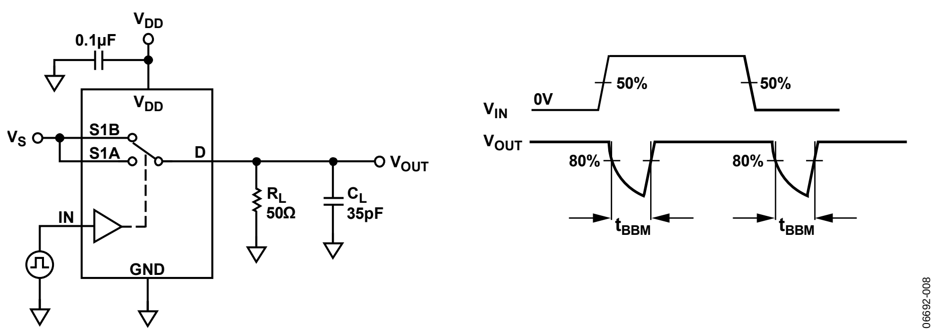


Figure 25. Break-Before-Make Time Delay, t_{BBM}

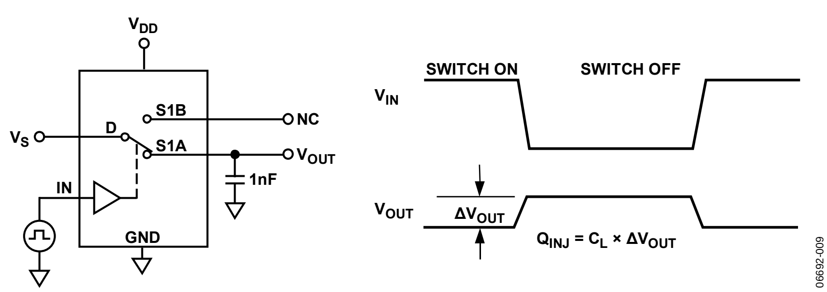


Figure 26. Charge Injection

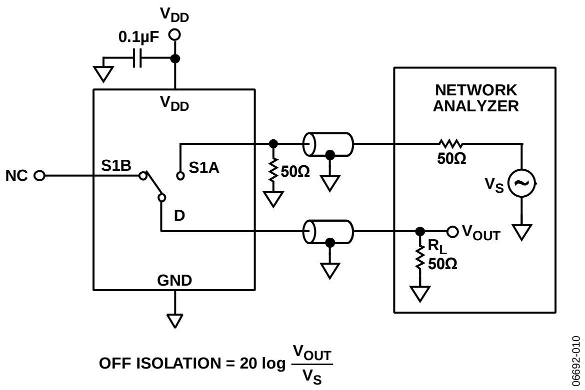


Figure 27. Off Isolation

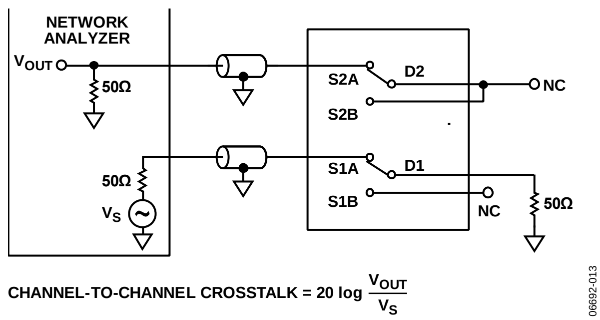


Figure 28. Channel-to-Channel Crosstalk (S1A to S2A)

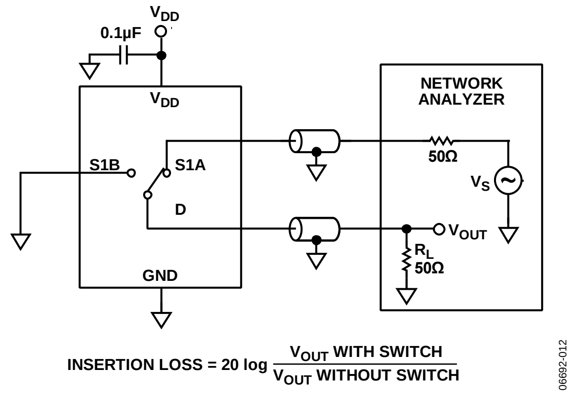


Figure 29. Channel-to-Channel Crosstalk (S1A to S1B)

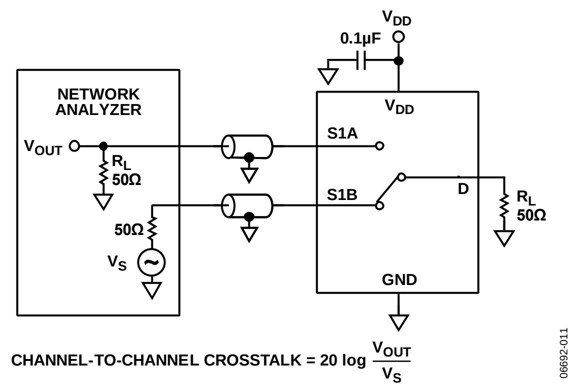


Figure 30. Bandwidth

TERMINOLOGY

I_{DD}
Positive supply current.

V_D,V_S
Analog voltage on Terminal D and Terminal S.

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

R_{FLAT} (On)
The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}
On resistance match between any two channels.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL},I_{INH}
Input current of the digital input.

C_S (Off)
Off switch source capacitance. Measured with reference to ground.

C_D (Off)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation
Measure of unwanted signal coupling through an off switch.

Crosstalk
Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

T_{SKEW}
The measure of the variation in propagation delay between each channel.