Evaluating the ADuM3195 Isolated Amplifier with Adjustable Gain and Single-Ended Output

FEATURES

- ADuM3195 isolated amplifier in a QSOP-16 package
- ADuM6028-5BRIZ isolated on-board power supply
- Maximum 1000 V DC pre-configured input
- Configurable for AC voltage input

EQUIPMENT NEEDED

- Power supply, 5 V DC ± 10%, 50 mA
- Adjustable DC voltage source, 0 to 1 kV
- 2 × DMM, 5½ digit

DOCUMENTS NEEDED

- ADuM3195 data sheet

GENERAL DESCRIPTION

The EVAL-ADuM3195EBZ is a compact isolated DC and AC (configurable) voltage monitoring board with an isolated on-board power supply to facilitate the setup and testing of the performance characteristics of the ADuM3195.

On the input side of the board (right-hand side), the high-voltage input connector P1 is pre-configured to accept up to 1 kV DC. The internal operational amplifier (op amp) on the input side is connected in a voltage-follower configuration. On the output side of the board (left-hand side), the overall output of the ADuM3195 is directly accessible on P6 (pre-configured) or can be first-order low-pass filtered by adding a resistor and capacitor. A single 5 V DC supply is sufficient to power both the input and output side of the board, while the optional power disable (PDIS) input can be used to disable the on-board isolated power supply in applications where low-power consumption is at a premium. Full details about the device are available in the ADuM3195 data sheet, which must be consulted when using the EVAL-ADuM3195EBZ.

EVALUATION BOARD PHOTOGRAPH

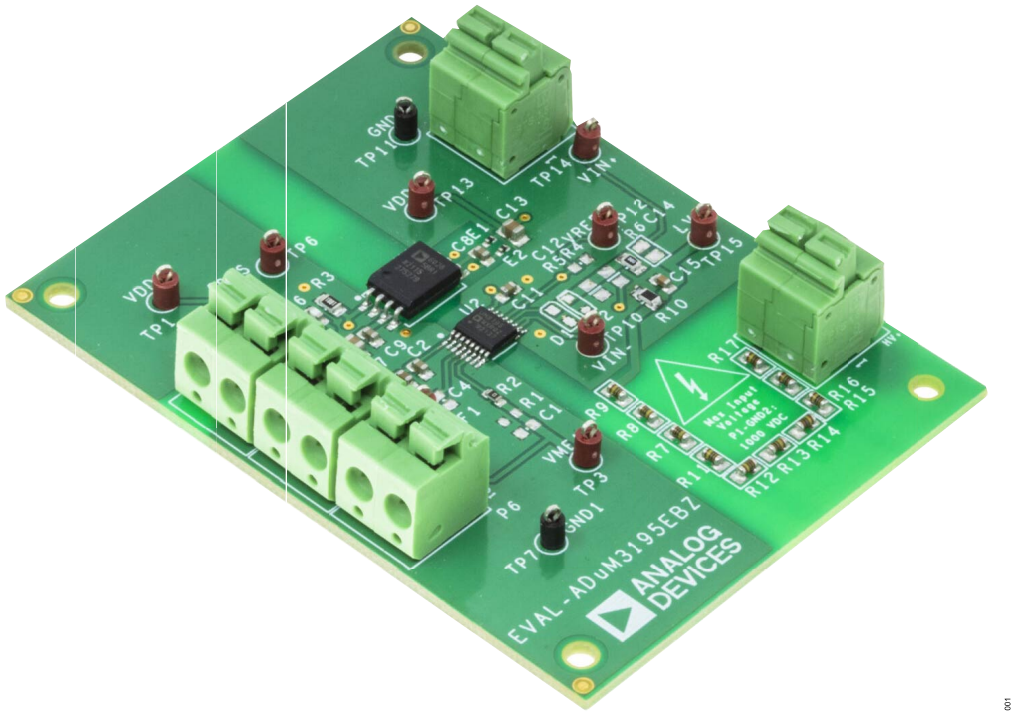

Figure 1. EVAL-ADuM3195EBZ

TABLE OF CONTENTS

REVISION HISTORY

4/2023—Revision 0: Initial Version

CONNECTORS

Figure 2 shows the locations of the push-in spring connectors for quick interfacing with the EVAL-ADuM3195EBZ and Table 1 provides the description for the connectors. Connectors are designed to take 14 to 26 American wire gauges (AWGs) wire stripped to approximately 8 mm.

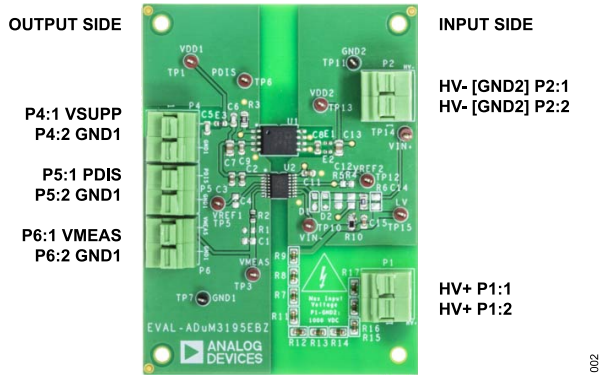

Figure 2. Location of Connectors

Table 1. Connectors List

Component	Net Name	Description
P1:1	HV+	Positive input of high-voltage divider
P1:2	HV+	Positive input of high-voltage divider
P2:1	HV−, GND2	Isolated power supply, output ground (right-hand side ground)
P2:2	HV−, GND2	Isolated power supply, output ground (right-hand side ground)
P4:1	VSUPP	+5 V DC input power supply (left-hand side)
P4:2	GND1	Power supply GND (left-hand side ground)
P5:1	PDIS	Disables the isolated power supply (input) R_{IN} = 1 kΩ Enable: Leave open Disable: Connect to VSUPP
P5:2	GND1	Power supply GND (left-hand side ground)
P6:1	VMEAS	Measured output voltage
P6:2	GND1	Power supply GND (left-hand side ground)

TEST POINTS

Test points are provided for measurement probes.

Table 2. Test Points

Pin	Net Name	Description
TP1	VDD1	Supply voltage (left-hand side) of isolated amplifier (U2:1)
TP3	VMEAS	Output of isolated amplifier, through R2
TP5	VREF1	Reference output voltage of isolated amplifier (left-hand side) (U2:4)
TP6	PDIS	Power-disable signal of isolated power supply (U1:1)
TP7	GND1	Isolated amplifier ground (left-hand side) (U2:2)

Table 2. Test Points (Continued)

Pin	Net Name	Description
TP10	VIN−	Inverting operational amplifier (op amp) input (U2:11), connected to op amp output (U2:10)
TP11	GND2	Isolated amplifier ground (right-hand side) (U2:9)
TP12	VREF2	Reference output voltage of op amp (right-hand side) (U2:13)
TP13	VDD2	Output of on-board isolated power supply feeding isolated amplifier (right-hand side) (U2:16)
TP14	VIN+	Noninverting op amp input (U2:12)
TP15	LV	Low-voltage end of user-configurable high-voltage divider

TEST SETUP

The EVAL-ADuM3195EBZ default configuration is capable of handling input voltages of up to 1000 V DC continuously. For such voltage levels, it is indispensable to secure the board on a dry, clean, and isolated surface, preferably using 15 mm nylon standoffs for extra clearance. The input side of the board refers to the noninverting input of the op amp (on the right-hand side of the isolation barrier), whereas the output side refers to the overall output of the isolated amplifier (on the left-hand side of the isolation barrier). The input and output side are fully isolated from each other but can be connected to the same GND to facilitate testing.

Use the following sequence to set up the EVAL-ADuM3195EBZ for evaluations up to 1000 V DC:

1. Secure the EVAL-ADuM3195EBZ on the workbench.
2. Connect a well-regulated low-noise 5 V DC power supply (current rating approximately 50 mA) to P4:1 (VSUPP) and P4:2 (GND1). Note that the power supply must not exceed the absolute maximum voltage ratings of the ADuM3195 during power cycling.
3. To measure the output voltage of the EVAL-ADuM3195EBZ, connect a digital multimeter (DMM) between P6:1 (VMEAS) and P6:2 (GND1).
4. In addition, the low-voltage (noninverting) input to the internal op amp (VIN+ = low voltage) and the output of the internal op amp (V_{OUT2} = VIN−) can be measured if required by connecting additional DMMs to TP15 (LV) and TP10 (VIN−), respectively (with reference to GND2). Note that the input resistance of the DMM poses an additional load on the input divider network of the EVAL-ADuM3195EBZ and therefore affects the accuracy of the divider ratio. Make sure that the DMM is set to high-impedance (R_{IN} > 10 MΩ). Although these are low-voltage connections, it is recommended to use the appropriate high-voltage cabling because of the proximity to the high-voltage input.
5. Switch on the 5 V DC power supply. The output current on the power supply must read I_{OUT} < 35 mA.
6. Connect a low-noise precision, high-voltage DC source (DC voltage calibrator) with its positive terminal to P1:1 (HV+) and its negative terminal to P2:1 (HV−, GND2). The voltage source must have a sufficient current rating of I_{OUT} > 3 mA. Use the appropriate high-voltage cabling for connecting the high-voltage DC source. Set the output voltage to 0 V DC and then turn the supply on to allow for a sufficient warmup time before starting to test the EVAL-ADuM3195EBZ.
7. The user can now analyze the performance of the ADuM3195 by varying the voltage at high-side input and record the voltage at low-side output P6:1.

CONFIGURATIONS

DC MEASUREMENT

The EVAL-ADuM3195EBZ default configuration is set up for a maximum input voltage of 1000 V DC through the high-voltage divider R7-R17. The ratio of the high-voltage divider can be calculated as:

$$V(LV)/V(HV+) = R10/(R10 + R_{HV}) \quad (1)$$

where the high-voltage input resistor (R_{HV}) = R7 + R8 + R9 + R11 + R12 + R13 + R14 + R15 + R16 + R17. (2)

R7 to R9 and R11 to R17 (1 MΩ each) are high-precision metal electrode leadless face (MELF) resistors. R10 is a high-accuracy resistor chosen so that a 1 kV DC input is translated into approximately 4.4 V DC on the divider output side. Modifications to the high-voltage divider must leave the high-voltage input unchanged to avoid the printed circuit board (PCB) area around them to be unnecessarily contaminated with flux residues. Resistor R10 can then be altered to adopt for input voltages lower than 1 kV DC. Choose resistor values such that U2:V_{IN+} (at TP14) never exceeds the system maximum value (VDD2 minimum – 0.6 V) under any operating conditions.

The following are two examples of full-scale input voltage range, assuming VDD2 minimum = 5 V DC (board default):

- Maximum 1000 V DC input at P1:1 pin (default setup)
  - R10 = 44.2 kΩ (full-scale input voltage: 1136.22 V)
- Maximum 500 V DC input at pin P1:1
  - R10 = 80.60 kΩ (full-scale input voltage: 623.09 V)

CONFIGURATIONS

AC MEASUREMENT

In addition to the DC measurement, the EVAL-ADuM3195EBZ performs AC input measurements by using an AC coupling circuit for the internal op amp of the ADuM3195. The components of the AC coupling circuit (C14, R4, and R5) are shown in Figure 3 but are not populated in the default configuration.

Use the following sequence to set up the EVAL-ADuM3195EBZ for AC measurement:

1. Unsolder R6.
2. Replace R10 as needed (refer to DC Measurement for details).
3. Populate C14, R4, and R5.
4. Follow the guidelines in Test Setup.

The values of C14, R4, and R5 shown in Figure 2, with R10 = 44.2 kΩ, were set up so that a 230 V (rms)/50 Hz sinusoidal input is translated into a sinusoidal waveform oscillating between 1 V (minimum) and 3 V (maximum) on the low-voltage side of the divider (1 V peak amplitude).

In the default configuration, C15 compensates the stray capacitance present across the input high voltage resistors string. Therefore, the AC-coupled circuit transfer function is:

$$\frac{V(VIN+)(j\omega)}{V(HV+)(j\omega)}$$

$$= \frac{j\,\omega\,R10\,R4\,R5\,C14}{j\omega(R_{HV}R4R5 + R10R4R5 + R_{HV}R10R4 + R_{HV}R10R5) + R_{HV}R4 + R10R4 + R10R5 + R_{HV}R5} \quad (3)$$

This is a high-pass filter with an origin-zero and a pole. At high frequencies with respect to the pole, the phase-shift is zero and the gain becomes simply:

$$A = \frac{V(VIN+)}{V(HV+)} = \frac{R10\,R4\,R5}{R_{HV}R4R5 + R10R4R5 + R_{HV}R10R4 + R_{HV}R10R5} \quad (4)$$

Use the values of the resistors in (4) to determine the required gain at the target frequency. In the default design, the gain is A = 1/($\sqrt{2}$ 230). For the high-frequency assumption to be true, the pole frequency (f_p) must be much lower than the target frequency. In the default case, the design was done so that the pole used is placed 100 times lower than 50 Hz.

$$f_p = \frac{R_{HV}R4 + R10R4 + R10R5 + R_{HV}R5}{2\pi C14(R_{HV}R4R5 + R10R4R5 + R_{HV}R10R4 + R_{HV}R10R5)} \quad (5)$$

In addition, the relationship between R4 and R5 (fed from VREF2, the reference voltage of the ADuM3195) sets up the offset voltage of the output waveform as per:

$$V_{OFFSET} = (VREF2\ R5)/(R4 + R5) \quad (6)$$

In the default board configuration, the desired output waveform has its average value at V_{OFFSET} = 2 V.

All values must be chosen such that U2:V_{IN+} (at TP14) never exceeds the system maximum or minimum values under any operating conditions.

The following are two examples of full-scale input voltage range, assuming VDD2 minimum = 5 V DC (board default):

- Maximum 230 V (rms) at 50 Hz input at Pin P1:1, to a 1 V (peak) output waveform with 2 V DC offset (default)
  - R10 = 44.2 kΩ, C1 = 3.3 nF, VREF2 = 2.5 V
  - R5 = 4 R4, from (6)
  - A = 0.003074
  - R4 = 127 kΩ and R5 = 510 kΩ, from (4)
  - C14 > 100 × 21.9 nF, from (5), so C14 = 2.2 µF
- Maximum 700 V (rms) at 50 Hz input at Pin P1:1, to a 1 V (peak) output waveform with 2 V DC offset
  - R10 = 44.2 kΩ, C1 = 3.3 nF, VREF2 = 2.5 V
  - R5 = 4 R4, from (6)
  - A = 0.00101015
  - R4 = 16.4 kΩ and R5 = 65.5 kΩ, from (4)
  - C14 > 100 × 55.7 nF, from (5), so C14 = 5.6 µF

USAGE INFORMATION

USEFUL INPUT RANGE

Configure the input divider so that the maximum U2:V_{IN+} always stays approximately 0% to 5% below (VDD2 minimum − 0.6 V), even if this requires dividing U2:V_{OUT2} to adopt for the input range of a downstream analog-to-digital converter (ADC). This ensures the full usage of the input range of the ADuM3195.

DIVIDER RESISTORS

An additional adjustment of R10 can reduce any nominal divider error further, if needed. However, in a voltage monitoring system, a downstream ADC, or processor takes care of the final calibration and adjustment of the gain and offset, thus eliminating the need for lower divider errors. However, the divider resistors must be chosen for the lowest possible temperature coefficients to ensure stable divider accuracy over the full required temperature range.

INPUT PROTECTION DIODES

In applications where accidental reverse input voltages are expected, a reverse input protection diode can be used. This is accomplished by Diode D1. In addition, a Zener Diode D2 can be used to limit the maximum voltage at the low-voltage input U2:V_{IN+}. However, it is to be noted that the leakage current through Diode D1 and Diode D2 can impair divider accuracy and linearity. Therefore, it is recommended to select D1and D2 for low reverse leakage current to avoid that effect. D1 and D2 are shown in the schematic in Figure 3 but are not populated in the default configuration.

EVALUATION BOARD SCHEMATIC AND ARTWORK

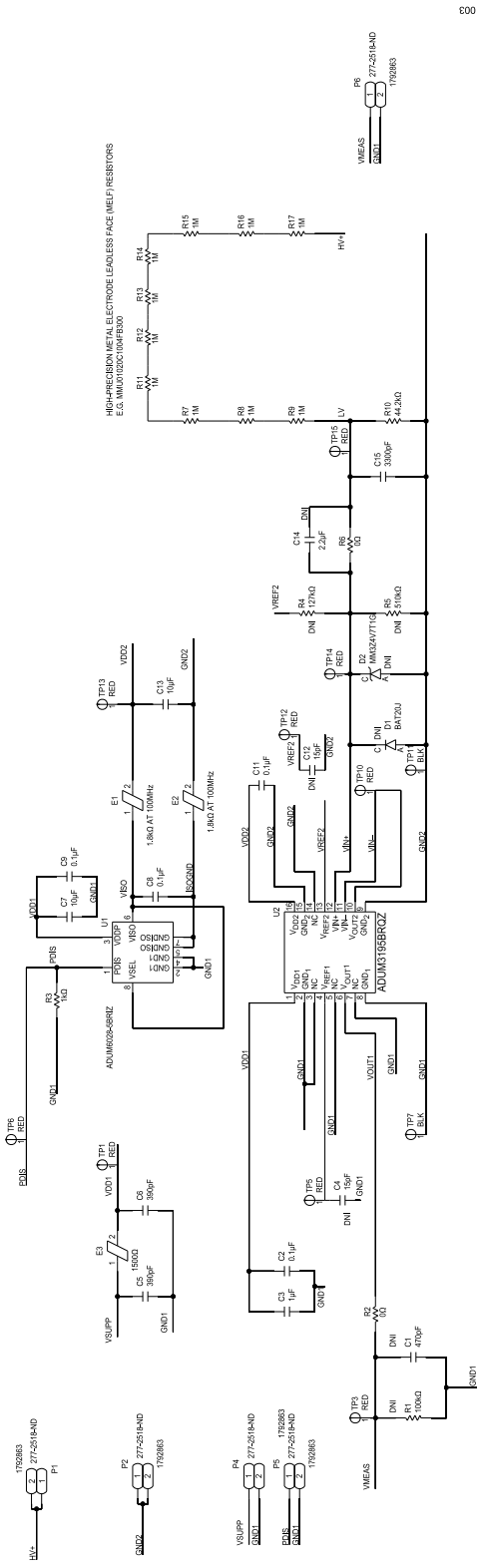

Figure 3. EVAL-ADuM3195EBZ Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

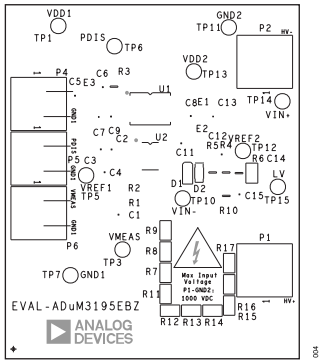

Figure 4. EVAL-ADuM3195EBZ Silkscreen

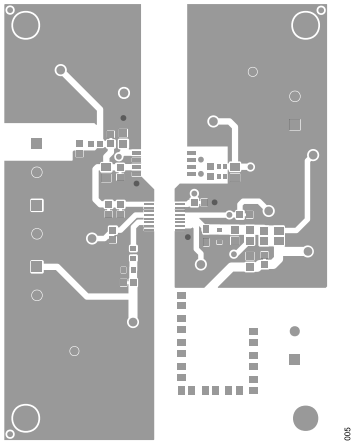

Figure 5. EVAL-ADuM3195EBZ Top Layer

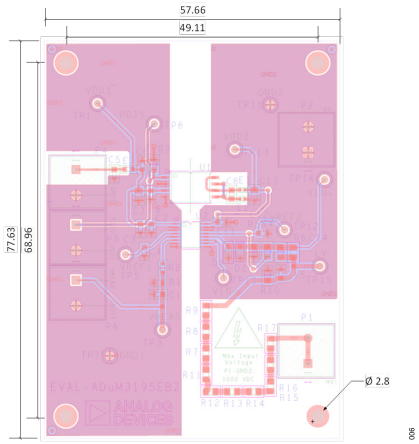

Figure 6. EVAL-ADuM3195EBZ Dimensions (mm)

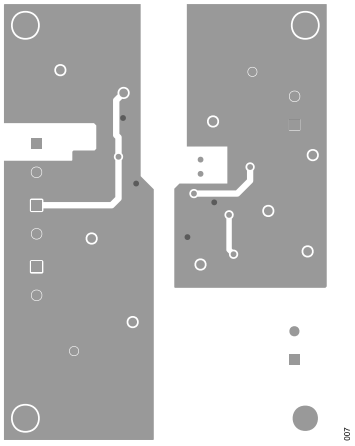

Figure 7. EVAL-ADuM3195EBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

QTY	Description	Value	Location	Manufacturer	Part Number	Comment[1]
1	PCB			Analog Devices, Inc.	08_068159a	
1	CAP CER, 470 pF, 25 V, 10% X7R, 0603	470 pF	C1	AVX Corporation	06033C471KAZ2A	DNP
4	CAP CER, 0.1 µF, 16 V, 10% X7R, 0603	0.1 µF	C2, C8, C9, C11	WURTH Elektronik	885012	
2	CAP CER, 15 pF, 16 V, 5% X7R, 0603	15 pF	C4, C12	WURTH Elektronik	885012000000	DNP
2	CAP CER, 10 µF, 10 V, 10% X7R, 0805	10 µF	C7, C13	WURTH Elektronik	885012	
1	CAP CER, 2.2 µF, 10 V, 10% X5R, 0805	2.2 µF	C14	Taiyo Yuden	LMK212BJ225KD-T	DNP
1	CAP CER, 3300 pF, 50 V, 10% X7R, 0603, AEC-Q200, low effective series resistance (ESR)	3300 pF	C15	TDK	CGA3E2X7R1H332K080AA	
1	CAP CER, 1 µF, 16 V, 20% X7R, 0603	1 µF	C3	AVX Corporation	0603YC105MAT2A	
2	CAP CER, 390 pF, 16 V, 10% X7R, 0603	390 pF	C5, C6	AVX Corporation	0603YC391KAT2A	
1	DIODE Schottky, BAT20J, 23 V, SOD-323	BAT20J	D1	STMicroelectronics	BAT20J	DNP
1	DIODE ZENER, 4.7 V, 1/5 W, SOD323	MM3Z4V7T1G	D2	Onsemi	MM3Z4V7T1G	DNP
2	IND FERRITE BEAD, 2.2 Ω, maximum DC resistance, 0.2 A	1.8 kΩ	E1, E2	Murata	BLM15HD182SN1D	
1	IND CHIP FERRITE BEAD, 0603	1500 Ω	E3	Murata	BLM18HE152SN1D	
5	CONN-PCB, two point-of-sale (POS) terminal blocks, 5 mm pitch	1792863	P1, P2, P4, P5, P6	Phoenix Contact	1792863	
1	RES SMD, 100 kΩ,1% 1/10 W, 0603, AEC-Q200	100 kΩ	R1	Vishay	CRCW0603100KFKEA	DNP
1	RES SMD, 44.2 kΩ, 0.1% 1/8 W, 0805, AEC-Q200	44.2 kΩ	R10	Panasonic	ERA-6ARB4422V	
10	RES SMD, 1 MΩ, 1% 0.3 W, 0102, AEC-Q200, sulfur resistant	1 MΩ	R7, R8, R9, R11, R12, R13, R14, R15, R16, R17	Vishay	MMU01020C1004FB300	
1	RES SMD, 0 Ω, 0603, AEC-Q200	0 Ω	R2	Vishay	CRCW0603000ZRT1	
1	RES SMD, 1 kΩ, 1% 1/8 W, 0805, AEC-Q200	1 kΩ	R3	Panasonic	ERJ-6ENF1001V	
1	RES SMD, 127 kΩ, 1% 1/8 W, 0805, AEC-Q200	127 kΩ	R4	Panasonic	ERJ-6ENF1273V	DNP
1	RES SMD, 0 Ω, 1/8 W, 0805, AEC-Q200	0 Ω	R6	Panasonic	ERJ-6GEY0R00V	
1	RES SMD, 510 kΩ, 1% 1/8 W, 0805, AEC-Q200	510 kΩ	R5	Stackpole	RMCF0805FT510K	DNP
9	CONN-PCB, test point red	RED	TP1, TP3, TP5, TP6, TP10, TP12, TP13, TP14, TP15	Vero Technologies	20-313137	
2	CONN-PCB, test point black	BLK	TP7, TP11	Vero Technologies	20-2137	
1	IC-ADI, low emission, 5 kV, isolated DC to DC converter	ADUM6028-5BRIZ	U1	Analog Devices	ADUM6028-5BRIZ	
1	IC-ADI, high-impedance, isolated amplifier	ADUM3195BRQZ	U2	Analog Devices	ADUM3195BRQZ	

[1] DNP means do not populate.