Isolated, Precision Gate Drivers with 2 A Output

Data Sheet

ADuM4120/ADuM4120-1

FEATURES

- 2.3 A peak output current (<2 Ω R_{DSON_x})
- 2.5 V to 6.5 V V_{DD1} input
- 4.5V to 35 V V_{DD2} output
- UVLO at 2.3 V V_{DD1}
- Multiple UVLO options on V_{DD2}
  - Grade A—4.4 V (typical) positive going threshold
  - Grade B—7.3 V (typical) positive going threshold
  - Grade C—11.3 V (typical) positive going threshold
- Precise timing characteristics
  - 79 ns maximum isolator and driver propagation delay falling edge (ADuM4120)
- CMOS input logic levels
- High common-mode transient immunity: 150 kV/µs
- High junction temperature operation: 125°C
- Default low output
- Safety and regulatory approvals (pending)
  - UL recognition per UL 1577
    - 5 kV rms for 1 minute SOIC long package
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 849 V peak
- 8 mm creepage
- Wide body, 6-lead SOIC with increased creepage

APPLICATIONS

- Switching power supplies
- IGBT/MOSFET gate drivers
- Industrial inverters
- Gallium nitride (GaN)/silicon carbide (SiC) power devices

GENERAL DESCRIPTION

The ADuM4120/ADuM4120-1[1] are 2 A isolated, single-channel drivers that employ Analog Devices, Inc., *i*Coupler® technology to provide precision isolation. The ADuM4120/ADuM4120-1 provide 5 kV rms isolation in the 6-lead wide body SOIC package with increased creepage. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics, such as the combination of pulse transformers and gate drivers.

The ADuM4120/ADuM4120-1 operate with input supplies ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM4120/ADuM4120-1 offer the benefit of true, galvanic isolation between the input and the output.

Options exist for models with and without an input glitch filter. The glitch filter helps reduce the chance of noise on the input pin triggering an output.

As a result, the ADuM4120/ADuM4120-1 provide reliable control over the switching characteristics of insulated gate bipolar transistor (IGBT)/metal-oxide semiconductor field effect transistor (MOSFET) configurations over a wide range of switching voltages.

FUNCTIONAL BLOCK DIAGRAM

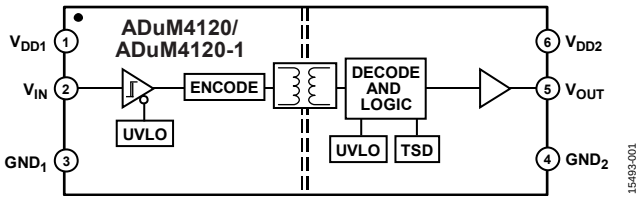

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. 0 Document Feedback

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REVISION HISTORY

5/2017—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND_1. High-side voltages referenced to GND_2; 2.5 V ≤ V_{DD1} ≤ 6.5 V; 4.5 V ≤ V_{DD2} ≤ 35 V, and T_J = −40°C to +125°C. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 15 V, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High-Side Power Supply						
V_{DD2} Input Voltage	V_{DD2}	4.5		35	V	
V_{DD2} Input Current, Quiescent	$I_{DD2(Q)}$		1.7	2.6	mA	
Logic Supply						
V_{DD1} Input Voltage	V_{DD1}	2.5		6.5	V	
Input Current	I_{DD1}		3.6	5	mA	V_{IN} = high
Logic Input	V_{IN}					
V_{IN} Input Current	I_{VIN}	−1	0.01	+1	µA	
Logic Input Voltage						
High	V_{IH}	0.7 × V_{DD1}			V	2.5 V ≤ V_{DD1} ≤ 5 V
		3.5			V	V_{DD1} > 5 V
Low	V_{IL}			0.3 × V_{DD1}	V	2.5 V ≤ V_{DD1} ≤ 5 V
				1.5	V	V_{DD1} > 5 V
Undervoltage Lockout (UVLO)						
V_{DD1}						
Positive Going Threshold	$V_{VDD1UV+}$		2.45	2.5	V	
Negative Going Threshold	$V_{VDD1UV-}$	2.3	2.35		V	
Hysteresis	$V_{VDD1UVH}$		0.1		V	
V_{DD2}						
Grade A						
Positive Going Threshold	$V_{VDD2UV+}$		4.4	4.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	4.1	4.2		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade B						
Positive Going Threshold	$V_{VDD2UV+}$		7.3	7.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	6.9	7.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade C						
Positive Going Threshold	$V_{VDD2UV+}$		11.3	11.6	V	
Negative Going Threshold	$V_{VDD2UV-}$	10.8	11.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Thermal Shutdown (TSD)						
TSD Positive Edge	T_{TSD_POS}		155		°C	
TSD Hysteresis	T_{TSD_HYST}		30		°C	
Internal NMOS Gate Resistance	R_{DSON_N}		0.6	1.6	Ω	Tested at 250 mA, V_{DD2} = 15 V
			0.6	1.6	Ω	Tested at 1 A, V_{DD2} = 15 V
Internal PMOS Gate Resistance	R_{DSON_P}		0.8	1.8	Ω	Tested at 250 mA, V_{DD2} = 15 V
			0.8	1.8	Ω	Tested at 1 A, V_{DD2} = 15 V
Peak Output Current	I_{PK}		2.3		A	V_{DD2} = 12 V, 4 Ω gate resistance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	50			ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Deglitch (V_{IN})	t_{IN_IN}, t_{IN_NIN}			20	ns	
ADuM4120						
Propagation Delay[1]						C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Rising Edge	t_{DLH}	44	57	68	ns	
Falling Edge	t_{DHL}	55	66	79	ns	
Skew	t_{PSK}			25	ns	C_L = 2 nF, R_{GON} = R_{GOFF} = 5 Ω
Rising Edge	t_{PSKLH}			19	ns	
Falling Edge	t_{PSKHL}			13	ns	
Pulse Width Distortion	t_{PWD}		9	16.5	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
ADuM4120-1						
Propagation Delay[1]						C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Rising Edge	t_{DLH}	22	33	42	ns	
Falling Edge	t_{DHL}	36	43	58	ns	
Skew	t_{PSK}			25	ns	C_L = 2 nF, R_{GON} = R_{GOFF} = 5 Ω
Rising Edge	t_{PSKLH}			14	ns	
Falling Edge	t_{PSKHL}			12	ns	
Pulse Width Distortion	t_{PWD}		9	16.5	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
OUTPUT RISE/FALL TIME (10% TO 90%)	t_R/t_F	11	18	26	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
COMMON-MODE TRANSIENT IMMUNITY (CMTI)	|CMTI|					
Static CMTI[2]		150			kV/µs	V_{CM} = 1500 V
Dynamic CMTI[3]		150			kV/µs	V_{CM} = 1500 V

[1] t_{DLH} propagation delay is measured from the time of the input rising logic high voltage threshold, V_{IH}, to the output rising 10% level of the V_{OUT} signal. t_{DHL} propagation delay is measured from the input falling logic low voltage threshold, V_{IL}, to the output falling 90% threshold of the V_{OUT} signal. See Figure 22 for waveforms of propagation delay parameters.

[2] Static CMTI is the largest dv/dt between GND_1 and GND_2, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.

[3] Dynamic CMTI is the largest dv/dt between GND_1 and GND_2 with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

REGULATORY INFORMATION

The ADuM4120/ADuM4120-1 are pending approval by the organizations listed in Table 2.

Table 2.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
UL1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, 849 V peak, V_{IOSM} = 10 kV peak	GB4943.1-2011
	Basic insulation at 800 V rms (1131 V peak)	Basic insulation 849 V peak, V_{IOSM} = 16 kV peak	Basic insulation at 800 V rms (1131 V peak)
	Reinforced insulation at 400 V rms (565 V peak)		Reinforced insulation at 400 V rms (565 V peak)
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 MOPP), 500 V rms (707 V peak)		
	Reinforced insulation (2 MOPP), 250 V rms (1414 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at: 600 V rms mains, 800 V secondary (1089 V peak)		
	Reinforced insulation at: 300 V rms mains, 400 V secondary (565 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
Junction to Ambient Thermal Resistance	θ_{JA}		123.7		°C/W	4-layer printed circuit board (PCB)

[1] The device is considered a 2-terminal device: Pin 1 through Pin 3 are shorted together, and Pin 4 through Pin 6 are shorted together.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the PCB Clearance	L(PCB)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5 min	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 3
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m =$ 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1019	V peak
Highest Allowable Overvoltage		V_{IOTM}	7000	V peak
Surge Isolation Voltage Basic	V peak = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	16,000	V peak
Surge Isolation Voltage Reinforced	V peak = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.0	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

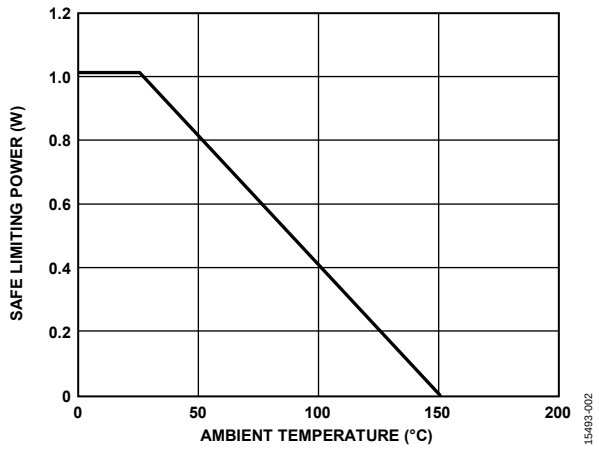

Figure 2. ADuM4120/ADuM4120-1 Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Operating Temperature Range (T_A)	−40°C to +125°C
Supply Voltages	
V_{DD1} − GND_1 or GND_2	2.5 V to 6.5 V
V_{DD2} − V_{SS2}[2]	4.5 V to 35 V

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Supply Voltages	
V_{DD1} – GND_1	−0.3 V to +7 V
V_{DD2} – GND_2	−0.3 V to +40 V
Input Voltages	
V_{IN}[1] – GND_1	−0.3 V to +7 V
Output Voltages	
V_{OUT} – GND_2	−0.3 V to V_{DD2} + 0.3 V
Common-Mode Transients (|CM|)[2]	−200 kV/µs to +200 kV/µs
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +125°C

[1] Rating assumes V_{DD1} is above 2.5 V. V_{IN} is rated up to 6.5 V when V_{DD1} is unpowered.
[2] |CM| refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. ADuM4120/ADuM4120-1 Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	600 V rms	20-year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	1092 V peak	Limited by the creepage of the package, Pollution Degree 2, Material Group II[2, 3]

[1] See the Insulation Lifetime section for details.
[2] Other pollution degree and material group requirements yield a different limit.
[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

Table 9. Truth Table ADuM4120/ADuM4120-1 (Positive Logic)

V_{IN} Input[1]	V_{DD1} State	V_{DD2} State	V_{OUT} Output
Low	Powered	Powered	Low
High	Powered	Powered	High
X	Unpowered[2]	Powered	Low
X	Powered	Unpowered[2]	High-Z

[1] X means don't care
[2] Output returns within 20 µs of being powered.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

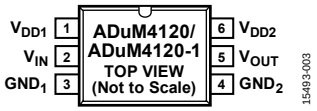

Figure 3. Pin Configuration

Table 10. ADuM4120/ADuM4120-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IN}	Gate Drive Logic Input.
3	GND_1	Ground 1. Ground reference for Isolator Side 1.
4	GND_2	Ground 2. Ground reference for Isolator Side 2.
5	V_{OUT}	Gate Drive Output. Connect this pin to the gate being driven through an external series resistor.
6	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

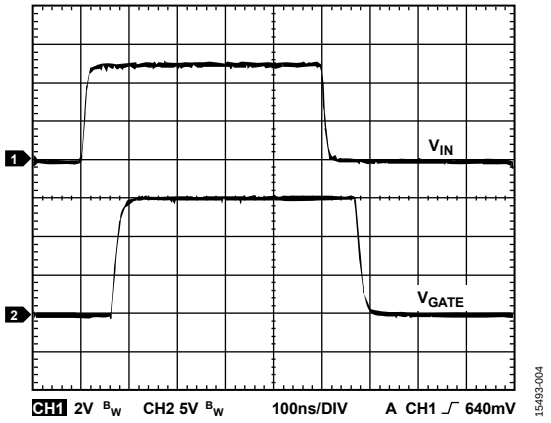

Figure 4. ADuM4120 V_{IN} to Gate Voltage (V_{GATE}) Waveform for 2 nF Load, 5 Ω Series Gate Resistor, V_{DD2} = 15 V

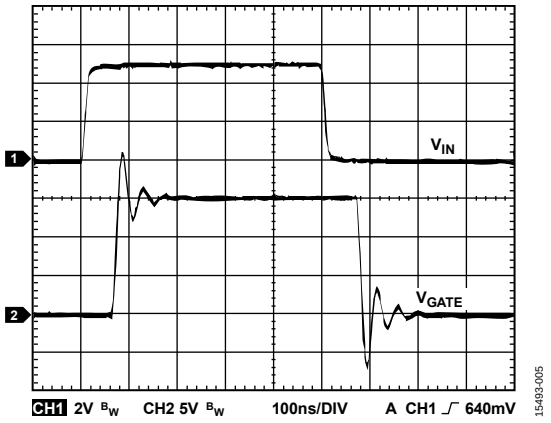

Figure 5. ADuM4120 V_{IN} to V_{GATE} Waveform for 2 nF Load, 0 Ω Series Gate Resistor, V_{DD2} = 15 V

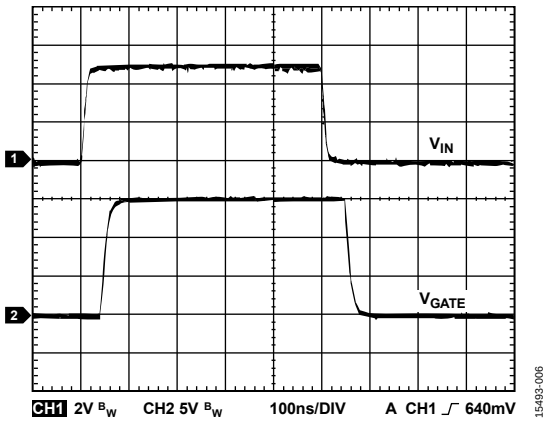

Figure 6. ADuM4120-1 V_{IN} to V_{GATE} Waveform for 2 nF Load, 5 Ω Series Gate Resistor, V_{DD2} = 15 V

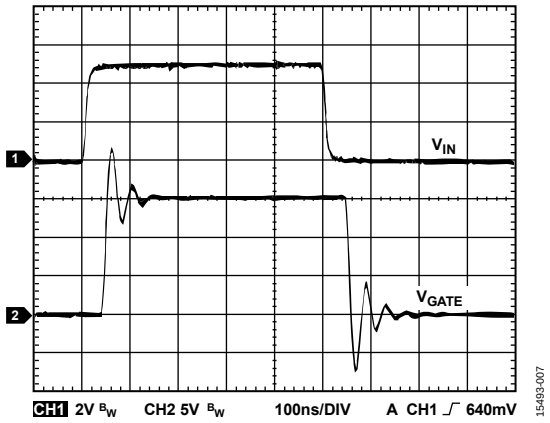

Figure 7. ADuM4120-1 V_{IN} to V_{GATE} Waveform for 2 nF Load, 0 Ω Series Gate Resistor, V_{DD2} = 15 V

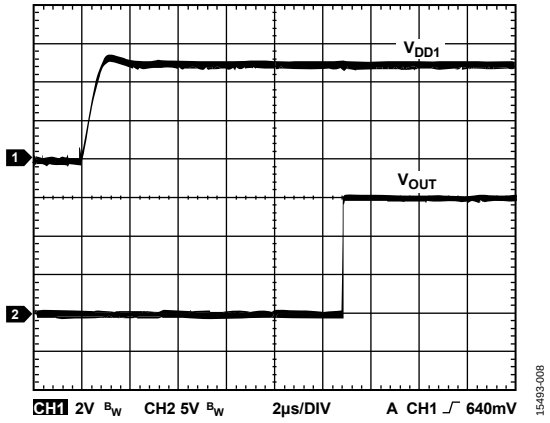

Figure 8. Typical V_{DD1} Delay to Output Waveform, V_{IN} = V_{DD1}

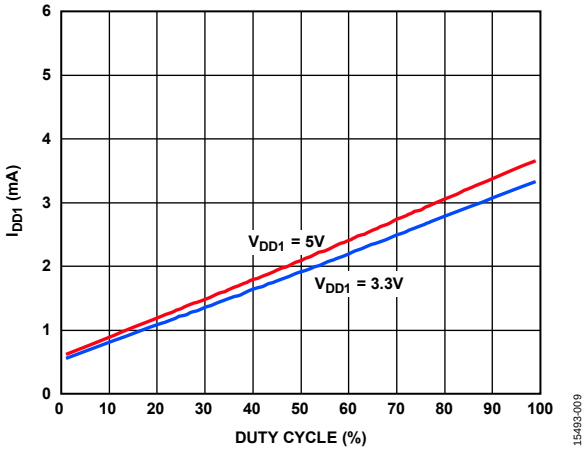

Figure 9. I_{DD1} vs. Duty Cycle, f_{SW} = 10 kHz

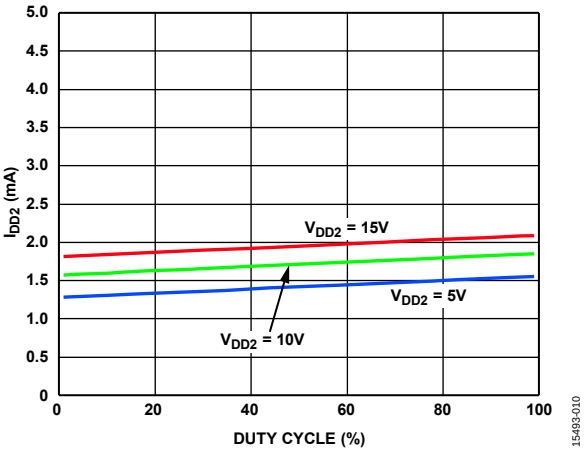

Figure 10. I_{DD2} vs. Duty Cycle, V_{DD1} = 5 V, f_{SW} = 10 kHz, 2 nF Load

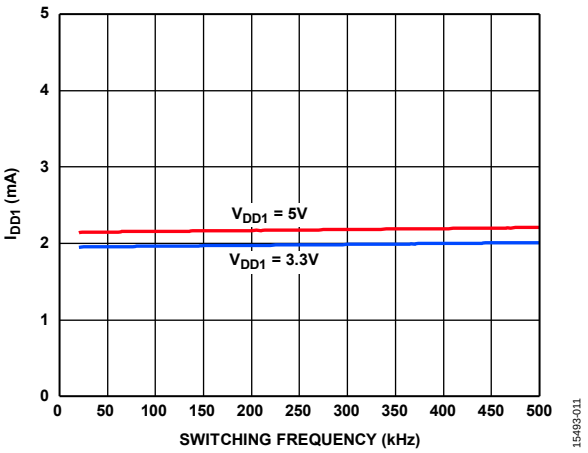

Figure 11. I_{DD1} vs. Switching Frequency

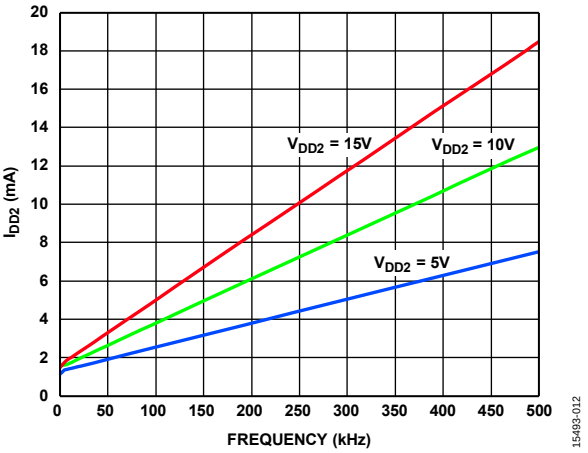

Figure 12. I_{DD2} vs. Switching Frequency, 2 nF Load

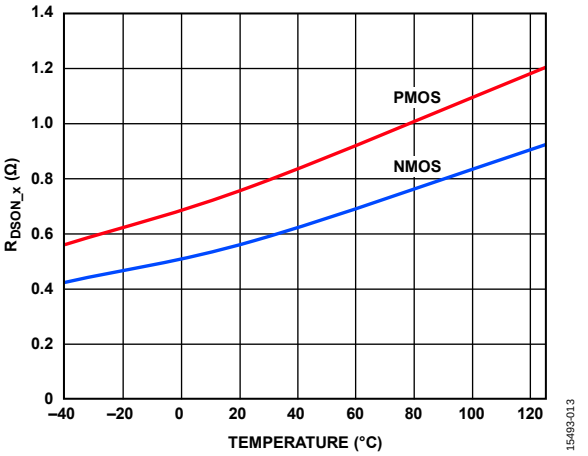

Figure 13. R_{DSON_x} vs. Temperature

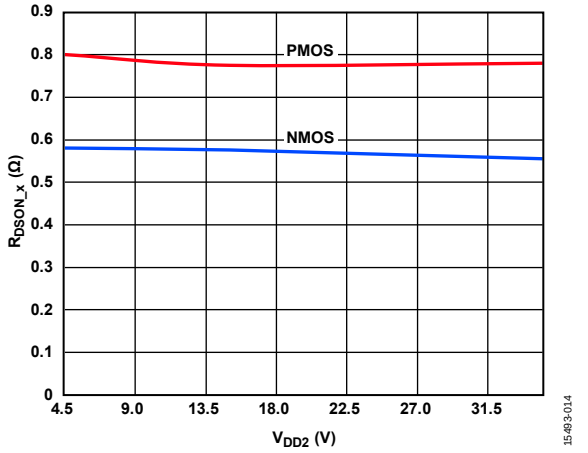

Figure 14. R_{DSON_x} vs. V_{DD2}

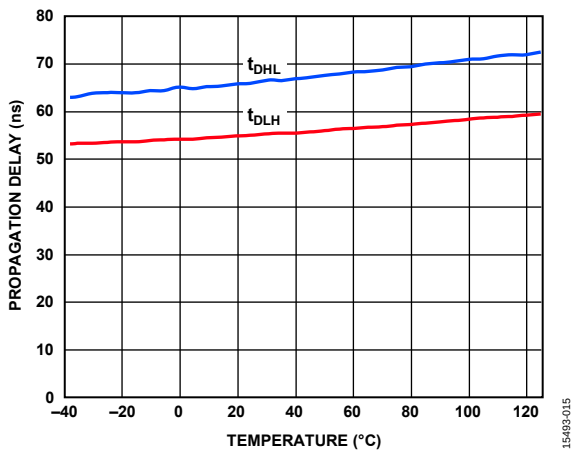

Figure 15. ADuM4120 Propagation Delay vs. Temperature, 2 nF Load

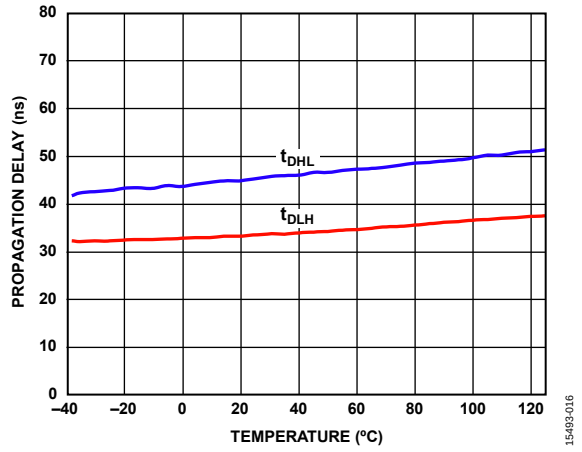

Figure 16. ADuM4120-1 Propagation Delay vs. Temperature, 2 nF Load

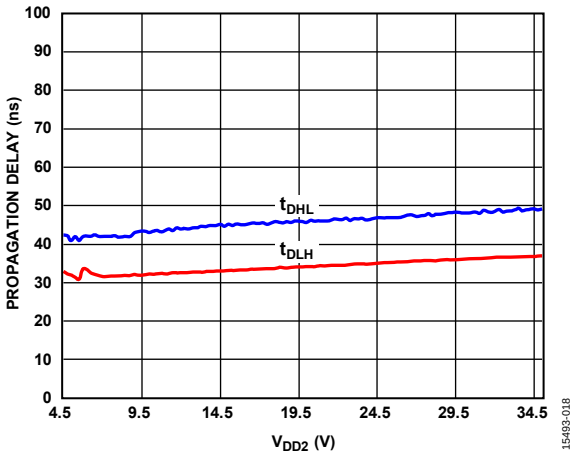

Figure 18. ADuM4120-1 Propagation Delay vs. V_{DD2}, 2 nF Load

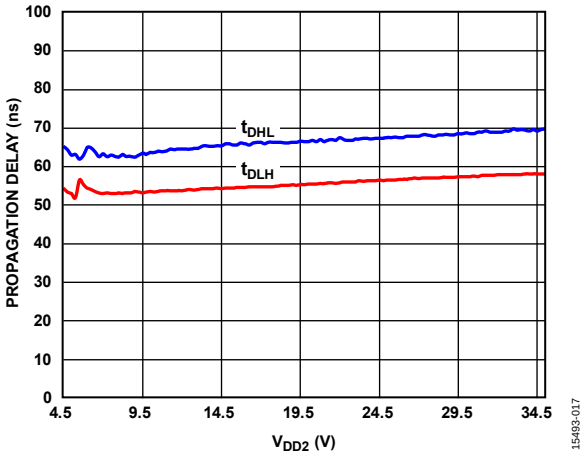

Figure 17. ADuM4120 Propagation Delay vs. V_{DD2}, 2 nF Load

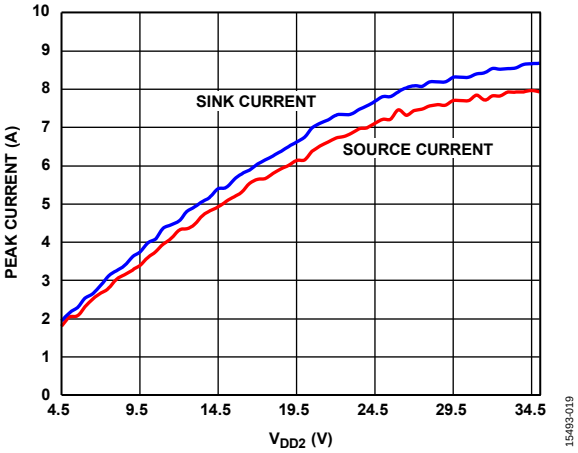

Figure 19. Peak Current vs. V_{DD2}, 2 Ω Resistor

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are desired. The gate signal for most enhancement type power devices are referenced to a source or emitter node. The gate driver must be able to follow this source or emitter node, necessitating isolation between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a CMOS output reduce total delay time and increase the final drive strength of the driver.

The ADuM4120/ADuM4120-1 achieve isolation between the control side and the output side of the gate driver by means of a high frequency carrier that transmits data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The encoding scheme used by the ADuM4120/ADuM4120-1 is a positive logic on/off keying (OOK), meaning a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is not powered. A low state is the most common safe state in enhancement mode power devices, driving in situations where shoot through conditions can exist. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques such as differential coil layout. Figure 20 illustrates the encoding used by the ADuM4120/ADuM4120-1.

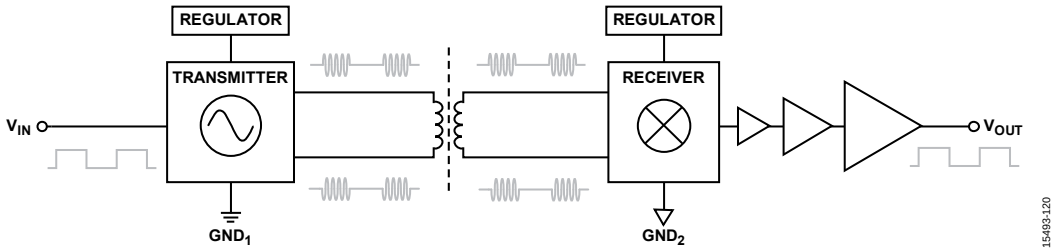

Figure 20. Operational Block Diagram of OOK Encoding

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4120/ADuM4120-1 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 21. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide an adequate high frequency bypass. On the output power supply pin, V_{DD1}, it is recommended to also add a 10 µF capacitor to provide the charge required to drive the gate capacitance at the ADuM4120/ADuM4120-1 outputs. Avoid the use of vias on the output supply pin and the bypass capacitor, or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must exceed 20 mm.

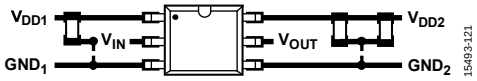

Figure 21. Recommended PCB Layout

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM4120/ADuM4120-1 specify t_{DLH} (see Figure 22) as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low voltage threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

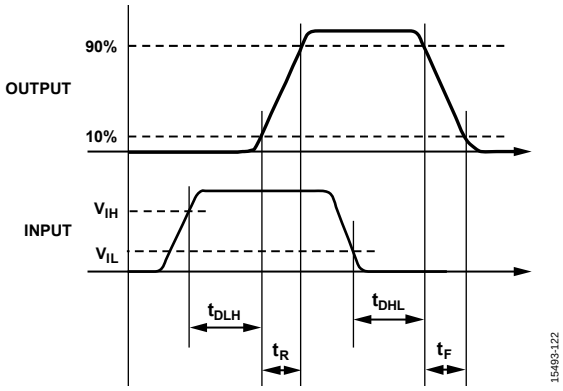

Figure 22. Propagation Delay Parameters

Channel to channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM4120/ADuM4120-1 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4120/ADuM4120-1 components operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the device. Therefore, heat dissipates mainly through the package pins.

If the internal junction temperature (θ_{JA}) of the device exceeds the TSD threshold, the output is driven low to protect the device. Operation above the recommended operating ranges is not guaranteed to be within the specifications shown in Table 1.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADuM4120/ADuM4120-1 have UVLO protections for both the primary and secondary side of the device. If either the primary or secondary side voltages are less than the falling edge UVLO, the device outputs a low signal. After the ADuM4120/ADuM4120-1 are powered above the rising edge UVLO threshold, the devices are able to output the signal found at the input. Hysteresis is built in to the UVLO to account for small voltage source ripple. The primary side UVLO thresholds are common among all models. Three options for the secondary output UVLO thresholds are listed in Table 11.

Table 11. List of Model Options

Model Number	Glitch Filter	UVLO (V)
ADuM4120ARIZ	Enabled	4.4
ADuM4120BRIZ	Enabled	7.3
ADuM4120CRIZ	Enabled	11.3
ADuM4120-1ARIZ	Disabled	4.4
ADuM4120-1BRIZ	Disabled	7.3
ADuM4120-1CRIZ	Disabled	11.3

OUTPUT LOAD CHARACTERISTICS

The ADuM4120/ADuM4120-1 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 23.

R_{SW} is the switch resistance of the internal ADuM4120/ADuM4120-1 driver output, which is about 1.5 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate to source capacitance, C_{GS}, of between 2 nF and 10 nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5 nH or less for a well designed layout with a very short and wide connection from the ADuM4120/ADuM4120-1 output to the gate of the MOSFET.

The following equation defines the Q factor of the resistor inductor capacitor (RLC) circuit, which indicates how the ADuM4120/ADuM4120-1 output responds to a step change. For a well damped output, Q is less than one. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

In Figure 4 and Figure 6, the ADuM4120/ADuM4120-1 output waveforms for a 15 V output are shown for a C_{GS} value of 2 nF and 5 Ω resistance. The ringing of the output in Figure 5 and Figure 7 with C_{GS} of 2 nF and no external resistor has a calculated Q factor of 1.5, where less than one is desired for adequate damping to prevent overshoot.

Output ringing can be reduced by adding a series gate resistance to dampen the response. For applications using a 1 nF or less load, it is recommended to add a series gate resistor of about 5 Ω. As shown in Figure 23, R_{GATE} is 5 Ω, which yields a calculated Q factor of about 0.7 which is well damped

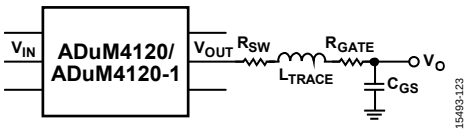

Figure 23. RLC Model of the Gate of an N-Channel MOSFET

POWER DISSIPATION

During the driving of a MOSFET or IGBT gate, the driver must dissipate power. This power is significant and can lead to TSD if considerations are not made. The gate of an IGBT can be roughly simulated as a capacitive load. With this value, the estimated total power dissipation, P_{DISS}, in the system due to switching action is given by the following equation:

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times fs$$

where:
$C_{EST} = C_{ISS} \times 5$.
fs is the switching frequency of IGBT.

This power dissipation is shared between the internal on resistances of the internal gate driver switches, and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4120/ADuM4120-1 chip.

$$P_{DISS\_ADuM4120/ADuM4120\text{-}1} = P_{DISS} \times 0.5((R_{DSON\_P}/(R_{GON} + R_{DSON\_P})) + (R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

Taking this power dissipation found inside the chip and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4120/ADuM4120-1 experiences.

$$T_{ADuM4120/ADuM4120\text{-}1} = \theta_{JA} \times P_{DISS\_ADuM4120} + T_A$$

For the device to remain within specification, $T_{ADUM4120}$ cannot exceed 125°C. If $T_{ADuM4120}$ exceeds the thermal shutdown (TSD), rising edge, the device enters TSD and the output remains low until the TSD falling edge is crossed.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4120/ADuM4120-1 is resistant to external magnetic fields. The limitation on the ADuM4120/ADuM4120-1 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which a false reading condition can occur. The 2.3 V operating condition of the ADuM4120/ADuM4120-1 is examined because it represents the most susceptible mode of operation.

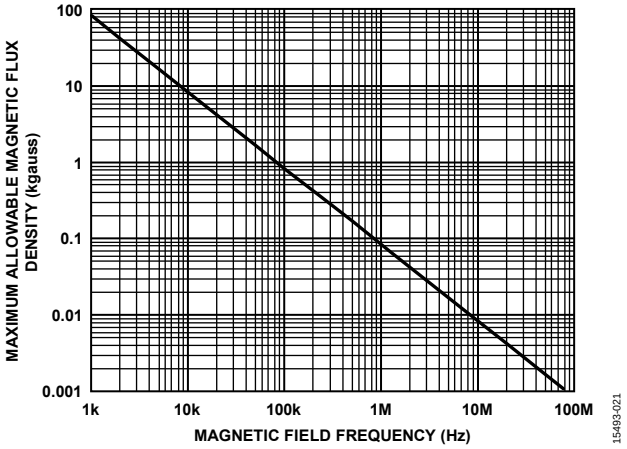

Figure 24. Maximum Allowable External Magnetic Flux Density

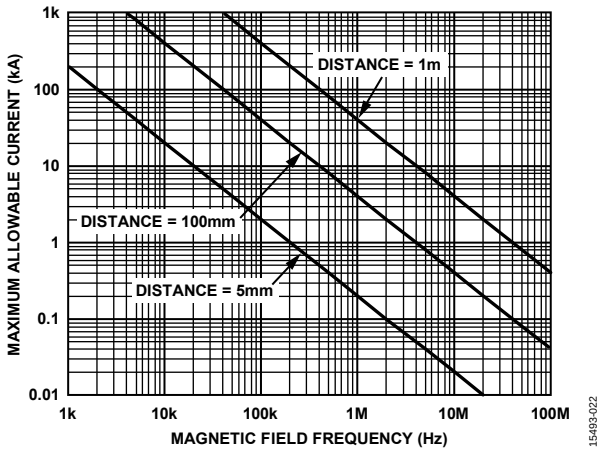

Figure 25. Maximum Allowable Current for Various Current to ADuM4120/ADuM4120-1 Spacings

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation, as well as on the materials and material interfaces.

Two types of insulation degradation are of primary interest: breakdown along surfaces exposed to air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and therefore can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM4120/ADuM4120-1 isolators are shown in Table 4.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this stress reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}^{\,2} + V_{DC}^{\,2}} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}^{\,2} - V_{DC}^{\,2}} \quad (2)$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following is an example that frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms, and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage clearance and lifetime of a device, see Figure 26 and the following equations.

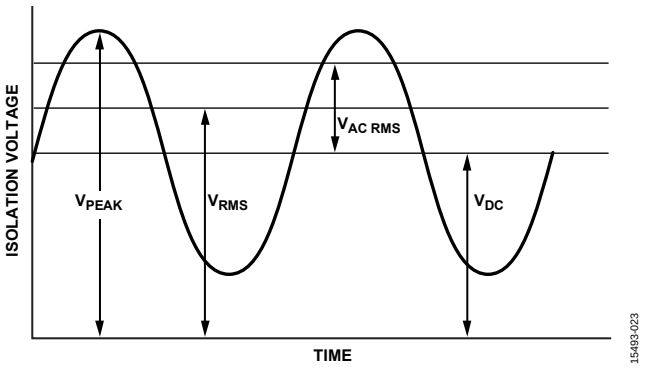

Figure 26. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V rms

This working voltage of 466 V rms is used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. Obtain the ac rms voltage from Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2}$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\ RMS}$ = 240 V rms

In this case, ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value of the ac waveform is compared to the limits for working voltage in Table 8 for expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 20-year service life.

Note that the dc working voltage limit in Table 8 is set by the creepage of the package as specified in IEC 60664-1. This value may differ for specific system level standards.