ADuM4135

Single-/Dual-Supply, High Voltage Isolated IGBT Gate Driver with Miller Clamp

FEATURES

- 13 A short-circuit source current (0 Ω gate resistance)
- 14 A short-circuit sink current (0 Ω gate resistance)
- 4.61 A peak current (2 Ω gate resistance)
- Output power device resistance: <1 Ω
- Desaturation protection
  - Isolated desaturation fault reporting
  - Soft shutdown on fault
- Miller clamp output with gate sense input
- Isolated fault and ready functions
- Low propagation delay: 55 ns typical
- Minimum pulse width: 50 ns
- Operating temperature range: −40°C to +125°C
- Output voltage range to 30 V
- Input voltage range from 2.5 V to 6 V
- Output and input undervoltage lockout (UVLO)
- Creepage distance: 7.8 mm minimum
- 100 kV/μs common-mode transient immunity (CMTI)
- 20-year lifetime for 600 V rms or 1092 V dc working voltage
- Safety and regulatory approvals
  - 5 kV ac for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - DIN VDE V 0884-11:2017-01
  - V_{IORM} = 849 V peak (reinforced)
- Qualified for automotive applications

APPLICATIONS

- MOSFET/IGBT gate drivers
- PV inverters
- Motor drives
- Power supplies
- Automotive

GENERAL DESCRIPTION

The ADuM4135 is a single-channel gate driver specifically optimized for driving insulated gate bipolar transistors (IGBTs). Analog Devices, Inc., *i*Coupler® technology provides isolation between the input signal and the output gate drive.

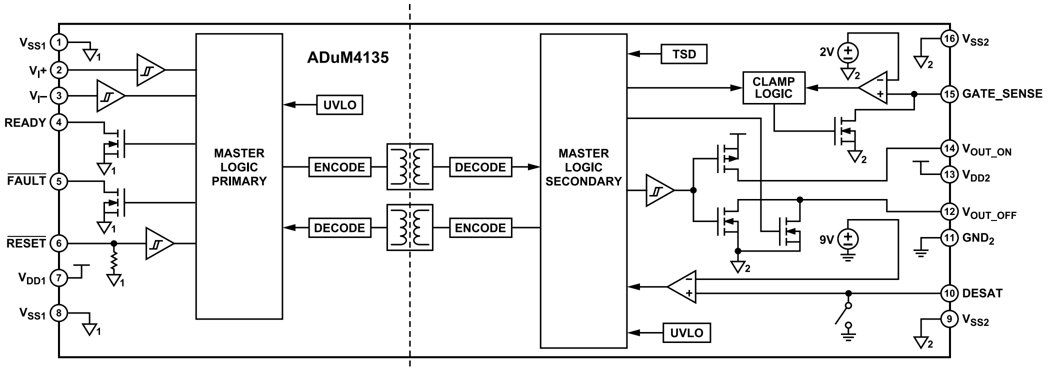
The ADuM4135 includes a Miller clamp to provide robust IGBT turn-off with a single-rail supply when the gate voltage drops below 2 V (typical). Operation with unipolar or bipolar secondary supplies is possible, with or without the Miller clamp operation.

The Analog Devices chip scale transformers also provide isolated communication of control information between the high voltage and low voltage domains of the chip. Information on the status of the chip can be read back from dedicated outputs. Control of resetting the device after a fault on the secondary is performed on the primary side of the device.

Integrated onto the ADuM4135 is a desaturation detection circuit that provides protection against high voltage short-circuit IGBT operation. The desaturation protection contains noise reducing features such as a 370 ns (typical) masking time after a switching event to mask voltage spikes due to initial turn-on. An internal 537 μA (typical) current source allows low device count and the internal blanking switch allows the addition of an external current source if more noise immunity is needed.

The secondary UVLO is set to 11.67 V (typical) with common IGBT threshold levels taken into consideration.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. GROUNDS ON PRIMARY AND SECONDARY SIDE ARE ISOLATED FROM EACH OTHER.

Figure 1.

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REVISION HISTORY

7/2022—Rev. D to Rev. E

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Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN VDE V 0884-11:2017-01 Insulation Characteristics Section...5
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to V_{SS1}. High-side voltages referenced to GND_2, 2.5 V ≤ V_{DD1} ≤ 6 V, 12.25 V ≤ V_{DD2} ≤ 30 V, and T_J = −40°C to +125°C. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High-Side Power Supply						
Input Voltage						
V_{DD2}	V_{DD2}	12.25		30	V	$V_{DD2} - V_{SS2} \leq 30$ V
V_{SS2}	V_{SS2}	−15		0	V	
Input Current, Quiescent						Ready high
V_{DD2}	$I_{DD2\ (Q)}$		3.62	4.95	mA	
V_{SS2}	$I_{SS2\ (Q)}$		4.82	6.21	mA	
Logic Supply						
V_{DD1} Input Voltage	V_{DD1}	2.5		6	V	
Input Current	I_{DD1}					
Output Low			1.95	3.0	mA	Output signal low
Output High			4.78	6.39	mA	Output signal high
Logic Inputs (V_I+, V_I−, $\overline{\text{RESET}}$)						
Input Current (V_I+, V_I− Only)	I_I	−1	+0.01	+1	μA	
Logic High Input Voltage	V_{IH}	0.7 × V_{DD1}			V	2.3 V ≤ $V_{DD1} - V_{SS1}$ ≤ 5 V
		3.5			V	$V_{DD1} - V_{SS1}$ > 5 V
Logic Low Input Voltage	V_{IL}			0.29 × V_{DD1}	V	2.3 V ≤ $V_{DD1} - V_{SS1}$ ≤ 5 V
				1.5	V	$V_{DD1} - V_{SS1}$ > 5 V
$\overline{\text{RESET}}$ Internal Pull-Down	$R_{\overline{\text{RESET}}\text{\_PD}}$		300		kΩ	
UVLO						
V_{DD1} Positive Going Threshold	$V_{VDD1UV+}$		2.439	2.5	V	
V_{DD1} Negative Going Threshold	$V_{VDD1UV-}$	2.3	2.342		V	
V_{DD1} Hysteresis	$V_{VDD1UVH}$		0.097		V	
V_{DD2} Positive Going Threshold	$V_{VDD2UV+}$		11.67	12.25	V	
V_{DD2} Negative Going Threshold	$V_{VDD2UV-}$	10.4	11.27		V	
V_{DD2} Hysteresis	$V_{VDD2UVH}$		0.4		V	
$\overline{\text{FAULT}}$ Pull-Down FET Resistance	$R_{\overline{\text{FAULT}}\text{\_PD\_FET}}$		11	50	Ω	Tested at 5 mA
READY Pull-Down FET Resistance	$R_{RDY\_PD\_FET}$		11	50	Ω	Tested at 5 mA
Desaturation (DESAT)						
Desaturation Detect Comparator Voltage	$V_{DESAT,\ TH}$	8.73	9.2	9.61	V	
Internal Current Source	I_{DESAT_SRC}	440	537	600	μA	
DESAT R_{DSON}	R_{DSON_DESAT}		8	15	Ω	Tested at 100 mA
Thermal Shutdown						
TSD Positive Edge	T_{TSD_POS}		155		°C	
TSD Hysteresis	T_{TSD_HYST}		20		°C	
Miller Clamp Voltage Threshold	V_{CLP_TH}	1.75	2	2.25	V	Referenced to V_{SS2}
Internal NMOS Gate Resistance	R_{DSON_N}		315	625	mΩ	Tested at 250 mA
			318	625	mΩ	Tested at 1 A
Internal PMOS Gate Resistance	R_{DSON_P}		471	975	mΩ	Tested at 250 mA
			479	975	mΩ	Tested at 1 A
Soft Shutdown NMOS	R_{DSON_FAULT}		10.2	22	Ω	Tested at 100 mA
Internal Miller Clamp Resistance	R_{DSON_MILLER}		1.1	2.75	Ω	Tested at 100 mA

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Short-Circuit Source Current	I_{SC_SOURCE}		13		A	V_{DD2} = 15 V, 0 Ω external gate resistance
Short-Circuit Sink Current	I_{SC_SINK}		14		A	V_{DD2} = 15 V, 0 Ω external gate resistance
Peak Current			4.61		A	V_{DD2} = 12 V, 2 Ω external gate resistance
SWITCHING SPECIFICATIONS						
Pulse Width[1]	PW	50			ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω
$\overline{\text{RESET}}$ Debounce	$t_{DEB\_\overline{RESET}}$	500	700	900	ns	
Propagation Delay[3]	t_{DHL}, t_{DLH}	40	55	70	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω
Propagation Delay Skew[4]	t_{PSK}			17.5	ns	C_L = 2 nF, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω, V_{DD1} = 5 V to 6 V
DESAT Soft Shutdown Delay	t_{D_DELAY}	130	150	320	ns	
Output Rise/Fall Time (10% to 90%)	t_R/t_F	11	16	22.9	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[2] = R_{GOFF}[2] = 3.9 Ω
Blanking Capacitor Discharge Switch Masking	t_{DESAT_DELAY}	213	370	529	ns	
Time to Report Desaturation Fault to $\overline{\text{FAULT}}$ Pin	t_{REPORT}		0.5	2.2	µs	
Common-Mode Transient Immunity (CMTI)	$\|CM\|$				kV/µs	
Static CMTI[5]		100				V_{CM} = 1500 V
Dynamic CMTI[6]		100				V_{CM} = 1500 V

[1] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.

[2] See the Power Dissipation section.

[3] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{OUTx} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{OUTx} signal. See Figure 20 for waveforms of propagation delay parameters.

[4] t_{PSK} is the magnitude of the worst case difference in tDLH and/or tDHL that is measured between units at the same operating temperature, supply voltages, and output loADuM4135 within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.

[5] Static common-mode transient immunity (CMTI) is defined as the largest dv/dt between V_{SS1} and V_{SS2}, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets. Guaranteed by design and characterization.

[6] Dynamic common-mode transient immunity (CMTI) is defined as the largest dv/dt between V_{SS1} and V_{SS2} with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets. Guaranteed by design and characterization.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	$R_{I\text{-}O}$		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	$C_{I\text{-}O}$		2.0		pF	
Input Capacitance	C_I		4.0		pF	
Junction to Ambient Thermal Resistance	θ_{JA}		75.4		°C/W	4-layer printed circuit board (PCB)
Junction to Case Thermal Resistance	θ_{JC}		35.4		°C/W	4-layer PCB

[1] The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

SPECIFICATIONS

REGULATORY INFORMATION

The ADuM4135 certification approval granted by the organizations listed in Table 3.

Table 3.

UL	CSA	VDE
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to VDE0884-11[2]
Single Protection, 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2, 780 V rms (1103 V peak) maximum working voltage Reinforced Insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2, 390 V rms (551 V peak) maximum working voltage	Reinforced insulation, 849 V peak
File E214100	File 205078	File 2471900-4880-0003

[1] In accordance with UL 1577, each ADuM4135 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 10 μA).

[2] In accordance with DIN VDE V 0884-11, each ADuM4135 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN VDE V 0884-11 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.026 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN VDE V 0884-11:2017-01 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN VDE V 0884-11:2017-01 approval.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1592	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1019	V peak

SPECIFICATIONS

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Highest Allowable Overvoltage		V_{IOTM}	8000	V peak
Surge Isolation Voltage	V_{PEAK} = 12.8 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.66	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

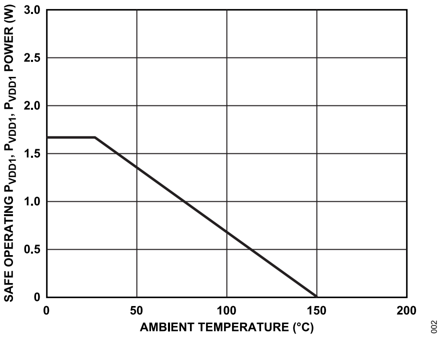


Figure 2. ADuM4135 Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN VDE V 0884-11:2017-01

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Operating Temperature Range (T_A)	−40°C to +125°C
Supply Voltages	
V_{DD1}[1]	2.5 V to 6 V
V_{DD2}[2]	12.25 V to 30 V
$V_{DD2} - V_{SS2}$[2]	12.25 V to 30 V
V_{SS2}[2]	−15 V to 0 V
Input Signal Rise/Fall Time	1 ms
Static Common-Mode Transient Immunity[3]	−100 kV/μs to +100 kV/μs
Dynamic Common-Mode Transient Immunity[4]	−100 kV/μs to +100 kV/μs

[1] Referenced to V_{SS1}.

[2] Referenced to GND_2. $V_{DD2} - V_{SS2}$ must not exceed 30 V.

[3] Static common-mode transient immunity is defined as the largest dv/dt between V_{SS1} and V_{SS2}, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.

[4] Dynamic common-mode transient immunity is defined as the largest dv/dt between V_{SS1} and V_{SS2} with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +125°C
Supply Voltages	
V_{DD1}[1]	−0.3 V to +6.5 V
V_{DD2}[2]	−0.3 V to +35 V
V_{SS2}[2]	−18 V to +0.3 V
$V_{DD2} - V_{SS2}$	35 V
Input Voltages	
V_I+[1], $V_I−$[1], $\overline{\text{RESET}}$[1]	−0.3 V to +6.5 V
V_{DESAT}[2]	−0.3 V to V_{DD2} + 0.3 V
V_{GATE_SENSE}[3]	−0.3 V to V_{DD2} + 0.3 V
V_{OUT_ON}[3]	−0.3 V to V_{DD2} + 0.3 V
V_{OUT_OFF}[3]	−0.3 V to V_{DD2} + 0.3 V
Common-Mode Transients (|CM|)	−150 kV/µs to +150 kV/µs

[1] Referenced to V_{SS1}.

[2] Referenced to GND_2. $V_{DD2} – V_{SS2}$ must not exceed 35 V.

[3] Referenced to V_{SS2}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	600 V rms	20 year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	1092 V peak	Limited by the creepage of the package, Pollution Degree 2, Material Group II[2, 3]

[1] See the Insulation Lifetime section for details.

[2] Other pollution degree and material group requirements yield a different limit.

[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TRUTH TABLE

Table 9. Truth Table (Positive Logic)[1]

V_I+ Input	$V_I−$ Input	$\overline{\text{RESET}}$ Pin	READY Pin	$\overline{\text{FAULT}}$ Pin	V_{DD1} State	V_{DD2} State	V_{GATE}[2]
L	L	H	H	H	Powered	Powered	L
L	H	H	H	H	Powered	Powered	L
H	L	H	H	H	Powered	Powered	H
H	H	H	H	H	Powered	Powered	L
X	X	H	L	Unknown	Powered	Powered	L
X	X	H	Unknown	L	Powered	Powered	L
L	L	H	L	Unknown	Unpowered	Powered	L
X	X	L[3]	Unknown	H[3]	Powered	Powered	L
X	X	X	L	Unknown	Powered	Unpowered	Unknown

[1] X is don't care, L is low, and H is high.

[2] V_{GATE} is the voltage of the gate being driven.

[3] Time dependent value. See the Absolute Maximum Ratings section for details on timing.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

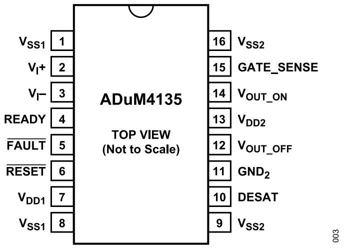


Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	V_{SS1}	Ground Reference for Primary Side.
2	V_I+	Positive Logic CMOS Input Drive Signal.
3	V_I-	Negative Logic CMOS Input Drive Signal.
4	READY	Open-Drain Logic Output. Connect this pin to a pull-up resistor to read the signal. A high state on this pin indicates that the device is functional and ready to operate as a gate driver. The presence of READY low precludes the gate drive output from going high.
5	$\overline{\text{FAULT}}$	Open-Drain Logic Output. Connect this pin to a pull-up resistor to read the signal. A low state on this pin indicates when a desaturation fault has occurred. The presence of a fault condition precludes the gate drive output from going high.
6	$\overline{\text{RESET}}$	CMOS Input. When a fault exists, bring this pin low to clear the fault.
7	V_{DD1}	Input Supply Voltage on Primary Side, 2.5 V to 6 V Referenced to V_{SS1}.
9, 16	V_{SS2}	Negative Supply for Secondary Side, −15 V to 0 V Referenced to GND_2.
10	DESAT	Detection of Desaturation Condition. Connect this pin to an external current source or a pull-up resistor. This pin can allow NTC temperature detection or other fault conditions. A fault on this pin asserts a fault on the $\overline{\text{FAULT}}$ pin on the primary side. Until the fault is cleared on the primary side, the gate drive is suspended. During a fault condition, a smaller turn-off FET slowly brings the gate voltage down.
11	GND_2	Ground Reference for Secondary Side. Connect this pin to the emitter of the IGBT or the source of the MOSFET being driven.
12	V_{OUT_OFF}	Gate Drive Output Current Path for Off Signal.
13	V_{DD2}	Secondary Side Input Supply Voltage, 12.25 V to 30 V Referenced to GND_2.
14	V_{OUT_ON}	Gate Drive Output Current Path for On Signal.
15	GATE_SENSE	Gate Voltage Sense Input and Miller Clamp Output. Connect this pin to the gate of the power device being driven. This pin senses the gate voltage for the purpose of Miller clamping. When the Miller clamp is not used, tie GATE_SENSE to VSS2.

TYPICAL PERFORMANCE CHARACTERISTICS

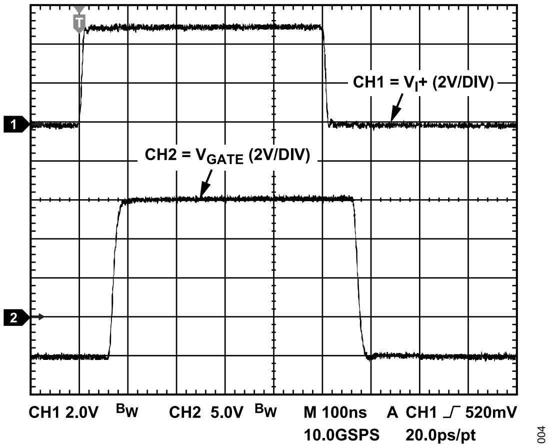


Figure 4. Typical Input to Output Waveform, 2 nF Load, 5.1 Ω Series Gate Resistor, V_{DD1} = +5 V, V_{DD2} = +15 V, V_{SS2} = −5 V

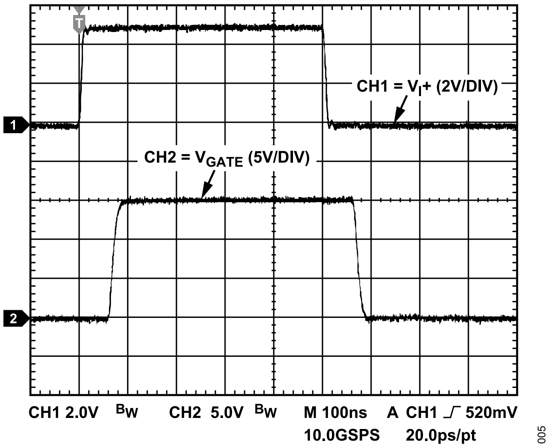


Figure 5. Typical Input to Output Waveform, 2 nF Load, 5.1 Ω Series Gate Resistor, V_{DD1} = 5 V, V_{DD2} = 15 V, V_{SS2} = 0 V

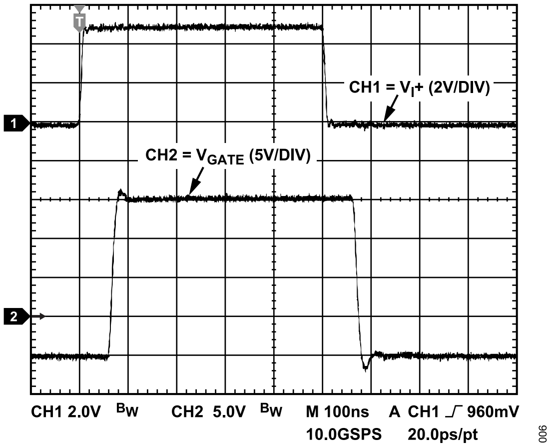


Figure 6. Typical Input to Output Waveform, 2 nF Load, 3.9 Ω Series Gate Resistor, V_{DD1} = +5 V, V_{DD2} = +15 V, V_{SS2} = −5 V

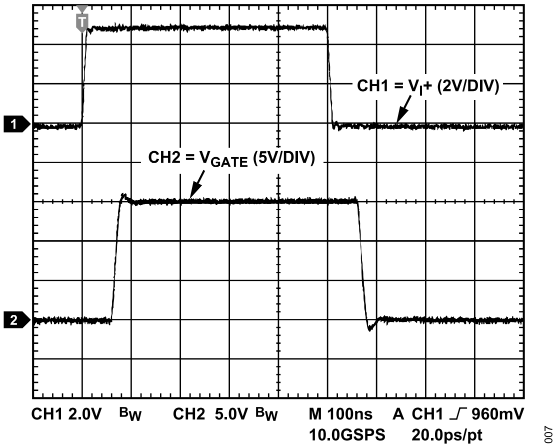


Figure 7. Typical Input to Output Waveform, 2 nF Load, 3.9 Ω Series Gate Resistor, V_{DD1} = 5 V, V_{DD2} = 15 V, V_{SS2} = 0 V

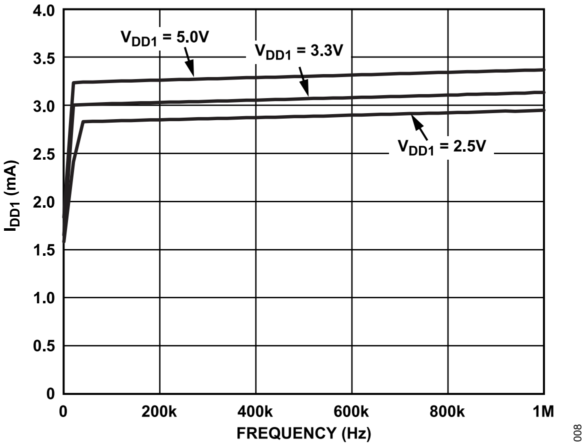


Figure 8. Typical I_{DD1} Current vs. Frequency, Duty = 50%, V_I+ = V_{DD1}

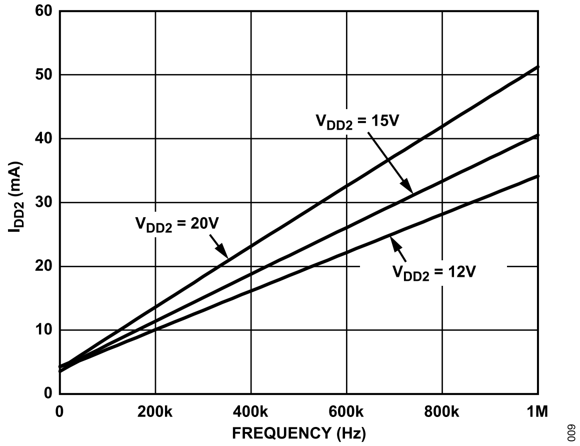


Figure 9. Typical I_{DD2} Current vs. Frequency, Duty = 50%, 2 nF Load, V_{SS2} = 0 V

TYPICAL PERFORMANCE CHARACTERISTICS

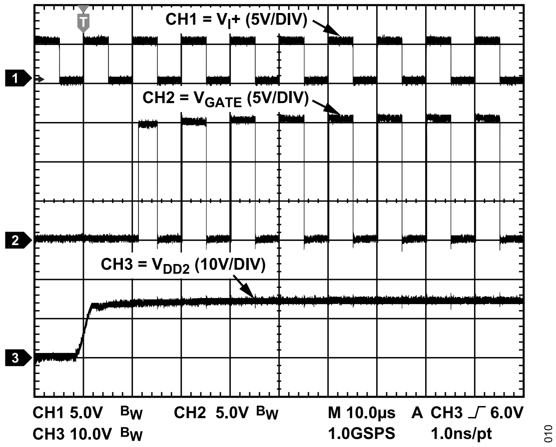


Figure 10. Typical V_{DD2} Startup to Output Valid

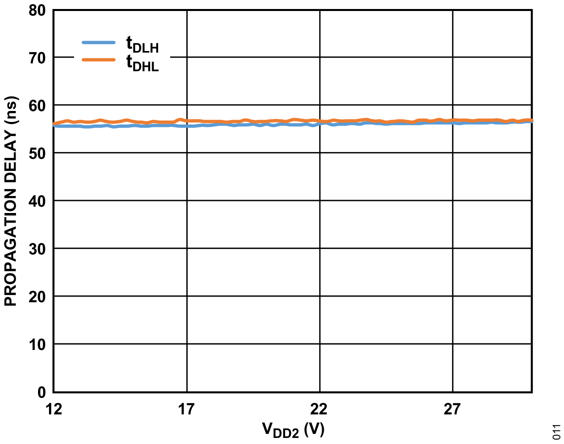


Figure 11. Typical Propagation Delay vs. Output Supply Voltage (V_{DD2}) for V_{DD2} = 15 V and V_{DD1} = 5 V

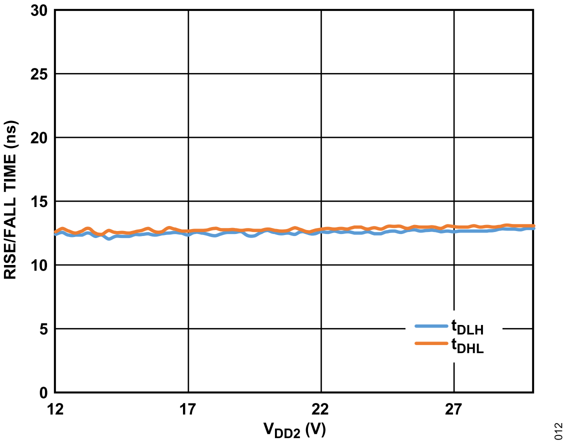


Figure 12. Typical Rise/Fall Time vs. V_{DD2}, V_{DD1} = 5 V, 2 nF Load, R_G = 3.9 Ω

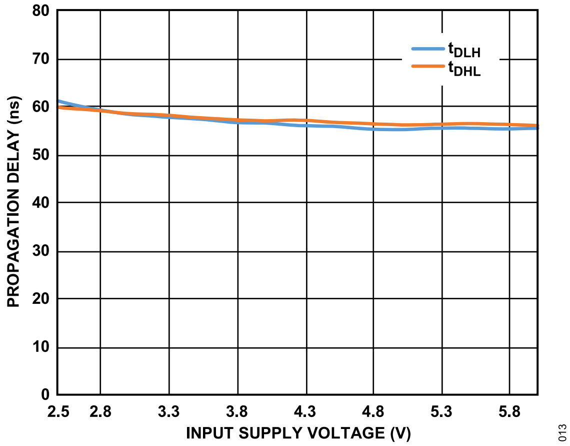


Figure 13. Typical Propagation Delay vs. Input Supply Voltage, $V_{DD2} - V_{SS2}$ = 12 V

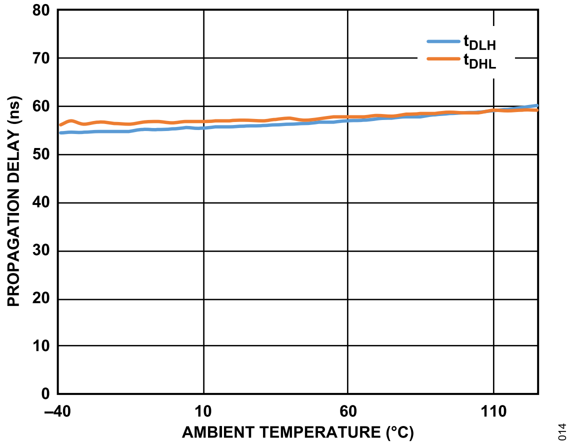


Figure 14. Typical Propagation Delay vs. Ambient Temperature, V_{DD2} = 5 V, $V_{DD2} - V_{SS2}$ = 12 V

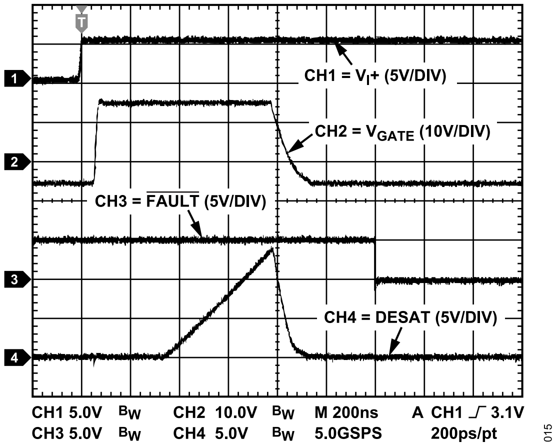


Figure 15. Example Desaturation Event and Reporting

TYPICAL PERFORMANCE CHARACTERISTICS

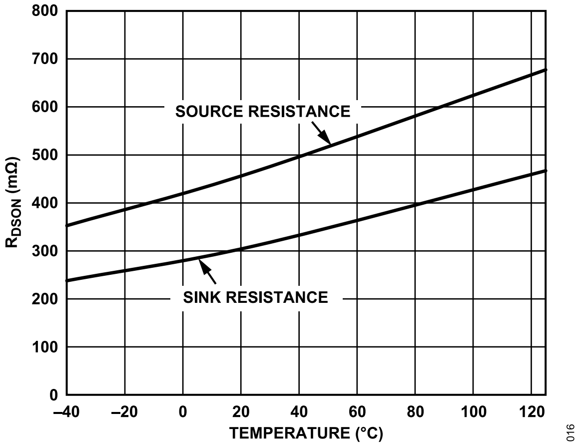


Figure 16. Typical Output Resistance (R_{DSON}) vs. Temperature, V_{DD2} = 15 V, 250 mA Test

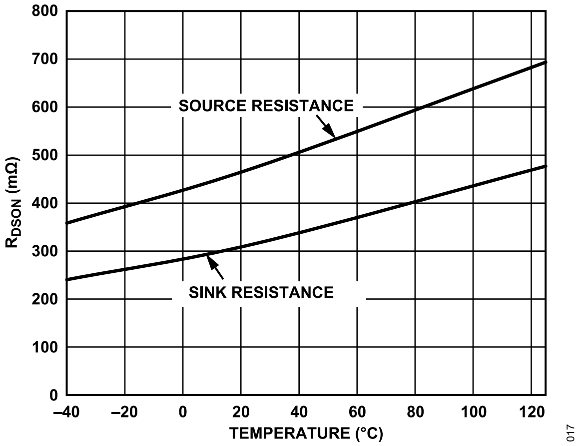


Figure 17. Typical Output Resistance (R_{DSON}) vs. Temperature, V_{DD2} = 15 V, 1 A Test

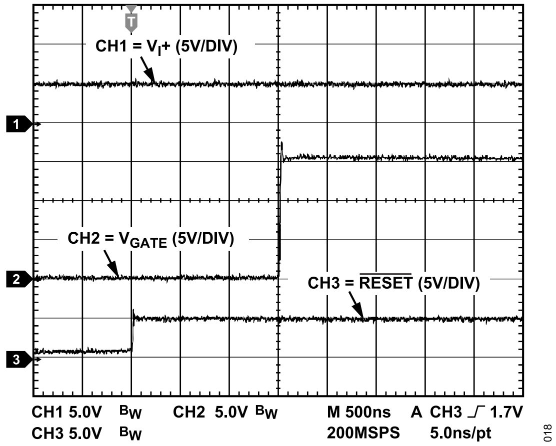


Figure 18. Example to Output Valid

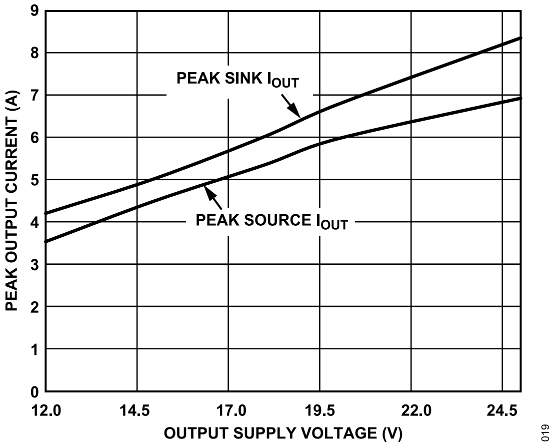


Figure 19. Typical Peak Output Current vs. Output Supply Voltage, 2 Ω Series Resistance (I_{OUT} is the Current Going into/out of the Device Gate)

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4135 IGBT gate driver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DD2}, it is recommended also to add a 10 µF capacitor to provide the charge required to drive the gate capacitance at the ADuM4135 outputs. On the output supply pin, avoid the use of vias on the bypass capacitor or employ multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 5 mm.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay describes the time it takes a logic signal to propagate through a component. The propagation delay to a low output can differ from the propagation delay to a high output. The ADuM4135 specifies t_{DLH} as the time between the rising input high logic threshold (V_{IH}) to the output rising 10% threshold (see Figure 20). Likewise, the falling propagation delay (t_{DHL}) is defined as the time between the input falling logic low threshold (V_{IL}) and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

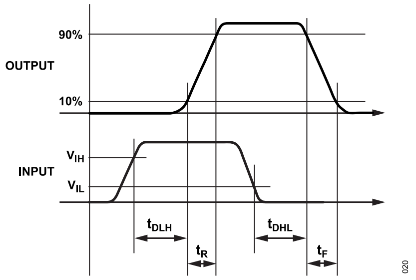


Figure 20. Propagation Delay Parameters

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4135 components operating under the same temperature, input voltage, and load conditions.

PROTECTION FEATURES

Fault Reporting

The ADuM4135 provides protection for faults that may occur during the operation of an IGBT. The primary fault condition is desaturation. If saturation is detected, the ADuM4135 shuts down the gate drive and asserts $\overline{\text{FAULT}}$ low. The output remains disabled until $\overline{\text{RESET}}$ is brought low for more than 900 ns (maximum), and is then brought high. $\overline{\text{FAULT}}$ resets to high on the falling edge of $\overline{\text{RESET}}$.

While $\overline{\text{RESET}}$ remains held low, the output remains disabled. The $\overline{\text{RESET}}$ pin has an internal, 300 kΩ (typical) pull-down resistor.

Desaturation Detection

Occasionally, component failures or faults occur with the circuitry connected to the IGBT connected to the ADuM4135. Examples include shorts in the inductor/motor windings or shorts to power/ground buses. The resulting excess in current flow causes the IGBT to come out of saturation. To detect this condition and to reduce the likelihood of damage to the FET, a threshold circuit is used on the ADuM4135. If the DESAT pin exceeds the desaturation threshold ($V_{DESAT,\ TH}$) of 9 V while the high-side driver is on, the ADuM4135 enters the failure state and turns the IGBT off. At this time, the $\overline{\text{FAULT}}$ pin is brought low. An internal current source of 537 µA (typical) is provided, as well as the option to boost the charging current using external current sources or pull-up resistors. The ADuM4135 has a built-in blanking time to prevent false triggering while the IGBT first turns on. The time between desaturation detection and reporting a desaturation fault to the $\overline{\text{FAULT}}$ pin is less than 2.2 µs (max t_{REPORT}). Bring $\overline{\text{RESET}}$ low to clear the fault. There is a 700 ns debounce (typical t_{DEB_RESET}) on the $\overline{\text{RESET}}$ pin. The time, t_{DESAT_DELAY}, shown in Figure 21, provides a 370 ns (typical) masking time that keeps the internal switch that grounds the blanking capacitor tied low for the initial portion of the IGBT on time.

APPLICATIONS INFORMATION

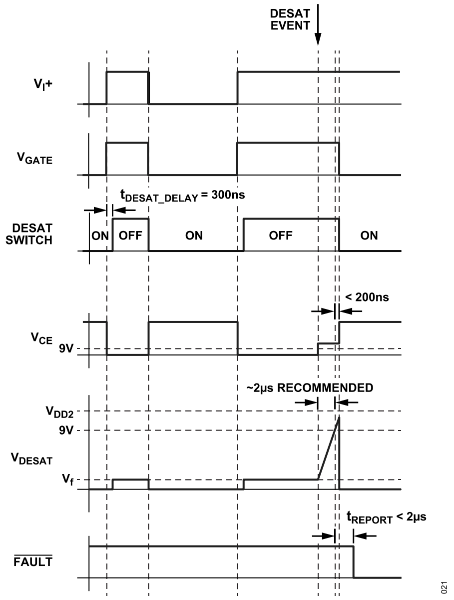


Figure 21. Desaturation Detection Timing Diagram

For the following design example, see the schematic shown in Figure 28 along with the waveforms in Figure 21. Under normal operation, during IGBT off times, the voltage across the IGBT, V_{CE}, rises to the rail voltage supplied to the system. In this case, the blocking diode shuts off, protecting the ADuM4135 from high voltages. During the off times, the internal desaturation switch is on, accepting the current going through the R_{BLANK} resistor, which allows the C_{BLANK} capacitor to remain at a low voltage. For the first 370 ns (typical) of the IGBT on time, the DESAT switch remains on, clamping the DESAT pin voltage low. After the 370 ns (typical) delay time, the DESAT pin is released, and the DESAT pin is allowed to rise towards V_{DD2} either by the internal current source on the DESAT pin, or additionally with an optional external pull-up, R_{BLANK}, to increase the current drive if it is not clamped by the collector or drain of the switch being driven. V_{RDESAT} is chosen to dampen the current at this time, usually selected around 100 Ω to 2 kΩ. Select the blocking diode to block above the high rail voltage on the collector of the IGBT and to be a fast recovery diode.

In the case of a desaturation event, V_{CE} rises above the 9 V threshold in the desaturation detection circuit. If no R_{BLANK} resistor is used to increase the blanking current, the voltage on the blanking capacitor, C_{BLANK}, rises at a rate of 537 µA (typical) divided by the C_{BLANK} capacitance. Depending on the IGBT specifications, a blanking time of approximately 2 µs is a typical design choice. When the DESAT pin rises above the 9.2 V (typical) threshold, a fault registers, and within t_{D_DELAY}, the gate output drives low through a soft shutdown. The output is brought low using the N-FET soft shutdown MOSFET, which is approximately 35 × more resistive than the internal gate driver N-FET, to perform a soft shutdown to reduce the chance of an overvoltage spike on the IGBT during an abrupt turn-off event. Within 2.2 µs (maximum), the fault is communicated back to the primary side $\overline{FAULT}$ pin. To clear the fault, a reset is required.

Miller Clamp

The ADuM4135 has an integrated Miller clamp to reduce voltage spikes on the IGBT gate caused by the Miller capacitance during shut-off of the IGBT. When the input gate signal calls for the IGBT to turn off (driven low), the Miller clamp MOSFET is initially off. When the voltage on the GATE_SENSE pin crosses the 2 V (typical) internal voltage reference, as referenced to V_{SS2}, the internal Miller clamp latches on for the remainder of the off time of the IGBT, creating a second low impedance current path for the gate current to follow. The Miller clamp switch remains on until the input drive signal changes from low to high. An example waveform of the timings is shown in Figure 22.

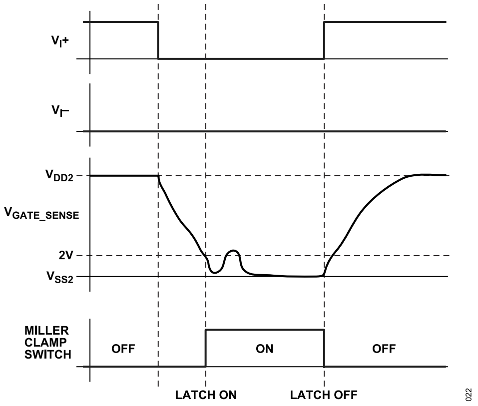


Figure 22. Miller Clamp Example

Thermal Shutdown

If the internal temperature of the ADuM4135 exceeds 155°C (typical), the device enters thermal shutdown (TSD). During the thermal shutdown time, the READY pin is brought low on the primary side, and the gate drive is disabled. When TSD occurs, the device does not leave TSD until the internal temperature drops below 135°C (typical), at which time the READY pin returns to high, and the device exits shutdown.

Undervoltage Lockout (UVLO) Faults

UVLO faults occur when the supply voltages are below the specified UVLO threshold values. During a UVLO event on either the primary side or secondary side, the READY pin goes low, and the gate drive is disabled. When the UVLO condition is removed, the device resumes operation, and the READY pin goes high.

READY Pin

The open-drain READY pin is an output that confirms communication between the primary to secondary sides is active. The READY pin remains high when there are no UVLO or TSD events present. When the READY pin is low, the IGBT gate is driven low.

APPLICATIONS INFORMATION

Table 11. READY Pin Logic Table

UVLO	TSD	READY Pin Output
No	No	High
Yes	No	Low
No	Yes	Low
Yes	Yes	Low

$\overline{\text{FAULT}}$ Pin

The open-drain $\overline{\text{FAULT}}$ pin is an output to communicate that a desaturation fault has occurred. When the $\overline{\text{FAULT}}$ pin is low, the IGBT gate is driven low. If a desaturation event occurs, the $\overline{\text{RESET}}$ pin must be driven low for at least 500 ns, then high to return operation to the IGBT gate drive.

$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin has an internal 300 kΩ (typical) pull-down resistor. The $\overline{\text{RESET}}$ pin accepts CMOS level logic. When the $\overline{\text{RESET}}$ pin is held low, after a 500 ns debounce time, any faults on the $\overline{\text{FAULT}}$ pin are cleared. While the $\overline{\text{RESET}}$ pin is held low, the switch on V_{OUT_OFF} is closed, bringing the gate voltage of the IGBT low. When $\overline{\text{RESET}}$ is brought high, and no fault exists, the device resumes operation.

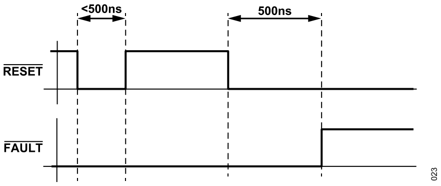


Figure 23. $\overline{\text{RESET}}$ Timing

V_I+ and V_I− Operation

The ADuM4135 has two drive inputs, V_I+ and V_I−, to control the IGBT gate drive signals, V_{OUT_ON} and V_{OUT_OFF}. Both the V_I+ and V_I− inputs use CMOS logic level inputs. The input logic of the V_I+ and V_I− pins can be controlled by either asserting the V_I+ pin high or the V_I− pin low. With the V_I− pin low, the V_I+ pin accepts positive logic. If V_I+ is held high, the V_I− pin accepts negative logic. If a fault is asserted, transmission is blocked until the fault is cleared by the $\overline{\text{RESET}}$ pin.

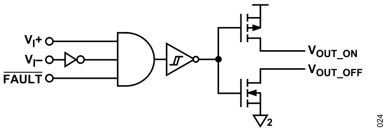


Figure 24. V_I+ and V_I− Block Diagram

The minimum pulse width, PW, is the minimum period in which the timing specifications are guaranteed.

Gate Resistance Selection

The ADuM4135 provides two output nodes for the driving of an IGBT. The benefit of this approach is that the user can select two different series resistances for the turn-on and turn-off of the IGBT. It is generally desired to have the turn-off occur faster than the turn-on. To select the series resistance, decide what the maximum allowed peak current is for the IGBT. Knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external resistor can be chosen.

$$I_{PEAK} = (V_{DD2} - V_{SS2})/(R_{DSON\_N} + R_{GOFF})$$

For example, if the turn-off peak current is 4 A, with a (V_{DD2} − V_{SS2}) of 18 V,

$$R_{GOFF} = ((V_{DD2} - V_{SS2}) - I_{PEAK} \times R_{DSON\_N})/I_{PEAK}$$

$$R_{GOFF} = (18\text{ V} - 4\text{ A} \times 0.6\ \Omega)/4\text{ A} = 3.9\ \Omega$$

After R_{GOFF} is selected, a slightly larger R_{GON} can be selected to arrive at a slower turn-on time.

POWER DISSIPATION

During the driving of an IGBT gate, the driver must dissipate power. This power is not insignificant and can lead to TSD if considerations are not made. The gate of an IGBT can be roughly simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance, C_{ISS}, of a given IGBT, and multiply it by a factor of 5 to arrive at a conservative estimate to approximate the load being driven. With this value, the estimated total power dissipation in the system due to switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - V_{SS2})^2 \times f_S$$

where:
$C_{EST} = C_{ISS} \times 5$.
f_S is the switching frequency of the IGBT.

This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4135 chip.

$$P_{DISS\_ADuM4135} = P_{DISS} \times 0.5(R_{DSON\_P}/(R_{GON} + R_{DSON\_P}) + R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

Taking the power dissipation found inside the chip and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4135 experiences.

$$T_{ADuM4135} = \theta_{JA} \times P_{DISS\_ADuM4135} + T_{AMB}$$

For the device to remain within specification, $T_{ADuM4135}$ must not exceed 125°C. If $T_{ADuM4135}$ exceeds 155°C (typical), the device enters thermal shutdown.

APPLICATIONS INFORMATION

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4135 is resistant to external magnetic fields. The limitation on the ADuM4135 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which a false reading condition can occur. The 2.5 V operating condition of the ADuM4135 is examined because it represents the most susceptible mode of operation.

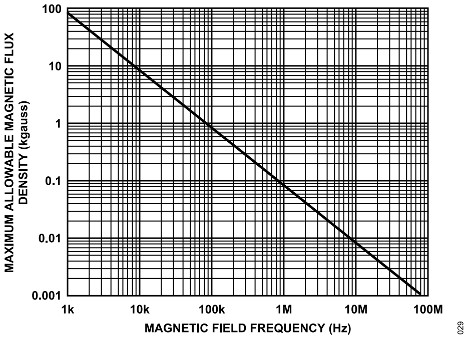


Figure 25. Maximum Allowable External Magnetic Flux Density

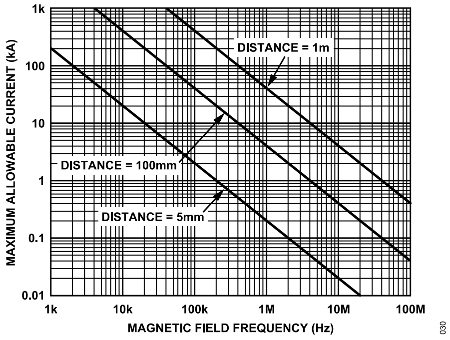


Figure 26. Maximum Allowable Current for Various Current-to-ADuM4135 Spacings

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation, as well as on the materials and material interfaces.

Two types of insulation degradation are of primary interest: breakdown along surfaces exposed to air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and therefore can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM4135 isolator are presented in Table 8.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling have shown that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as: dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this stress reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{{V_{AC\ \ RMS}}^2 + {V_{DC}}^2} \tag{1}$$

or

$$V_{AC\ RMS} = \sqrt{{V_{RMS}}^2 - {V_{DC}}^2} \tag{2}$$

where:
V_{RMS} is the total rms working voltage.
$V_{AC\ RMS}$ is the time varying portion of the working voltage.
V_{DC} is the dc offset of the working voltage.

APPLICATIONS INFORMATION

Calculation and Use of Parameters Example

The following is an example that frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms, and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage clearance and lifetime of a device, see Figure 27 and the following equations.

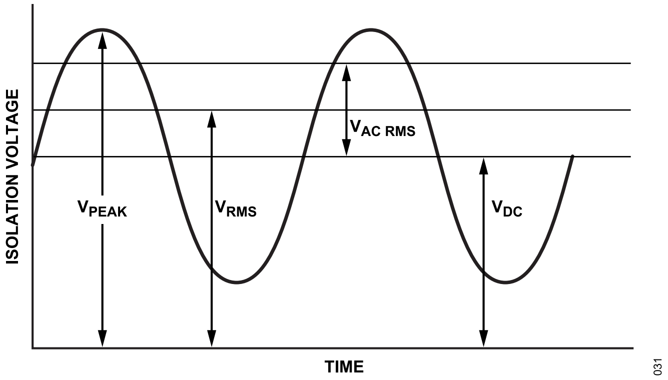


Figure 27. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^{2} + V_{DC}^{2}}$$

$$V_{RMS} = \sqrt{240^{2} + 400^{2}}$$

V_{RMS} = 466 V rms

This working voltage of 466 V rms is used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. The ac rms voltage can be obtained from Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^{2} - V_{DC}^{2}}$$

$$V_{AC\ RMS} = \sqrt{466^{2} - 400^{2}}$$

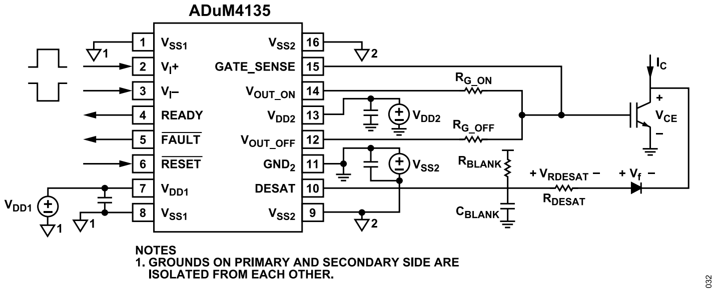
$V_{AC\ RMS}$ = 240 V rms

In this case, ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value of the ac waveform is compared to the limits for working voltage in Table 8 for expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 20-year service life.

Note that the dc working voltage limit in Table 8 is set by the creepage of the package as specified in IEC 60664-1. This value may differ for specific system level standards.

TYPICAL APPLICATION

The typical application schematic in Figure 28 shows a bipolar setup with an additional R_{BLANK} resistor to increase charging current of the blanking capacitor for desaturation detection. The R_{BLANK} resistor is optional. If unipolar operation is desired, the V_{SS2} supply can be removed, and V_{SS2} must be tied to GND_2.



NOTES
1. GROUNDS ON PRIMARY AND SECONDARY SIDE ARE ISOLATED FROM EACH OTHER.

Figure 28. Typical Application Schematic