Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0269.

Devices Connected/Referenced	
AD7984	18-Bit, 1.33 MSPS PulSAR 10.5 mW ADC in MSOP/QFN
AD8475	Precision, Selectable Gain, Fully Differential Funnel Amp
AD8065	High Performance, 145 MHz *FastFET* Op Amps
ADG5208	High Voltage, Latch-Up Proof, 8-Channel Multiplexers
ADG5236	High Voltage Latch-Up Proof, Dual SPDT Switches
ADR444	Ultralow Noise, 4.096 V, LDO XFET Voltage References with Current Sink and Source

18-Bit, 1.33 MSPS, 16-Channel Data Acquisition System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0269 Circuit Evaluation Board (EVAL-CN0269-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a high performance industrial signal level multichannel data acquisition circuit that has been optimized for fast channel-to-channel switching. It can process 16-channels of single-ended inputs or 8-channels of differential inputs with up to 18-bit resolution.

A single channel can be sampled at up to 1.33 MSPS with 18-bit resolution. A channel-to-channel switching rate of 250 kHz between all input channels provides 16-bit performance.

The signal processing circuit combined with a simple 4-bit up-down binary counter provides a simple and cost effective way to realize channel-to-channel switching without an FPGA, CPLD, or high speed processor. The counter can be programmed to count up or count down for sequentially sampling multiple channels, or can be loaded with a fixed binary word for sampling a single channel.

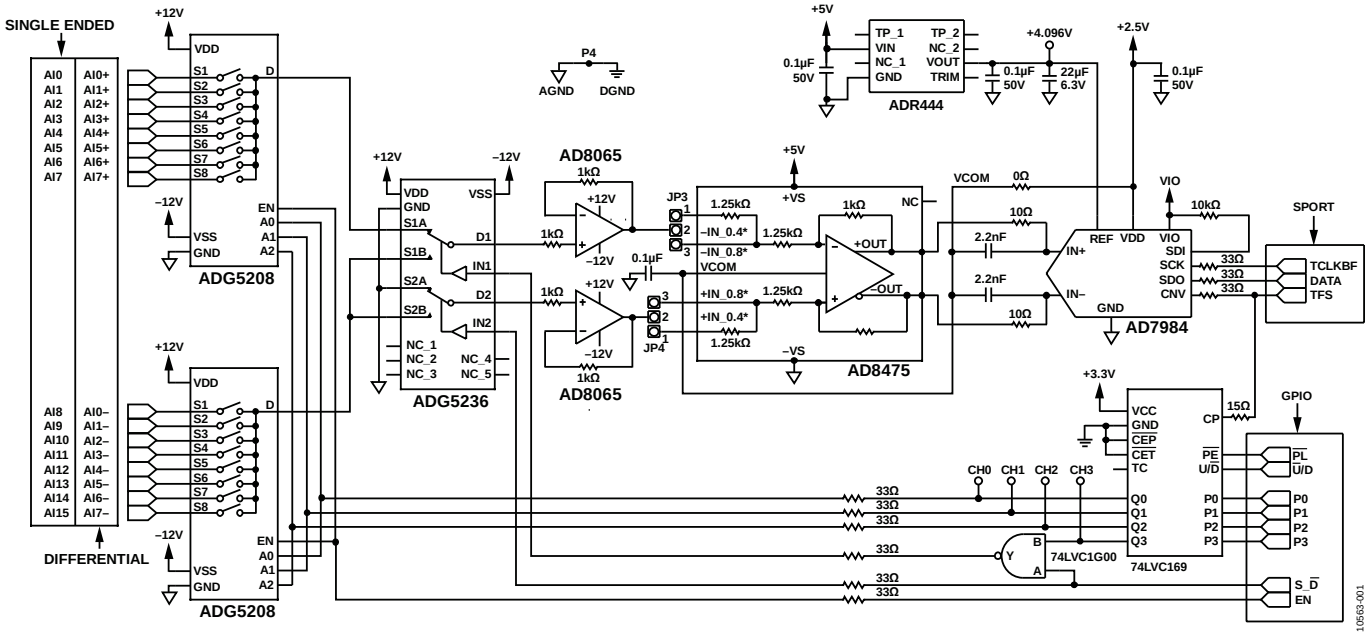

Figure 1. Multichannel Data Acquisition Circuit (Simplified Schematic: All Components, Connections, and Decoupling Not Shown)

Rev. 0

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Fax: 781.461.3113

This circuit is an ideal solution for a multichannel data acquisition card for many industrial applications including process control, and power line monitoring.

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is a classic multichannel non-synchronous data acquisition signal chain consisting of a multiplexer, amplifiers, and an ADC.

The architecture allows fast sampling of multiple channels using a single ADC, providing low cost and excellent channel-to-channel matching.

Channel-to-channel switching speed is limited by the settling time of the various components following the multiplexer in the signal chain, because the multiplexer can present a full-scale step voltage output to the downstream amplifier and ADC. The components in this circuit have been specifically chosen to minimize the settling time and maximize channel-to-channel switching speed.

Component Selection

The ADG5208 multiplexer switches one of eight inputs to a common output, as determined by the 3-bit binary address lines. The ADG5236 contains two independently selectable single-pole/double throw (SPDT) switches. Two ADG5208 switches, combined with one ADG5236, allow 16 single-ended channels or 8 true differential channels to be connected to the rest of the signal chain using a 4-bit digital control signal.

The 4-bit digital signal is generated by a 4-bit binary up/down counter triggered by the same signal used for the convert (CNV) input to the 18-bit, 1.33 MSPS AD7984 ADC.

The AD8065 JFET input op amp has a 145 MHz bandwidth and is configured as a unity-gain buffer to provide excellent settling time performance and extremely high input impedance. The AD8065 also provides very low impedance output to drive the AD8475 funnel amp attenuation stage.

The advantages of fully differential signal chain are good common-mode rejection and reduction in second-order distortion products. In order to process ±10 V industrial level signals by modern low voltage differential input ADCs, the attenuation and level shifting stage is necessary.

The AD8475, fully differential, attenuating (funnel) amplifier with integrated precision gain resistors provides precision attenuation (by 0.4× or 0.8×), common-mode level shifting, and single-ended-to-differential conversion along with input overvoltage protection. Fast settling time (50 ns to 0.001%), and low noise performance (10 nV/√Hz) make the AD8475 well suited to drive 18-bit differential input ADCs at sampling rates up to 4 MSPS.

The AD7984, 18-bit, PulSAR® ADC selected in this circuit provides 18-bit resolution at 1.33 MSPS when sampling a single channel. However, the settling time of various components in the signal chain limit the overall accuracy when sequentially switching between channels. For example, 16-bit performance is achieved when switching between channels at a 250 kHz rate.

Timing Analysis

When the circuit shown in Figure 1 is operating in the continuous switching mode, all the 16-channel signal-ended or 8-channel differential signal streams are merged into a time-division multiplexed signal by the two stage multiplexer comprised of the ADG5208 and the ADG5236. The multiplexed signal drives the buffer circuit (AD8065) and the attenuation and level shift circuit (AD8475). The output signal of the AD8475 drives the differential input ADC through an RC filter (2.2 nF, 10 Ω).

The multiplexed input signal typically consists of large voltage steps when switching between channels. In the worst case, one channel is at negative full scale, while the next channel is at positive full scale. Therefore, the step can be as large as the full range of input signal, in this case, 20 V. It is a tremendous challenge for the analog signal chain to settle to high precision from such a large step signal level in a short time. The timing of the circuit must be carefully examined to determine the amount of settling time available at various sampling rates and the settling time required by the circuits in the signal chain.

Figure 2 shows the basic timing diagram of the system, and this is where the analysis starts.

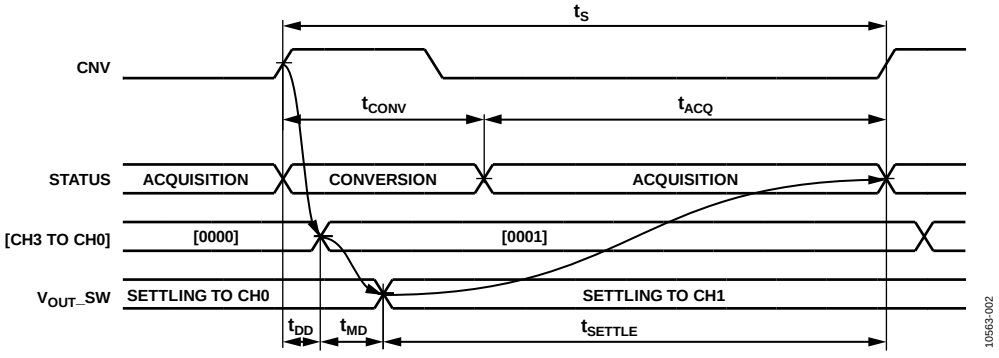

Figure 2. Multichannel Data Acquisition Circuit Timing

Digital Delay

In the circuit shown in Figure 1, the ADC and multiplexer are both triggered by the rising edge of CNV signal from digital controller. At this point, the SAR ADC has completed the acquisition of the sample and starts the conversion cycle.

Ideally, the signal chain has one full sampling period to settle to the next channel, but there are delays in the digital circuits that decrease the available settling time. In Figure 2, t_{DD} is the sum of the delay through the NAND gate and the counter CLK-to-OUT delay. This digital delay can be found from the data sheet of each component, and is approximately 8 ns total.

The time shown as t_{MD} in Figure 2 is the delay through the two stage multiplexer measured from the 50% point of the digital input to the point that the analog output signal starts to settle.

Since the ADG5208 and ADG5236 are switched simultaneously in this circuit, the t_{MD} marked in Figure 2 is equal to the delay generated by the slower one, which is the ADG5208.

The transition time delay of multiplexer is easy to find in the data sheet. However, the transition delay on the data sheet is the delay time between the 50% of the digital input and the 90% point of the digital output as shown in Figure 3.

So t_{MD} is calculated using the equation:

$$t_{MD} = t_{TRANSITION} - t_{SETTLE\ (90\%)} \quad (1)$$

The maximum settling time left for analog signal chain at a sampling rate of f_S can be estimated by the equation:

$$t_{SETTLE(fs)} = 1/f_S - t_{DD} - t_{MD} \quad (2)$$

A good first order approximation for estimating multiplexer settling time is to treat the multiplexer in the on state as a simple RC circuit with time constant of $R_{ON} \times C_D$.

The time for switch to settle to within a *% error* can be calculated by the equation below. See the AN-1024 Application Note, "How to Calculate the Settling Time and Sampling Rate of a Multiplexer" for more details.

The test circuit for measuring the transition delay with a load of 300 Ω||35 pF is shown in Figure 3. Under this test configuration, the settling time can be estimated by Equation 3.

$$t_{SETTLE} = -\ln\left(\frac{\%\,error}{100}\right)\left(\frac{R_{ON}\,R_L}{R_{ON}+R_L}\right)(C_D + C_L) \quad (3)$$

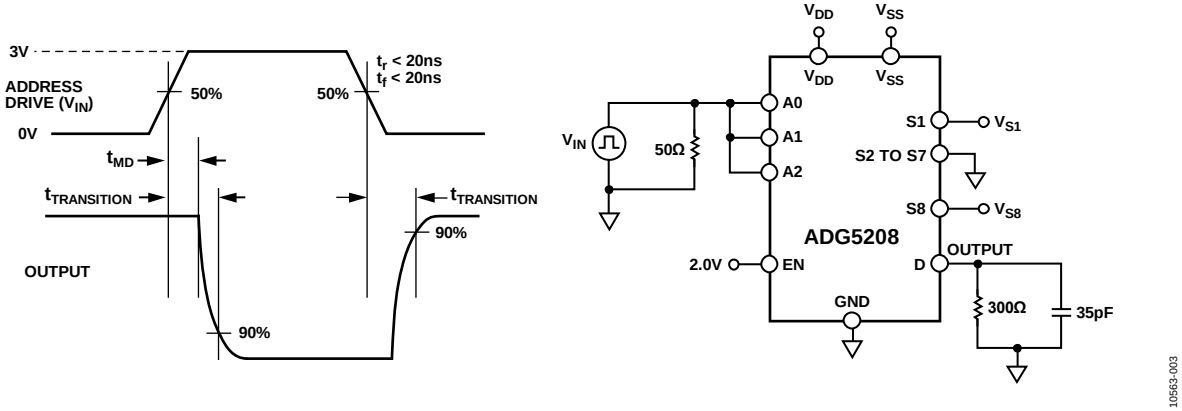

Figure 3. ADG5208 Transition Delay Test Circuit

For the ADG5208, R_{ON} is 160 Ω, and C_D is 52 pF. The transition delay of ADG5208 is 160 ns. So, the 90% settling time of the ADG5208 is

$$t_{SETTLE\ (90\%)} = -\ln\left(\frac{10}{100}\right)(160 \,||\, 300\ \Omega)(52\ \text{pF} + 35\ \text{pF}) = 21\ \text{ns}$$

From Equation 1,

$t_{MD} = t_{TRANSITION} - t_{SETTLE(90\%)} = 160\ \text{ns} - 21\ \text{ns} = 139\ \text{ns}$

Therefore, under this circuit configuration with the ADG5208 and the ADG5236, the total extra time delay due to the digital circuits is

$t_{DD} + t_{MD} = 8\ \text{ns} + 139\ \text{ns} = 147\ \text{ns}$

Actually, this digital delay of 147 ns due to the digital control circuit and part of the transition delay from multiplexer can be compensated by delaying the rising edge of the convert signal with respect to the multiplexer update signal by an amount of time equal to $t_{DD} + t_{MD}$. However, both t_{DD} and t_{MD} are a function of temperature, power supply voltage, and normal variations from part to part. The time margin must be enough to account for the variation and drift. For example, under this configuration with 147 ns digital delay, switching the multiplexer 100 ns to 120 ns ahead of the ADC convert signal (t_{AHEAD}) increases the available settling time by the same amount.

The optimized timing is shown in Figure 4, but was not implemented in the actual circuit in order to minimize complexity.

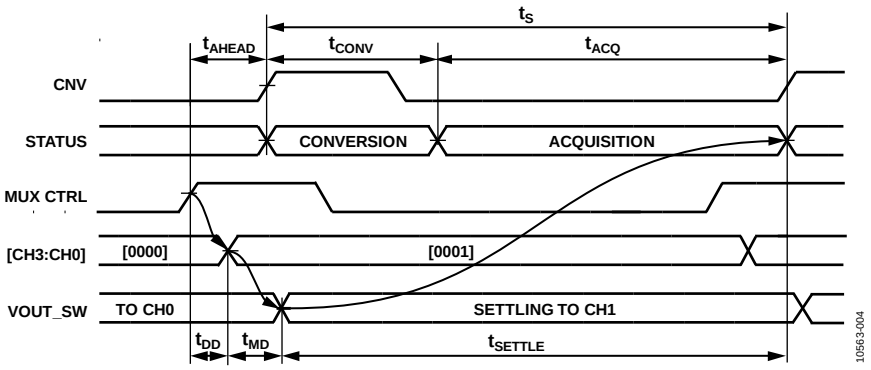

Figure 4. Optimized Timing of Multichannel Data Acquisition Circuit

Settling Time Analysis

When the circuit shown in Figure 1 is operating in the continuous switching mode, all the 16-channel signal-ended or 8-channel differential signal streams are merged into a time-division multiplexed signal by the two stage multiplexer, the ADG5208 and ADG5236. The signal is then buffered by the AD8065 that has a high impedance, low capacitance input.

Then the low impedance output of AD8065 buffer drives the AD8475 stage that attenuates, level shifts, and performs the single-ended to differential conversion. An RC (10 Ω, 2.2 nF) filter is placed at the input of the AD7984 ADC in order to limit out-of-band noise and attenuate the kickback from the switched capacitor input of the ADC. The −3 dB bandwidth of the filter is 7.2 MHz. (See *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converters*, Analog Dialogue 46-12, December 2012).

For the purposes of calculating settling time, the circuit can be divided into four parts as shown in Figure 5.

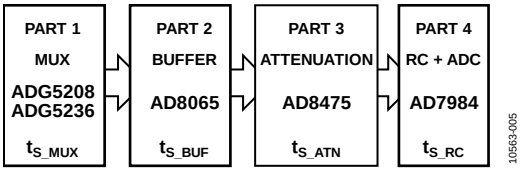

Figure 5. Sub-Stage Block Diagram for Settling Time Analysis

Then the total settling time is estimated to be the root sum square (rss) of settling time of each stage

$$t_{S\_ALL} = \sqrt{t_{S\_MUX}^{2} + t_{S\_BUF}^{2} + t_{S\_ATN}^{2} + t_{S\_RC}^{2}}$$

In order to settle to within a specific error band at a sampling rate, f_S , the relationship below must be satisfied.

$$t_{S\_ALL} + t_{DD} + t_{MD} < 1/f_S$$

Or, $f_S < 1/(t_{S\_ALL} + t_{DD} + t_{MD})$

Settling Time for the Multiplexer Stage

The equivalent circuit for a CMOS switch can be approximated as an ideal switch in series with a resistor (R_{ON}) and in parallel with two capacitors (C_S, C_D). The multiplexer stage and associated filters can therefore be modeled as shown in Figure 6.

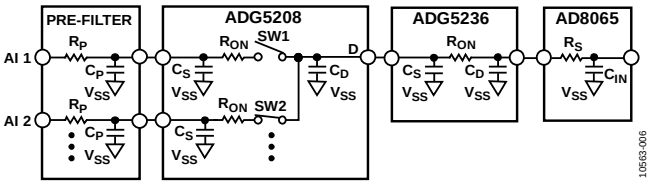

Figure 6. First-Order Model for Input Pre-Filter, Multiplexer, and AD8065 Input

Note that the ADG5236 model does not show the series switch because it only switches when changing from single-ended to differential mode inputs.

The pre-filter in front of multiplexer is not shown in Figure 1. This pre-filter is used for noise suppression. Also, the R_P resistor combined with protection diodes and the TVS provides additional transient and over-voltage protection for hostile environments. The protection components are shown in the complete circuit schematic contained in the CN-0269 Design Support Package.

The R_S is the 1 kΩ resistor in series with non-inverting input of the AD8065, and C_{IN} is the input capacitance of AD8065. The input impedance of AD8065 is 1 GΩ||2.2 pF, and the 1 GΩ resistance can be ignored.

The circuit in Figure 6 was simulated using NI Multisim™ as shown in Figure 7, with the following component values:

Pre-filter: R_P = 300 Ω; C_P = 120 pF;

ADG5208: R_{ON} =160 Ω; C_S = 5.5 pF; C_D = 52 pF;

ADG5236: R_{ON} =160 Ω; C_S = 2.5 pF; C_D = 12 pF;

AD8065: R_S =1 kΩ; C_{IN} = 2.2 pF;

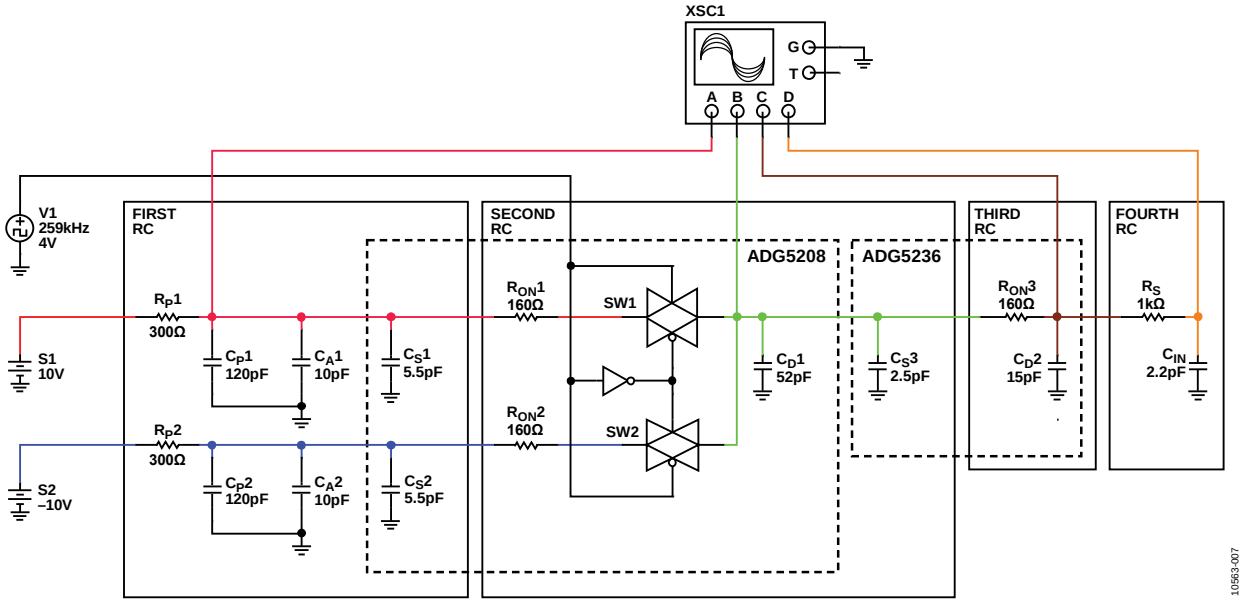

Figure 7. NI Multisim Simulation Circuit for the Pre-Filter, Multiplexer, and AD8065 Input

The simulation result is shown in Figure 8. From the simulation result, the settling of the circuit shown in Figure 7 is:

t_{S_MUX} = 10.1300 − 8.0011 = 2.129 µs

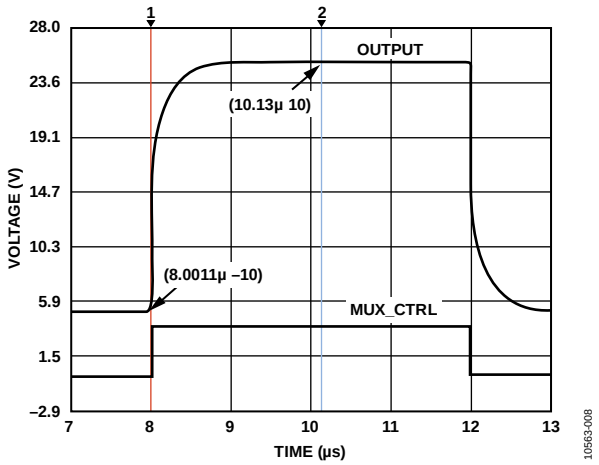

Figure 8. Pre-Filter, Multiplexer, and AD8065 Input Settling Time Simulation

Because the multiplexer settling time is 2.1 µs, this will limit the maximum throughput rate per channel to 476 kSPS (1/2.1 µs), even if the multiplexer was the only element in the signal chain. Since the settling time contributions of each stage in the signal chain add on an rss basis, stages having settling times of less than approximately 2.1 µs ÷ 3 = 700 ns will have a minimum effect on the total settling time.

Settling Time for AD8065 Buffer and AD8475 Attenuation Stages

The settling time of an amplifier is defined as the time it takes the output to respond to a step change at the input and come into and remain within a defined error band, as measured relative to the 50% point of the input pulse, as shown in Figure 9.

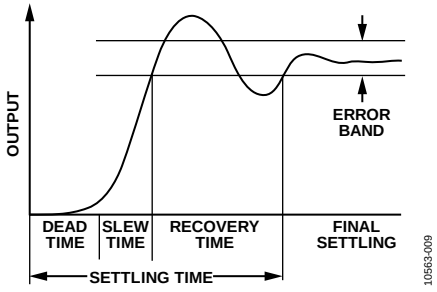

Figure 9. Settling Time of an Op Amp

The error band is usually defined to be a specific percentage of the step, such as 0.1%, 0.01%, 0.001%, etc. As shown in Figure 9, the dead time, slew time, and recovery time together constitute the total settling time.

For a high speed fast settling op amp, such as AD8065, the dead time is only a small percentage of the total settling time and can usually be ignored.

Op amp settling time is nonlinear; it may take 30 times as long to settle to 0.01% as to 0.1%. Thermal effects within the op amp can cause the op amp to take hundreds of microseconds to settle to 0.01%, although 0.1% settling may be less than 100 ns. Some op amps that have a settling time specified to 0.1% may never settle to 0.01% or 0.001% due to low amplitude ringing and/or long term thermal effects.

Settling time is also a function of the op amp closed-loop gain and the feedback network, as well as the compensation. Settling time depends on the amplitude of the output voltage step. A large output step generally has a longer settling time than a small one.

Measuring 0.01% or 0.001% settling time for a 10 V or 20 V output step is an extremely difficult task due to the effects of oscilloscope overdrive, sensitivity, and the difficulty of generating an input pulse that settles to the required accuracy.

The AD8065 op amp has a 0.1% settling time specification of 250 ns for a 10 V output step and a slew rate of 180 V/µs. The slew time for the output to swing 10 V is approximately 55 ns, and the slew time for a 20 V output step is approximately 110 ns. We can estimate the 0.1 % settling time for a 20 V step by adding the additional slew time to the specification for a 10 V step, and obtain approximately 250 ns + 55 ns = 305 ns. Based on empirical data, we will assume the 0.01% settling time is approximately 600 ns for a 20 V output step.

The AD8475 differential attenuating amplifier has a settling time specification of 50 ns to 0.0001%, and a slew rate of 50 V/µs for a 2 V output step. In the circuit, the output is 8 V, so assuming that the settling time is proportional to the output voltage step, the 8 V settling time will be approximately 200 ns.

Settling Time for the Noise Filter and the AD7984 ADC

The AD7984 ADC is a member of the PulSAR® family and is based on a charge-redistribution digital-to-analog converter capacitive DAC. The output code is determined in two phases. The first phase is the *acquisition* phase. The internal capacitive DAC is switched to the ADC input pins in order to acquire the signal. The external support circuitry driving the ADC input must be able to settle to the required voltage at the end of acquisition phase. The ADC then enters the *conversion* phase, and the capacitive DAC is disconnected from the input. The conversion is then performed during this phase using the SAR conversion algorithm.

The equivalent analog input circuit combined with the external RC filter is shown in Figure 10. The R_{EXT} and C_{EXT} are the external filter in front of the ADC, which is 10 Ω and 2.2 nF in this circuit. The pin capacitance (C_{PIN}) of several pF can be ignored because of the large C_{EXT}.The value of R_{IN} is typically 400 Ω, and C_{IN} is typically 30 pF.

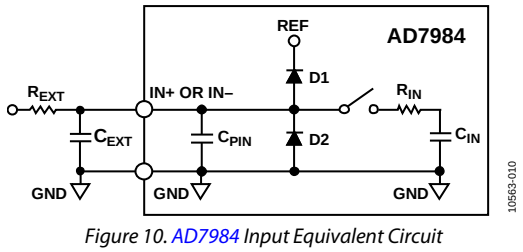

Figure 10. AD7984 Input Equivalent Circuit

During the conversion phase, the switch is open and the R_{EXT} and C_{EXT} time constant determines the input settling time.

When the switch is closed and the ADC enters the acquisition phase, the internal R_{IN} and C_{IN} is connected in parallel with the external network, and a charge transient can be injected onto the input.

In this circuit, with a 0.4× gain of the AD8475 and a 20 V single-ended input step, the voltage step into the AD7984 is 4 V single-ended and 8 V differential.

When the step voltage is initially applied, the AD8475 is in the conversion mode, and the switch is open. The R_{EXT} and C_{EXT} time constant is 22 ns, and 12.48 time constants is 275 ns (time required to settle to 18 bits shown in Table 1), which is less than the 500 ns allowable conversion time when sampling at 1 MSPS.

When the AD7984 enters the acquisition mode at the end of the 500 ns interval, the switch closes. At this point, the voltage at the RC filter input can be positive full-scale, and the voltage on C_{IN} can be negative full-scale, or vice-versa. The settling time of the voltage across C_{IN} is now a function of R_{EXT}, C_{EXT}, R_{IN}, and C_{IN}.

The settling time for this circuit can be simulated by the Multisim and is shown in Figure 11. The SIN is a component of Multisim named PULSE_VOLTAGE which provides the 4 V step input with 50% duty cycle. Another PULSE_VOLTAGE in Figure 11 is SW_ADC. This PULSE_VOLTAGE combined with ideal switch A1 controls the CONVERSION and ACQUISITION cycle timing of the SAR ADC. The pulse is 500 ns wide which equals the CONVERSION time of the AD7984. The 5 µs is the half-period of the input switching signal. The SIN and SW_ADC are controlled by the same phase of the clock. The switch A1 is open during the first 500 ns after SIN is switched. Switch A1 then closes, allowing the capacitive DAC to acquire the input signal from the external RC filter.

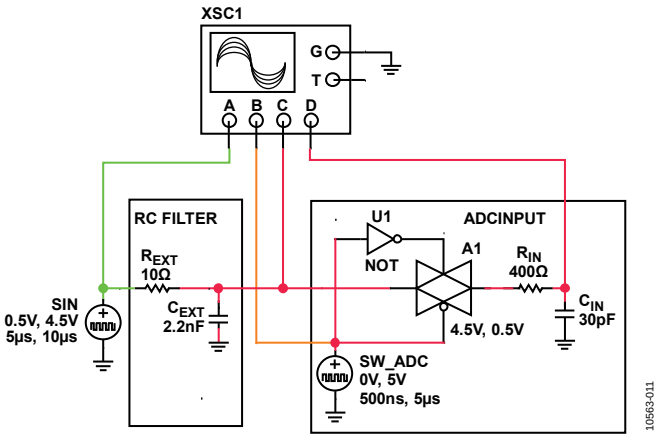

Figure 11. Multisim Settling Time Model of the AD7984 Front End

The simulation result is shown in Figure 12. The blue label shows that the voltage on C_{IN} settled to 4 V with 18-bit accuracy 469 ns after the input step signal. Therefore the total settling time of the front end of the AD7984 is t_{SRC} = 469 ns.

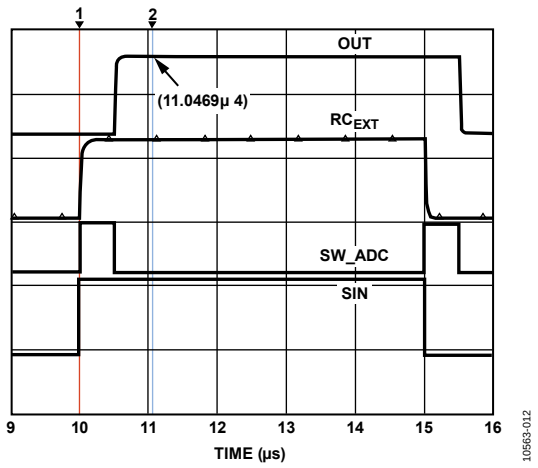

Figure 12. Settling Time Waveforms for AD7984 Front End Simulation Model

Table 1 is useful and shows the number of time constants required to settle to a given accuracy for a simple RC network.

Table 1. Number of Time Constants Required to Settle to a Given Accuracy for an Simple RC Network

Resolution, No. of Bits	LSB (%FS)	No. of Time Constants = −ln (%Error/100)
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

The total settling time of the entire circuit shown in Figure 1 can now be estimated:

$$t_{S\_ALL} = \sqrt{t_{S\_MUX}^{\ 2} + t_{S\_BUF}^{\ 2} + t_{S\_ATN}^{\ 2} + t_{S\_RC}^{\ 2}}$$

$$= \sqrt{2129^2 + 600^2 + 200^2 + 469^2} = 2270\ \text{ns}$$

Therefore for settling to 18 bits, the maximum switching rate of this circuit is:

$$f_S < 1/(2270\ \text{ns} + 147\ \text{ns}) = 414\ \text{kHz}$$

Noise Analysis

The Noise of the AD8065 Buffer Stage

The noise sources in the signal chain of this circuit are the thermal noise from resistors and the voltage and current noise from the AD8065 and the AD8475. The on resistance of the two switches is small enough to ignore.

A simplified noise analysis model for the AD8065 circuit is shown in Figure 13.

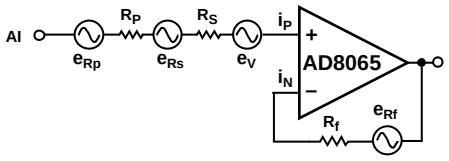

Figure 13. AD8065 Noise Model

The noise sources shown in Figure 13 must be converted to the output by multiplying the noise gain, which is 1 for a unity-gain buffer.

$$e_{AD8065\_RTO} =$$

$$\sqrt{e_{RP}^{\ 2} + e_{RS}^{\ 2} + e_{Rf}^{\ 2} + e_{V}^{\ 2} + (R_P + R_S)^2 i_p^{\ 2} + R_f^{\ 2} i_p^{\ 2}}$$

The noise from resistors can be calculated from the equation:

$$e_R = 4 \times \sqrt{\frac{R}{1000}}\ \text{nV}/\sqrt{\text{Hz}}\ \text{ at 25°C}$$

where R is in Ω.

e_{RP} = 2.2 nV/√Hz

$e_{RS} = e_{Rf}$ = 4 nV/√Hz

e_V = 7 nV/√Hz

$i_p = i_N$ = 1 pA/√Hz

$e_{VAD8065}$ = 10 nV/√Hz

The Noise of the AD8475 Attenuation Stage

The e_{AD8065_RTO} term is the noise from the circuit at the input to AD8475 stage. This noise is reflected to the output of the AD8475 by multiplying the signal gain (0.4) of AD8475 stage as shown in Figure 14.

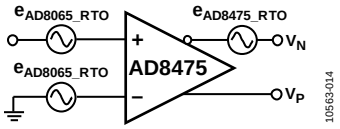

Figure 14. AD8475 Noise Model

The AD8475 output voltage noise is also 10 nV/√Hz, including amplifier voltage and current noise, as well as noise of internal resistors.

The noise density of the whole signal chain in front of ADC is

$$e_{TOTAL\_GAIN} = \sqrt{2 \times \left(GAIN_{AD8475} \times e_{AD8475\_RTO}\right)^2 + e_{AD8475\_RTO}^{\ 2}}$$

For the ±10 V input range, the $GAIN_{AD8475}$ = 0.4.

$e_{TOTAL\_0.4}$ = 11.5 nV/√Hz

For the ±5 V input range, the $GAIN_{AD8475}$ = 0.8.

$e_{TOTAL\_0.8}$ = 15.1 nV/√Hz

The total output noise of the AD8475 is applied to the RC filter (10 Ω, 2.2 nF) that has a bandwidth of 7.23 MHz. The bandwidth of the AD8065 is 145 MHz, and the bandwidth of the AD8475 is 150 MHz. The input bandwidth of the AD7984 ADC is 10 MHz, therefore the noise at the input of the AD7984 is limited by the RC noise filter to 7.23 MHz.

When the AD8475 is operating at a gain of 0.8 (worst case noise condition) the input rms noise to the ADC is therefore

$$V_{TOTAL\_RMS} = (15.1\text{nV}/\sqrt{\text{Hz}} \times \sqrt{1.57 \times 7.23\ \text{MHz}} = 51\ \mu\text{V}$$

V_{TOTAL_PP} = 6.6 × 51 µV = 337 µV

For the 18-bit AD7984 with reference voltage of 4.096 V, the differential input span is 8.196 V. The LSB value is 31 µV. The peak-to-peak noise of 337 µV therefore corresponds to 11 LSBs peak-to-peak.

Effect of Multiplexer Switching Transients

The multiplexer has source and drain capacitance. The drain capacitance of the multiplexer holds the voltage of previous input channel. When the multiplexer switches to the next channel, this can create a transient or kick-back glitch through the R_{ON} resistance. This transient can affect the next conversion. Therefore, the pre-filter driver needs to have a very low output impedance and a fast settling time to the transient.

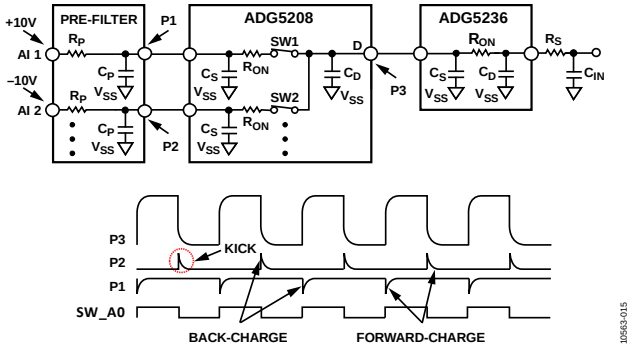

Figure 15. Multiplexer Switching Transients

The driver needs to be able to charge the input to the required accuracy (forward-charge) before the switch opens. The back-charge occurs when the switch opens, and generally is short and doesn't present a problem.

In order to make the circuit easy to drive, a buffer can be placed in front of the multiplexer (front buffer). The evaluation board EVAL-CN0269-SDPZ has footprints for the input buffer on each input channel and has an AD8065 installed in Channel 1 to Channel 4. Adding the buffer slightly increases the noise density and the settling time. However, in a practical application, the parasitic inductance and capacitance from the input cable or terminal connector will significantly increase the time of settling time and generate ringing due to the forward and back charge without the buffer. The additional input buffer isolates the parasitic effects and provides very low impedance to the multiplexer. The difference in performance between the circuit with or without input buffer is shown in the test part of this circuit note.

Another reason for adding the input buffer is for that an additional filter can be placed ahead of it for anti-aliasing and noise reduction.

Histogram Test Results

Figure 16 shows the results of a 10,000 sample histogram taken by shorting the 16 single-ended channels together and connecting them to the GND of the PCB. Note that the peak-to-peak noise is approximately 12 LSBs, including the input buffer.

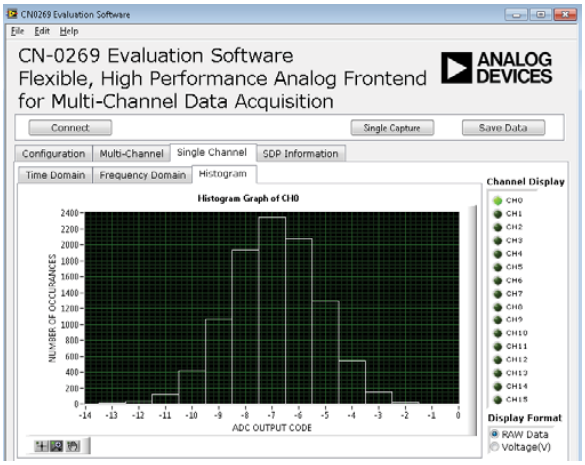

Figure 16. DC Histogram at 0 V Input, 1 MSPS Sampling Rate, 10,000 Samples

AC Test Results

The ac performance was tested at the system level with the AD7984 sampling at 300 kSPS with 2.5 V p-p 10.675 kHz input sine wave signal provided by a Type 1051 B&K sine generator,. The circuit was sampling continuously on Channel 4, and does not include the effects of the input buffer. The FFT shows an SNR = 91.33 dBFS.

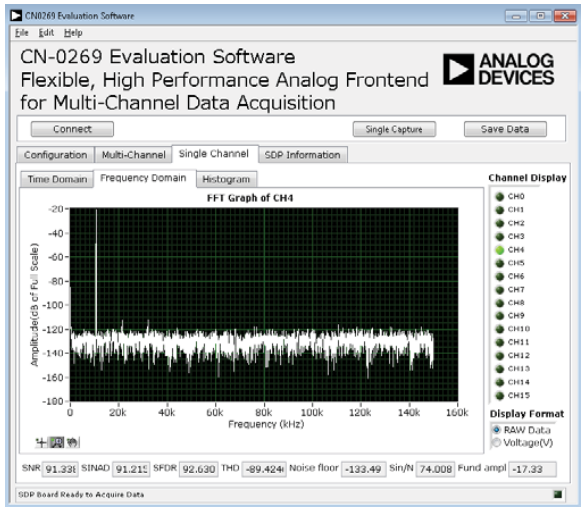

Figure 17. FFT with a Kaiser Window (Parameter = 20), 2.5 V p-p 10.675 kHz Input, 300 kSPS Sampling Rate on CH4 Without Input Buffer

Switching Speed and Settling Time Test Results

The follow figures show the settling performance. The lab test setup is shown in Figure 18.

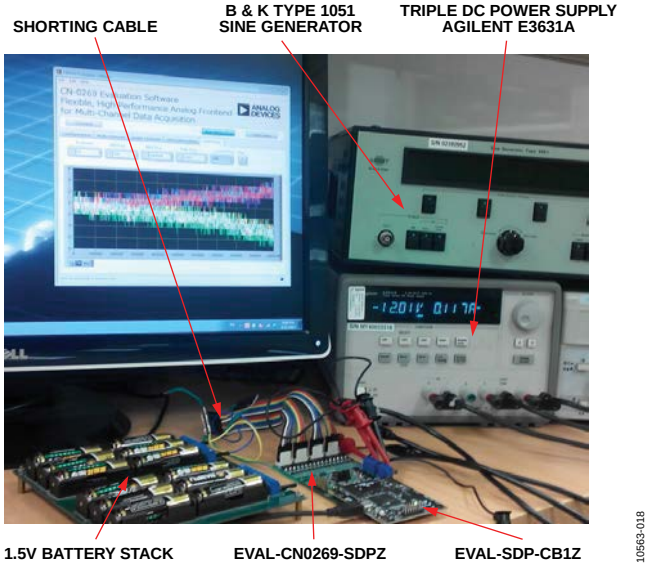

Figure 18. Switching Speed and Settling Time Lab Test Setup

The CN-0269 evaluation board was configured in the 16-channel singled input mode, the 8 odd channels were shorted together, and the 8 even channels were shorted together.

A battery stack was used to generate the different dc input voltages for low noise and low impedance.

The odd and even channels were connected to different voltages. The LabVIEW™ software controls the EVAL-SDP-CB1Z channel-to-channel and switches continually between the input channels. The switching rate was varied from 100 Hz to 1 MHz in 1 kHz increments. There were 10 samples taken at each switching rate, and the results averaged. The average value at the lowest switching rate was used as a reference point. The error at each different switching rate was calculated by taking the difference between the 10-sample and the reference value. The test results are shown in Figure 19 to Figure 23.

In the figures, an error of 2 LSBs corresponds to 17-bit settling, and an error of 4 LSBs corresponds to 16-bit settling.

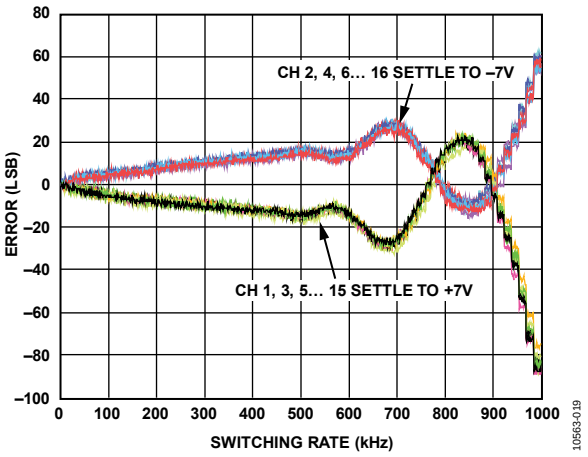

Figure 19. Errors vs. Switching Rate Without Front Buffer at 16-Channel Single-Ended, 14 V Step

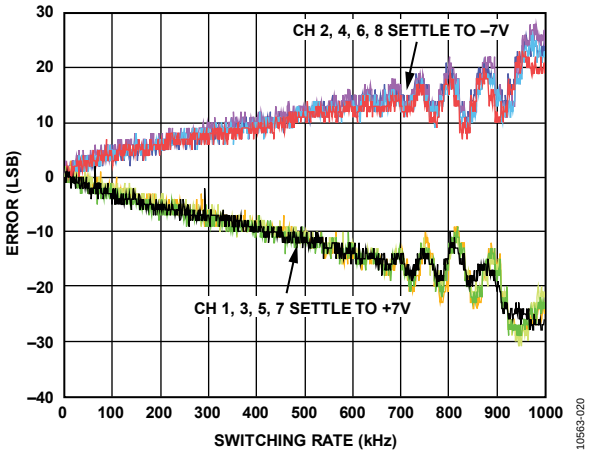

Figure 20. Errors vs. Switching Rate Without Input Buffer, 8-Channel Differential Mode, 14 V Step

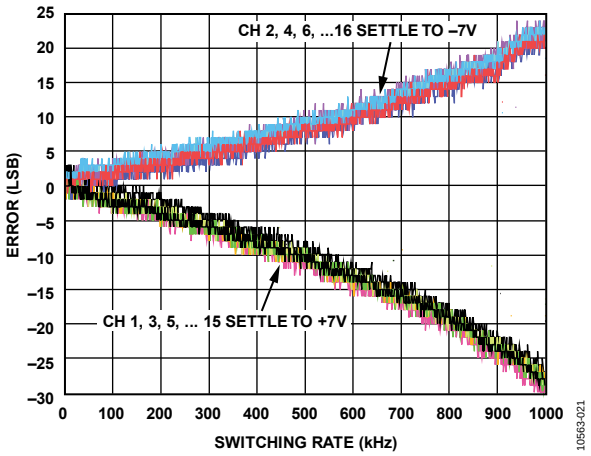

Figure 21. Errors vs. Switching Rate with Input Buffer, 16-Channel Single-Ended Mode, 14 V Step

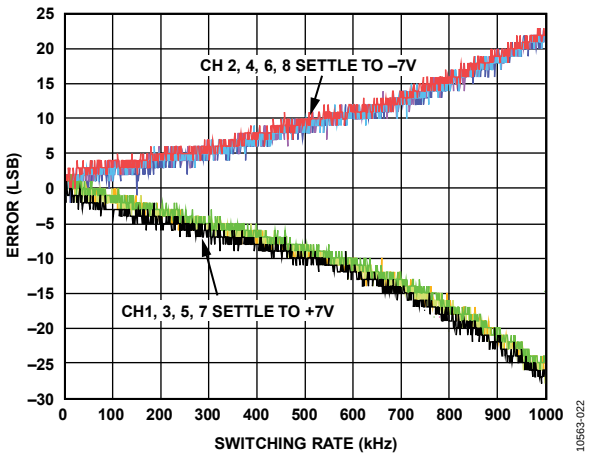

Figure 22. Errors vs. Switching Rate with Front Buffer, 8-Channel Differential Mode, 14 V Step

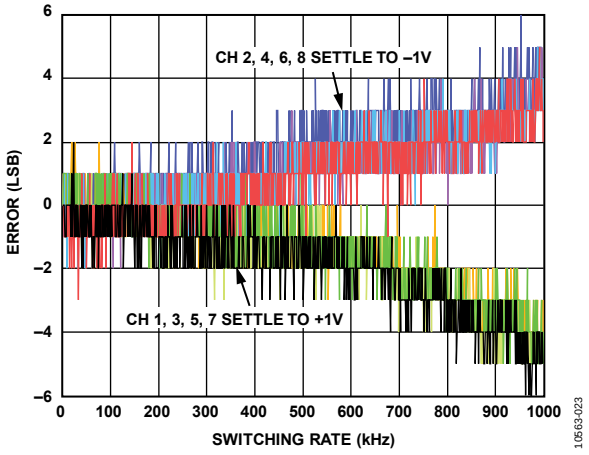

Figure 23. Errors vs. Switching Rate with Input Buffer, 8-Channel Differential Mode, 2 V Step

From the figures above, we can see the circuit with the input buffer has a better settling performance than the circuit without front buffer at switching rates less than 1 MHz.

Figure 21, Figure 22, and Figure 23 show that with the input buffer connected the circuit settles to 16 bits at channel-to-channel switching rates up to 250 kHz.

COMMON VARIATIONS

The 18-bit AD7984 is available in a 10-lead MSOP or a 10-lead QFN (LFCSP) package. There are a number of other PulSAR ADCs available in the same package with 14-bit, 16-bit, and 18-bit resolutions having various sampling rates.

Another possible choice for the buffer amplifiers is the AD8021. If programmable gain is required, the AD8250, AD8251, and AD8253 have 685 ns settling time to 0.001%. The ADG12xx series of multiplexers can be used if lower capacitance is required.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0269-SDPZ circuit board and the EVAL-SDP-CB1Z SDP-B System Demonstration Platform controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The EVAL-CN0269-SDPZ board contains the circuit to be evaluated, as described in this note, and the SDP-B controller board is used with the CN-0269 evaluation software to capture the data from the EVAL-CN0269-SDPZ circuit board.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP (32 bit), Windows Vista®, or Windows 7
- EVAL-CN0269-SDPZ circuit board
- EVAL-SDP-CB1Z SDP-B controller board
- CN-0269 SDP Evaluation Software
- 6 V dc (500 mA), ±12 V(300 mA) power supply
- Low distortion signal generator to provide ±10 V output with frequency from dc to 1MHz

Getting Started

Load the evaluation software by placing the CN-0269 evaluation software into the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software.

Functional Block Diagram

See Figure 1 for the circuit block diagram and the **EVAL-CN0269-SDPZ-SCH-RevX.pdf** file for the complete circuit schematic. This file is contained in the CN-0269 Design Support Package. A functional block diagram of the test setup is shown in Figure 24.

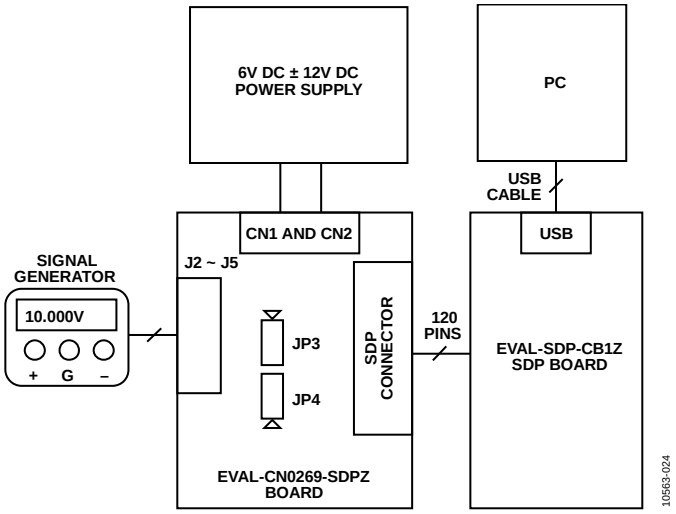

Figure 24. Test Setup Block Diagram

Setup

Connect the 120-pin connector on the EVAL-CN0269-SDPZ circuit board to the **CON A** connector on the EVAL-SDP-CB1Z controller board (SDP-B). Use nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V and ±12 V dc power supply to the pins on CN1, CN2 marked with +6 V, ±12 V and GND on the board. If available, a 6 V wall wart can be connected to the barrel connector on the board and used in place of the 6 V power supply. Connect the USB cable supplied with the SDP-B board to the USB port on the PC. Do not connect the USB cable to the Mini-USB connector on the SDP-B board at this time. Turn on the 6 V and ±12 V power supply at the same time and then connect the USB cable to the Mini-USB connector.

Test

With the 6 V and ±12 V power supply on, launch the evaluation software. Once USB communications are established, the SDP-B board can be used to send, receive, and capture data from the EVAL-CN0269-SDPZ board and do the data analysis under time and frequency domain to evaluate the performance of the whole circuit.

Figure 25 shows a photo of the EVAL-CN0269-SDPZ evaluation board connected. Information regarding the SDP-B board can be found in the SDP-B User Guide.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0269 Software User Guide.

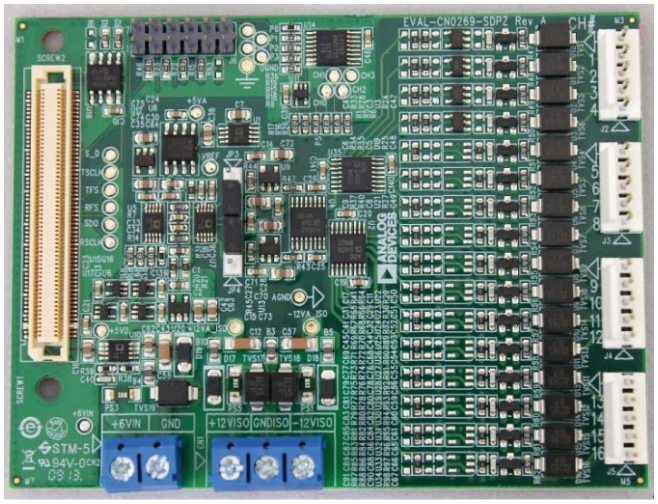

Figure 25. EVAL-CN0269-SDPZ Evaluation Board

Connectivity for Prototype Development

The EVAL-CN0269-SDPZ evaluation board is designed to be evaluated with the EVAL-SDP-CB1Z SDP-B board based on the Black-Fin DSP through SPORT port; however, any microprocessor can be used to interface to serial port of AD7984 through the 14 pin PMOD connector. In order for another controller to be used with the EVAL-CN0269-SDPZ evaluation board, software must be developed by a third party.

There are existing interposer boards that can be used to interface to the Altera and Xilinx field programmable gate arrays (FPGAs). The BeMicro SDK board from Altera can be used with the BeMicro SDK/SDP interposer using Nios Drivers. Any Xilinx evaluation board that features the FMC connector can be used with the FMC-SDP Interposer board.