ANALOG DEVICES

Circuit Note
CN-0276

Circuits from the Lab™ Reference Circuits

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Devices Connected/Referenced	
AD2S1210	Variable Resolution, 10-Bit to 16-Bit R/D Converter with Reference Oscillator
AD8397	Rail-to-Rail, High Output Current Amplifier
ADG1611/ ADG1612	1 Ω On Resistance, ±5 V, +12 V, +5 V, and +3.3 V Quad SPST Switches
ADM6328	Ultralow Power, 3-Lead, SOT-23 Microprocessor Reset Circuits
ADP7104	20 V, 500 mA, Low Noise, CMOS LDO
AD8692/ AD8694	Low Cost, Low Noise, Dual/Quad CMOS, RRO Op Amps

High Performance, 10-Bit to 16-Bit Resolver-to-Digital Converter

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0276 Circuit Evaluation Board (EVAL-CN0276-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a complete high performance resolver-to-digital (RDC) circuit that accurately measures angular position and velocity in automotive, avionics, and critical industrial applications where high reliability is required over a wide temperature range.

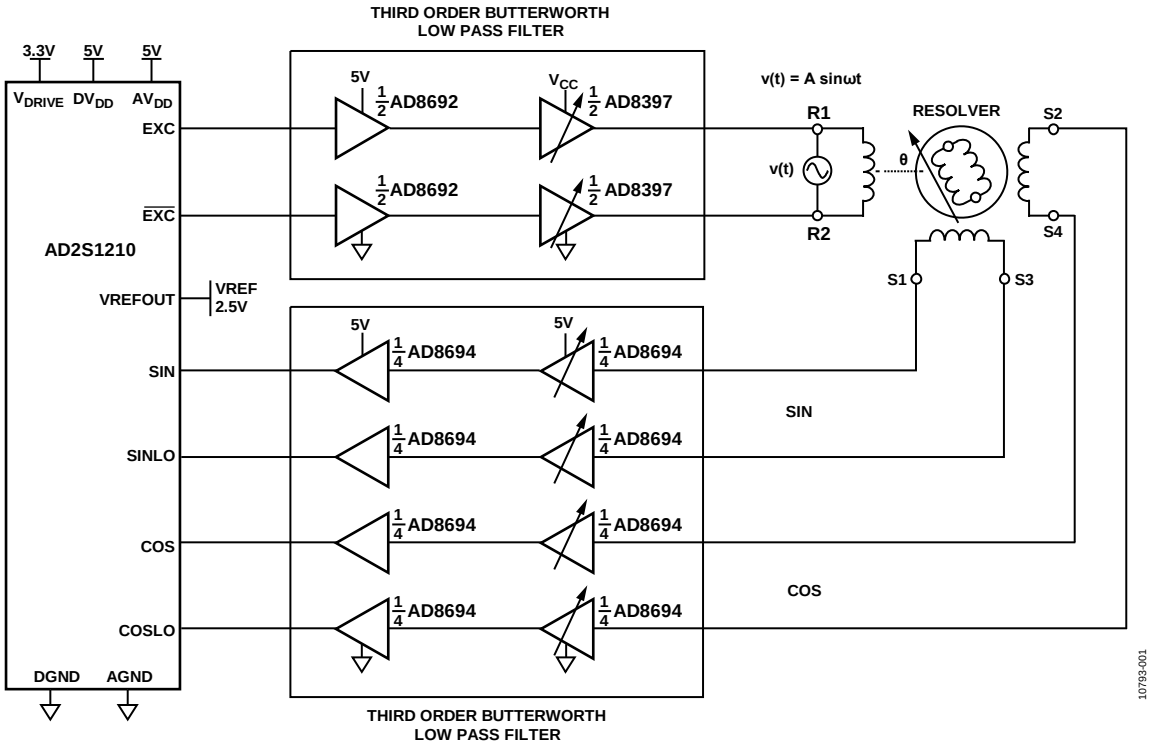

Figure 1. High Performance Resolver-to-Digital (RDC) Circuit. Simplified Schematic: All Components, Connections, and Decoupling Not Shown

Rev. 0

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The circuit has an innovative resolver rotor driver circuit that has two modes of operation: high performance and low power. In the high performance state, the system operates on a single 12 V supply and can supply 6.4 V rms (18 V p-p) to the resolver. In the low power state, the system operates on a single 6 V supply and can supply 3.2 V rms (9.2 V p-p) to the resolver, with less than 100 mA of current consumption. Active filtering is provided in both the driver and receiver to minimize the effects of quantization noise.

The maximum tracking rate of the RDC is 3125 rps in the 10-bit mode (resolution = 21 arc min) and 156.25 rps in the 16-bit mode (resolution = 19.8 arc sec).

CIRCUIT DESCRIPTION

The signal chain must be designed with care to consider not only amplitude and frequency, but also phase shift and stability. In addition, the resolver rotor winding impedance has both a resistive and an inductive component.

The AD2S1210 RDC excitation signal range is 2 kHz to 20 kHz and can be set in increments of 250 Hz. Most resolvers are specified at a fixed excitation fequency, typically around 10 kHz. Different resolvers have difference phase shifts that must also be considered in the signal chain design.

The excitation signal is applied to the resolver rotor winding which is a non-ideal inductor and has a typical resistive component of 50 Ω to 200 Ω and a reactive component of 0 Ω to 200 Ω. For example, the impedance of the Tamagawa TS2620N21E11 resolver used in the circuit of Figure 1 is 70 Ω + j100 Ω at 10 kHz.

Typical excitation voltages can be as high as 20 V p-p (7.1 V rms), so both maximum current and maximum power consumption of the resolver driver must be considered. The AD8397 was chosen for the circuit because of its wide supply range (24 V), high output current (310 mA peak into 32 Ω on ±12 V supplies), rail-to-rail output voltage, and low thermal resistance package (θ_{JA} = 47.2°C/W for the 8-pin SOIC EP package).

The excitation output signals from the AD2S1210 are generated from an internal DAC that produces a certain amount of quantization noise and distortion. For this reason, the dual AD8692 op amp is configured as a third-order active Butterworth filter in order to reduce the noise of the drive signals. Similarly, the SIN and COS receiver circuits use two quad AD8694 op amps as an active noise filter.

Signal Chain Design

These factors must be considered in the design of the signal chain:

- AD2S1210 excitation signal output range : 3.2 V min, 3.6 V typical, 4.0 V max
- AD8692 output voltage range: 0.29 V to 4.6 V with +5 V supply
- AD8397 output voltage range: 0.18 V to 5.87 V with +6 V supply.
- AD8397 output voltage range: 0.35 V to 11.7 V with +12 V supply
- Resolver(TS2620N21E11) transformation ratio: 0.5
- Resolver(TS2620N21E11) phase shift: 0°
- AD8694 output voltage range: 0.37 V to 4.6 V with +5 V supply
- AD2S1210 input differential p-p signal range (SIN, COS) is 2.3 V min, 3.15 V typ, 4.0 V max
- Resolver output SIN, COS loads should be equal.
- Resolver output loads should be at least 20 times the resolver output impedance
- Total signal chain phase shift range: $n \times 180° - 44° \leq \varphi \leq n \times 180° + 44°$, n is an integer.

Resolver Excitation Filter and Driver Circuits

The AD2S1210 excitation signal filter and power amplifier circuit are shown in Figure 2. Careful attention must be paid to the gain and signal levels at each point in the chain so that the AD8397 output driver does not saturate for the maximum excitation (EXE) of 4.0 V p-p from the AD2S1210. Note that because the resolver is driven differentially there are two identical channels as shown in Figure 2 corresponding to the true and complementary EXE outputs, respectively.

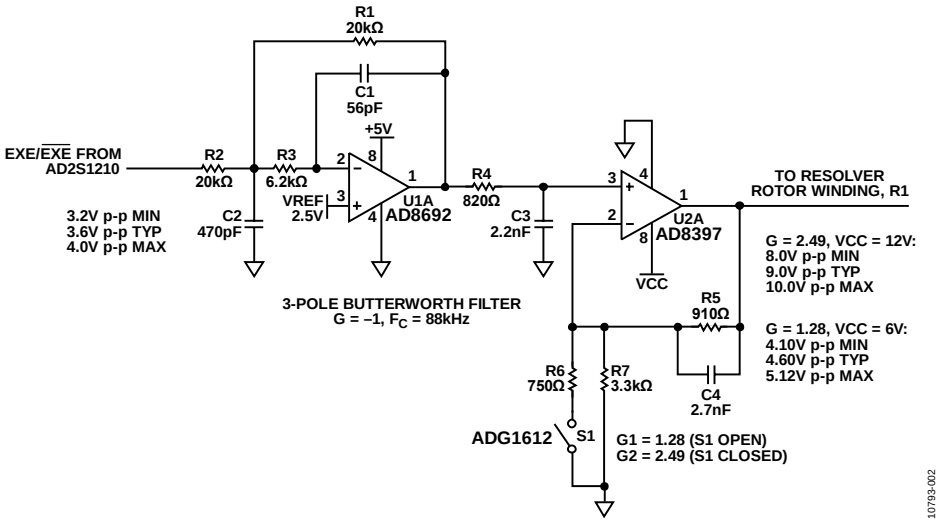

Figure 2. Excitation Driver and Filter Circuit (All Connections and Decoupling Not Shown)

The dc gain of the AD8692 filter circuit is −1. For the high performance mode (S1 closed), the gain of the AD8397 driver stage is set for 2.5 (2.49 using actual available resistor values) so that a 4.0 V p-p EXE input produces a 10 V p-p output when using a 12 V supply. This allows 1 V headroom from either rail at the output of the AD8397. For the low power mode (S1 open), the gain is set for 1.28 so that a 4.0 V p-p EXE input produces a 5.12 V p-p output when using a 6 V supply.

The ADG1612 has a typical on-resistance of less than 1 Ω and is ideal for the gain switch. However, because the off capacitance of the switch is typically 72 pF, it should not be connected directly to the input of the op amp. Note that in the circuit it connects R6 to ground, and when off, the capacitance has minimum effect on performance.

The AD8692 is configured as a multiple feedback (MFB) third order Butterworth lowpass filter. It should have a phase shift in range of 180° ± 15°. The design procedure is described in Chapter 8 of Linear Circuit Design Handbook. It is important to select the proper op amp for this filter, and as a general rule, the gain-bandwidth product of the op amp should be at least 20 times the −3dB cutoff frequency of the active filter. In this case, the cutoff frequency is 88 kHz, and the gain-bandwidth product of the AD8692 is 10 MHz, which is 113 times the cutoff frequency. Because the AD8692 is a CMOS op amp, the input bias current is low, and will not significantly affect the dc characteristics of the filter.The input capacitance is 7.5 pF which minimizes the effect on cutoff frequency for the capacitor values chosen in the filter design.

The −3dB cutoff frequency of the filter is 88 kHz, the phase shift is −13° at 10 kHz, and the dc gain is 1 at 10 kHz.

The AD8397 power amplifier can be configured with a gain of 1.28 (low gain mode) and 2.49 (high gain). Phase shift at 10 kHz in the low gain mode is −1.9°, and phase shift in the high gain mode is −5.2°.

The AD8692 third order low pass filter transfer function is shown in Figure 3.

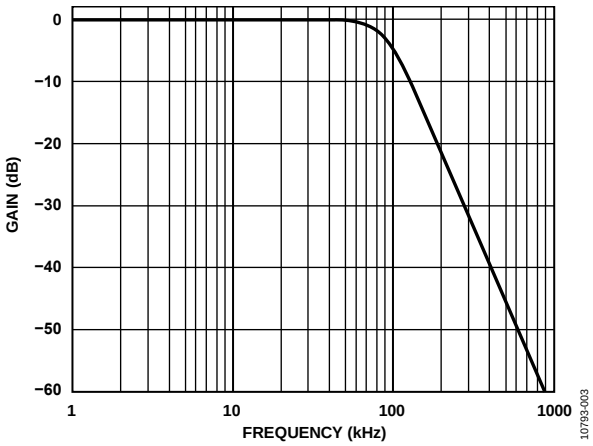

Figure 3. AD8692 Third-Order Low Pass Filter Response

The filter is very effective in reducing the noise on the excitation signals driving the resolver. Figure 4 shows the 10 kHz EXE signal measured directly at the output of the AD2S1210. Figure 5 shows the signal measured at C3 (input to AD8397) and the effectiveness of the filter in removing the noise.

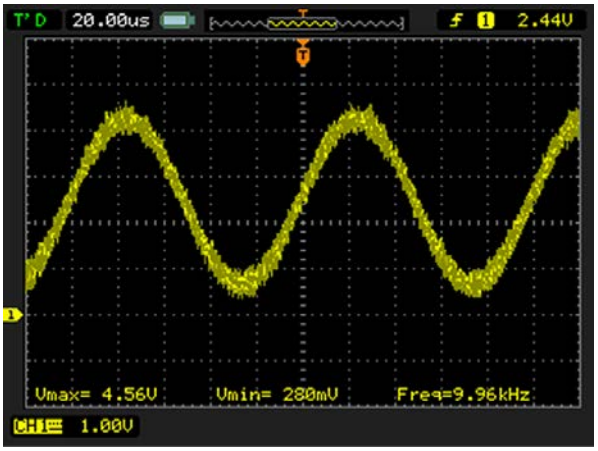

Figure 4. Signal Measured on the EXC Pin of the AD2S1210

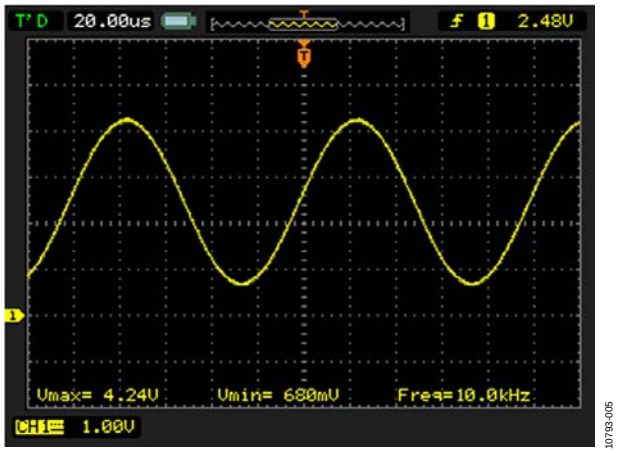

Figure 5. Signal Measured on C3 (Input to the AD8397 Driver)

Figures 6 and 7 show the output of the AD8397 measured at one input to the resolver for the low power mode (Figure 6) and the high performance mode (Figure 7). Note that these signals are measured on one side of the resolver input, and the actual differential signal applied to the resolver has twice the amplitude.

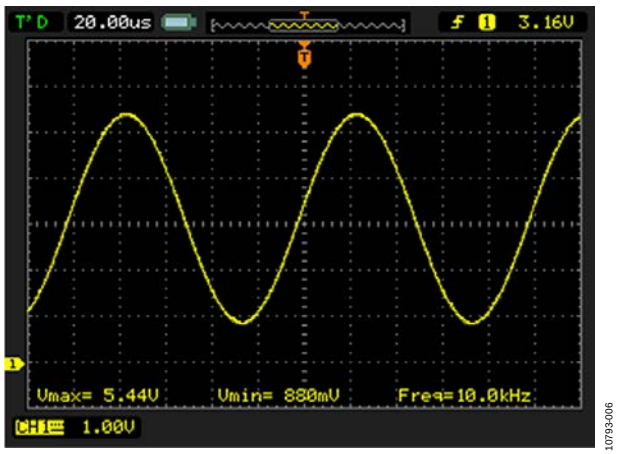

Figure 6. Signal at the Resolver Input When Using Low Power Mode

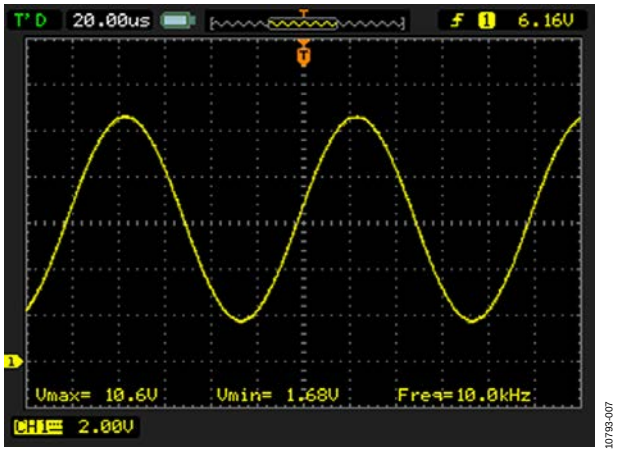

Figure 7. Signal at the Resolver Input When Using High Performance Mode

Resolver SIN/COS Receiver Circuit and Filter

Figure 8 shows the receiver circuit that includes a third order Butterworth filter and a programmable gain stage. When the driver circuit is in the high performance mode (VCC = 12 V), S1 is open, and the overall gain is 0.35. The input drive to the resolver is 18 V p-p (differential), and the SIN/COS outputs are 9 V p-p differential because the resolver transformation ratio is 0.5. The 9 V p-p differential is 4.5 V p-p single-ended, and when multiplied by the 0.35 gain factor, yields 1.58 V p-p (3.16 V p-p differential) which is the optimum input voltage for the SIN/COS inputs of the AD2S1210. Similarly, in the low power mode S1 is closed, and the overall gain is 0.7 which again provides an optimum input signal level for the SIN/COS inputs of the AD2S1210.

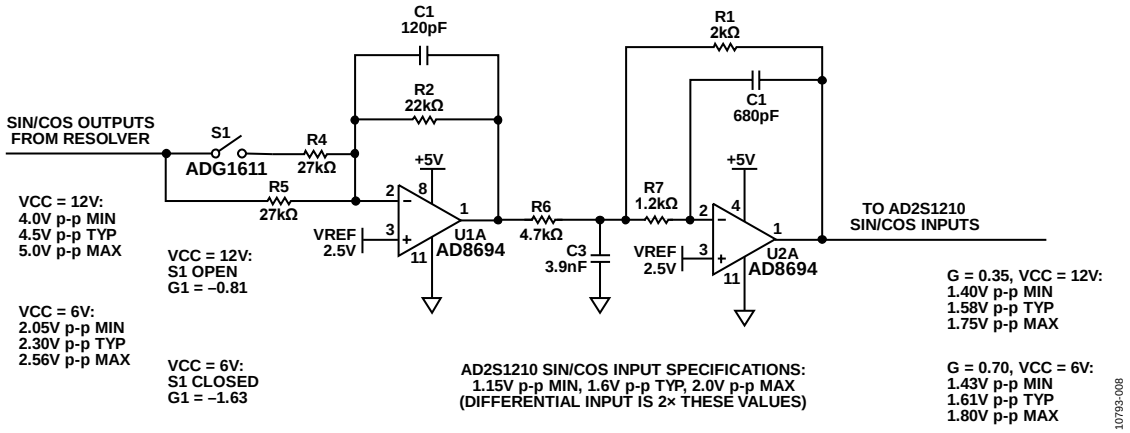

Figure 8. Resolver Receiver Circuit (Simplified Schematic: All Connections and Decoupling Not Shown)

In addition to providing the gain adjustment, the receiver circuit also acts as a third order Butterworth filter with a cutoff frequency of 63 kHz and a phase shift of −18.6° at 10 kHz.

The frequency response of the filter in the low gain and high gain modes is shown in Figure 9 and Figure 10, respectively.

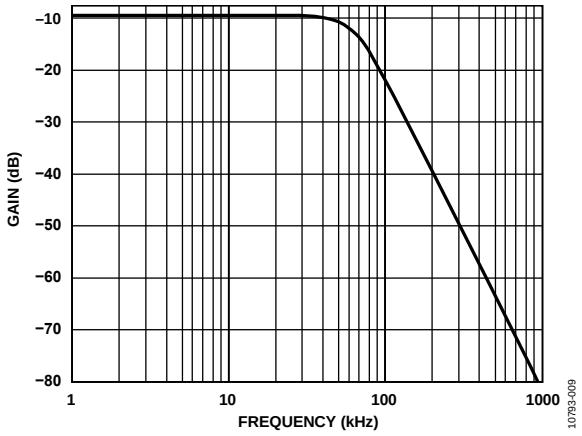

Figure 9. Resolver Receiver Circuit, Low Gain Transfer Function

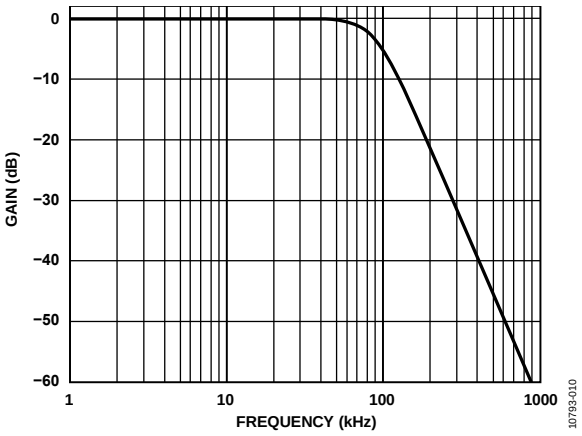

Figure 10. Resolver Receiver Circuit, High Gain Transfer Function

The voltage at the SIN/COS inputs of the AD2S1210 is shown in Figure 11, and is 1.64 V p-p (3.28 V p-p differential).

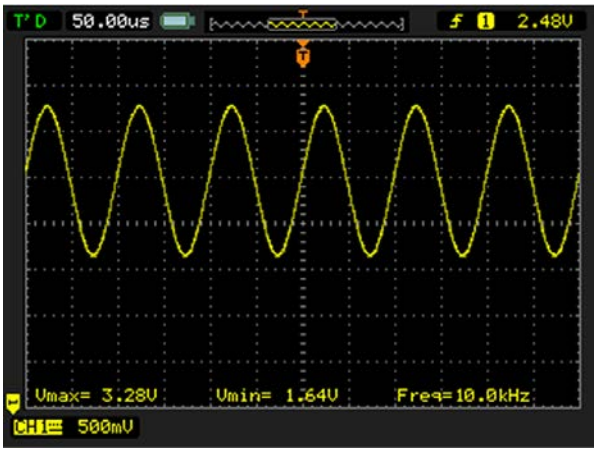

Figure 11. Signal on the AD2S1210 Sine and Cosine Inputs

Figure 12 shows that the total phase shift between the AD2S1210 EXC pin (CH1 yellow) to the SIN input pin (CH2 blue) is approximately 40° which is below the maximum design value of 44°.

Figure 12. Phase Shift Between the AD2S1210 EXC and SIN Pins

Automatic Mode Detection Circuit

The reset circuit shown in Figure 13 uses the ADM6328 microprocessor reset circuit to determine the gain in the driver and receiver based on the value of the VCC voltage. The threshold voltage is set so that if VCC is greater than 11.5 V, the circuit switches to the high performance mode. If VCC is less than 11.5 V, the circuit switches to the low power mode.

Because the ADM6328 consumes only 1 µA it can use the high impedance R1/R3 resistor divider output as its power supply without significant voltage drop.

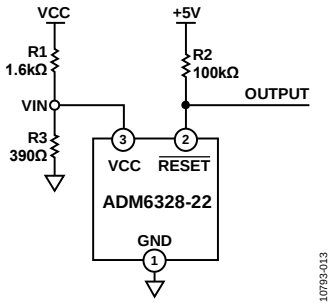

Figure 13. VCC Detection Circuit

The ADM6328 has an open drain output, and resistor R2 acts as a pull-up. This ensures that the output swing is independent of the VCC input. The ADM6328 power supply voltage is given by:

$$VIN = VCC \times \frac{R3}{R1 + R3}$$

The circuit uses the ADM6328-22 that has a typical threshold voltage of 2.2 V, and a maximum of 2.25 V. The maximum VCC threshold voltage is 11.5 V, therefore:

$$\frac{R1}{R3} = \frac{11.5\ \text{V}}{2.25\ \text{V}} - 1 = 4.1$$

Resistors R1 and R3 are chosen to be 1.6 kΩ and 390 Ω, respectively, giving a ratio of 4.102.

Resolver Driver Power Amplifier Power Dissipation

Because of the relatively low impedance of the resolver and the large VCC voltage, it is important to know the power dissipated in the AD8397 driver amplifier to make sure the maximum power dissipation specification is not exceeded. The maximum power that can be safely dissipated by the AD8397 is limited by the associated rise in junction temperature.

The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package.

The junction temperature rise can be calculated from the ambient temperature (T_A), the package thermal resistance (θ_{JA}), and the amplifier power dissipation (P_{AMP}):

$$T_J = T_A + P_{AMP} \times \theta_{JA}$$

The circuit uses the AD8397ARDZ that is housed in an 8-pin SOIC package with exposed pad (EP), and θ_{JA} = 47.2°C/W.

The power dissipated in the amplifier, P_{AMP}, is calculated by subtracting the power dissipated in the load, P_{LOAD}, from the power supplied by the power supply P_{SUPPLY}:

$$P_{AMP} = P_{SUPPLY} - P_{LOAD}$$

The equivalent load impedance of the resolver rotor winding is equal to:

$Z = R + jX_L$, where $X_L = \omega L$

The magnitude of the impedance is:

$$|Z| = \sqrt{R^2 + X_L^2}$$

The signal applied to the rotor winding is

$v(t) = A \sin\omega t$

The rms voltage applied to Z is

$V = A/\sqrt{2}$

The rms current through Z is given by:

$$I = \frac{V}{|Z|}$$

$$I = \frac{(A/\sqrt{2})}{|Z|}$$

$$P_{LOAD} = V \times I \cos\theta = \frac{A^2 \times \frac{R}{|Z|}}{2|Z|}$$

Where $\cos\theta$ = *power factor* = $\frac{R}{|Z|}$

The power supplied by the power supplies is calculated by first calculating the average current from the supplies. Note that these calculations neglect the op amp quiescent current and consider only the current due to the excitation current. The equivalent circuit for these calculations is shown in Figure 14.

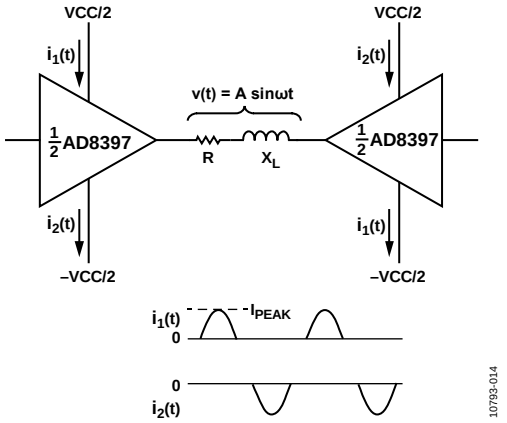

Figure 14. Equivalent Circuit for Calculating Power Supply Current

The peak current from the supply is:

$$I_{PEAK} = \frac{A}{|Z|}$$

Because the signal applied to the load is a sine wave, each supply must supply a half-wave rectified sine wave current to the load. The average current is equal to I_{PEAK}/π.

$$I_{AVG} = \frac{I_{PEAK}}{\pi} = \frac{A}{\pi|Z|}$$

Because this current must be supplied by each rail,

$$P_{SUPPLY} = 2 \times VCC \times I_{AVG} = \frac{2 \times VCC \times A}{\pi|Z|}$$

We can now calculate P_{AMP}:

$$P_{AMP} = P_{SUPPLY} - P_{LOAD} = \frac{2 \times VCC \times A}{\pi|Z|} - \frac{A^2 \times \frac{R}{|Z|}}{2|Z|}$$

$$P_{AMP} = \frac{4 \times VCC \times A - \pi A^2 \times \frac{R}{|Z|}}{2\pi|Z|}$$

When using Tamagawa TS2620N21E11 resolver, the impedance is 70 Ω+j100 Ω at 10 kHz. In the high performance state (VCC = 12 V, A = 10 V), the AD8397 power dissipation is 390 mW using the derived equation.

The thermal resistance to ambient, θ_{JA}, is 47.2°C/W for the AD8397 (EP package), and therefore the junction temperature rise above ambient is 47.2°C/W × 0.39W = 18.4°.

Power Supplies

The entire circuit operates on either an external VCC of +6 V or +12 V, depending on the mode. The 5 V supply for the circuits is developed using a 5 V, 500 mA ADP7104-5 low dropout regulator (LDO). A 3.3 V ADP7104-3.3 is used to develop the 3.3 V supply. Details of the power circuits can be found in the complete schematic included in the CN0276 Design Support Package (www.analog.com/CN0276-DesignSupport).

PCB Design and Layout Considerations

Even at the lower frequencies associated with the RDC circuits, poor layout can lead to poor performance. For instance, although the resolver operates with a 10 kHz excitation signal, the AD2S1210 operates on an 8.192 MHz clock; therefore it must be treated as a high speed device with respect to layout, grounding, and decoupling. Tutorials MT-031 and MT-101 cover these topics in detail.

A design support package is available for the CN-0276, including complete schematic, PADs and Gerber layout files, and bill of materials. This is located at http://www.analog.com/CN0276-DesignSupport.

System Performance Results

A good method to measure the overall system noise in the circuit is to apply a fixed position to the resolver and generate a histogram of the output codes. This test should be performed with the hysteresis function disabled. The following Figures show the AD2S1210 output histogram of codes for the 10-bit, 12-bit, 14-bit, and 16-bit angular accuracy modes. In each case, the full 16-bits of the RDC are used in generating the histogram, and the circuit is placed in the high performance mode with VCC = +12 V.

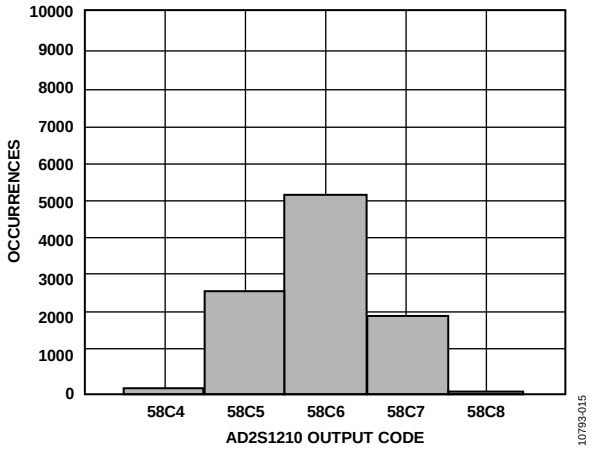

Figure 15. Histogram of Output Codes, 10,000 Samples, Hysteresis Disabled,10-Bit Angular Accuracy Mode, 16-Bit ADC Resolution

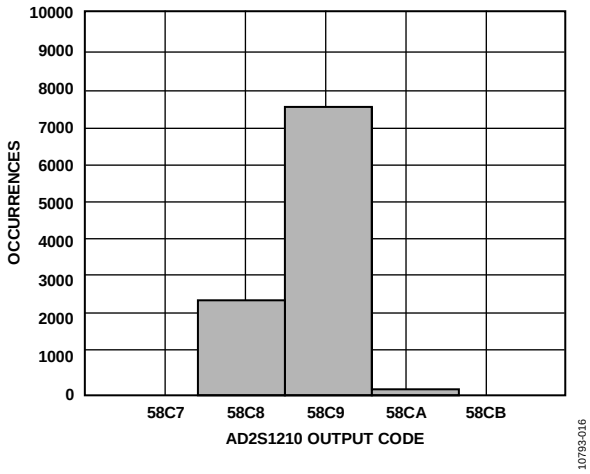

Figure 16. Histogram of Output Codes, 10,000 Samples, Hysteresis Disabled,12-Bit Angular Accuracy Mode, 16-Bit ADC Resolution

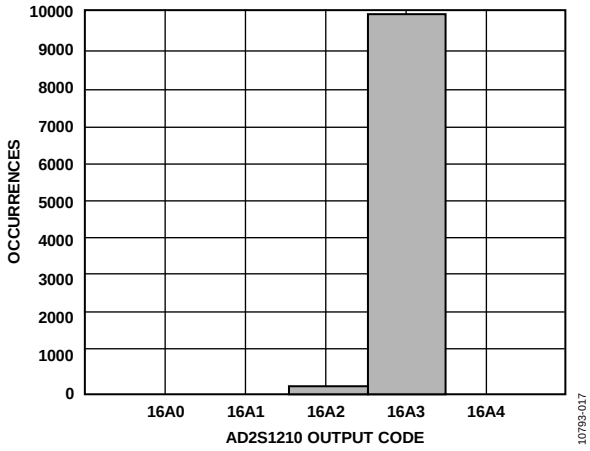

Figure 17. Histogram of Output Codes, 10,000 Samples, Hysteresis Disabled, 14-Bit Angular Accuracy Mode, 16-Bit ADC Resolution

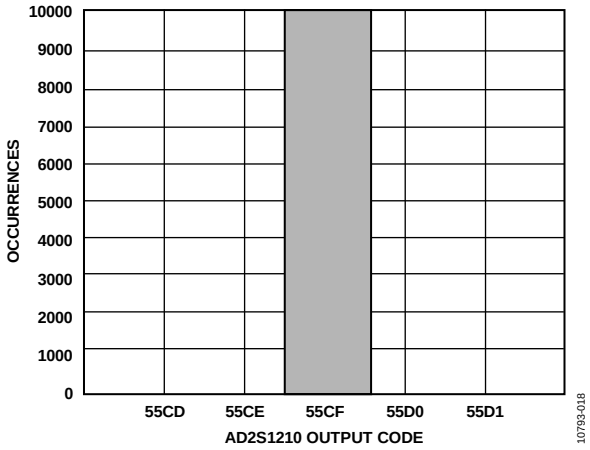

Figure 18. Histogram of Output Codes, 10,000 Samples, Hysteresis Disabled,16-Bit Angular Accuracy Mode, 16-Bit ADC Resolution

The histograms show that the AD2S1210 with a low pass filter on the driver and receiver circuit can be achieve high angular resolution in all modes.

COMMON VARIATIONS

The CN-0276 circuit can used for various types of resolver. For the best performance, the designer should adjust the passive components appropriately. The basic principles in adapting the circuit to different resolvers are:

1. Ensure that each amplifier output remains within the allowable voltage range.
2. Ensure that none of the components are subjected to overvoltage. For example, I the resolver output voltage is too high for the ADG1611 switch, a resistor can be added in series with the input to the circuit shown in Figure 8.
3. Ensure that the total signal chain phase shift remains within the range: $n \times 180° - 44° \leq \varphi \leq n \times 180° + 44°$, where n is an integer.

In some applications, a capacitor is added in parallel with the primary winding of the resolver, and the value chosen so that it resonates with the resolver inductance at the frequency of operation. This makes the load appear resistive. For example, the resolver used in the circuit has a reactance of 100 Ω at 10 kHz, corresponding to an inductor value of 1.6 mH. A 160 nF capacitor placed in parallel with the primary causes the load to be approximately 70 Ω, the real part of the impedance.

However, at higher frequencies that are still within the bandwidth of the op amp, the op amp may oscillate because of the capacitive load. The op amp must be carefully compensated in this application so that it maintains stability over its entire bandwidth.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0276-SDPZ circuit board and the EVAL-SDP-CB1Z SDP-B system demonstration platform controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The EVAL-CN0276-SDPZ contains the circuit to be evaluated, and the EVAL-SDP-CB1Z (SDP-B) is used with the CN-0276 Evaluation Software to exchange the data from the EVAL-CN0276-SDPZ.

Equipment Needed

The following equipment is needed:

- A PC with a USB port and Windows® 7 or later
- The EVAL-CN0276-SDPZ circuit board
- The EVAL-SDP-CB1Z SDP-B controller board
- The CN-0276 Evaluation Software
- A 6 V/1 A bench supply
- A 12 V/1 A bench supply
- Tamagawa TS2620N21E11 Resolver

Getting Started

Load the evaluation software by placing the CN-0276 Evaluation Software into the CD drive of the PC. Using My Computer, locate the drive that contains the evaluation software. Further details regarding the software operation can be found in the CN0276 Software User Guide.

Functional Block Diagram

A functional block diagram of the test setup is shown in Figure 19.

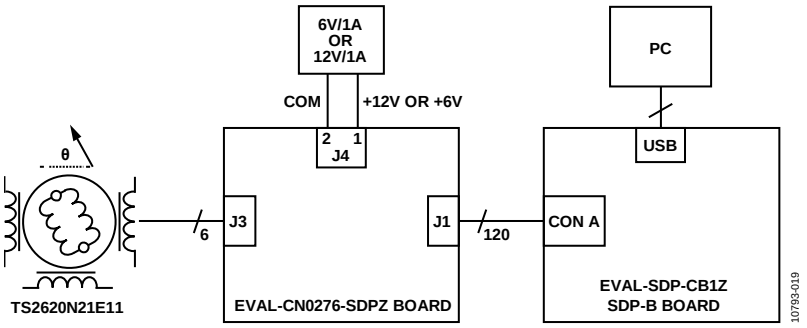

Figure 19. Functional Diagram of Test Setup

Setup

Connect the 120-pin connector on the EVAL-CN0276-SDPZ circuit board to the CON A connector on the EVAL-SDP-CB1Z controller board (SDP-B). Use nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V or 12 V power supply to the VCC and GND pins on the board. Connect the USB cable supplied with the SDP-B board to the USB port on the PC. Do not connect the USB cable to the Mini-USB connector on the SDP-B board at this time. Connect the resolver TS2620N21E11 to the J3 of EVAL-CN0276-SDPZ circuit board.

Test

Apply power to the 6 V or 12 V supply connected to the EVAL-CN0276-SDPZ. Launch the evaluation software and connect the USB cable from the PC to the mini-USB connector on the EVAL-SDP-CB1Z.

When USB communications are established, the EVAL-SDP-CB1Z can send, receive, and capture parallel data from the EVAL-CN0276-SDPZ.

Figure 20 shows a screen shot of the software output display when using the circuit to measure position and velocity.

Figure 21 shows a photo of the EVAL-CN0276-SDPZ evaluation board.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0276 Software User Guide.

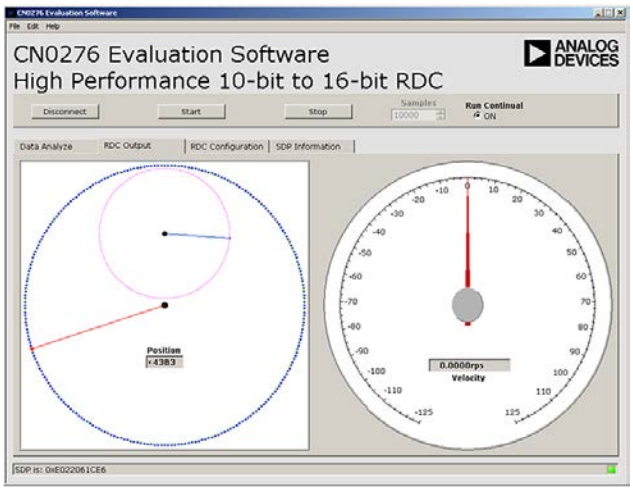

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Figure 20. Screenshot of Software Output Window

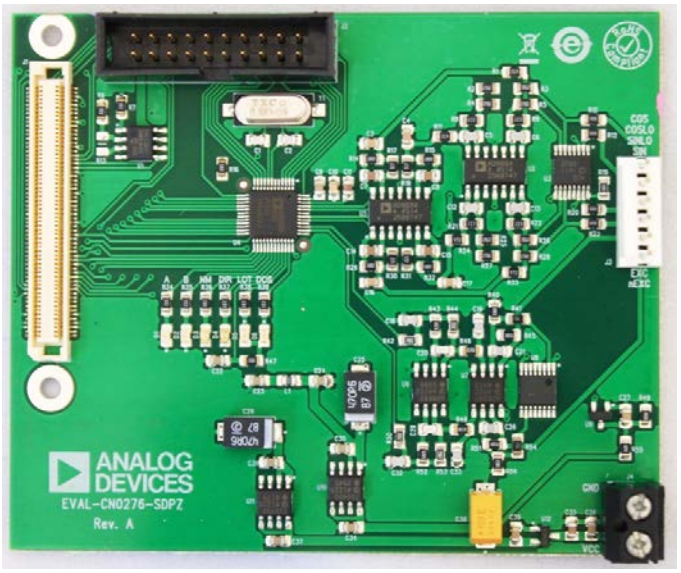

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Figure 21. Photo of EVAL-CN0276-SDPZ PCB

Connectivity for Prototype Development

The EVAL-CN0276-SDPZ evaluation board is designed to use the EVAL-SDP-CB1Z SDP-B board; however, any microprocessor can be used to interface to the SPI port of the AD2S1210 (the user should set $\overline{\text{SOE}}$ pin low to active SPI interface). In order for another controller to be used with the EVAL-CN0276-SDPZ evaluation board, software must be developed by a third party.

There are existing interposer boards that can be used to interface to the Altera and Xilinx field programmable gate arrays (FPGAs). The BeMicro SDK board from Altera can be used with the BeMicro SDK/SDP interposer using Nios Drivers. Any Xilinx evaluation board that features the FMC connector can be used with the FMC-SDP Interposer board.