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Devices Connected/Referenced	
AD698	Universal LVDT Signal Conditioner
AD8615	Precision, 20 MHz, CMOS, Single RRIO Operational Amplifier
AD7992	2-Channel, 12-Bit ADC with I²C-Compatible Interface in 10-Lead MSOP

Universal LVDT Signal Conditioning Circuit

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0301 Circuit Evaluation Board (EVAL-CN0301-SDPZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a complete adjustment-free linear variable differential transformer (LVDT) signal conditioning circuit. This circuit can accurately measure linear displacement (position).

The LVDT is a highly reliable sensor because the magnetic core can move without friction and does not touch the inside of the tube. Therefore, LVDTs are suitable for flight control feedback systems, position feedback in servomechanisms, automated measurement in machine tools, and many other industrial and scientific electromechanical applications where long term reliability is important.

This circuit uses the AD698 LVDT signal conditioner that contains a sine wave oscillator and a power amplifier to generate the excitation signals that drive the primary side of the LVDT. The AD698 also converts the secondary output into a dc voltage. The AD8615 rail-to-rail amplifier buffers the output of the AD698 and drives a low power 12-bit successive approximation analog-to-digital converter (ADC). The system has a dynamic range of 82 dB and a system bandwidth of 250 Hz, making it ideal for precision industrial position and gauging applications.

The signal conditioning circuitry of the system consumes only 15 mA of current from the ±15 V supply and 3 mA from the +5 V supply.

This circuit note discusses basic LVDT theory of operation and the design steps used to optimize the circuit shown in Figure 1 for a chosen bandwidth, including noise analysis and component selection considerations.

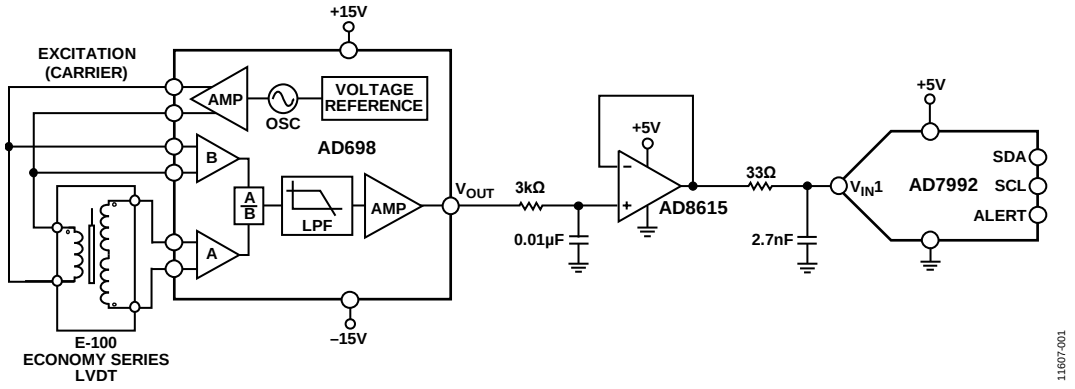

Figure 1. Universal LVDT Signal Conditioning Circuit (Simplified Schematic: All Connections and Decoupling Not Shown)

Rev. A

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CIRCUIT DESCRIPTION

Theory of Operation

An LVDT is an absolute displacement transducer that converts a linear displacement or position from a mechanical reference (or zero) into a proportional electrical signal containing phase (for direction) and amplitude information (for distance). The LVDT operation does not require electrical contact between the moving part (probe or core rod assembly) and the transformer. Instead, it relies on electromagnetic coupling. For this reason, and because they operate without any built-in electronic circuitry, LVDTs are widely used in applications where long life and high reliability under severe environments are a required, such military and aerospace applications.

For this circuit, the E-100 Economy Series LVDT sensor from Measurement Specialties™, Inc. was used with the AD698. With a linearity of ±0.5% of full range, the E Series is suitable for most applications with moderate operation temperature environments.

The AD698 is a complete, LVDT signal conditioning subsystem. It converts the transducer mechanical position of LVDTs to a unipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passives components to set frequency and gain, the AD698 converts the raw LVDT secondary output to a scaled dc signal.

The AD698 contains a low distortion sine wave oscillator to drive the LVDT primary. The frequency of the sine wave is determined by a single capacitor and can range from 20 Hz to 20 kHz with amplitudes from 2 V rms to 24 V rms.

The LVDT secondary output consists of two sine waves that drive the AD698 directly. The AD698 decodes LVDTs by synchronously demodulating the amplitude modulated input (secondaries), A, and a fixed input reference (primary or sum of secondaries or fixed input), B. A common problem with earlier solutions was that any drift in the amplitude of the drive oscillator corresponded directly to a gain error in the output. The AD698 eliminates these errors by calculating the ratio of the LVDT output to its input excitation in order to cancel out any drift effects. This device differs from the AD598 LVDT signal conditioner in that it implements a different circuit transfer function and does not require the sum of the LVDT secondaries (A + B) to be constant with stroke length.

The block diagram of the AD698 is depicted Figure 2. The inputs consist of two independent synchronous demodulation channels. The B channel monitors the drive excitation to the LVDT. The full wave rectified output is filtered by C2 before being sent to the computational circuit. Channel A is identical except that the comparator's pins are externally available. Since the A channel may reach 0 V output at the LVDT null, the A channel demodulator is usually triggered by the primary voltage (B Channel). In addition, a phase compensation network may be required to add phase lead or lag to the A Channel to compensate for the LVDT primary to secondary phase shift. For half-bridge circuits the phase shift in noncritical, and the A channel voltage is large enough to trigger the demodulator.

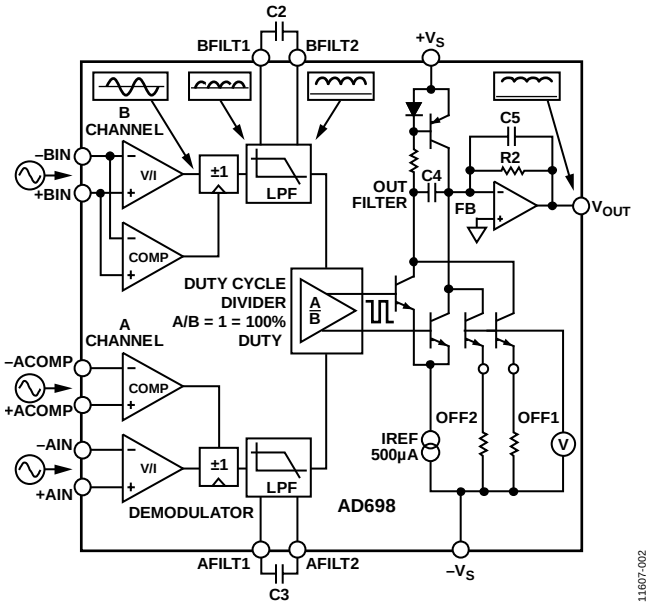

Figure 2. AD698 Block Diagram

Once both channels are demodulated and filtered a division circuit, implemented with a duty cycle multiplier, is used to calculate the ratio A/B. The output of the divider is a duty cycle. When A/B is equal to 1, the duty cycle will be equal to 100%. (This signal can be used as is if a pulse width modulated output is required.) The duty cycle drives a circuit that modulates and filters a reference current proportional to the duty cycle. The output amplifier scales the 500µA reference current converting to a voltage. The output transfer function is thus:

$$V_{OUT} = I_{REF} \times \frac{A}{B} \times R2$$

where I_{REF} = 500 µA.

Component Selection

The design procedure for the dual supply operation (±15 V) found in the AD698 data sheet was followed to set the excitation frequency to 2.5 kHz, system bandwidth to 250 Hz, and an output voltage from 0 V to 5 V.

It is normal for the AD698 internal oscillator to produce a small amount of ripple that feeds through to the output. A passive low-pass filter is used to reduce this ripple to the required level.

When selecting capacitor values to set the bandwidth of the system, a trade-off is involved. Choosing smaller capacitors give higher system bandwidth but increase the amount of output voltage ripple. The ripple can be reduced by increasing the shunt capacitance across the feedback resistor used to set the output voltage level; however, this also increases phase lag.

The AD8615 operational amplifier buffers the output of the AD698, which ensures that the AD7992 ADC is driven by a low impedance source (high source impedances significantly affect the ac performance of the ADC).

The low-pass filter between the output of the AD698 and the input of the AD8615 serves two purposes:

- It limits the input current to the AD8615.
- It filters the output voltage ripple.

The AD8615 has internal protective circuitry that allows voltages exceeding the supply to be applied at the input. This is important because the output voltage of the AD698 can swing ±11 V with ±15 V supplies. As long as the input current is limited to less than 5 mA, higher voltages can be applied to the input. This is primarily due to the extremely low input bias current of the AD8615 (1 pA) which allows the use of larger resistors. The use of these resistors adds thermal noise, which contributes to the overall output voltage noise of the amplifier.

The AD8615 is an ideal amplifier to buffer and drive the input of the AD7992 12-bit SAR ADC because of its input overvoltage protection, and its ability to swing rail-to-rail at both the input and output.

Noise Analysis

With all signal condition components selected, the amount of resolution needed to convert the signal must be determined. As in most noise analyses, only the key contributors need to be identified. Noise sources combine in an rss manner; therefore, any single noise source that is at least three-to-four times larger than any of the others dominates.

In the case of the LVDT signal conditioning circuit, the dominant source of the output noise is the output ripple of the AD698. The other sources of noise (resistor noise, input voltage noise, and output voltage noise of the AD8615) are significantly smaller in comparison.

The output voltage ripple of the AD698 is 0.4 mV rms with a 0.39 µF capacitor value and with a 10 nF shunt capacitor across the feedback resistor shown in Figure 3. Note that these components and related pin connections are not shown in the simplified schematic in Figure 1; however, details can be found in the AD698 data sheet.

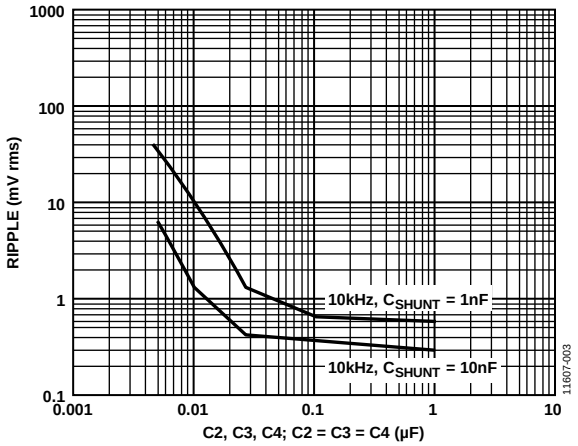

Figure 3. Output Voltage Ripple vs. Filter Capacitance

The maximum number of rms counts that can be resolved can now be calculated by dividing the full-scale output by the total system rms noise.

$$\textit{Total RMS Counts} = 5\text{ V}/0.4\text{ mV} = 12,500$$

The effective resolution is found by taking the base 2 logarithm of the total rms counts.

$$\textit{Effective Resolution} = \log_2(12,500) = 13.6\text{ Bits}$$

Noise-free code resolution can be obtained by subtracting 2.7 bits from the effective resolution.

$$\textit{Noise-Free Code Resolution} = \textit{Effective Resolution} - 2.7\text{ Bits}$$
$$= 13.6\text{ Bits} - 2.7\text{ Bits}$$
$$= 10.9\text{ Bits}$$

The total output dynamic range of the system can be calculated by dividing the full-scale output signal (5 V) by the total output rms noise (0.4 mV rms) and converting it to decibels, yielding approximately 82 dB.

$$\textit{Dynamic Range} = 20\log(5\text{ V}/0.4\text{ mV}) = 82\text{ dB}$$

The AD7992 is a good candidate for this application because it has 12-bit resolution and a sampling rate of 188 kSPS per channel when used with a 3.4 MHz serial clock.

Compensating for Phase Lag/Lead

The AD698 uses demodulation to generate an output signal by multiplying the return signal with the reference oscillator fed to the primary. Small amounts of phase shift can produce significant linearity error which is seen as undershoot in the output.

The phase lead network compensates for the −3° of primary to secondary phase shift of the E-100 series LVDT. Figure 4 shows two different phase compensation networks.

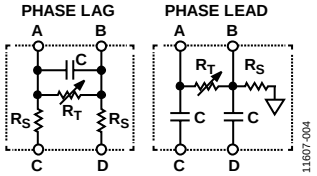

Figure 4. Phase Lag/Lead Network

When choosing component values for the appropriate network, it is important to note that R_S and R_T effectively constitute a resistor divider that reduces the amplitude of the excitation signals before it reaches the ±ACOMP inputs of the AD698. This suggests that R_T needs to be much larger than R_S. The lag/lead circuitry also adds load to the excitation output therefore, larger resistive values are recommended. The end goal is to achieve the desired phase lag/lead on the ACOMP inputs of the AD698 with a small amplitude drop.

The amount of phase lag/lead can be calculated by using the following formulas:

$$Phase\ Lag = \tan^{-1}\left(Hz \times R \times C\right)$$

$$Phase\ Lead = \tan^{-1}\left(\frac{1}{Hz \times R \times C}\right)$$

where

$$R = \frac{1}{R_S} + \frac{1}{R_S + R_T}$$

Hz = Excitation Frequency

Test Results

Using a Measurement Specialties, Inc. E-100 Economy Series LVDT connected to J3 and using a digital oscilloscope to monitor the output of the AD698 found on J6 on the EVAL-CN0301-SDPZ evaluation board, the actual output ripple found was 6.6 mV p-p, as is shown in Figure 5.

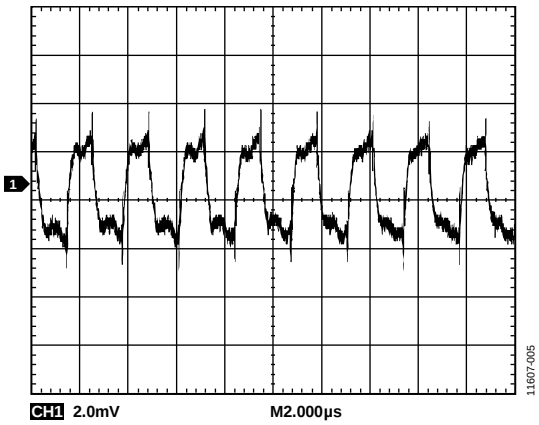

Figure 5. Output Voltage Ripple Before Low-Pass Filter

The low-pass filter (3 kΩ, 0.01 µF) between the AD698 output and the AD8615 input has a −3 dB bandwidth of 5.3 kHz and reduces the ripple to 2 mV p-p.

With the low-pass filter installed between the output stage of the AD698 and the input stage of the AD8615, data was collected from the EVAL-CN0301-SDPZ evaluation board, as shown in Figure 6.

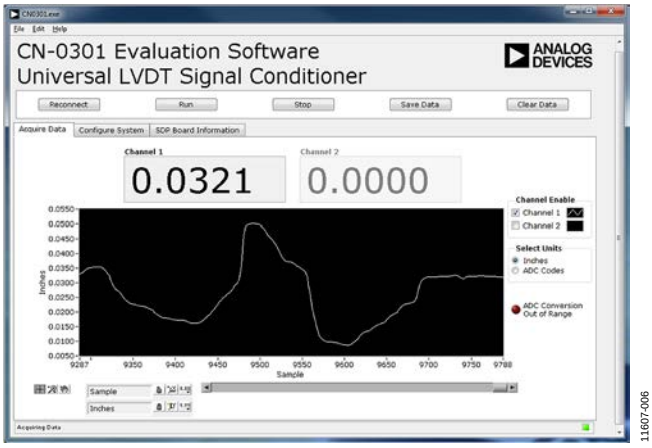

Figure 6. Screenshot of the CN-0301 Evaluation Software

The ripple from the AD698 was attenuated to 2 mV p-p, and the system was able to achieve 11 bits of noise-free code resolution.

A complete design support package for this circuit note can be found at http://www.analog.com/CN0301-DesignSupport.

Applications in Flight Control Surface Position Feedback

Unmanned autonomous vehicles (UAVs), or drones, are playing an ever-increasing part in the national security of the United States. These high technology, complex aerial platforms are controlled by a crew miles away and are multimission capable. They include roles such as aerial reconnaissance, combat weapons platforms, battlefield theater command and control oversight, or unmanned in-flight refueling station.

The complex systems employed on UAVs use a myriad of electronic sensors for precise control and feedback. To control the altitude (pitch, roll, and yaw) of the UAV, actuators are used to exert forces on the flight control surfaces. The precise measurement of the position of these actuators is crucial in maintaining the proper flight of path.

The sensors used to measure actuator position need to meet three essential criteria: high accuracy, high reliability, and light weight. All three of these attributes are found in the LVDTs designed by Measurement Specialties, Inc.

Synchronous Operation of Multiple LVDTs

In many applications, such as multiple gaging measurement, a large number of LVDTs are used in close proximity. If these LVDTs operate at similar carrier frequencies, stray magnetic coupling can cause beat notes to be generated. The resulting beat notes may interfere with the accuracy of measurements made under these conditions. To avoid this situation, all LVDTs operate synchronously.

The EVAL-CN0301-SDPZ evaluation board can be configured to have one master oscillator between two LVDTs by populating Jumper JP1, JP2, and JP4 with a shorting jumper and leaving JP3 unpopulated. Each LVDT primary is driven from its own power amplifier, and, thus, the thermal load is shared between the AD698 devices.

COMMON VARIATIONS

The components selected were optimized for a maximum 5 V unipolar output from the AD698; however, other combinations can be substituted.

Other suitable single-supply amplifiers are the AD8565 and AD8601. These amplifiers are suitable replacements for the AD8615 because they have input overvoltage protection and the ability to swing rail-to-rail at both the input and output. If dual-supply operation is required, the ADA4638-1 or ADA4627-1 is suggested.

If the AD698 outputs ±10 V bipolar signals, the AD7321 is suggested. The AD7321 is a 2-channel, bipolar input, 12-bit ADC that can accept true bipolar analog input signals as large as ±10 V.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0301-SDPZ circuit board and the EVAL-SDP-CB1Z SDP-B system demonstration platform controller board. The two boards have 120-pin mating connectors, allowing for the quick setup and evaluation of the performance of the circuit. The EVAL-CN0301-SDPZ contains the circuit to be evaluated, and the EVAL-SDP-CB1Z (SDP-B) is used with the CN-0301 Evaluation Software to capture the data from the EVAL-CN0301-SDPZ.

Equipment Needed

The following equipment is needed:

- A PC with a USB port and Windows® XP (32 bit), Windows Vista®, or Windows 7
- The EVAL-CN0301-SDPZ circuit board
- The EVAL-SDP-CB1Z SDP-B controller board
- The CN-0301 Evaluation Software
- The EVAL-CFTL-6V-PWRZ dc power supply or equivalent 6 V/1 A bench supply
- Measurement Specialties, Inc., E-100 Economy Series LVDT (EVAL-CFTL-LVDT)

Getting Started

Load the evaluation software by placing the CN-0301 Evaluation Software into the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software.

Functional Block Diagram

See Figure 1 for the circuit block diagram and the **EVAL-CN0301-SDPZ-PADSSchematic.pdf** file for the complete circuit schematic. The PDF file can be found in the CN-0301 Design Support Package.

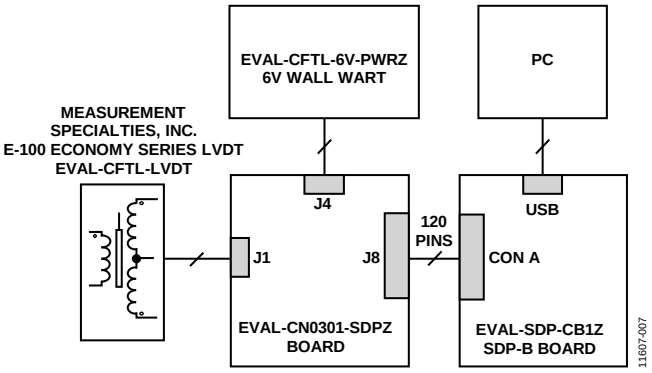

Figure 7. Test Setup Block Diagram

Setup

Connect the 120-pin connector on the EVAL-CN0301-SDPZ to the **CON A** connector on the EVAL-SDP-CB1Z (SDP-B). Use nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. With power to the supply off, connect a 6 V power supply to the +6 V and GND pins on the board. If available, a 6 V wall wart can be connected to the barrel connector on the board and used in place of the 6 V power supply. Connect the USB cable supplied with the EVAL-SDP-CB1Z to the USB port on the PC. Do not connect the USB cable to the Mini-USB connector on the EVAL-SDP-CB1Z at this time.

Test

Apply power to the 6 V supply (or wall wart) connected to the EVAL-CN0301-SDPZ. Launch the evaluation software and connect the USB cable from the PC to the Mini-USB connector on the EVAL-SDP-CB1Z.

When USB communications are established, the EVAL-SDP-CB1Z can send, receive, and capture parallel data from the EVAL-CN0301-SDPZ.

Figure 8 shows a photo of the EVAL-CN0301-SDPZ connected to the EVAL-SDP-CB1Z. Information regarding the EVAL-SDP-CB1Z can be found in the UG-277 User Guide.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0301 Software User Guide.

Connectivity for Prototype Development

The EVAL-CN0301-SDPZ is designed to use the EVAL-SDP-CB1Z; however, any microprocessor can be used to interface to the I²C 2-wire serial interface of the AD7992. In order for another controller to be used with the EVAL-CN0301-SDPZ, software must be developed by a third party.

There are existing interposer boards that can be used to interface to the Altera and Xilinx field programmable gate arrays (FPGAs). The BeMicro SDK board from Altera can be used with the BeMicro SDK/SDP interposer using nios drivers. Any Xilinx evaluation board that features the FMC connector can be used with the FMC-SDP interposer board.

The EVAL-CN0301-SDPZ is also compatible with the Digilent, Imod interface specification.

A photo of the system is shown in Figure 8.

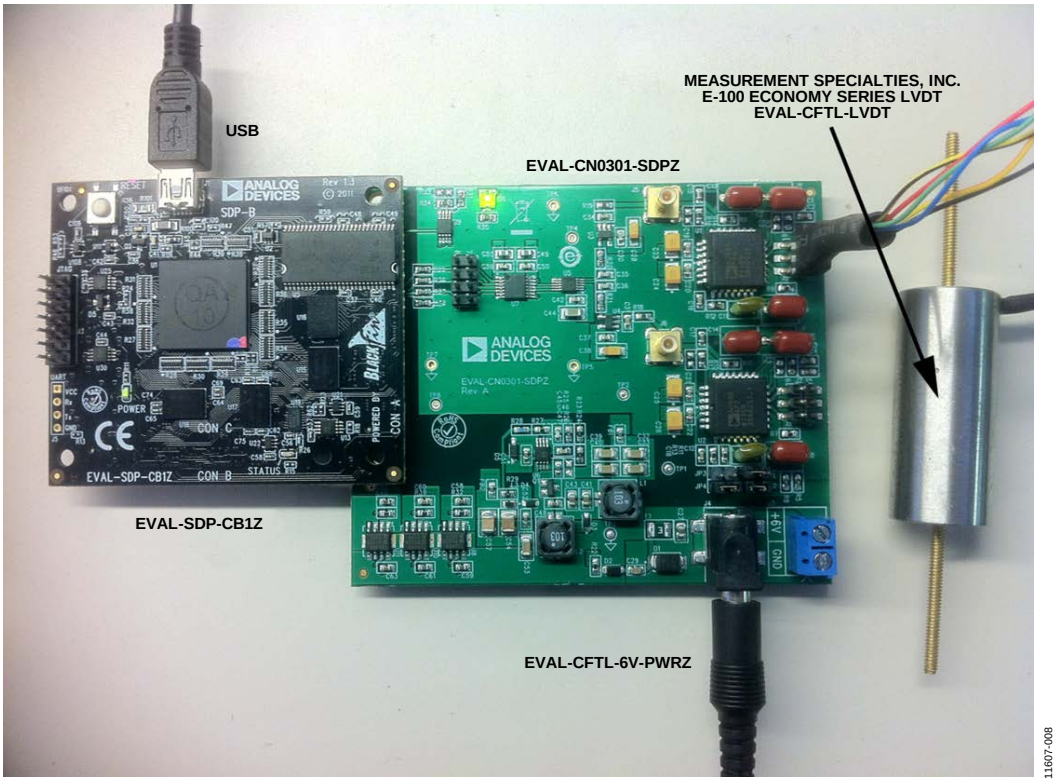

Figure 8. The EVAL-CN0301-SDPZ Board Connected to EVAL-SDP-CB1Z (SDP-B) Board and Measurement Specialties, Inc., E-100 Economy Series LVDT