ANALOG DEVICES

Circuit Note
CN-0370

Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0370.

Devices Connected/Referenced	
AD5542A	Serial-Input, Voltage Output, Unbuffered 16-Bit DAC
ADA4500-2	Rail-to-Rail Input/Output, Zero Input Crossover Distortion Amplifier
ADR4525	Ultralow Noise, High Accuracy, 2.5 V Voltage Reference

16-Bit, Single-Supply LED Current Driver with Less than ±1 LSB Integral and Differential Nonlinearity

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0370 Circuit Evaluation Board (EVAL-CN0370-PMDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)
PMOD to SDP Interposer Board (SDP-PMD-IB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a complete single-supply, low noise LED current source driver controlled by a 16-bit digital-to-analog converter (DAC). The system maintains ±1 LSB integral and differential nonlinearity and has a 0.1 Hz to 10 Hz noise of less than 45 nA p-p for a full-scale output current of 20 mA.

The innovative output driver amplifier eliminates the crossover nonlinearity normally associated with most rail-to-rail input op amps that can be as high as 4 LSBs or 5 LSBs for a 16-bit system.

This industry-leading solution is ideal for pulse oximetry applications where 1/f noise superimposed on the LED brightness levels affects the overall accuracy of the measurement.

Total power dissipation for the three active devices is less than 20 mW typical when operating on a single 5 V supply.

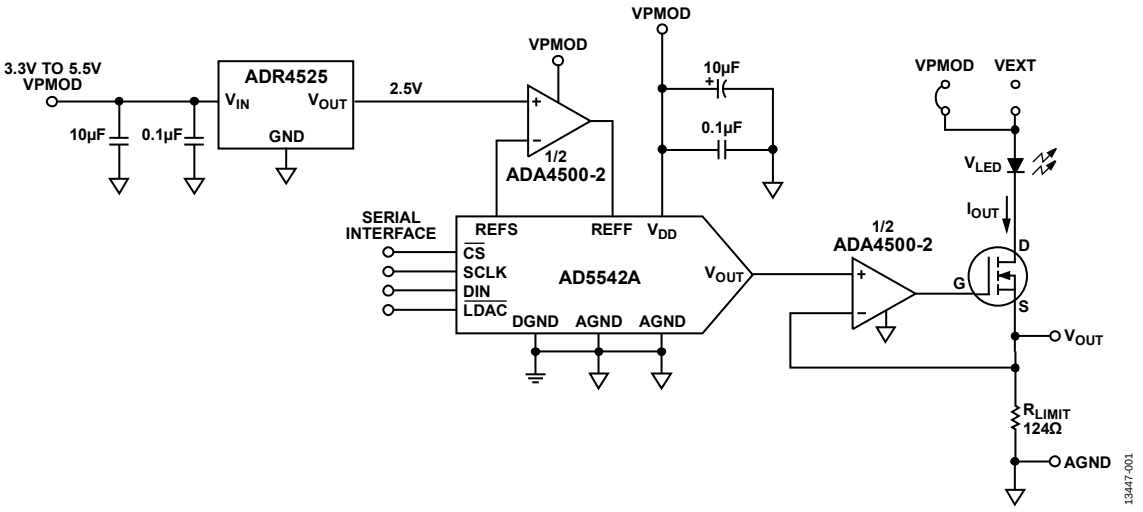

Figure 1. ±1 LSB Linear 16-Bit LED Current Source Driver (Simplified Schematic: All Connections and Decoupling Not Shown)

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CIRCUIT DESCRIPTION

In a typical pulse oximetry application, an LED is pulsed from a high level of current (for example, 3/4 scale) to a lower level of current (for example, 1/4 scale). The on-time of these pulses is typically in the order of several hundred microseconds. Peak-to-peak 1/f noise superimposed on the LED brightness levels during the on-time affects the accuracy of the overall measurement and must be minimized.

Figure 1 shows the single-supply signal chain that consists of a voltage reference, a DAC, a DAC output buffer, and a current source.

The DAC is the AD5542A 16-bit, serial input, voltage output segmented R-2R CMOS DAC. The output voltage of the DAC is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal data word loaded in the DAC register.
N is the number of bits.

For a reference of 2.5 V and N = 16, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 \times D}{2^{16}} = \frac{2.5 \times D}{65{,}536}$$

This gives a V_{OUT} of 1.25 V at mid scale, and 2.5 V at full scale.

The LSB size is 2.5 V/65,536 = 38.1 µV.

One LSB at 16 bits is also 0.0015% of full scale or 15 ppm full scale.

The DAC reference pin is driven by an 2.5 V ADR4525 voltage reference buffered with the ADA4500-2. The ADR4525 voltage reference provides a high precision, low noise (1.25 µV p-p, 0.1 Hz to 10 Hz), and stable reference to the DAC. The ADR4525 uses an innovative core topology to achieve high accuracy while offering industry-leading temperature stability and noise performance. The low output voltage temperature coefficient (2 ppm/°C maximum) and low long-term output voltage drift of the device also improve system accuracy over time and temperature variations. The initial room temperature error of the ADR4525B is ±0.02% maximum, which is approximately 13 LSBs at 16 bits.

The dual ADA4500-2 is selected as the DAC output buffer as well as the voltage reference buffer. The ADA4500-2 is a high precision amplifier with maximum offset voltage of 120 µV, offset drift of less than 5.5 µV/°C, 0.1 Hz to 10 Hz noise of 2 µV p-p, and maximum input bias current of 2 pA. Its innovative rail-to-rail input structure eliminates crossover distortion and therefore makes it an excellent choice as a DAC buffer.

A typical rail-to-rail input amplifier uses two differential pairs (PNP and NPN, or PMOS and NMOS) to achieve rail-to-rail input swing (see the MT-035 Tutorial). One differential pair is active at the low range of the input common-mode voltage, and the other pair is active at the high end. This classic complementary dual differential pair topology introduces crossover distortion during the transition between one differential pair to the other. The change in offset voltage causes nonlinearity when the amplifier is used as a DAC buffer.

The ADA4500-2 uses an integrated charge pump in its input structure to achieve rail-to-rail input swing without the need for a second differential pair. Therefore, it does not exhibit crossover distortion. Using a zero crossover distortion amplifier in this single-supply system provides wide dynamic output range while maintaining linearity over the entire input common-mode range. Details of the operation of the ADA4500-2 can be found in the ADA4500-2 data sheet.

The output impedance of the DAC is constant (typically 6.25 kΩ) and code independent. The output buffer must therefore have a high input impedance and low input bias current to minimize errors. The ADA4500-2 is a suitable candidate with high input impedance and 2 pA maximum of input bias current at room temperature, and 190 pA maximum of input bias current over temperature. This results in 1.2 µV worst-case error due to input bias current flowing through the 6.25 kΩ DAC impedance, which is significantly less than 1 LSB.

The output of the DAC is buffered and used to drive the power MOSFET (IRLMS2002TRPBF). The MOSFET converts the DAC output voltage into current that drives the LED. The MOSFET in the circuit is able to handle currents up to 6.5 A; however, the current is limited to 20 mA, which is the maximum rated current of the LED supplied on the EVAL-CN0370-SDPZ board. The board has provisions to easily change the full-scale current to the LED by changing the R_{LIMIT} resistor. The maximum current can be calculated by

$$I_{MAX} = 2.5\ V/R_{LIMIT}$$

Jumper options allow the LED to be connected to either the PMOD voltage (VPMOD) or an external voltage (VEXT).

The VEXT option is required to provide sufficient headroom for the MOSFET when operating with VPMOD = 3.3 V. For example, if V_{OUT} = 2.5 V, V_{DS} = 0.7 V, and V_{LED} = 0.7 V, then VEXT must be greater than 2.5 V + 0.7 V + 0.7 V = 3.9 V.

An alternative that allows 3.3 V supply operation is to limit the full-scale output voltage to approximately 1.9 V and only use 76% of the DAC output range. The R_{LIMIT} resistor must be changed to approximately 95 Ω to maintain 20 mA full-scale output current at 1.9 V output.

The AD5542A is available in a 10-lead MSOP or 10-lead LFCSP. The ADR4525 is available in an 8-lead SOIC, and the ADA4500-2 is available in an 8-lead MSOP or 8-lead LFCSP.

Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) Measurements

INL is the deviation in LSB of the actual DAC transfer function from an idealized transfer function. DNL is the difference between an actual step size and the ideal value of 1 LSB. This system solution provides a 16-bit resolution with ±1 LSB DNL and INL. Figure 2 and Figure 3 show the DNL and INL performance of the circuit.

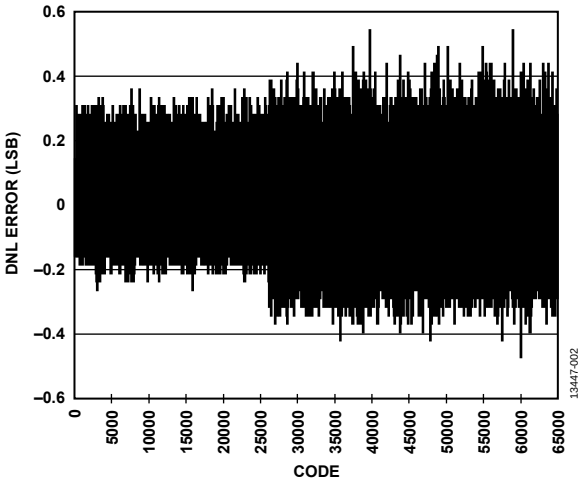

Figure 2. Differential Nonlinearity (DNL)

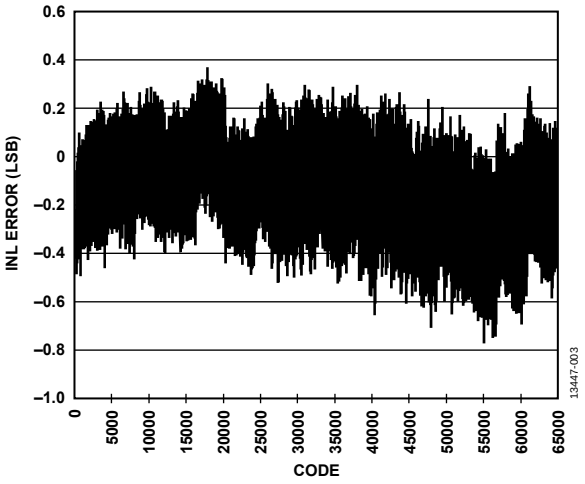

Figure 3. Integral Nonlinearity (INL)

Note that the DNL and INL measurements exclude the 100 codes (approximately 4 mV) from the lower end of the range. This is because the MOSFET leakage current causes the output voltage to become nonlinear in this region.

Figure 4 shows the nonlinearity introduced using an op amp with a traditional rail-to-rail input stage. This plot shows the crossover distortion when the active differential pair changes from the PNP pair to the NPN pair. The error swings from +4 LSB to −15 LSB in this region.

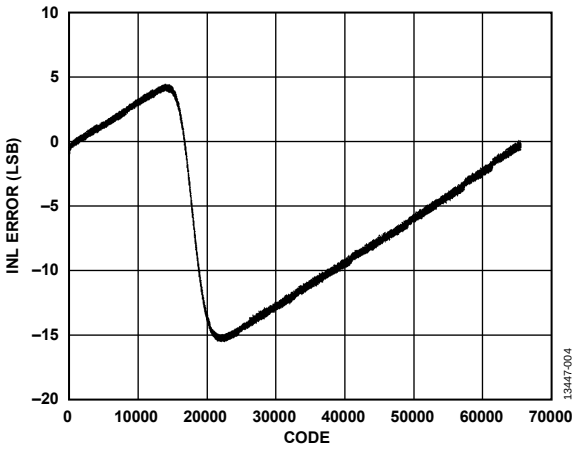

Figure 4. DAC Nonlinearity when Using Op Amp Buffer with Traditional Rail-to-Rail Input Stage

Noise Measurements

The targeted 0.1 Hz to 10 Hz noise for the complete system was less than 14 µV p-p measured at V_{OUT}. The noise of the three components can be combined in a root-sum-squares (RSS) manner to estimate the total system noise. The 0.1 Hz to 10 Hz values are

- AD5542A: 0.134 µV p-p
- ADR4525: 1.25 µV p-p
- ADA4500-2 (reference buffer): 2 µV p-p
- ADA4500-2 (DAC buffer): 2 µV p-p

The RSS value of the above contributors is 3.1 µV p-p.

The true noise of the circuit is measured by using a noise measuring box with a gain of 10,000 combined with a 0.1 Hz to 10 Hz filter. Figure 5 shows the noise test setup.

The EVAL-SDP-CB1Z System Development Platform (SDP) and SDP-PMD-IB1Z interposer boards were removed from the setup, and the supply was taken from a 4.5 V battery.

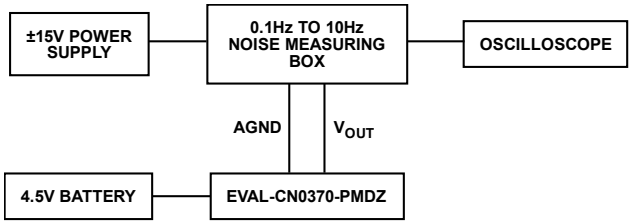

Figure 5. Test Setup for Measuring 0.1 Hz to 10 Hz Noise with Gain of 10,000

The noise output of the box with the input shorted and the noise with the circuit connected were measured and were 7.81 µV p-p and 9.6 µV p-p, respectively, as shown in Figure 6 and Figure 7. The noise of the two systems is uncorrelated and therefore combines in an RSS manner, and the system noise is calculated as follows:

$$System\ Noise = \sqrt{(9.6)^2 - (7.81)^2} = 5.58\ \mu V\ p\text{–}p$$

The corresponding noise current driving the LED is 5.58 µV ÷ 124 Ω = 45 nA for a full-scale current of 20 mA.

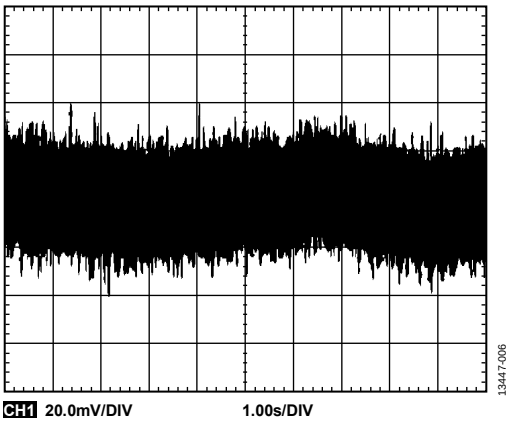

Figure 6. Output Noise with Input to Noise Measuring Box Shorted Measures 78.1 mV p-p (7.81 µV p-p Referenced to Input)

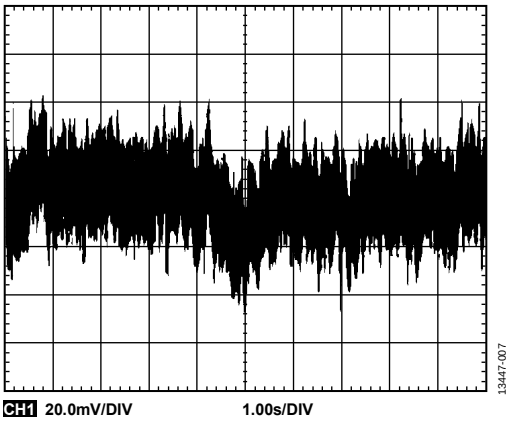

Figure 7. Output Noise with EVAL-CN0370-PMDZ Connected Measures 96 mV p-p (9.6 µV p-p Referenced to Input)

Board Layout Considerations

It is important to carefully consider the power supply and ground return layout on the board. The printed circuit board must have separate analog and digital sections. If the circuit is used in a system where multiple devices require an analog ground to digital ground connection, make the connection at only one point. Power supplies to all components must be bypassed with at least 0.1 µF capacitors. These bypass capacitors must be as physically close as possible to the device, with the capacitor ideally right up against the device. Choose the 0.1 µF capacitor to have low effective series resistance (ESR) and low effective series inductance (ESL), such as ceramic capacitors. This 0.1 µF capacitor provides a low impedance path to ground for transient currents. The power supply line must also have as large a trace as possible to provide a low impedance supply path. Use proper layout, grounding, and decoupling techniques to achieve optimum performance (see the the MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND* and the MT-101 Tutorial, *Decoupling Techniques*).

A complete design support package including layout files, schematics, and bill of materials, is available at www.analog.com/CN0370-DesignSupport.

COMMON VARIATIONS

For a lower power consumption solution (at lower speed), use the ADA4505-1/ADA4505-2/ADA4505-4 as the output buffer. The ADA4505-1/ADA4505-2/ADA4505-4 are micropower, zero crossover distortion amplifiers with low input bias current. The ADR441 and ADR421are suitable candidates to provide the 2.5 V reference. They feature high accuracy, low noise and accept input voltages up to 18 V.

The AD5063 is a 16-bit, unbuffered voltage output DAC that allows bipolar mode operation in a dual-supply application.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0370-PMDZ circuit board and the EVAL-SDP-CB1Z SDP board with the SDP-PMD-IB1Z interposer board. The SDP board and the interposer boards have 120-pin mating connectors, allowing quick setup and evaluation of the circuit performance. The EVAL-CN0370-PMDZ board is connected via the PMOD connector J3. The EVAL-CN0370-PMDZ contains the circuit to be evaluated, as described in this circuit note. The SDP board and the interposer board are used with the CN-0370 evaluation software to capture the data from the EVAL-CN0370-PMDZ circuit board. The software user guide is available at www.analog.com/wiki-CN0370.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista (32-bit), or Windows 7 (32-bit)
- EVAL-CN0370-PMDZ circuit evaluation board
- EVAL-SDP-CB1Z SDP board
- SDP-PMD-IB1Z interposer board
- CN-0370 evaluation software (download from ftp://ftp.analog.com/pub/cftl/CN0370/)
- Power supply: 6 V wall wart or EVAL-CFTL-6V-PWRZ
- Agilent 34401A multimeter or equivalent
- GPIB to USB cable (required only when making linearity measurements on the circuit)

Getting Started

Download the CN-0370 evaluation software and install it on the PC.

Functional Block Diagram

Figure 8 shows the functional block diagram of the test setup.

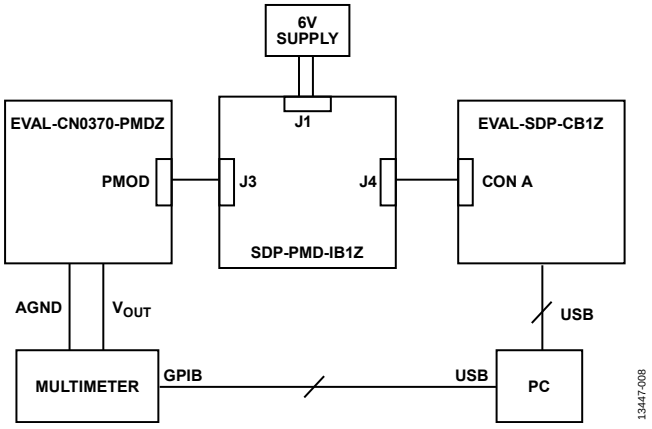

Figure 8. Test Setup Functional Block Diagram

Setup

Connect the 120-pin connector on the SDP-PMD-IB1Z interposer board to the connector marked CON A on the EVAL-SDP-CB1Z SDP board. Use nylon hardware to secure the two boards firmly, using the holes provided at the ends of the 120-pin connectors. Connect the EVAL-CN0370-PMDZ to the J3 PMOD connector.

With power to the supply off, connect a 6 V wall wart power supply to the J1 connector. Connect the USB cable supplied with the SDP board to the USB port on the PC. Do not connect the USB cable to the mini USB connector on the SDP board at this time.

Test

Apply power to the interposer board then connect the USB cable from the PC to the USB mini connector on the SDP board and launch the evaluation software. The software communicates with the EVAL-CN0370-PMDZ if the EVAL-SDP-CB1Z System Development Platform is listed in Windows **Device Manager**.

After USB communications are established, the SDP board can be used to write date to the EVAL-CN0370-PMDZ circuit evaluation board.

Figure 9 shows a photograph of the EVAL-CN0370-PMDZ circuit evaluation board.

Information and details regarding test setup and how to use the evaluation software for data capture can be found in the CN-0370 Software User Guide.

Information regarding the SDP board is available in the SDP User Guide (UG-277).

Figure 9. EVAL-CN0370-PMDZ Circuit Evaluation Board