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Devices Connected/Referenced	
AD4003	18-Bit, 2 MSPS, PulSAR®, 7.0 mW ADC in MSOP/QFN
AD8251	10 MHz, 20 V/µs, G = 1, 2, 4, 8, *i*CMOS Programmable Gain Instrumentation Amplifier
ADuM141E	Robust, Quad Channel Isolator with Output Enable and 1 Reverse Channel
ADG5207	High Voltage, Latch-Up Proof, 8-Channel Differential Multiplexer
AD8475	Precision, Selectable Gain, Fully Differential Amplifier
ADA4807-2	3.1 nV/√Hz, 1 mA, 180 MHz, Rail-to-Rail Input/Output Dual Op Amp

Isolated, Multichannel Data Acquisition System with PGIA for Single-Ended and Differential Industrial Level Signals

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0385 Circuit Evaluation Board (EVAL-CN0385-FMCZ)
System Demonstration Platform (EVAL-SDP-CH1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a cost effective, isolated, multichannel data acquisition system that is compatible with standard industrial signal levels. The components are specifically selected to optimize settling time between samples, providing 18-bit performance at channel switching rates up to approximately 750 kHz.

The circuit can process eight gain-independent channels and is compatible with both single-ended and differential input signals.

The analog front end includes a multiplexer, programmable gain instrumentation amplifier (PGIA); precision analog-to-digital converter (ADC) driver for performing the single-ended to differential conversion; and an 18-bit, 2.0 MSPS precision PulSAR® ADC for sampling the signal on the active channel. Gain configurations of 0.4, 0.8, 1.6, and 3.2 are available.

The maximum sample rate of the system is 2 MSPS in turbo mode, and 1.5 MSPS in normal mode. The channel switching logic is synchronous to the ADC conversions, and the maximum channel switching rate is 1.5 MHz. A single channel can be sampled at up to 2 MSPS with 18-bit resolution in turbo mode. Channel switching rates up to 750 kHz also provide 18-bit performance.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

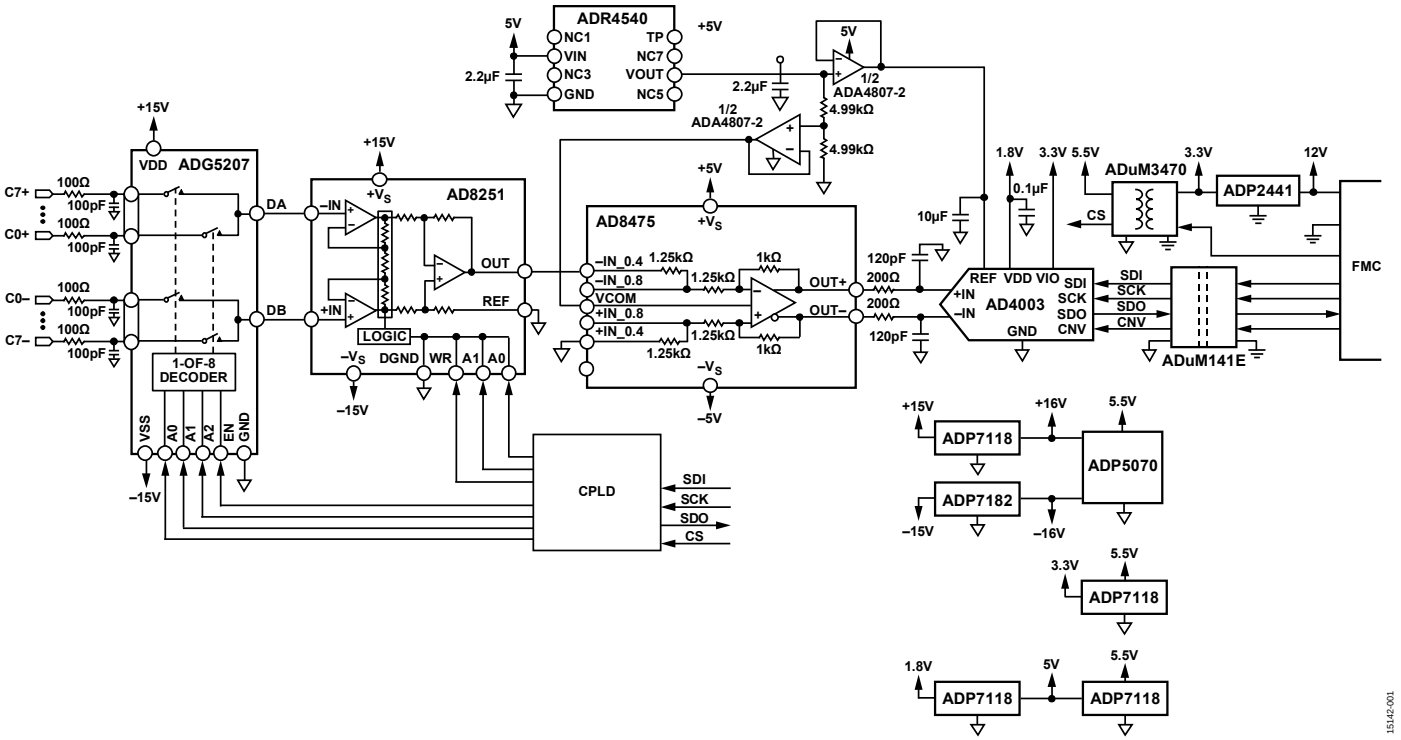

Figure 1. Isolated Multichannel Data Acquisition Simplified Circuit (All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

The circuit shown in Figure 1 is an isolated multichannel data acquisition signal chain consisting of a multiplexer, programmable gain stage, ADC driver, and a fully differential, precision, successive approximation register (SAR) ADC. The channel switching and gain switching is synchronized to the conversion period of the ADC.

The system can monitor up to eight channels using a single ADC, reducing component count and cost compared to systems with one ADC per channel. Each channel can be configured with a different gain, allowing for flexibility of input ranges. It is manipulated by the complex programmable logic device (CPLD) which can be configured in the Labview graphical user interface (GUI). The effective sample rate for each channel is equal to the sample rate of the ADC divided by the total number of channels being sampled.

The maximum sample rate of the system is limited by the settling time of the components (such as the programmable gain amplifier (PGA) bandwidth and RC filter bandwidth) in the analog front end and the isolated digital interface clock rate which runs at 75 MHz. Multiplexed signals are discontinuous in nature, resulting in potentially large voltage steps between sampling intervals. The components in the signal chain must be given adequate time to settle to these steps before the ADC performs a conversion. To maximize the time given for the signal to settle, the multiplexer channels are switched immediately after the ADC begins a new conversion.

The board power supply can take a dc input from 5 V to 12 V at the dc jack or 12 V from the SDP-H1 controller board. The ADP2441 dc-to-dc converter generates 3.3 V for the digital interface and the ADuM3470 primary supply input. The ADP5070, ADP7118, and ADP7182 are used to generate positive and negative ±15 V supplies. The ADP7118 is used to generate 5 V, 3.3 V, and 1.8 V for the analog and digital power supplies. The ADuM141E is selected for isolated high speed SPI communication. It has 150 Mbps maximum data rate, low propagation delay, and low dynamic power consumption.

Component Selection

The ADG5207 is a high voltage, latch-up proof, 8-channel differential multiplexer. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. A switching network at the inputs of the ADG5207 adds compatibility with both single-ended and differential input signals. The active channel is selected via the address pins of the device, which are controlled by the CPLD, and which can be configured in the GUI.

The AD8251 is a programmable gain instrumentation amplifier that provides selectable gain settings of 1, 2, 4, and 8. The higher gain settings boost smaller input signals to the full-scale input range of the AD4003. Each gain setting has its own suitable input range, which is shown in Table 1.

Table 1. Input Range for Each of the Four Gain Configurations

Gain	Full-Scale Input Range
0.4	±10.24 V
0.8	±5.12 V
1.6	±2.56 V
3.2	±1.28 V

The AD8475 funnel amplifier provides high precision attenuation (0.4×), accurate common-mode level shifting, and single-ended to differential conversion. Its low output noise spectral density (10 nV/√Hz) and fast settling time (50 ns to 0.001% for a 2 V output step) make it well suited to drive the AD4003.

The AD4003 is a fully-differential, 2 MSPS, 18-bit precision SAR ADC that features a typical signal-to-noise ratio (SNR) of 98 dB when using a 4.096 V reference. The AD4003 is also low power, and only consumes approximately 17 mW at full throughput. Its power consumption scales with throughput, and can operate at lower sample rates to cut its power use (for example, 0.17 mW at 100 kSPS).

System DC Accuracy Errors

Figure 2 shows the ideal transfer function of the data acquisition system.

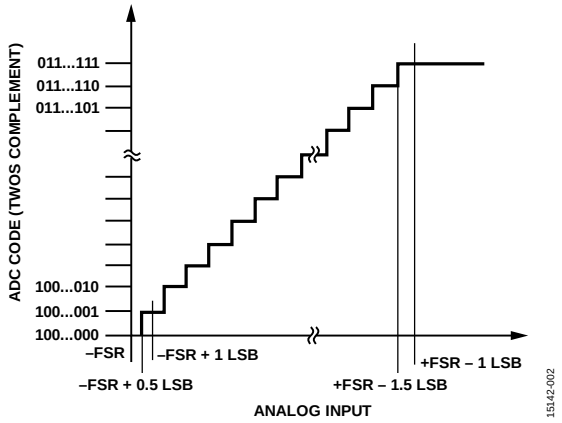

Figure 2. ADC Ideal Transfer Function

Each of the components in the data acquisition signal chain adds its own offset error and gain error that cause the real transfer function of the system to deviate from the ideal transfer function shown in Figure 2. The cumulative effects of these errors can be measured at a system level by comparing known dc inputs near zero and full scale at the input to the ADG5207 (RC filter if it is present) and the resulting output codes from the AD4003 to obtain a system calibration factor.

Offset Error Measurement

For ideal bipolar, differential ADCs, a 0 V differential input results in an output code of 0. Real ADCs typically exhibit some offset error (ε_b), which is defined as the deviation between the ideal output code and the measured output code for a 0 V input.

The offset error for the data acquisition system can be found by grounding its input and observing the resulting output code. This error varies between each of the gain settings of the AD8251 and between each of the channels of the ADG5207. Offset error is therefore measured for each of the channels in all four gain configurations.

Because the system monitors multiple channels, it is also important to quantify the amount by which the offset error deviates between channels. Offset error match ($\Delta\varepsilon_{b,MAX}$) is a measure of the maximum deviation between the offset error of each of the channels and the average offset error of all of the channels. Offset error match is calculated using the following equation:

$$\overline{\Delta\varepsilon_{b,MAX}} = (\max(\varepsilon_{b,i} - \frac{\sum_{j=0}^{7}\varepsilon_{b,j}}{8}) \mid i = 0, 1, ..., 7)$$

where $\varepsilon_{b,i}$ and $\varepsilon_{b,j}$ are the offset errors for the i and j channels, respectively.

This offset error match can be found for each of the gain configurations. Note that offset error can be expressed either in codes or volts.

Gain Error Measurement

Error in the gain of the system also contributes to overall system inaccuracy. The ideal transfer function of the AD4003 is shown in Figure 2, where the -2^{17} and $2^{17} - 1$ output codes correspond to a negative full-scale input voltage (−FS) and a positive full-scale input voltage (+FS), respectively; however, the combination of offset error (ε_b) and gain error (ε_m) results in a deviation from this relationship.

Gain error can be expressed as a percentage error between the actual system gain and the ideal system gain. The more common expression is in percent full-scale error (%FS), which is a measure of the error between the ideal and actual input voltages that produces the $2^{17} - 1$ code.

The ideal full-scale input voltage ($V_{FS,IDEAL}$) is a function of the resolution of the ADC (18-bits for the AD4003) and the accuracy of the reference voltage (V_{REF}). Errors in the voltage reference translate to gain errors in the ADC. To decouple reference errors from ADC gain error, V_{REF} is measured using a precision multimeter. The ideal full-scale input voltage can then be calculated using

$$V_{FS,IDEAL} = \frac{2^{18}}{2 \times V_{REF,MEAS}} = \frac{2^{17}}{V_{REF,MEAS}}$$

The actual system gain can be found by calculating the slope of the linear regression of a group of several input voltages (m_{LR}) and the resulting output codes:

$$Y_{REAL} = m_{LR} \times V_{IN}$$

The real full-scale input voltage ($V_{FS,REAL}$) can then be calculated using

$$V_{FS,REAL} = \frac{Y_{REAL}}{m_{LR}} = \frac{2^{17}}{m_{LR}}$$

The gain error (expressed in %FS error) can then be calculated using

$$\varepsilon_m = \frac{V_{FS,IDEAL} - V_{FS,REAL}}{V_{FS,IDEAL}} \times 100\%$$

The gain error of the system varies with the gain of the AD8251, but is channel independent. Therefore, gain error is measured for each of the four gain configurations, but only using one of the ADG5207 channels in this system.

System Noise Analysis

One of the key design goals in precision data acquisition systems is achieving a high SNR, which can be achieved by increasing the full-scale signal amplitude and/or by decreasing the noise power generated by the components in the system.

The total noise power present in the system can be found by taking the root sum square (rss) of the noise power contributed by its individual components, referred to the input of the AD4003:

$$v_{n,\,TOTAL} = \sqrt{v_{n,\,ADG5207}{}^2 + v_{n,\,AD8251}{}^2 + v_{n,\,AD8475}{}^2 + v_{n,\,AD4003}{}^2}$$

The expected SNR of the system ($SNR_{EXPECTED}$) can then be found using

$$SNR_{EXPECTED} = 20\log\left(\frac{V_{REF}/\sqrt{2}}{v_{n,\,TOTAL}}\right)$$

The expected noise contributions for each component in the system and the resulting expected SNR performance of the whole system is shown in Table 2. The total system noise calculation ignores thermal noise contributed by the passive components in the system.

Noise Due to the AD4003 ADC

The noise of the AD4003 ADC is a function of both its inherent quantization error and noise caused by internal components (such as passive components producing thermal noise).

The rms input voltage noise of the AD4003 can be calculated from its specified SNR using

$$v_{n,\,AD4003} = \frac{V_{REF}}{\sqrt{2}} \times 10^{\left(\frac{SNR_{AD4003}}{20}\right)}$$

The SNR for the AD4003 (SNR_{AD4003}) is specified as approximately 98 dB for a 4.096 V reference.

The single-pole RC filter at the input of the AD4003 limits the wideband noise from the upstream components. A smaller filter bandwidth improves SNR by further limiting noise power; however, its time constant must also be sufficiently short to settle voltage kickbacks due to charge injections that occur as the AD4003 inputs reconnect to the front-end circuitry during the acquisition phase. The appropriate bandwidth for the system is at least 5 MHz (for more information, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*).

Noise Due to the AD8475 Funnel Amplifier

The rms noise contributed by the AD8475 ($v_{n,\,AD8475}$) is a function of its referred to output noise spectral density (NSD) (e_{AD8475}) and the RC filter bandwidth at the input to the AD4003 (BW_{RC}):

$$v_{n,\,AD8475} = e_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

where e_{AD8475} = 10 nV/√Hz.

Noise Due to the AD8251 Instrumentation Amplifier

The AD8251 functions as a gain stage that improves SNR for small amplitude signals by boosting their amplitude to more closely fill the $\pm V_{REF}$ range at the input to the AD4003. Ideally, if the system gain increases by a factor of G, the SNR (in dB) of the input signal improves by

$$\Delta SNR = \log_{10}(G)$$

This level of improvement is not achievable in reality, however, because wideband noise is also amplified by the noise gain of the circuit. Fortunately, this degradation is not as large as the improvement due to signal gain.

The rms noise contributed by the AD8251 is a function of its referred to input NSD (e_{AD8251}), its gain setting (G_{AD8251}), the attenuation factor of the AD8475 (G_{AD8475}), and the noise filter bandwidth at the input of the AD4003:

$$v_{n,\,AD8251} = e_{AD8251} \times G_{AD8251} \times G_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

The value of e_{AD8251} is also dependent on the AD8251 gain; the value of e_{AD8251} can be found in the AD8251 data sheet.

Noise Due to the ADG5207 Multiplexer

The NSD and resulting rms noise contributed by the ADG5207 can be found by using the Johnson/Nyquist noise equation, because the device acts like a series resistance between the source and the rest of the analog front end:

$$e_{n,\,ADG5207} = \sqrt{4 \times k_B \times T \times R_{ON}}$$

and

$$v_{n,\,ADG5207} = e_{n,\,ADG5207} \times G_{AD8251} \times G_{AD8475} \times \sqrt{\frac{\pi}{2} \times BW_{RC}}$$

The resistance of each channel (R_{ON}) can be found in the ADG5207 data sheet.

A summary of the calculated noise performance of the system is shown in Table 2. The largest contributors to the total noise are the AD8251 in-amp and the AD4003 ADC.

Table 2. Noise Performance for the Multichannel Data Acquisition System

	ADG5207		AD8251		AD8475		AD4003	Total	
Gain	e_n, ADG5207 (nV/√Hz)	v_n, ADG5207 (µV rms)	e_n, AD8251 (nV/√Hz)	v_n, AD8251 (µV rms)	e_n, AD8475 (nV/√Hz)	v_n, AD8475 (µV rms)	v_n, AD4003 (µV rms)	v_n, total (µV rms)	SNR (dB)
0.4	2.04	2.29	40	44.7	10	28	35.4	63.6	93.2
0.8	2.04	4.57	27	60.4	10	28	35.4	75.5	91.7
1.6	2.04	9.15	22	98.4	10	28	35.4	108.6	88.5
3.2	2.04	18.3	18	161	10	28	35.4	168.2	84.7

Settling Time Analysis

When the circuit shown in Figure 1 is sampling multiple channels, each of the different inputs are merged into a time-division multiplexed signal by the ADG5207. Multiplexed signals are discontinuous in nature, and typically have large voltage steps occurring in short time intervals. For the system in Figure 1, the voltage differential between two consecutive channels may be as large as 20 V at the inputs of the ADG5207, and the time allotted for settling is only as long as the sampling period.

Figure 3 shows the settling time model of the circuit in Figure 1. Each of the components in the system has its own settling characteristics (see the following sections).

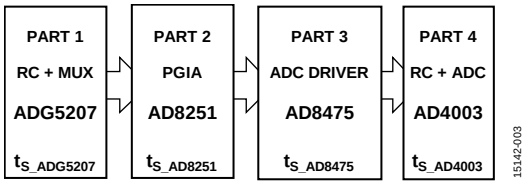

Figure 3. Settling Time Model of CN-0385 Circuit

Settling time is defined as the time required for the analog front-end circuitry to settle an input step to a certain precision. This precision is usually specified in percent error (for example, 0.1% or 0.01%); however, in conversion systems, it is also helpful to relate it to resolution. For example, settling to a 16-bit resolution is roughly equivalent to settling to 0.001%. Table 3 shows the relationship between settling to percent error and to resolution for a single-pole system.

Table 3. Percent Error and Effective Resolution

Resolution, No. of Bits	LSB (%FS)	No. of Time Constants = −ln (% Error/100)
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Estimating the settling time of an analog front end with multiple components is not trivial for a variety of reasons. First, many devices do not specify settling characteristics to very high precision. Settling time for an active device is also not linearly related to settling precision, and it may take up to 30 times as long to settle to 0.01% as to 0.1%. The settling time can be due to long-term thermal effects inside the amplifier. Settling time is also dependent on the load that the device is driving, and settling time is generally not characterized for multiple load conditions.

Measuring high precision settling is also difficult without a specialized characterization platform, because of the effects of oscilloscope overdrive and sensitivity, and the difficulty of generating an input pulse with sufficient rise time and settling time.

Settling time can be estimated provided certain bounds and assumptions are used in analyzing the circuit. The total settling time can be calculated by taking the rss of the settling times of the individual components:

$$t_{S\_TOTAL} = \sqrt{t_{S\_ADG5207}^{\ 2} + t_{S\_AD8251}^{\ 2} + t_{S\_AD8475}^{\ 2} + t_{S\_AD4003}^{\ 2}}$$

The maximum throughput of the system is inversely proportional to the total settling time:

$$f_{SR} < \frac{1}{t_{S\_TOTAL}}$$

Settling Time of the ADG5207

The equivalent circuit for a CMOS switch can be approximated as an ideal switch in series with a resistor (R_{ON}) and in parallel with two capacitors (C_S, C_D). The multiplexer stage and associated filters can therefore be modeled as shown in Figure 4.

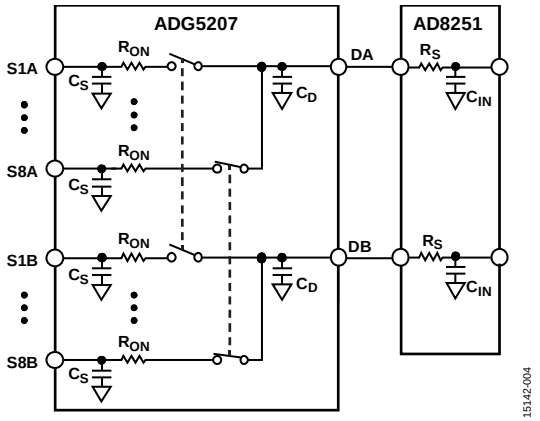

Figure 4. Settling Time Model of the ADG5207

Each channel functions similarly to an RC circuit having an associated time constant that dominates settling time. Dynamically switching channels complicates signal settling; at the time channels are switched, the difference between the previous output and the current input produces a kickback transient. This kickback is similar to the one that occurs at the input to the AD4003 as it enters the acquisition phase. For a more detailed description, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*.

The circuit in Figure 4 was simulated using NI Multisim™, as shown in Figure 5, with the following component values from the respective device data sheets:

- R_{ON} = 250 Ω
- C_S = 3.5 pF
- C_D = 36 pF
- $R_{IN}||C_{IN}$ = 1.25 GΩ||2 pF

The input resistance of the AD8251 (R_{IN}) is sufficiently large (1.25 GΩ) to be omitted from simulation.

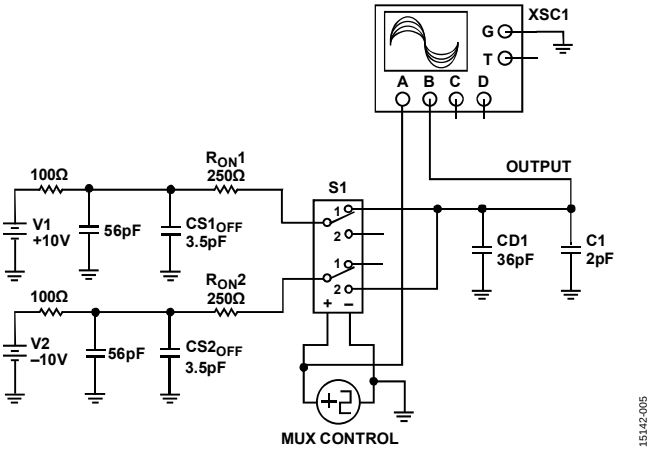

Figure 5. Multisim Settling Time Model of the ADG5207

The simulation results are shown in Figure 6. The time required for the output of the ADG5207 to settle to 0.001% of 10 V is $t_{S\_ADG5207}$ = 188 ns.

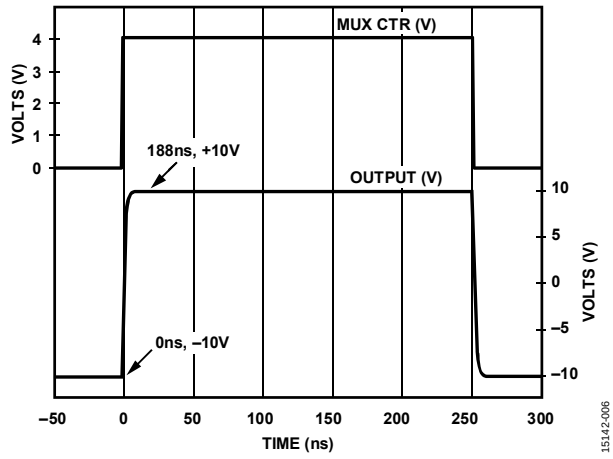

Figure 6. Settling Time Waveforms for the ADG5207 Simulation Model

Settling Time of the AD8251 and AD8475

The AD8251 data sheet specifies its settling time for a variety of input voltage step sizes down to a 0.001% error for each gain configuration. Given a load of 10 kΩ and gain setting of 1, the AD8251 can settle a 20 V step at its output to 0.001% in approximately 1 µs. The gain of 1 setting requires the most settling time; therefore, the settling time analysis uses 1 µs.

However, the 1 µs number may not be accurate when the AD8251 is driving one of the inputs of the AD8475, which has an input impedance of 2.92 kΩ instead of 10 kΩ. It is also not possible to ascertain settling time of the AD8251 to 18-bit resolution, because of the nonlinear relationship between settling time and precision. Therefore, the best settling time estimation is 0.001% error (or 16-bit resolution).

The AD8475 has a settling time specification of 50 ns to 0.001% for a 2 V differential output step. The maximum voltage step size expected on the outputs of the AD8475 is twice the reference voltage (V_{REF}), or approximately 8 V. Assuming that the settling time is proportional to the output voltage step, the settling time to 0.001% (16 bits) for an 8 V step is approximately 200 ns (4 × 50 ns).

The settling time of each amplifier is, therefore,

- t_{S_AD8251} = 1 µs
- t_{S_AD8475} = 200 ns

Settling Time of the RC Noise Filter and AD4003

Figure 7 shows the equivalent circuit of the inputs of the AD4003. R_{EXT} and C_{EXT} are the components in the RC wideband noise filter in front of the ADC. R_{IN} and C_{IN} are the input resistance and capacitance of the AD4003, respectively. C_{IN} is mainly the internal capacitive digital-to-analog converter (DAC). C_{PIN} is primarily the pin capacitance, and is ignored. The values for these components are as follows:

- R_{EXT} = 200 Ω
- C_{EXT} = 120 pF
- R_{IN} = 400 Ω
- C_{IN} = 40 pF

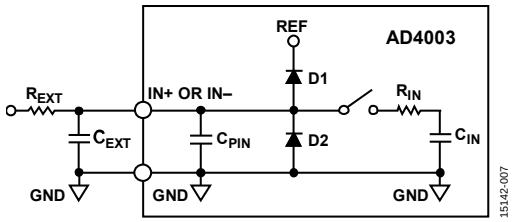

Figure 7. Settling Time Model of the AD4003 and RC Noise Filter

The AD4003 employs an internal capacitive DAC and a charge redistribution algorithm to determine its output code. The conversion process contains two phases, acquisition and conversion. During acquisition, the capacitive DAC is connected to the input terminals of the AD4003. During conversion, it is disconnected from the input terminals, and internal logic performs the charge-redistribution algorithm. Compared to other PulSAR ADCs, the AD4003 has a much

shorter conversion time, and it allows the user to return to acquisition phase before the end of conversion. Therefore, if the user runs the ADC at slower throughput, there is have more time to settle the kickback.

The signal must be settled by the end of the acquisition phase for an accurate conversion. To maximize the time given for the signal to settle, the multiplexer switches channels immediately after the AD4003 begins its conversion phase.

In addition to settling from the multiplexed signal from the output of the AD8475, the RC noise filter and AD4003 inputs also need to settle to the voltage kickback that occurs at the beginning of the acquisition phase. For more information, see the Analog Dialogue article, *Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter*.

The settling time for the circuit in Figure 7 was simulated in NI Multisim, as shown in Figure 8. V1 represents the maximum voltage step expected at either input of the AD4003 (from a single-ended output of the AD8475). CNV and S1 simulate the AD4003 switching from the conversion phase (occurring when V1 changes value) to the acquisition phase (300 ns after start of conversion). CNV keeps S1 open until 300 ns after V1 steps from 0 V to 4 V to represent the transition from the conversion phase to the acquisition phase. ADC_IN is the voltage that is sampled by the AD4003 on a CNV rising edge.

The settling time for this portion of the system is equal to the time between V1 switching to 4 V (at TIME = 0, see Figure 9) to ADC_IN settling to 0.001% of 4 V.

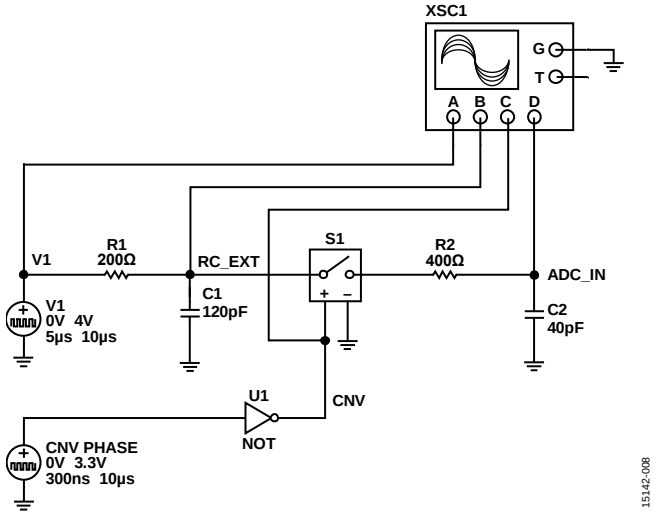

Figure 8. Multisim™ Settling Time Model of the AD4003 and RC Noise Filter

The simulation results are shown in Figure 9. The time taken for the output to settle to 0.001% of 4 V is t_{S_AD4003}= 711 ns.

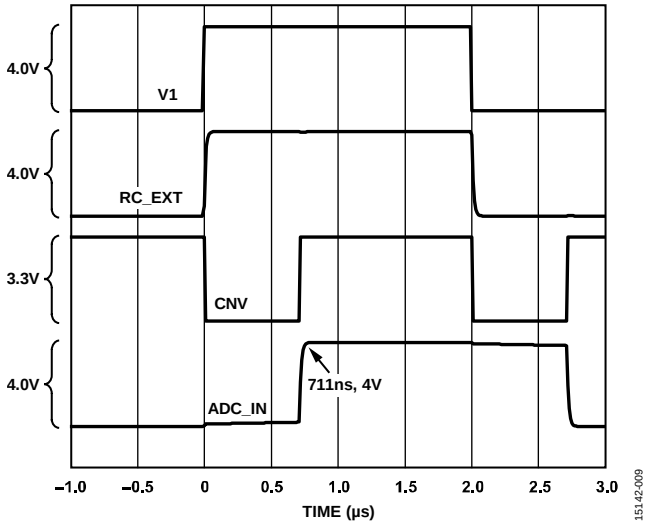

Figure 9. Settling Time Waveforms for the AD4003 and RC Noise Filter Simulation Model

Total System Settling Time

The total settling time of the entire circuit shown in Figure 1 can now be estimated by calculating the rss of the settling times for each component:

- $t_{S\_ADG5207}$ = 188 ns
- t_{S_AD8251} = 1000 ns
- t_{S_AD8475} = 200 ns
- t_{S_AD4003} = 711 ns
- $t_{S\_TOTAL} = \sqrt{188\,\text{ns}^2 + 1\,\mu\text{s}^2 + 200\,\text{ns}^2 + 711\,\text{ns}^2} \approx 1257\,\text{ns}$

The expected maximum channel switching sample rate of the system is then

$$f_{SR} < \frac{1}{1257\,\text{ns}} \approx 795\,\text{kSPS}$$

Offset and Gain Error Results

Table 4 shows the offset error measured (in LSBs) for each of the channels in each gain configuration for the circuit in Figure 1. Table 4 also shows the average offset error of all of the channels for each gain configuration.

The offset errors were measured by grounding all of the channel inputs and collecting and averaging 32,768 samples taken on each of the channels in each gain configuration.

Table 4. Offset Error Measurements for all Channels and Gain Configurations (Error in LSBs)

Gain	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8	Channel Average
0.4	1.34	1.33	1.31	1.36	1.44	1.45	1.46	1.48	1.40
0.8	1.98	1.99	2.02	2.06	2.00	1.98	1.99	1.97	2.00
1.6	3.25	3.19	3.22	3.19	3.17	3.08	3.13	3.14	3.17
3.2	5.57	5.66	5.67	5.55	5.57	5.50	5.54	5.52	5.57

Table 5 shows the gain error measured for each of the gain configurations for the circuit in Figure 1. The %FS error was found using the analysis methods described previously, and the actual gain in V/V was calculated by subtracting this error from the ideal gain.

Table 5. Gain Error Measurements for all Gain Configurations

Gain	Gain Error (%FS)
0.4	0.02
0.8	0.02
1.6	0.03
3.2	0.02

Performance Results Without Channel Switching

Figure 10, Figure 11, Figure 12, and Figure 13 show the fast Fourier transform (FFT) plots for a 10 kHz, full-scale, sine wave input on a single channel for gain configurations of 0.4, 0.8, 1.6, and 3.2, respectively. Table 6 shows the SNR and rms noise measured for each of the gain configurations.

Table 6. SNR, Noise, and THD vs. Gain for 10 kHz Input

Gain	SNR (dB)	RMS Noise (µV rms)	THD (dB)
0.4	93.9	55.2	−99.2
0.8	92.8	62.6	−98.5
1.6	90.6	80.7	−97.0
3.2	88.0	108.9	−94.6

The input signal was supplied by an Audio Precision SYS-2700 series signal generator, with the board set in differential input mode. Figure 14 shows total harmonic distortion (THD) measurements vs. the frequency of the input signal for each gain configuration.

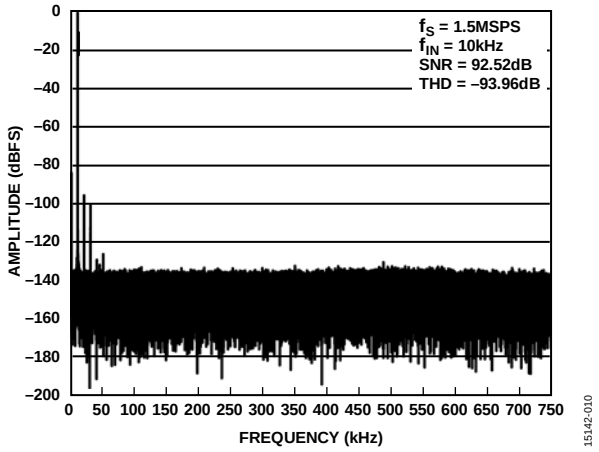

Figure 10. FFT for 10 kHz, 20 V p-p Input for Gain = 0.4 on Single, Static Channel

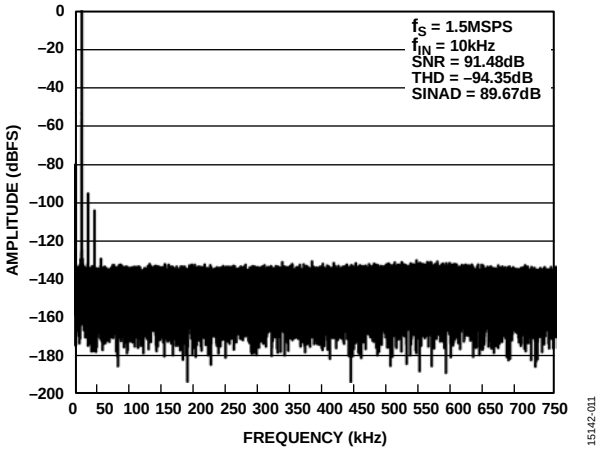

Figure 11. FFT for 10 kHz, 10 V p-p Input for Gain = 0.8 on Single, Static Channel

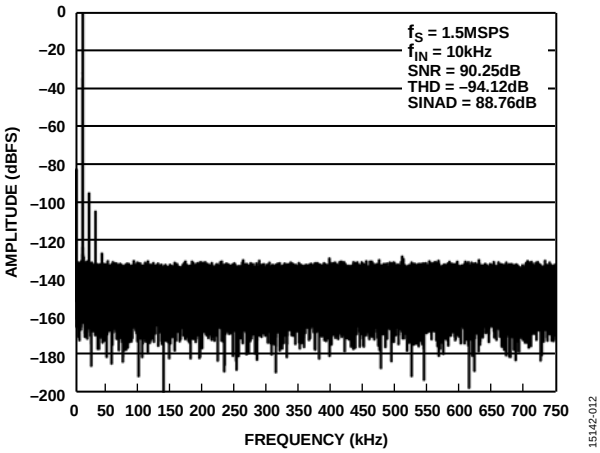

Figure 12. FFT for 10 kHz, 5 V p-p Input for Gain = 1.6 on Single, Static Channel

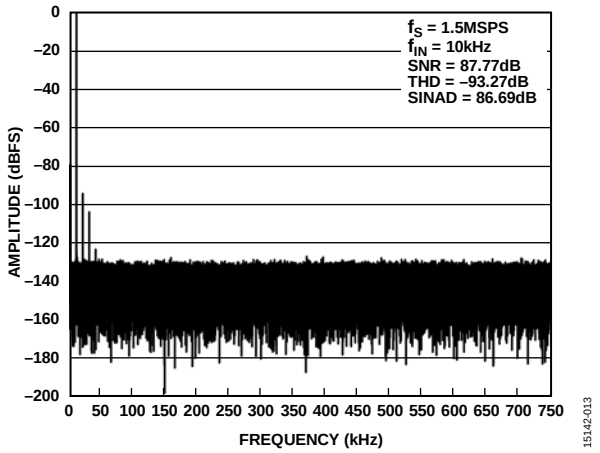

Figure 13. FFT for 10 kHz, 2.5 V p-p Input for Gain = 3.2 on Single, Static Channel

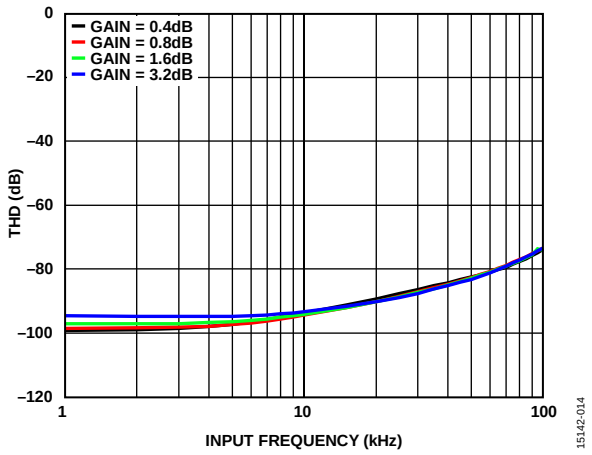

Figure 14. THD Measured for Various Input Frequencies on a Single, Static Channel

System Performance with Channel Switching

Several tests were performed to evaluate the performance of the system when scanning multiple channels. Experiments using precision dc sources measured the error in output code with respect to sample rate (see the Circuit Note CN-0269 for similar tests) and voltage step size between channels. AC performance was also measured for switching between two out of phase, full-scale inputs from a precision ac source (Audio Precision AP SYS-2712).

Figure 15 and Figure 16 show the test setup for dc and ac performance tests, respectively. The channel switching rate is the rate at which the ADG5207 switches from one channel to another, and is equivalent to the sample rate of the AD4003.

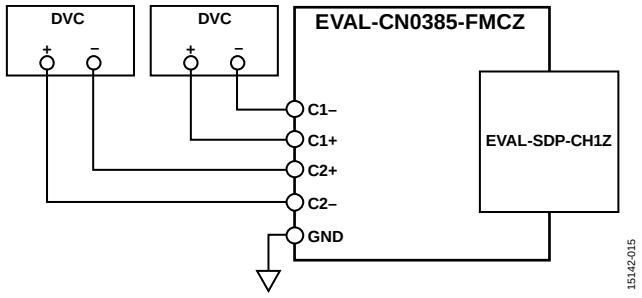

Figure 15. Settling Time Evaluation Setup Using DC Calibrators

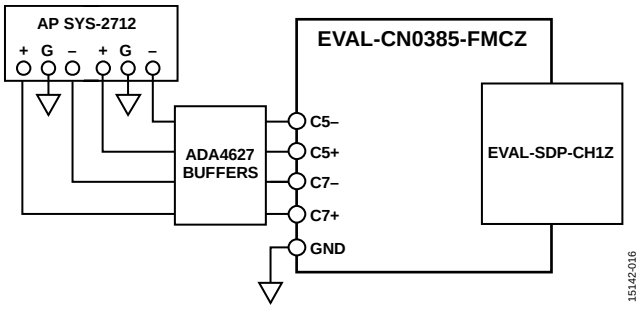

Figure 16. Settling Time Evaluation Setup Using AC Signal Generator

The dc tests involved varying the voltage step size between the two channels and the channel switching rate. The channel switching rate was varied from 50 kHz to 1 MHz in 50 kHz increments. The voltage step size was varied over different ranges for each of the gain configurations. A mean code result was measured for each channel for each voltage step size and channel switching rate by averaging 8,192 samples taken on each channel. A mean code result was also measured for each channel in the static case (no switching between channels). The mean code errors discussed below were found by taking the difference between the mean codes measured for the static case and for the switching channels.

Figure 17, Figure 18, Figure 19, and Figure 20 show the mean code error for various voltage step sizes at several switching rates in each of the four gain configurations. Figure 21, Figure 22, Figure 23, and Figure 24 show the mean code error for full-scale voltage steps at various switching rates in each of the four gain configurations.

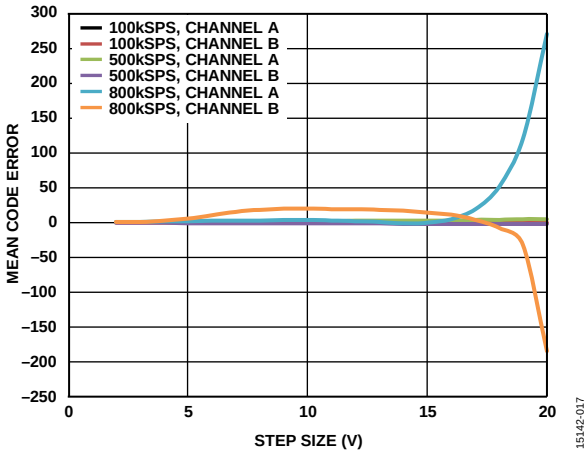

Figure 17. Mean Code Error vs. Voltage Step Size, Gain = 0.4

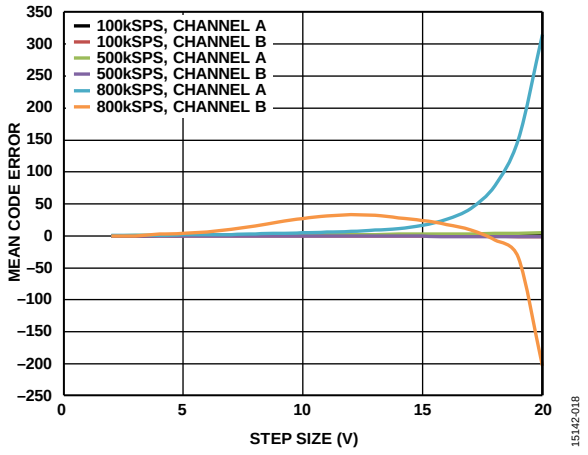

Figure 18. Mean Code Error vs. Voltage Step Size, Gain = 0.8

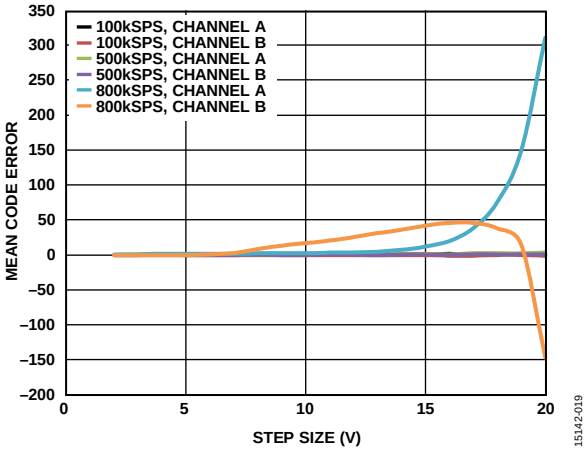

Figure 19. Mean Code Error vs. Voltage Step Size, Gain = 1.6

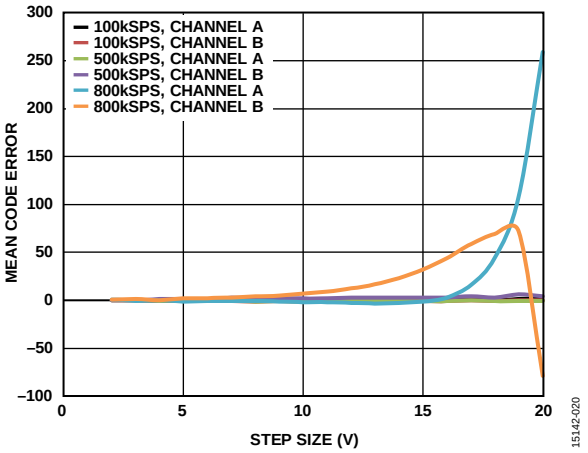

Figure 20. Mean Code Error vs. Voltage Step Size, Gain = 3.2

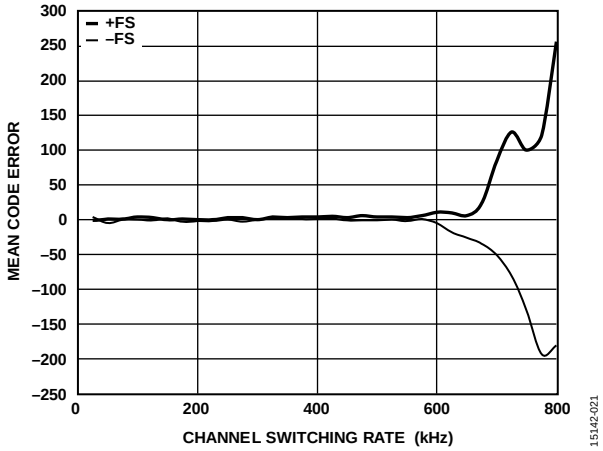

Figure 21. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 0.4

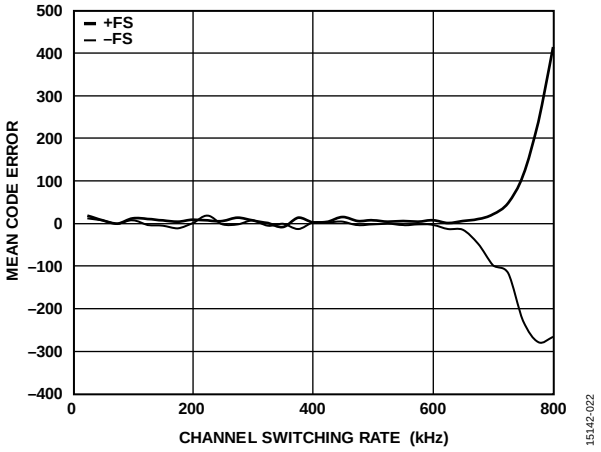

Figure 22. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 0.8

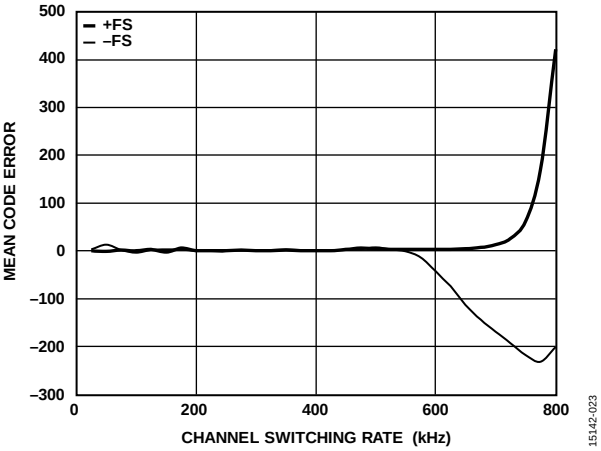

Figure 23. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 1.6

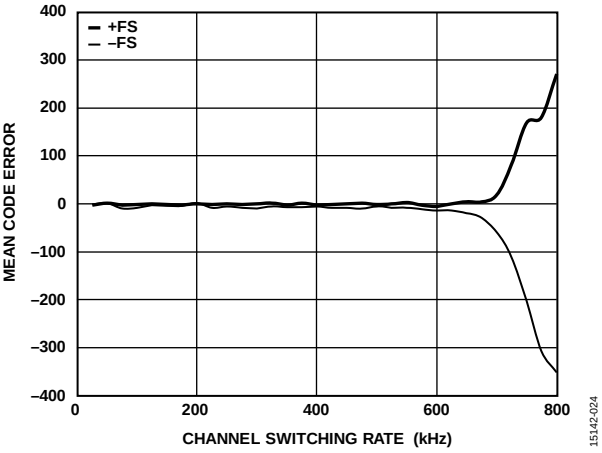

Figure 24. Mean Code Error vs. Channel Switching Rate for Full-Scale Input Step, Gain = 3.2

The mean code error increases as the voltage step size and channel switching rate increase. This increase is caused by the combined slew and settling time limitations of the components in the signal chain. Increasing the step size forces the system to settle larger changes in voltage and increasing the channel switching rate decreases the amount of time the system is given to settle these changes. At sufficiently high step sizes and switching rates, the mean code error becomes unpredictably large, as in the gain of 0.4 configuration (see Figure 17 and Figure 21). This code error is caused by the slew rate limitations of the input buffer amplifiers in the AD8251 in-amp.

The performance of the system when using the ac source was evaluated by comparing its THD with respect to the channel switching rate. The AP SYS-2712 provided a full-scale sine wave input on one channel and an inverted version of the sine wave on another channel. THD was measured for various sample rates, ranging from 25 kSPS to 1.5 MSPS in 25 kSPS increments. Figure 25 shows the THD measured for each of the channels in each of the gain configurations.

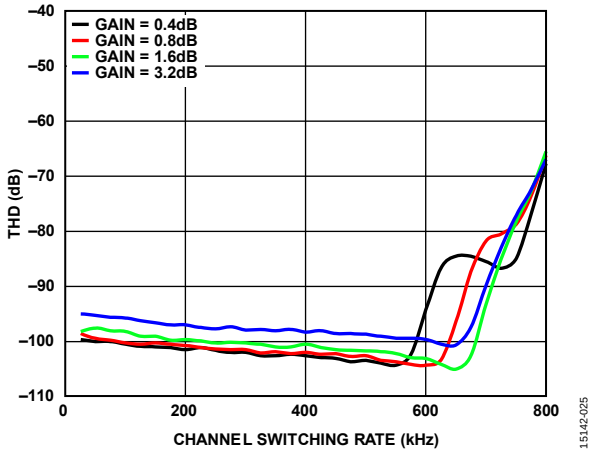

Figure 25. THD vs. ADG5207 Channel Switching Rate for Full-Scale 1 kHz Input

The THD performance of the system begins to degrade at roughly 700 kSPS (depending on the gain configuration). The whole signal chain SNR and THD performance is mainly limited by the PGA AD8251. A smaller RC filter at the front of AD4003 also gives better THD at higher channel switching sampling rate.

COMMON VARIATIONS

The AD4003 ADC is pin-for-pin compatible with various other 14-bit, 16-bit, and 18-bit, 10-lead precision SAR ADCs that can be used in the CN-0385 system. The ADG1207, with wider bandwidth, can be an alternative to the ADG5207. The ADG5248F, with fault protection and detection function, can be used for single-ended inputs. The AD8475 provides a differential output signal for other differential ADCs, such as the AD7690. The ADA4805-1 op amp is an alternative for the AD8475 when driving pseudo differential or single-ended ADCs, such as the AD4000. Other Analog Devices, Inc., LDOs, such as the ADP7102 and ADP7142, can replace the ADP7118.

CIRCUIT EVALUATION AND TEST

This circuit uses the EVAL-CN0385-FMCZ circuit board and the EVAL-SDP-CH1Z SDP-H1 system demonstration platform controller board. The two boards have 160-pin mating connectors, allowing quick setup and evaluation of the performance of the circuit. The circuit board contains the circuit to be evaluated, as described in this circuit note, and the SDP-H1 controller board is used with the CN-0385 Evaluation Software to capture the data from the circuit board.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP or Windows Vista® (32-bit), or Windows 7 (32-bit)
- EVAL-CN0385-FMCZ circuit evaluation board
- EVAL-SDP-CH1Z SDP-H1 controller board
- CN-0385 Evaluation Software (download from ftp://ftp.analog.com/pub/cftl/CN0385/)
- 5 V to 12 V dc power supply or wall wart (9 V wall wart included with EVAL-CN0385-FMCZ board)
- USB to micro-USB cable
- Low distortion, low output impedance signal generator to provide ±10 V output
- Low noise, high precision dc supply to provide ±10 V output

Getting Started

Download the evaluation software from ftp://ftp.analog.com/pub/cftl/CN0385/, and then install the software on the PC.

Functional Block Diagram

See Figure 1 for the circuit block diagram and the **EVAL-CN0385-FMCZ-SCH.pdf** file for the complete circuit schematic. This file is contained in the CN-0385 Design Support Package (available at www.analog.com/CN0385-DesignSupport). A functional block diagram of the test setup is shown in Figure 26.

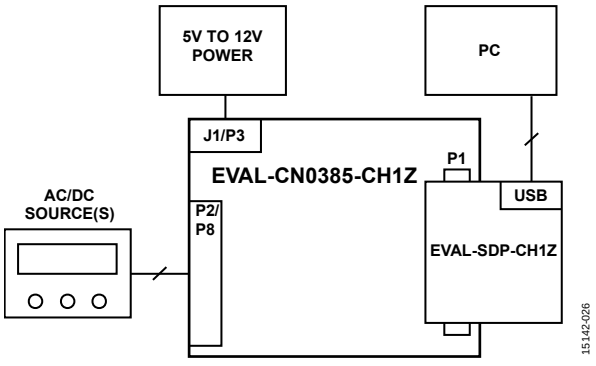

Figure 26. Test Setup Functional Block Diagram

Hardware Setup

Figure 27 shows the EVAL-CN0385-FMCZ evaluation hardware. Information and details regarding the SDP-H1 board can be found in the SDP-H1 User Guide.

Connect the 160-pin connector on the circuit board to the J4 connector on the SDP-H1 controller board.

First, connect a 5 V to 12 V dc wall wart to the P3 dc jack or to Terminal Block J1 and Jumper J2 on position V_EXT. Or, place J2 in position V_FMC to use the 12 V supply from the SDP-H1 board. Then connect the SDP-H1 board to the PC via the USB to micro-USB cable.

Test

With the power supply or dc wall wart and USB cable connected, launch the evaluation software. When USB communications are established, the SDP-H1 board can be used to send, receive, and capture data from the EVAL-CN0385-FMCZ board and perform data analysis in the time and frequency domains.

Information and details regarding test setup and calibration, and how to use the evaluation software for data capture can be found in the CN-0385 Software User Guide (available at www.analog.com/CN0385-UserGuide).

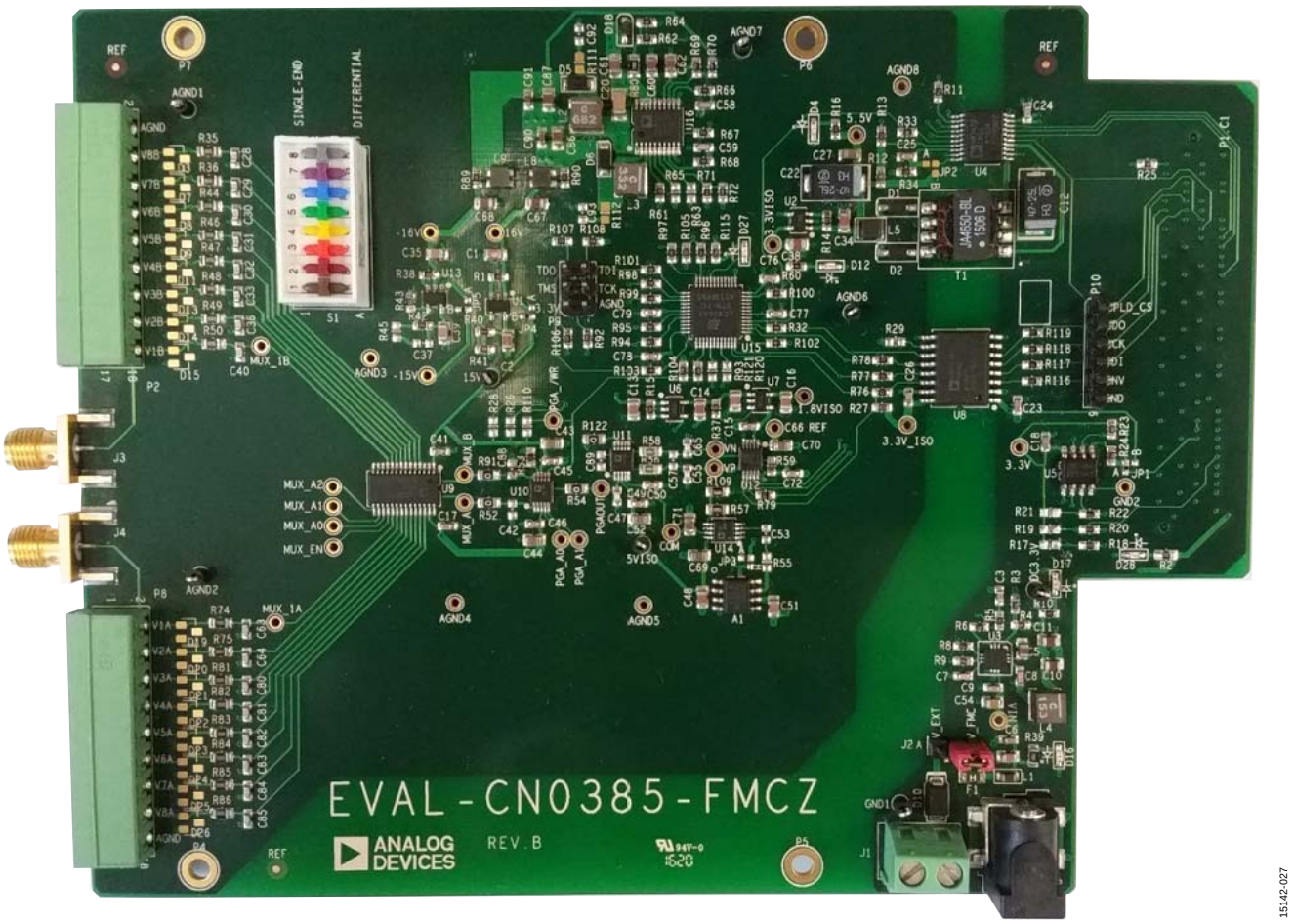

Figure 27. EVAL-CN0385-FMCZ Evaluation Hardware