

**Circuits
from the Lab®**
Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0393.

Devices Connected/Referenced

ADAQ7988	16-Bit, 500 kSPS, μ Module Data Acquisition System
AD8251	10 MHz, 20 V/ μ s, G = 1, 2, 4, 8 iCMOS Programmable Gain Instrumentation Amplifier
ADuM3470	PWM Controller and Transformer Driver with Quad-Channel Isolators
ADuM3150	3.75 kV, 6-Channel, SPI Isolator Digital Isolator for SPI with Delay Clock
ADR4550	Ultralow Noise, High Accuracy Voltage Reference (5 V)
ADP7118	20 V, 200 mA, Low Noise CMOS LDO Linear Regulator
ADP7182	-28 V, -200 mA, Low Noise, Linear Regulator
ADP1614	650 kHz/1.3 MHz, 4 A, Step-Up, PWM, DC-to-DC Switching Converter

Bank Isolated, 2-Channel, 16-Bit, 500 kSPS, Simultaneous Sampling Signal Chain Featuring μ Module Data Acquisition System

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[CN-0393 Circuit Evaluation Board \(EVAL-CN0393-FMCZ\)](#)
[System Demonstration Platform \(EVAL-SDP-CH1Z\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

The circuit in Figure 1 is a two-channel, bank isolated, wide bandwidth data acquisition (DAQ) system, implemented with a simultaneous sampling architecture using an analog-to-digital converter (ADC) per channel. The system achieves high channel density along with isolation between the bank and the digital backplane, all while delivering exceptional performance. The design also makes efficient use of isolation channels by configuring the ADCs in daisy-chain mode and utilizing an isolator product with a trimmed delay clock feature. Power generation is also simplified using an isolator with an integrated pulse width modulation (PWM) controller and transformer

driver to perform dc-to-dc conversion across the isolation barrier. The system also includes many common features of a typical DAQ signal chain, including input circuit protection, programmable gain channels, high accuracy, and high performance.

The simultaneous sampling realizes multiple channels without sample rate limitations inherent in multiplexed DAQ signal chains. The analog front end (AFE) design is also simpler than the multiplexed option, because the settling performance requirements of the system are less demanding. Sampling occurs simultaneously for each channel, while sequential sampling systems have delays between channels.

Digital bank isolated DAQ designs provide protection for digital back end circuitry and reduce ground loop and common-mode interference between banks. They feature multiple DAQ signal chains per ground plane, and can be implemented with fewer digital isolation devices than channel-to-channel isolated systems.

Rev. A

Circuits from the Lab® reference designs from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

Evaluation software is provided to allow easy interfacing with the circuit shown in Figure 1. The software includes a graphical user interface (GUI) to control various circuit parameters and settings, which communicates to the FPGA on the [SDP-H1](#) board. For more information on obtaining the software, see the Circuit Evaluation and Test section.

Component Selection

The [ADAQ7988](#) is a 16-bit, 500 kSPS, μ Module[®] data acquisition system that integrates four common signal processing and conditioning blocks into a system in package (SiP) design that supports a variety of applications. The [ADAQ7988](#) also contains the most critical passive components, eliminating many of the design challenges associated with traditional signal chains that utilize successive approximation register (SAR) ADCs. These passive components are crucial to achieving the specified device performance.

The [ADAQ7988](#) is part of an all Analog Devices, Inc., active component solution that contains a high accuracy, low power, 16-bit SAR ADC; a low power, high bandwidth ADC driver; a wideband noise RC filter; a low power, stable reference buffer; a 10 μ F reference decoupling capacitor; and an efficient power management block, all housed in a tiny 5 mm \times 4 mm LGA package. This integration reduces design complexity and can save up to 50% PCB area when compared to similar individual component designs. The [ADAQ7988](#) also provides a significant level flexibility to adapt to a wide assortment of applications; for example, the integrated ADC driver can be set in a variety of configurations and gains, enabling compatibility with multiple input ranges.

The [ADAQ7988](#) SPI-compatible serial interface features the ability to daisy-chain multiple devices on a single, 3-wire bus. This is ideal for isolated applications, as it limits the number of isolator channels required for communication between the device and the digital host.

The [AD8251](#) is an instrumentation amplifier with digitally programmable gains. It features $G\Omega$ input impedance, low output noise, wide bandwidth (10 MHz) and low distortion. These qualities make the [AD8251](#) an excellent candidate for wide bandwidth data acquisition applications. The high input impedance of the [AD8251](#) enable it to interface with a variety of sensors, and provides an impedance translation between the input source and the ADC driver housed within the [ADAQ7988](#). It can be configured for gains of 1, 2, 4, and 8 via its address pins, which are controlled by the digital host via the digital isolator channels of the [ADuM3470](#).

The [ADR4550](#) is a high precision, low power, low noise, 5 V voltage reference featuring $\pm 0.02\%$ maximum initial error, excellent temperature stability, and low output noise. The [ADR4550](#) provides a 5 V reference to the integrated reference buffers of the two [ADAQ7988](#) devices. The reference voltage is also divided by a precision resistor network to provide dc biasing (level shifting) to the ADC drivers of the [ADAQ7988](#) devices.

The [ADuM3470](#) is a quad-channel digital isolator with an integrated PWM controller and transformer driver for an isolated dc-to-dc converter. Based on the Analog Devices *iCoupler*[®] technology, the dc-to-dc converter provides up to 2 W of regulated, isolated power from 3.3 V to 24 V using a 3.3 V or 5.0 V input supply. This eliminates the need for a separate, isolated dc-to-dc converter in 2 W isolated designs. The *iCoupler* chip-scale transformer technology is used to isolate the logic signals, and the integrated transformer driver with isolated secondary side control provides higher efficiency for the isolated dc-to-dc converter. The rated dielectric insulation voltage of the [ADuM3470](#) is 2500 V rms. The result is a small form factor, total isolation solution.

The [ADuM3150](#) is a 6-channel SPI Isolator[™] digital isolator optimized for isolated serial peripheral interfaces (SPIs). Based on the Analog Devices *iCoupler*[®] chip scale transformer technology, the low propagation delay in the CLK, MO/SI, MI/SO, and \overline{SS} SPI bus signals operate with 14 ns propagation delay and 1 ns jitter to optimize timing for SPI. The [ADuM3150](#) also features a delay clock output on the master side of the device. This output can be used with an additional clocked port on the master to support 40 MHz clock performance. The rated dielectric insulation voltage of the [ADuM3150](#) is 3750 V rms.

The power management on the secondary side of the system is handled by the [ADP7118](#) and [ADP7182](#) low dropout (LDO) linear regulators. A cascade of [ADP7118](#) devices are used to regulate the positive rail provided by the [ADuM3470](#) for the positive rails of the system. The [ADP7182](#) devices on board do the same for the negative rails. See the Power Distribution section for more information.

Analog Front End

The analog front end (AFE) of the system consists of input protection diodes, the [AD8251](#) PGIA, the [ADAQ7988](#) μ Module[®] data acquisition system, and precision resistor networks used to configure the ADC driver of the [ADAQ7988](#). The AFEs of both channels are identical in design, but their input ranges can be set independently by the gain settings of their respective [AD8251](#). Figure 2 shows a simplified schematic of the AFE.

integrated reference buffer is negligible. This assumption is suitable because even with the maximum reference buffer offset specified for the [ADAQ7988](#), the output code only deviates by less than one LSB (code value).

System Noise Analysis

One of the key design considerations for data acquisition systems is limiting the effects of system noise. AFE noise limits the system effective resolution (noise free bits) and ac performance metrics, such as signal-to-noise ratio (SNR). This section explains the noise analysis method used for the circuit shown in Figure 1.

The total noise power present in the system can be predicted by taking the root sum square (rss) of the noise power contributed by its individual components, referred to the input of the [ADAQ7988](#) integrated ADC:

$$v_{n,TOTAL} = \sqrt{v_{n,AD8251}^2 + v_{n,ADC\ DRIVER}^2 + v_{n,ADC}^2 + v_{n,R}^2}$$

where:

$v_{n,TOTAL}$ is the total system noise.

$v_{n,R}$ is the noise due to resistors.

$v_{n,AD8251}$ is the noise due to the [AD8251](#).

$v_{n,ADC\ DRIVER}$ is the noise contributed by the [ADAQ7988](#) integrated ADC driver.

$v_{n,ADC}$ is the noise contributed by the [ADAQ7988](#) ADC.

The expected SNR of the system can then be found using

$$SNR_{EXPECTED} = 20 \times \log \left(\frac{V_{REF}/2\sqrt{2}}{v_{n,TOTAL}} \right)$$

The [ADAQ7988](#) houses a low-pass RC filter between its ADC driver and ADC input. The RC filter acts to limit the amount of out-of-band noise arriving at the ADC input, and also helps to attenuate the voltage step associated with the switched capacitor input of the ADC. The bandwidth of this filter was selected to reduce wideband noise from the peripheral components as much as possible while still allowing adequate settling of the ADC input signal between conversions (see the Analog Dialogue article, [Improving Precision Data Acquisition Signal Chain Density Using SiP Technology](#) for more information).

The components in the RC filter are a 20 Ω resistor and a 1.8 nF capacitor, with a resulting bandwidth (BW_{RC}) of 4.42 MHz. The effective noise bandwidth ($ENBW_{RC}$) is calculated by the following equation, and is roughly 2635 $\sqrt{\text{Hz}}$.

$$ENBW_{RC} = \sqrt{\frac{\pi}{2}} \times BW_{RC}$$

The $ENBW_{RC}$ is used to calculate the rms noise contributed by the individual components referred to the input of the ADC.

The noise analysis calculations for each of the major noise contributors in this system can be found in Table 1.

Table 1. AFE Noise Analysis^{1, 2}

Gain ³ (V/V)	AD8251		ADAQ7988			Resistors	System Total	
	$e_{n,AD8251}$ (nV/ $\sqrt{\text{Hz}}$)	$v_{n,AD8251}$ ($\mu\text{V rms}$)	$e_{n,ADC\ DRIVER}$ (nV/ $\sqrt{\text{Hz}}$)	$v_{n,ADC\ DRIVER}$ ($\mu\text{V rms}$)	$v_{n,ADC}$ ($\mu\text{V rms}$)	$v_{n,R}$ ($\mu\text{V rms}$)	$v_{n,TOTAL}$ ($\mu\text{V rms}$)	SNR Expected (dB)
-0.25	40	26.53	5.2	17.13	47.0	13.43	58.19	89.65
-0.5	27	35.82	5.2	17.13	47.0	13.43	62.98	88.96
-1	22	58.37	5.2	17.13	47.0	13.43	78.04	87.10
-2	18	95.52	5.2	17.13	47.0	13.43	108.66	84.23

¹ All rms noise calculations are referred to the input of the [ADAQ7988](#) integrated ADC.

² Calculations using T = 300 K.

³ This gain refers to the full system gain. These correspond to [AD8251](#) gains of 1, 2, 4, and 8.

Noise Contributed by AD8251

The rms noise contributed by the AD8251 is a function of its input-referred voltage noise (e_{AD8251}), its gain setting (G_{AD8251}), the signal gain of the ADAQ7988 ADC driver (set by R_F and R_G in Figure 2), and $ENBW_{RC}$.

$$V_{n,AD8251} = e_{AD8251} \times G_{AD8251} \times (R_F/R_G) \times ENBW_{RC}$$

It is worth noting that e_{AD8251} is provided as the maximum specification and is different for each of its four gain settings. In practice, the noise contributed by the AD8251 is typically less than predicted using the voltage noise numbers from the AD8251 data sheet because the noise specifications of the AD8251 are statistically guardbanded.

Noise Contributed by Passive Components

Figure 3 illustrates the equivalent noise sources for the matched resistor networks used in the circuit shown in Figure 1. R_F and R_G are the resistors used to set the signal gain of the ADC driver, and R_1 and R_2 are the resistors used to set the level shifting voltage (also shown in Figure 2). R_1 and R_2 are represented by a single resistor, with a resistance equal to the R_1 in parallel with R_2 ($R_1 || R_2$). Each of these resistors has their own thermal noise which is included in the full system noise.

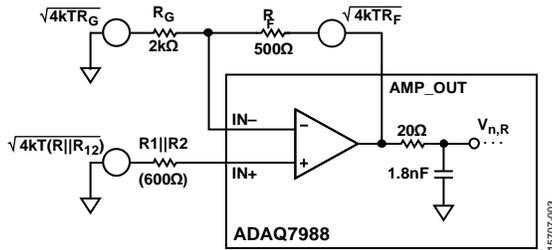


Figure 3. ADAQ7988 ADC Driver and Passive Component Noise Sources

The noise contributed by each of the resistors is subject to different gain factors depending on its place in the circuit.

The noise contributed by R_F is

$$v_{n,R_F} = \sqrt{4k_B T R_F} \times ENBW_{RC}$$

where:

k_B is Boltzmann's constant.

T is the absolute temperature in Kelvin (assumed 300 K).

The noise contributed by R_G is multiplied by the signal gain of the ADC driver, which is set by R_F and R_G :

$$v_{n,R_G} = \sqrt{4k_B T R_G} \times \left(\frac{R_F}{R_G} \right) \times ENBW_{RC}$$

R_1 and R_2 appear to be in parallel from a noise point of view, and therefore their combined thermal noise is equivalent to that of a single resistance with a value of $R_1 || R_2$. Their combined thermal noise is then multiplied by the noise gain of the ADC driver:

$$v_{n,R_{1,2}} = \sqrt{4k_B T (R_1 || R_2)} \times \left(1 + \frac{R_F}{R_G} \right) \times ENBW_{RC}$$

The total noise contributed by the resistors can then be found by taking the root sum square of these individual noise contributions:

$$v_{n,R} = \sqrt{v_{n,R_F}^2 + v_{n,R_G}^2 + v_{n,R_{1,2}}^2}$$

For more information on these calculations, see the MT-049 and MT-050 tutorials.

Noise Contributed by ADAQ7988 Integrated ADC Driver and ADC

The ADC driver of the ADAQ7988 is ideal for driving the integrated SAR ADC. Its low input voltage noise helps minimize system performance degradation.

The noise contributed by the ADC driver ($v_{n,ADC\ DRIVER}$) can be found with the following equation:

$$v_{n,ADC\ DRIVER} = e_{ADC\ DRIVER} \times \left(1 + \frac{R_F}{R_G} \right) \times ENBW_{RC}$$

where $e_{ADC\ DRIVER}$ is the input voltage noise of the ADC driver.

The noise is multiplied by the noise gain of the ADC driver because it is specified as a noise source on its noninverting node. In this case, the current noise of the ADC driver is ignored because it is small relative to the voltage noise.

The rms input voltage noise of a unipolar SAR ADC ($v_{n,ADC}$) can be derived from its specified SNR at the given reference voltage using the following equation:

$$v_{n,ADC} = \frac{V_{REF} / 2}{\sqrt{2}} \times 10^{\frac{-SNR}{20}}$$

where:

V_{REF} is the reference voltage used (5 V for the circuit in Figure 1).

SNR is the SNR specified for that reference voltage in the ADAQ7988 data sheet (91.5 dB).

System Accuracy Analysis

Data acquisition systems are typically designed to achieve high accuracy and precision. The components that make up the system introduce some amount of error and uncertainty, however, which limits the overall accuracy and precision of the system. Two commonly specified system errors are offset and gain error. These errors are affected by temperature drift, as well. They can typically be calibrated out at a specific temperature, but not over the full operating temperature range. The following sections explain how to estimate the maximum expected system inaccuracy at ambient and over temperature for the system shown in Figure 1 using the error specifications of its individual components.

Offset Error Analysis

Offset error is a system inaccuracy that is independent of the input signal. The sources of offset error in this system include the offset of the [AD8251](#) ($V_{OS,AD8251}$), the zero error of the [ADAQ7988](#) ($V_{OS,ADAQ7988}$), the offset caused by the input bias currents of the ADC driver ($V_{OS,IB}$), and the inaccuracy in the generation of the level shifting voltage on the noninverting node of the ADC driver ($V_{OS,LS}$). The maximum expected system offset error (referred to input) can be found by adding these together:

$$V_{OS,SYSTEM} = V_{OS,AD8251} + V_{OS,LS} + V_{OS,ADAQ7988} + V_{OS,IB}$$

Table 2 shows the calculation of the maximum expected referred to input (RTI) system offset error. To convert the offsets of the components to the system offset, they must be multiplied or divided by the relevant gain factors, that is, the noninverting and inverting gains of the ADC driver and the gain settings of the [AD8251](#). The nominal non-inverting and inverting gains of the ADC driver are 1.25 and 0.25, respectively, and these numbers are used to calculate system RTI offset.

The maximum input referred offset of the [AD8251](#) is specified as a function of its gain setting. Table 2 shows the RTI offset error of the [AD8251](#) for all four of its gain settings. See the [AD8251](#) data sheet for more information.

The zero error of the [ADAQ7988](#) specifies the total input referred offset error, and can be treated as an input voltage offset error at the input to its integrated ADC driver. The maximum zero error of the [ADAQ7988](#) is specified as ± 0.5 mV. This error can be converted to system RTI offset error by multiplying it by the ADC driver noninverting gain (1.25) and dividing it by the ADC driver inverting gain (-0.25) and [AD8251](#) gain:

$$V_{OS,ADAQ7988} = \frac{\pm 0.5 \times (1.25)}{(-0.25) \times G_{AD8251}} \text{ (mV)}$$

or

$$V_{OS,ADAQ7988} = \frac{\pm 2.5}{G_{AD8251}} \text{ (mV)}$$

where G_{AD8251} is the gain setting of the [AD8251](#).

The input bias currents of the ADC driver create an offset error when they interact with the matched resistor networks at its inputs. The output referred offset this creates can be found with

$$V_{OS,IB(RTO)} = I_B \times [R_F - (R_1 || R_2)(1.25)]$$

or

$$V_{OS,IB(RTO)} = -0.2 \text{ mV}$$

where I_B is the input bias current specification for the [ADAQ7988](#) integrated ADC driver (800 nA maximum).

In this case, the bias currents were assumed to be equal, because the input offset current of the device is considerably small compared to its input bias current. (See the [MT-038](#) tutorial for more information on input bias current errors.)

To convert the output referred offset caused by the input bias currents ($V_{OS,IB(RTO)}$) to system input referred offset error, it is divided by the inverting gain of the ADC driver and the gain of the [AD8251](#):

$$V_{OS,IB} = \frac{-0.2}{-0.25 \times G_{AD8251}} \text{ (mV)} = \frac{0.8}{G_{AD8251}} \text{ (mV)}$$

This offset error is always positive referred to input; therefore, it is used for calculating the maximum positive offset error, but is ignored for calculating the maximum negative offset error.

Inaccuracies in the generation of the level shift voltage in the ADC driver also introduce offset errors to the system; however, because the level shift voltage is provided by the reference source of the ADC, the system offset is not sensitive to deviations in the reference voltage (see the Analog Front End section), which means that the only error source for the level shift voltage is the tolerance of the resistors in the divider circuit consisting of R_1 and R_2 . The ideal level shift voltage at the noninverting input of the [ADAQ7988](#) integrated ADC driver can be found with the following equation:

$$V_{LS,NOMINAL} = V_{REF} \times \frac{R_2}{R_1 + R_2} = 0.4 \times V_{REF} \text{ (nominal)}$$

The resistor divider is constructed of a matched resistor network and is shown R_1 and R_2 in Figure 2. The network contains four 1 k Ω resistors that are configured to create an attenuation factor of 0.4 ($R_1 = 1.5$ k Ω , $R_2 = 1$ k Ω). The resistors in the network are specified with a relative tolerance of $\pm 0.05\%$, which helps to reduce the deviation from the 0.4 attenuation. The worst-case error of the divider circuit, given the configuration and relative tolerance of the matched resistor network used, is $\pm 0.03\%$. (The resistor networks used for generating the level shift voltage can be found in the [CN-0393](#) schematic, in the [CN-0393 Design Support Package](#).)

The range of the level shift voltage at the noninverting input of the [ADAQ7988](#) integrated ADC driver is, therefore,

$$V_{LS} = 5 \text{ V} \times (0.4 \pm 0.03\%) = 2 \text{ V} \pm 0.6 \text{ mV}$$

Referred to the input of the system, the offset error contributed by the level shift inaccuracy is

$$V_{OS,LS} = \frac{\pm 0.6 \text{ mV} \times 1.25}{-0.25 \times G_{AD8251}} = \frac{\pm 3 \text{ mV}}{G_{AD8251}}$$

The maximum expected input referred offset error for the system in Figure 1 is then the sum of these errors. Table 2 shows the calculations for all four channel gain configurations. Note that these are the maximum expected errors at ambient temperature (25°C).

Table 2. Maximum Expected RTI System Offset Error

Channel Gain	$V_{OS,AD8251}$ (mV)	$V_{OS,LS}$ (mV)	$V_{OS,ADAQ7988}$ (mV)	$V_{OS,IB}$ (mV)	$V_{OS,SYSTEM}$ (mV)	
					Min	Max
-0.25	±0.8	±3	±2.5	+0.8	-6.3	+7.1
-0.5	±0.5	±1.5	±1.25	+0.4	-3.25	+3.65
-1	±0.35	±0.75	±0.625	+0.2	-1.725	+1.925
-2	±0.275	±0.375	±0.3125	+0.1	-0.9715	+1.0715

Offset Error Temperature Drift

System calibration routines can correct for the ambient offset error of the system, but typically not error variations due to temperature drift. Quantifying how the offset changes for temperature variations is useful for evaluating how the system operates over a specified temperature range. Each of the active components in the signal chain have specified temperature drifts for their offsets. The resistor networks also have a relative temperature coefficient specification that guarantees the relative matching of the variation of each resistor over temperature.

The temperature drift of the offset error can be treated as a system specification by combining the temperature drift effects of each of the individual components, assuming there is no temperature variation between the components in the signal chain. Assuming all devices are at equal temperature and that their drifts all trend in the same direction, the maximum expected system offset temperature drift is

$$TCV_{OS,SYSTEM} = TCV_{OS,AD8251} + TCB_{OS,LS} + TCV_{OS,ADAQ7988}$$

where:

$TCV_{OS,AD8251}$ is the input-referred offset drift of the [AD8251](#) over its specified temperature range (in $\mu\text{V}/^\circ\text{C}$).

$TCV_{OS,LS}$ is the temperature drift of the level shift voltage supplied to the [ADAQ7988](#) integrated ADC driver (referred to the input of the [AD8251](#), in $\mu\text{V}/^\circ\text{C}$).

$TCV_{OS,ADAQ7988}$ is the offset drift of the [ADAQ7988](#) (referred to the input of [AD8251](#), in $\mu\text{V}/^\circ\text{C}$).

$TCV_{OS,SYSTEM}$ is the equivalent input-referred offset temperature drift of each channel in the circuit shown in Figure 1.

The [AD8251](#) input referred offset drift ($TCV_{OS,AD8251}$) is given in its data sheet for all four of its gain settings; these values are shown in Table 3.

The [ADAQ7988](#) zero error temperature drift is also provided in its data sheet, with a specified maximum of $1.3 \mu\text{V}/^\circ\text{C}$. This drift can be converted to system RTI temperature drift with the same method used to convert its ambient offset error (see the Offset Error Analysis section):

$$TCV_{OS,ADAQ7988} = \frac{\pm 1.3 \times (1.25)}{(-0.25) \times G_{AD8251}} (\mu\text{V}/^\circ\text{C})$$

or

$$TCV_{OS,ADAQ7988} = \frac{\pm 6.5}{G_{AD8251}} (\mu\text{V}/^\circ\text{C})$$

where G_{AD8251} is the gain setting of the [AD8251](#).

The temperature drift of the level shift voltage is due to the temperature drift of the resistor divider composed of R_1 and R_2 . The offset drift of the reference source is negated by the system because it is shared by the level shift voltage and the [ADAQ7988](#) integrated ADC (see the Analog Front End section). The temperature drift of the level shift voltage is therefore determined by the drift of R_1 and R_2 , and

$$\begin{aligned} V_{LS} \pm TCV_{LS} \\ &= V_{REF} \times \frac{R_2 \pm TCR_2}{(R_1 \pm TCR_1)(R_2 \pm TCR_2)} \\ &= V_{REF} \times (0.4 \pm TCR_{DIV}) \end{aligned}$$

where:

V_{LS} is the nominal level shift voltage (nominally 2 V).

TCV_{LS} is the equivalent temperature drift of the level shift voltage (in $\mu\text{V}/^\circ\text{C}$).

V_{REF} is the reference voltage supplied by the [ADR4550](#) (nominally 5 V).

TCR_1 and TCR_2 are the temperature coefficients of R_1 and R_2 , respectively (in ppm/ $^\circ\text{C}$).

TCR_{DIV} is the equivalent temperature drift of the resistor divider (in ppm/ $^\circ\text{C}$). TCR_{DIV} is the deviation of the divider ratio, which is nominally 0.4 (see the Analog Front End section).

The resistors in the matched resistor network have a specified maximum relative temperature coefficient of resistance (TCR) of ± 15 ppm. To determine the effective temperature drift of the level shift voltage, R_2 is assumed to have no temperature drift, and the components comprising R_1 are assumed to have an absolute TCR of ± 15 ppm ($TCR_1 = 15 \text{ ppm}/^\circ\text{C}$ and $TCR_2 = 0 \text{ ppm}/^\circ\text{C}$). This scenario exhibits the worst-case error of the resistor divider. The maximum expected temperature drift of the resistor divider is, therefore,

$$TCR_{DIV,MAX} = \frac{1 \text{ k}\Omega}{(1.5 \text{ k}\Omega \pm 15 \text{ ppm}/^\circ\text{C}) + 1 \text{ k}\Omega} - 0.4$$

$TCR_{DIV,MAX}$ is equivalent to $\pm 9 \text{ ppm}/^\circ\text{C}$.

The temperature drift of the level shift voltage is, therefore,

$$V_{LS} \pm TCV_{LS} = V_{REF} \times (0.4 \pm 9 \text{ ppm}/^\circ\text{C}) = 2 \text{ V} \pm 9 \text{ ppm}/^\circ\text{C}$$

Because TCV_{LS} is in ppm/ $^\circ\text{C}$, it can be directly applied to the input of the [AD8251](#); $TCV_{OS,LS}$ is $\pm 9 \text{ ppm}/^\circ\text{C}$ at the input of the [AD8251](#), or

$$TCV_{OS,LS} = \frac{\pm 90 \mu\text{V}/^\circ\text{C}}{G_{AD8251}}$$

The maximum expected offset temperature drift for the system shown in Figure 1 is the sum of the temperature drifts for the individual components. Table 3 shows the calculations for all four channel gain configurations.

Table 3. Maximum Expected System Offset Temperature Drift

Channel Gain	TCV _{OS,AD8251} (μV/°C)	TCV _{OS,LS} (μV/°C)	TCV _{OS,ADAQ7988} (μV/°C)	TCV _{OS,SYSTEM} (μV/°C)
-0.25	±6.2	±90	±6.5	±102.7
-0.5	±3.7	±45	±3.25	±51.95
-1	±2.45	±22.5	±1.63	±26.58
-2	±1.83	±11.25	±0.82	±13.9

Gain Error Analysis

Gain error is a system inaccuracy that scales with the input signal. The sources of gain error include the gain errors of the AD8251 and ADAQ7988, the errors in the signal gain of the ADC driver caused by the tolerances of the gain setting resistors, and the error of the reference voltage source (ADR4550). The nominal gain of a channel in the circuit shown in Figure 1 is

$$\begin{aligned}
 G_{SYSTEM,IDEAL} &= G_{AD8251} \times \frac{-R_F}{R_G} \times \frac{2^{16}}{V_{REF}} \text{ (codes/V)} \\
 &= \frac{-3276.8}{G_{AD8251}} \text{ (codes/V)}
 \end{aligned}$$

where:

G_{AD8251} is the gain setting of the AD8251.

V_{REF} is the reference voltage supplied by the ADR4550.

R_F and R_G are the resistors used to set the gain of the ADAQ7988 integrated ADC driver (shown in Figure 2).

The worst-case range of the system can be found by adding the individual component gain errors, as follows:

$$\begin{aligned}
 G_{SYSTEM} &= \left(G_{AD8251} \pm e_{AD8251} \right) \times \left(\frac{-R_F}{R_G} \pm e_G \right) \times \\
 &\quad \left[\frac{2^{16}}{V_{REF} \pm e_{REF}} \times \left(1 \pm e_{ADAQ7988} \right) \right] \text{ (codes/V)}
 \end{aligned}$$

where:

G_{SYSTEM} is the full system gain (the gain of each channel).

e_{AD8251} is the AD8251 gain error (for each of its gain settings).

e_G is the error in the ratio of R_F and R_G .

e_{REF} is the reference voltage error.

$e_{ADAQ7988}$ is the ADAQ7988 gain error.

The maximum expected system gain error (e_{SYSTEM}) is the sum of each of the individual maximum expected gain errors of each of the components in the signal chain:

$$e_{SYSTEM} = e_{AD8251} + e_G + e_{REF} + e_{ADAQ7988}$$

Table 4 shows the calculation of the maximum expected system gain error for each of the four channel gain configurations.

The AD8251 specifies a maximum gain error for each of its four gain configurations. These gain errors are shown in the e_{AD8251} column in Table 4. The ADAQ7988 also specifies a maximum gain error in percent full scale, also shown in Table 4.

The maximum signal gain error of the ADAQ7988 integrated ADC driver can be calculated based on the relative tolerance errors of the gain setting resistors in the matched resistor network (R_F and R_G in Figure 2). Like the networks used in setting the level shifting voltage, this network contains four 1 kΩ resistors. These resistors are configured to create an R_F of 500 Ω and R_G of 2 kΩ, with a resulting nominal gain of -0.25 (see the CN-0393 schematic). The resistors in the network are specified with a relative tolerance of ±0.05%, and the resulting maximum deviation of the signal gain is also roughly ±0.05%.

Though deviations in the reference source do not impact system offset error, it does affect the system gain error. Major errors in the reference source include initial output voltage error (±0.02% or ±1 mV), solder heat shift (±0.02% or ±1 mV), and inaccuracies caused by load regulation limitations (80 ppm/mA). These specifications can be found in the ADR4550 data sheet. In the circuit shown in Figure 1, the ADR4550 is directly connected to the matched resistor networks making the level shift voltage for both channels. Each of these networks acts as a 2.5 kΩ load; therefore, the ADR4550 sources a total of 4 mA, which means its worst-case load regulation error is 320 ppm, or ±1.6 mV. The total maximum error in the reference voltage is the sum of these three errors, which is ±3.6 mV or ±0.072%.

The total maximum expected system gain error for the system in Figure 1 can be found using these individual component errors. Table 4 shows the maximum expected system gain error for all four channel gain configurations. Note that these values are the maximum expected errors at ambient temperature (25°C).

Table 4. Maximum Expected System Gain Error

Channel Gain	e_{AD8251}	e_G	e_{REF}	$e_{ADAQ7988}$	e_{SYSTEM}
-0.25	±0.03%	±0.05%	±0.072%	±0.01%	±0.162%
-0.5	±0.04%	±0.05%	±0.072%	±0.01%	±0.172%
-1	±0.04%	±0.05%	±0.072%	±0.01%	±0.172%
-2	±0.04%	±0.05%	±0.072%	±0.01%	±0.172%

Gain Error Temperature Drift

The system gain error is also subject to variations in temperature. Like with offset error drift, it is important to quantify the gain temperature drift because these variations typically cannot be corrected for with calibration. Each of the active components in the signal chain have specified temperature drifts for their gains. The resistor networks also have a relative temperature coefficient specification that guarantees the relative matching of the variation of each resistor over temperature.

The temperature variation of the system gain is a function of the temperature drift specifications of individual component. Like with the ambient system gain error, the maximum expected

system gain temperature drift is the sum of component gain temperature drifts:

$$TC_{SYSTEM} = TC_{AD8251} + TC_G + TC_{REF} + TC_{ADAQ7988}$$

where:

TC_{SYSTEM} is the maximum expected system gain temperature drift.

TC_{AD8251} is the gain temperature drift specification of the AD8251.

TC_G is the gain temperature drift of the closed-loop gain of the ADAQ7988 integrated ADC driver (a function of the temperature drift of R_F and R_G).

TC_{REF} is the temperature drift specification of the ADR4550.

$TC_{ADAQ7988}$ is the gain error temperature drift specification for the ADAQ7988.

TC_{AD8251} , TC_{REF} , and $TC_{ADAQ7988}$ can be found in the AD8251, ADR4550, and ADAQ7988 data sheets. TC_{AD8251} is 10 ppm/°C (for all AD8251 gain settings), TC_{REF} is 2 ppm/°C, and $TC_{ADAQ7988}$ is 0.4 ppm/°C.

TC_G is dependent upon the relative TCR of the matched resistor network that comprises R_F and R_G . As discussed in the Offset Error Temperature Drift section, these resistors have a relative TCR matching of 15 ppm/°C. Because the ADC driver closed-loop gain is the ratio of R_F to R_G , the temperature drift of the closed-loop gain is equivalent to this relative TCR matching specification; therefore, TC_G is 15 ppm/°C.

TC_{SYSTEM} is then

$$\begin{aligned} TC_{SYSTEM} &= \pm 10 \text{ ppm/}^\circ\text{C} \pm 15 \text{ ppm/}^\circ\text{C} \pm 2 \text{ ppm/}^\circ\text{C} \pm 0.4 \text{ ppm/}^\circ\text{C} \\ &= \pm 27.4 \text{ ppm/}^\circ\text{C} \end{aligned}$$

Digital Interface and Isolation

The system shown in Figure 1 features isolation between the digital host and data acquisition signal chain. The ADuM3470 and ADuM3150 provide digital isolation channels for the AD8251 address signals and the ADAQ7988 SPI signals, respectively.

A key design consideration for digital isolation applications is efficient usage of isolation channels; that is, optimizing the number of isolation channels used to accomplish a design. This is because additional isolation channels may require the addition of new components, which adds to design cost, circuit area, and power consumption. The digital implementation of this system achieves this efficiency by not only optimizing the routing of the ADAQ7988 SPI signals across the isolation barrier, but by including power distribution circuitry in the isolator device controlling the AD8251 address signals.

Figure 4 shows the digital interface connections between the ADAQ7988 devices and the master through the ADuM3150 isolation channels.

The ADuM3150 SPI Isolator™ digital isolator device is optimized for isolated SPI interfaces. It features four high speed isolation channels for slave select, MOSI, MISO, and serial clock signals, which connect to both ADAQ7988 digital input/output pins.

Additionally, the ADuM3150 supports a delay clock (DCLK) output, which significantly relaxes the digital timing constraints on the SPI interface and allows for SPI transfer rates of 40 Mbps without requiring an isolator channel to feed the serial clock back to the master. Figure 4 shows the wiring diagram for the SPI signals plus the DCLK signal.

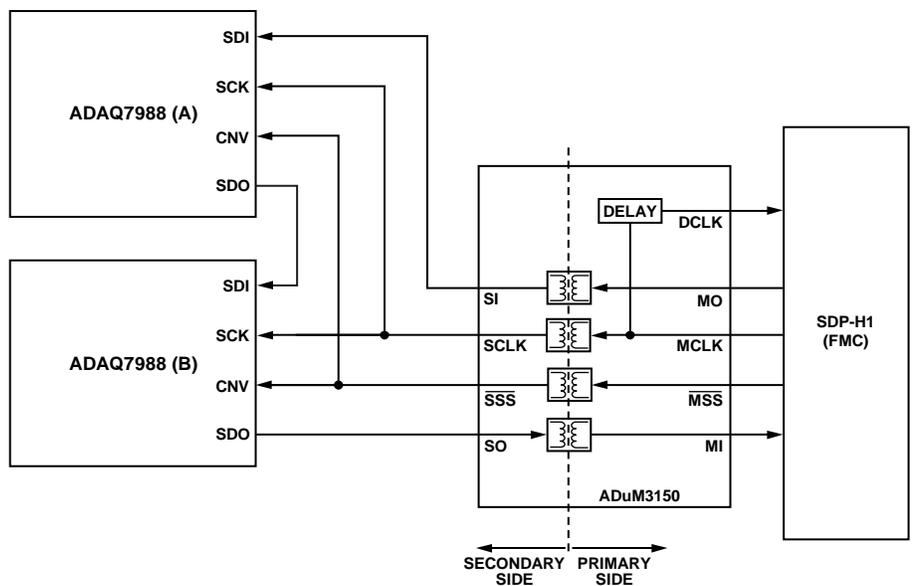


Figure 4. Digital Interface Simplified Schematic

The DCLK signal is a delayed reproduction of the serial clock provided by the master (MCLK). The delay between MCLK and DCLK is trimmed at production test to match the roundtrip propagation delay of the serial clock and MISO channels of the ADuM3150. The DCLK can be used as an independent read clock by the master to clock in the data on the MISO line. This configuration ensures that MISO data are ready when they are clocked in with DCLK. See the [MS-2689 Technical Article, Isolating SPI for High Bandwidth Sensors](#) for more information.

The ADAQ7988 devices in the design are configured in daisy-chain mode. This configuration allows for the 16-bit results of both ADAQ7988 devices to be transmitted along a single MISO (SDO) line, thus requiring only a single isolator channel to transmit the data back to the master. The conversion results from both devices are clocked out by falling edges on their SCK pins, analogous to two serially connected 16-bit shift registers. This arrangement requires the master to output 32 serial clock cycles to read both results.

For information on layout design using the digital isolators, consult the ADuM3470 and ADuM3150 data sheets.

Power Distribution

In addition to providing isolation channels for the AD8251 addresses, the ADuM3470 supplies power from the primary side to the secondary side of the circuit shown in Figure 1. The ADuM3470 features integrated PWM controllers and low impedance transformer drivers (X1 and X2), which drive an external transformer, full-wave Schottky diode rectifier, and low-pass filter. The power circuit provides up to 2 W of regulated, isolated power when supplied from a 5 V or 3.3 V input, thereby eliminating the need for a separate isolated dc-to-dc converter.

The ADuM3470 regulation is from the positive supply. The feedback for regulation is from a divider network chosen such that the feedback voltage is 1.25 V when the output voltage is roughly 16.5 V. The feedback voltage is compared with the ADuM3470 internal feedback set point of 1.25 V. Regulation is achieved by varying the duty cycle of the PWM signal driving the external transformer.

The positive and negative power outputs of the transformer are regulated by several ADP7118 and ADP7182 low dropout (LDO) regulators. Table 5 shows the rails provided on the secondary side.

Table 5. Supply Rails on Secondary Side

Rail Name	Voltage	Function	Device Used
+VS	+15 V	AD8251 positive rail	ADP7118
V+	+7.5 V	ADAQ7988 ADC driver positive rail	ADP7118
VDD	+5 V	ADAQ7988 LDO input supply	ADP7118
-VS	-15 V	AD8251 negative rail	ADP7182
V-	-2.5 V	ADAQ7988 ADC driver negative rail	ADP7182

Performance Measurements

AC Performance Results

Table 6 shows the ac performance for input tones of 1 kHz and 10 kHz measured for one of the channels in the circuit shown in Figure 1. Measured specs include signal-to-noise ratio (SNR), total harmonic distortion (THD), and signal-to-noise-and distortion ratio (SINAD). Figure 5, Figure 6, and Figure 7 show SNR, THD, and SINAD vs. frequency for each of the four channel gain settings. THD includes up to the fifth harmonic.

The input signals were supplied by an Audio Precision SYS-2700 series signal generator, which provided differential, full-scale signals at 1 kHz, 10 kHz, 20 kHz, and 50 kHz. Full-scale input signals for gains of -0.25, -0.5, -1, and -2 were ±10 V, ±5 V, ±2.5 V, and ±1.25 V, respectively.

Table 6. CN-0393 AC Performance Results

Gain (V/V)	f _{IN} = 1 kHz			f _{IN} = 10 kHz		
	SNR	THD	SINAD	SNR	THD	SINAD
-0.25	90.4	-104.5	90.3	90.4	-95.5	89.3
-0.5	89.2	-103.4	89.1	89.1	-95.2	88.2
-1	89.1	-105.9	89.1	88.9	-94.7	88.0
-2	87.2	-102.8	87.2	87.0	-94.6	86.4

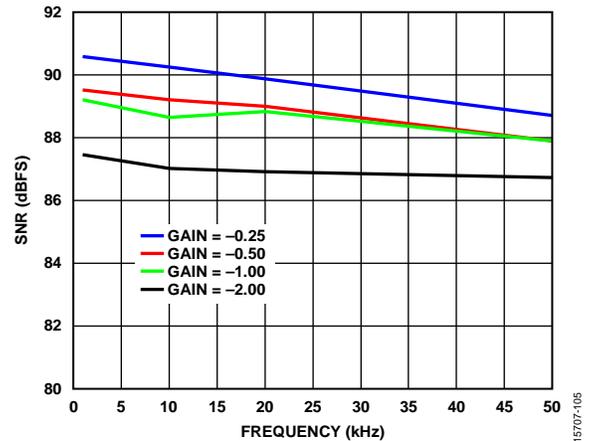


Figure 5. SNR vs. Input Frequency

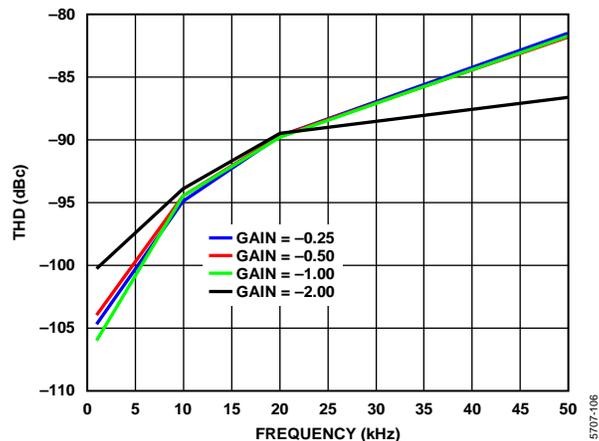


Figure 6. THD vs. Input Frequency

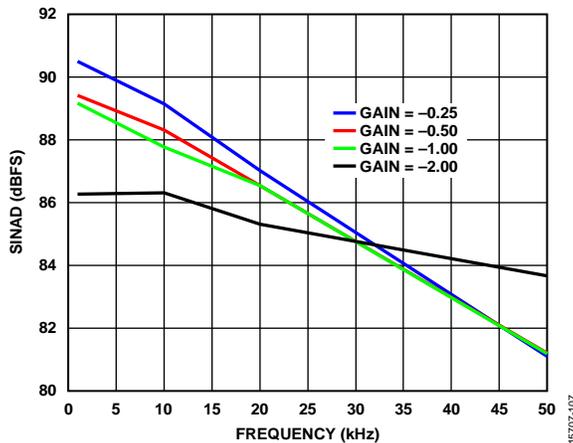


Figure 7. SINAD vs. Input Frequency

DC Performance Results

The offset error and gain error for each of the channels were measured for each of the four gain settings. Table 7 shows the measured offset and gain errors for both channels on the same board, for all four gain settings.

The offset errors reported in Table 7 are in millivolts referred to the system inputs. First, the inputs to the [AD8251](#) were grounded for both channels, and 131,072 output codes were captured averaged to yield the average code offset of the system (N_{OS}). The referred to input offset is converted to volts using the following equation:

$$V_{OS}(RTI) = N_{OS} \times \left(\frac{V_{REF}}{2^N \times G} \right)$$

where:

V_{REF} is the reference voltage (5 V for this system),.

N is the resolution of the integrated SAR ADC of the [ADAQ7988](#) (16 bits).

G is the gain of the system and is equal to the gain of the [AD8251](#) multiplied by the gain of the ADC driver.

The offset error was measured for both channels on a single board in all of the gain settings.

The gain error was determined by applying two known voltage inputs, recording their resulting output codes (also averages of 131,072 results), and comparing the slope of the line between these resulting codes to the ideal slope. The ideal slope (m_{IDEAL}) is a function of the reference voltage (V_{REF}), and the resolution of the SAR ADC (N):

$$m_{IDEAL} = \frac{2^N}{V_{REF}}$$

The measured slope is

$$m_{REAL} = \frac{N_2 - N_1}{V_2 - V_1}$$

where:

N_1 and N_2 are the average output codes measured for two inputs, V_1 and V_2 .

V_1 and V_2 are voltages close to positive and negative full-scale of the system.

The gain errors are reported as percent full scale (%FS) errors in Table 7. They are calculated with the following equation:

$$\%FS = \frac{m_{REAL} - m_{IDEAL}}{m_{IDEAL}} \times 100\%$$

Table 7. Offset and Gain Error vs. Gain and Channel

Gain (V/V)	Channel A		Channel B	
	Offset Error (mV)	Gain Error (%FS)	Offset Error (mV)	Gain Error (%FS)
-0.25	-2.9	-0.01	-4.9	0.11
-0.5	-1.4	-0.01	-2.5	0.12
-1	-0.7	-0.01	-1.3	0.12
-2	-0.4	-0.01	-0.8	0.12

COMMON VARIATIONS

More Precise Resistor Networks

In the System Accuracy Analysis section, the full system offset and gain errors and drifts were quantified based on the performance of the individual components. The tolerance and temperature coefficient matching of the resistor networks setting the [ADAQ7988](#) ADC driver gain and level shift voltage contributed the most to each of these errors (especially for offset temperature drift). To mitigate errors contributed by these passive components, the system can utilize matched resistor networks with tighter tolerance and TCR matching specifications. These matched resistor networks improve the full system accuracy, but add to the system cost. The end requirements of the application must be considered when selecting these components.

ADAQ7988 Single-Supply Configuration

The [ADAQ7988](#) can operate in a single-supply configuration. In designs that aim to reduce power consumption and component count, it may be suitable to run the device with a single positive supply rail while grounding the negative supply rail. This configuration can be done with minimal impact on the device operating specifications, provided that the headroom requirements of the integrated ADC driver and reference buffer are not violated. See the [ADAQ7988](#) data sheet for these specifications.

The reference voltage must be set to not violate the headroom specifications of the [ADAQ7988](#) reference buffer. For example, when using a 5 V supply on V_+ , the reference voltage cannot exceed 3.3 V.

Additional Circuit Protection

The circuit shown in Figure 1 has several means of overvoltage protection. TVS protection diodes are included at both inputs of both channels to protect them from large transient voltage spikes. The **ADAQ7988** design is also robust enough to handle an overvoltage event where the output of the **AD8251** overranges; the ESD diodes of the ADC, the integrated $20\ \Omega$ resistor, and the short-circuit current limitations of the integrated reference buffer and ADC driver prevent damage to the device (see the **ADAQ7988** data sheet for more information). Figure 8 shows the connections of the internal ESD diodes of the ADC.

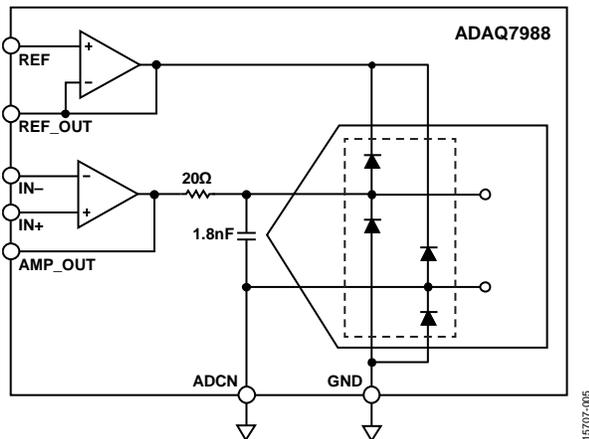


Figure 8. ADC Input ESD Diodes

If the **ADAQ7988** integrated ADC driver exceeds the reference voltage, the ESD diode connecting the ADC input to REF_OUT turns on. The current going through the diode depends on the voltage at AMP_OUT and REF_OUT, as well as the $20\ \Omega$ series resistor. In typical SAR ADC designs, care must be taken to make sure that the current going through the ESD diode does not cause the reference source to deviate, especially if the source is shared between multiple devices; however, the short-circuit current limitations for the two amplifiers ensures that the reference buffer is able to sink the current from the ADC driver without deviating.

If more protection is desired, however, Schottky diodes can be used to clamp the voltage at the input of the ADC to REF_OUT. The Schottky diodes provide alternative paths for the output current of the ADC driver in the case of an overvoltage event, preventing it from going through the ADC ESD diodes and disturbing the reference. Figure 9 shows the implementation of Schottky diodes in a SAR ADC signal chain.

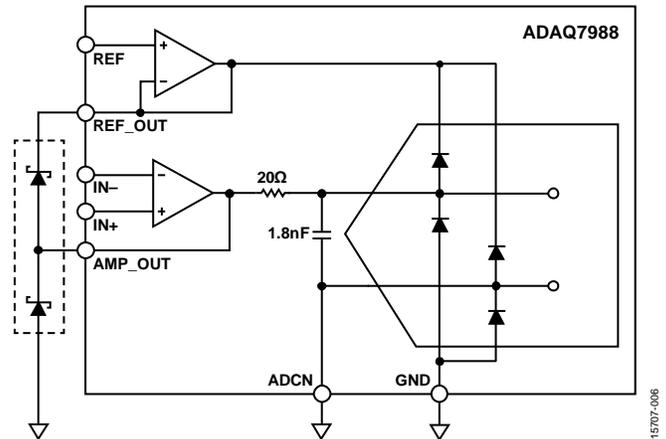


Figure 9. Using Schottky Diodes for Additional Overvoltage Protection

The circuit in Figure 1 provides footprints for the installation of Schottky diodes on the output of the **ADAQ7988** integrated ADC driver, identical to the connection diagram in Figure 9. A complete set of documentation for the **EVAL-CN0393-FMCZ** board including schematics, board layout, and bill of materials can be found in the **CN-0393 Design Support Package** at www.analog.com/CN0393-DesignSupport.

Additional Channels

The circuit in Figure 1 uses an isolation channel for each of the four address signals running to the two **AD8251** devices. Although this is adequate for a two-channel design, a different approach must be taken when utilizing more channels.

Depending on channel count, the design can either include more digital isolator devices to account for additional signals, or incorporate a controller on the secondary side to create these signals from instructions sent from the master device. The latter option can be achieved with a single SPI interface, and therefore does not require the addition of more isolator devices.

Single Supply Across Isolation Barrier

The power supply scheme used in the circuit in Figure 1 was designed to reduce component count and board area. It accomplishes this by using the **ADuM3470** supplying positive and negative rails that are large enough for the **AD8251** devices. The **ADuM3470** can also provide a single regulated supply for applications that do not require two. The **ADP5070** dc-to-dc switching regulator can be used to generate larger, bipolar supplies using a single dc input. The combination of the **ADuM3470** with the **ADP5070** to generate bipolar rails for a data acquisition signal chain is used in the **CN-0385**.

CIRCUIT EVALUATION AND TEST

This circuit uses the [EVAL-CN0393-FMCZ](#) circuit board and the [SDP-H1](#) system demonstration platform controller board ([EVAL-SDP-CH1Z](#)). The two boards connect via a 160-pin FMC connector, allowing quick setup and evaluation of the performance of the circuit. The [EVAL-CN0393-FMCZ](#) board contains the circuit shown in Figure 1, and the [SDP-H1](#) board interfaces with the [CN-0393 Evaluation Software](#) to operate this circuit.

Equipment Needed

The following equipment is needed:

- PC with a USB port and Windows® XP, Windows Vista®, or Windows 7®
- [EVAL-CN0393-FMCZ](#) circuit evaluation board
- [SDP-H1](#) controller board ([EVAL-SDP-CH1Z](#))
- [CN-0393 Evaluation Software](#) (download from <ftp://ftp.analog.com/pub/cftl/CN0393/>)
- 12 V dc switched mode power supply
- USB to micro-USB cable
- Low distortion, low noise signal generator to provide ± 10 V input signals
- Low noise, high precision dc supply to provide ± 10 V input

Software Installation

Load the evaluation software by first downloading it from <ftp://ftp.analog.com/pub/cftl/CN0393/>, and then installing it on the PC. The [CN-0393 User Guide](#) has instructions for installing and running this software.

Setup and Test

Do not connect power to the hardware until both the [EVAL-CN0393-FMCZ](#) and [SDP-H1](#) boards are connected via the 160-pin FMC connector. To set up the [EVAL-CN0393-FMCZ](#) and [SDP-H1](#) hardware, take the following steps:

1. Connect the [EVAL-CN0393-FMCZ](#) and the [SDP-H1](#) via the 160-pin FMC connector.
2. Connect the 12 V dc switched-mode power supply to the +12V_VIN jack on the [SDP-H1](#) board. Note that power is not provided to the [EVAL-CN0393-FMCZ](#) board until the [CN-0393 Evaluation Software](#) has initialized.
3. Connect the [SDP-H1](#) board to the PC via the USB cable.
4. Run the [CN-0393 Evaluation Software](#) (see the [CN-0393 User Guide](#) for instructions).

Figure 10 shows the functional block diagram of the test setup. The signal source can be connected to either channel via the SMA connectors or test points. See the [CN-0393 Design Support Package](#) for the complete [EVAL-CN0393-FMCZ](#) schematic.

Figure 11 shows a photograph of the [EVAL-CN0393-FMCZ](#) board.

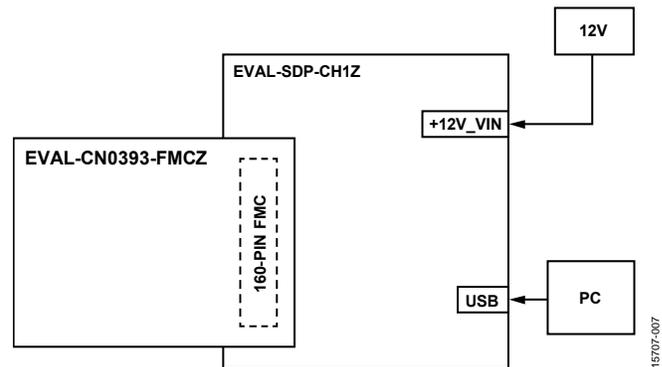


Figure 10. [CN-0393 Evaluation Hardware Connections](#)



Figure 11. Photograph of [EVAL-CN0393-FMCZ](#) Board