ANALOG DEVICES

Circuit Note

CN-0584

Circuits from the Lab®
Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0584.

Devices Connected/Referenced	
ADAQ23876	16-Bit, 15 MSPS, µModule Data Acquisition Solution
AD3552R	Dual Channel, 16-Bit, 33 MUPS, Multispan, Multi-IO SPI DAC
ADG5421F	±60 V Fault Protection and Detection,11 Ω R_{ON}, Dual SPST Switch
ADA4898-1	High Voltage, Low Noise, Low Distortion, Unity-Gain Stable, High Speed Op Amp

Precision Low Latency Development Kit

EVALUATION AND DESIGN SUPPORT

- Circuit Evaluation Boards
  - CN0584 Circuit Evaluation Board (EVAL-CN0584-EBZ)
  - CN0585 Circuit Evaluation Board (EVAL-CN0585-FMCZ)
- Design and Integration Files
  - Schematics, Layout Files, Bill of Materials, Software

CIRCUIT FUNCTIONS AND BENEFITS

As modern electronic, electromechanical, and electro-optical systems continue to shrink in size, require faster response times, and have more stringent accuracy requirements, performance of the data acquisition and hardware-in-the-loop (HIL) systems required to simulate, develop, and test these systems must keep pace. This is particularly true for applications requiring high power elements, such as the testing of motor controllers, linear actuators, generator controllers, electric vehicle chargers, or power grid elements for the automotive and energy industries. The increasing complexity of these modeled components leads to increased computation times, demanding faster solutions for signal acquisition and generation.

The circuit shown in Figure 1 is a complete precision low latency development kit, with 200 ns latency, and high-accuracy input bandwidth. This solution enables real-time HIL simulations and development of complex systems, significantly easing the design and testing of digital or mixed signal control loops. It is consists of four 16-bit analog-to-digital converter (ADC) channels and four 16-bit digital-to-analog converter (DAC) channels that allow synchronous acquisition of analog inputs and generation of output waveforms at 15 MSPS.

The development kit provides up to 5 MHz analog input bandwidth with extended analog and digital connectivity to simplify analog front end (AFE) design. Both the analog input range and output are hardware-selectable with five bipolar input ranges from ±1.5 V to ±10 V, and five output ranges from 5 V unipolar to ±10 V bipolar.

The software interface is available through the Linux industrial input/output (IIO) framework, providing a host of debug and development utilities and cross platform application support through Python, MATLAB®, C, C#, and other languages. The project integrates with Simulink®, where real-time models can be generated and loaded into the field programmable gate array (FPGA) board for testing with external hardware.

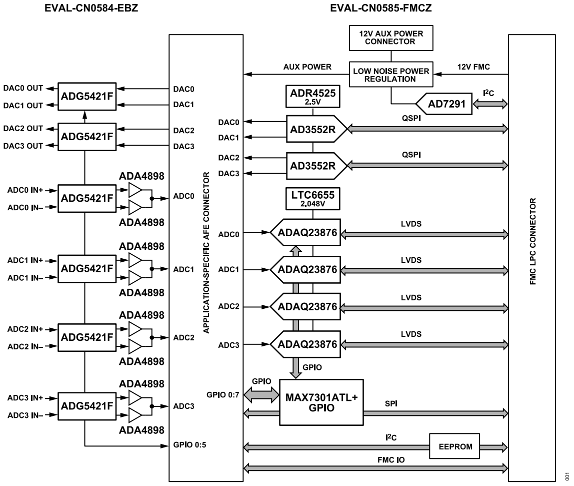

Figure 1. Simplified Block Diagram

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CIRCUIT DESCRIPTION

HARDWARE-IN-THE-LOOP

The CN0584 simplifies and accelerates the development and test process for control systems using HIL emulation of expensive, complex, or not-yet-developed hardware. Figure 2 shows a high-level block diagram of a typical HIL setup using the CN0584 kit.

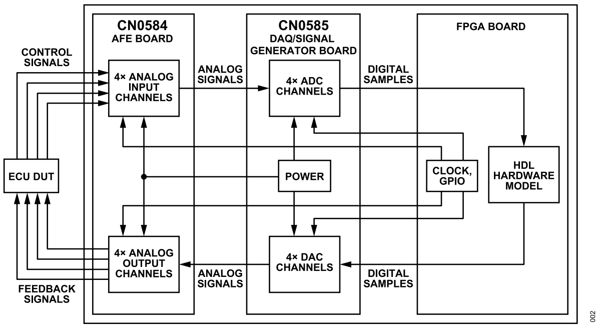


Figure 2. Hardware-in-the-Loop Simulation Setup

The electronic control unit (ECU) device under test (DUT) represents a controller, which produces digital output signals based on analog feedback inputs from the device it is controlling. The CN0584 emulates a device with custom hardware description language (HDL) loaded into an FPGA board, providing a real-time simulation of realistic performance.

One example of an HIL simulation that can be performed using the CN0584 is emulating the load for a 3-phase motor controller. The motor's behavior is first described in Simulink®, which is used to generate an HDL module that can be integrated into the CN0584 HDL template.

Applying this example to Figure 2, the ECU produces pulse width modulation (PWM) control signals, which are conditioned by three channels on the analog front end board and digitized by the ADCs on the data acquisition and signal generation board. Based on these inputs, the HDL hardware model simulates parameters such as the current draw, speed, inertia, and position of a modeled motor. These parameters are converted to analog signals and routed back to the ECU, which then closes the loop, adjusting its output PWM signals based on this feedback.

The ECU can be quickly evaluated for nominal operating conditions, corner cases (for example, maximum and minimum motor load), and various failure modes, each of which can be quickly implemented in simulation with no additional associated costs or damage to physical hardware.

ANALOG MEASUREMENT AND SIGNAL GENERATION

Input Voltage Range

The CN0584 supports an analog input voltage range of ±10 V by default. Additional input ranges of ±5 V, ±4.096 V, ±2.5 V, and ±1.5 V are hardware-selectable.

Analog Input Protection

The CN0584 provides analog input protection on all four ADC and DAC channels using the ADG5421F high voltage dual single-pole, single-throw (SPST) switch, offering overvoltage protection up to ±60 V. This protection is particularly important for HIL applications where high power signals may be present, and it also enables users to quickly adapt or modify their setups without worrying about miswiring or improper connections.

The ADG5421F is supplied by the +15 V and -15 V power rails, and if either the S1 or S2 pin exceeds one of those voltage levels by V_T (0.7 V), the switch automatically turns off. For the ADCs, these pins connect to the differential input ports; and for the DACs, they connect to the two DAC channel output ports.

The ADG5421F also provides a fault flag (FF), which is routed to the CN0585 and read by a MAX7301 serial peripheral interface (SPI), 28-port I/O expander. The expander's SPI port is routed to the FMC connector, and read by the FPGA board. In normal operation, the FF pin is pulled high. However, if an overvoltage condition is detected, the FF pin is pulled low to indicate a fault has occurred.

Output Voltage Range

The CN0584 supports an analog output voltage range of ±10 V by default. Additional output ranges of ±5 V, 0 V to +2.5 V, 0 V to +5 V, and 0 V to +10 V are hardware-selectable. Note that the register settings, which are controlled using the provided software interfaces, must also be updated for these output range modifications to take effect.

SYSTEM PERFORMANCE

Latency

Figure 3 shows the test setup used to measure the latency of the CN0584. A 1 MHz pulsed sine wave was generated from memory using the FPGA and passed through to one DAC output channel. This DAC output was monitored using an external scope and fed back via subminiature version-A (SMA) cable as an input to one of the ADC channels, where it was used as the input signal to the corresponding DAC channel. The output from this DAC channel was measured using the same oscilloscope, enabling the measurement of signal latency through the ADC input path, FPGA board, and DAC output path.

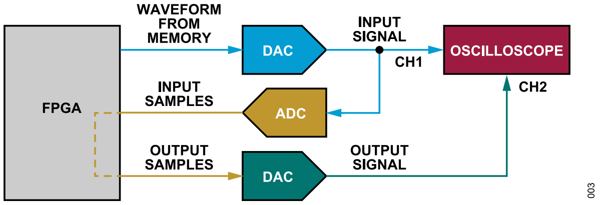


Figure 3. Latency Test Setup

Figure 4 shows the latency and settling time of the CN0584 output as captured by an oscilloscope. With the CN0584 DAC output set to ADC input mode, a pulse was applied to one of the ADC channel inputs, and the corresponding DAC channel output was monitored. The latency from the measured input signal to the DAC output signal beginning to rise was approximately 250 ns; 50 ns of this delay is attributed to the internal FPGA data processing, while the remaining 200 ns of the delay is attributed to ADC data capture and DAC update.

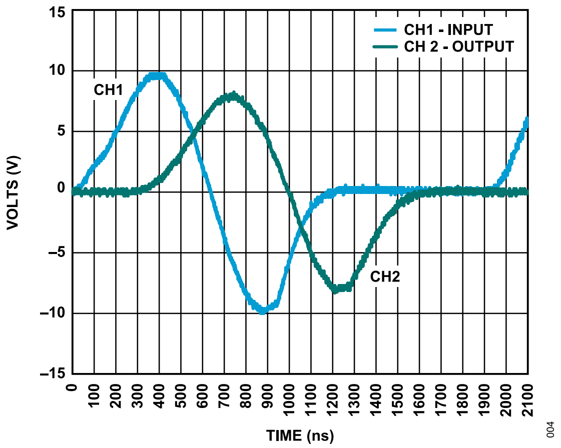


Figure 4. DAC Output Latency

Analog Input Performance

The analog signal acquisition path of the CN0584 exhibits very high spurious-free dynamic range (SFDR). Figure 5 shows a 16K point FFT of the ADC's data at a sample rate of 15 MSPS, with a 1 kHz, ±10 V sinusoidal input signal. The CN0584 achieves 105 dB of SFDR, dominated by the 3rd harmonic. All other spurs are lower than 120 dBc across the full 7.5 MHz input frequency range.

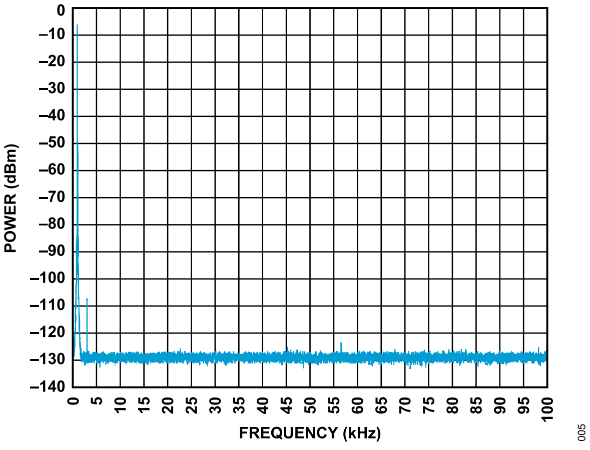


Figure 5. CN0584 Analog Input Acquisition Spectrum

Figure 6 shows the same spectrum plot over a frequency range extending to 1 MHz, showing that no other harmonics or spurs over -120 dBm are present.

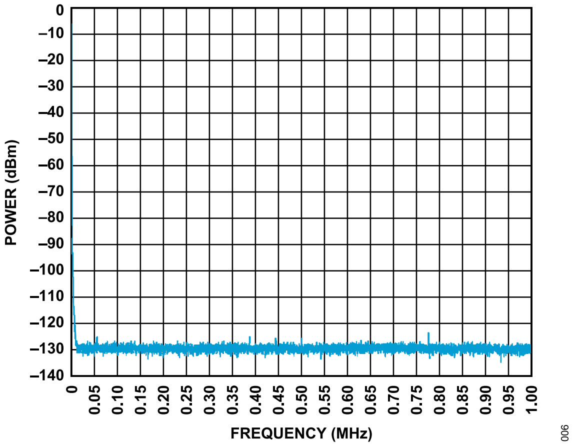


Figure 6. Analog Input Acquisition Spectrum to 1 MHz

Figure 7 shows the input frequency response of the ADC.

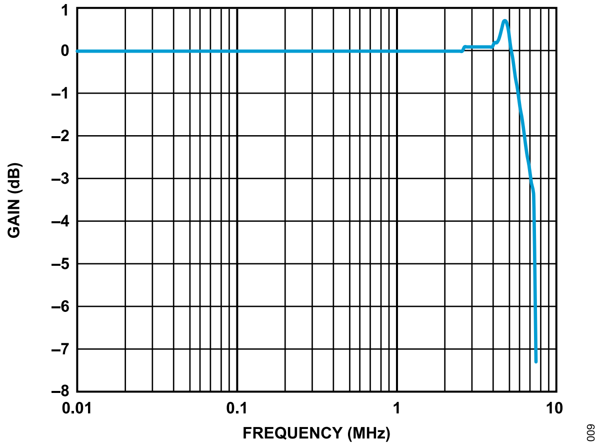


Figure 7. ADC Input Frequency Response

Output Filtering

A low pass filter is present at the output of each DAC. Figure 8 shows the frequency response of the filter as measured to 7.5 MHz, with the ADC output used as the DAC input.

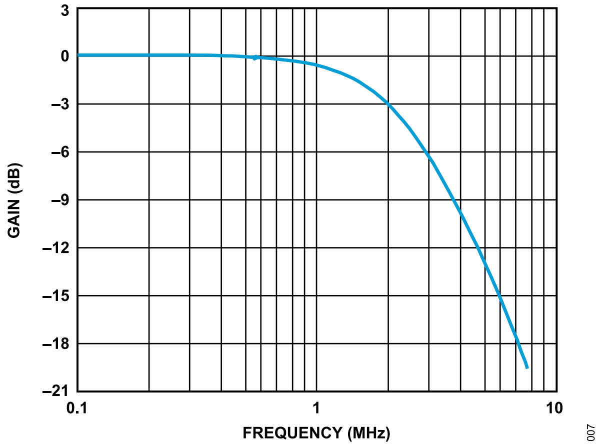


Figure 8. ADC and DAC Filter Composite Response

Figure 9 shows the frequency response of the output path, with ideal waveforms generated in software, loaded into a cyclic buffer, and written to the DAC. Slightly less attenuation is seen in this plot due to the lower latency when compared to the full loopback measurement, which must pass samples to the FPGA and back.

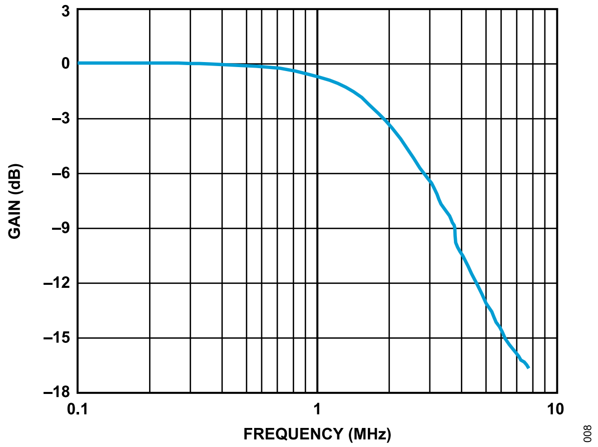


Figure 9. DAC Output Frequency Response

POWER ARCHITECTURE

All power for the CN0584 is provided by the CN0585 through the AFE connector.

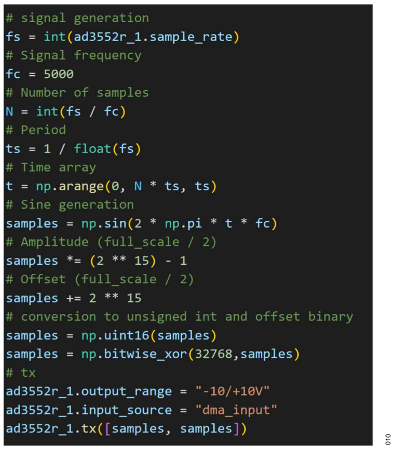
The CN0584 uses the +15 V and -15 V rails to provide the positive and negative supply voltages for the ADG5421F input protection switches. The +12 V and -12 V rails provide the positive and negative supply voltages for the ADA4898-1 ADC buffer amplifiers. The +3.3 V rail powers the EEPROM circuit.

SOFTWARE OVERVIEW

Python

The CN0584 can be interfaced to Python using the pyADI-IIO library, which enables device configuration, capture of incoming samples from the ADCs, and generation of waveforms to be transmitted by the DACs. The output waveforms can then be pre- or post-processed based on ADC data, allowing a user to quickly and easily implement control loops or simulations of other hardware.

Figure 10 shows an arbitrary waveform generated using Python and written to the DAC output. This example shows the generation of a ±10 V peak-to-peak 5 kHz sine wave, but any waveform can be implemented. For example, for an HIL setup one can generate a damped sine wave, chirp, noise, or distorted waveform to simulate defective hardware.



```
# signal generation
fs = int(ad3552r_1.sample_rate)
# Signal frequency
fc = 5000
# Number of samples
N = int(fs / fc)
# Period
ts = 1 / float(fs)
# Time array
t = np.arange(0, N * ts, ts)
# Sine generation
samples = np.sin(2 * np.pi * t * fc)
# Amplitude (full_scale / 2)
samples *= (2 ** 15) - 1
# Offset (full_scale / 2)
samples += 2 ** 15
# conversion to unsigned int and offset binary
samples = np.uint16(samples)
samples = np.bitwise_xor(32768,samples)
# tx
ad3552r_1.output_range = "-10/+10V"
ad3552r_1.input_source = "dma_input"
ad3552r_1.tx([samples, samples])
```

Figure 10. Example DAC Output Generation with Python

Figure 11 shows the measured input waveform for analysis, plotting the sine wave generated in Figure 10. The samples read from the ADCs can be processed and used as inputs to user-implemented Python algorithms implementing control loops, hardware emulations, or any other desired feedback systems.

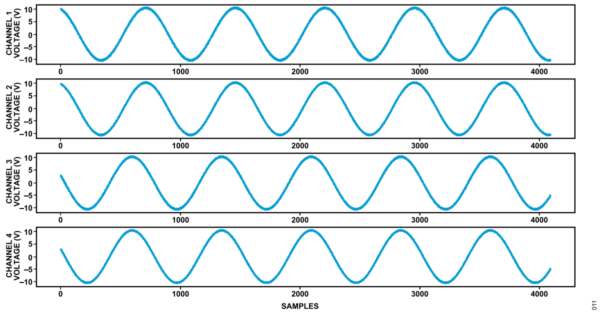


Figure 11. ADC Samples Read and Plotted Using Python

MATLAB and Simulink

MATLAB® can also be used to interface with the CN0584 using the High Speed Converter Toolbox, which enables largely the same set of features as described for Python above. In addition to this, Simulink® can be used to create custom HDL models which can be loaded into the FPGA and run in real time using the CN0584. Existing Simulink models or custom algorithms can be used to implement control systems, perform digital signal processing (DSP) operations on measured signals, or emulate hardware functions.

Figure 12 shows the placement of a Simulink model inserted in both receive and transmit mode within the CN0584 block diagram. This means that ADC samples are passed through the HDL model and stored into memory and that DAC samples are passed through the HDL model and output on the CN0584. HDL models could also be inserted in receive-only or transmit-only modes, which gives access exclusively to ADC inputs or DAC outputs, respectively.

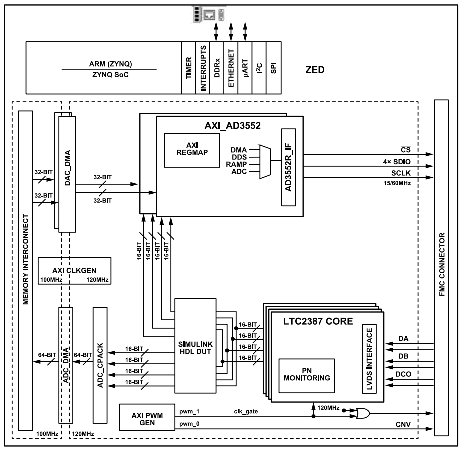


Figure 12. CN0584 Block Diagram with Simulink Block

For any receive signal path models inserted, the modified samples can be accessed using Python or MATLAB®, or viewed using the IIO Oscilloscope software.

COMMON VARIATIONS

Variations are possible on both the data acquisition and signal generation board and AFE board. For variations on the signal acquisition and generation paths, refer to the CN0585 circuit note.

The CN0584 allows a wide array of variations to tailor functionality to a specific application. A non-exhaustive set of examples is provided, but many additional possibilities exist and can be implemented to create any desired setup for HIL testing or other applications.

Bypassing the ADA4898 input buffer amplifier is possible for applications not requiring high input impedance. For higher speed applications where amplifier bandwidth is critical and slightly higher noise can be tolerated, the ADA4895 can be used in its place. For applications where high bandwidth is not as essential but a wider input voltage range is desired, the LTC6373 can be used. Alternatively, the ADA4255, which includes overvoltage protection, can be used for similar applications to replace both the ADA4895 and ADG5421F.

Application-specific variations are possible on the DAC output path as well. For example, for high voltage operations, the ADHV4702 which can drive outputs up to ±110 V, can be added to the output signal path.

CIRCUIT EVALUATION AND TEST

This section covers the setup and procedure for evaluating the EVAL-CN0584-EBZ. For complete details and other important information, refer to the CN0584 User Guide.

EQUIPMENT NEEDED

Required Hardware

- EVAL-CN0584-EBZ
- EVAL-CN0585-FMCZ
- Zedboard Xilinx Zinq development board
- 16 GB SD card
- Micro-USB cable
- USB-C wall adapter
- Ethernet cable
- 4x SMA cables
- 4x SMA 50 Ω terminations
- Host PC (Windows/Linux)

Required Software

- UART terminal capable of 115200 baud rate (recommended PuTTY)
- IIO Oscilloscope
- Analog Devices, Inc. Kuiper Linux image

GETTING STARTED

1. Flash an SD card with the Analog Devices Linux Kuiper image.
2. Configure the SD card with the appropriate boot files.
3. Attach the EVAL-CN0584-EBZ to the EVAL-CN0585-FMCZ through the AFE connector.
4. Connect the Zedboard to the EVAL-CN0585-FMCZ using the FMC connector.
5. Connect the power supply to the EVAL-CN0585-FMCZ.
6. Connect the Ethernet cable and the UART micro-USB cable to Zedboard, and the other ends to the host PC.
7. Connect the EVAL-CN0584-EBZ analog I/O ports as shown in Figure 14 using the SMA cables and terminations.

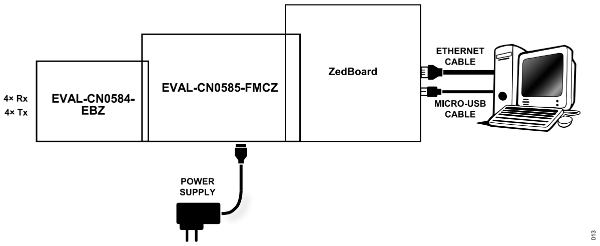


Figure 13. CN0584 Functional Test Block Diagram

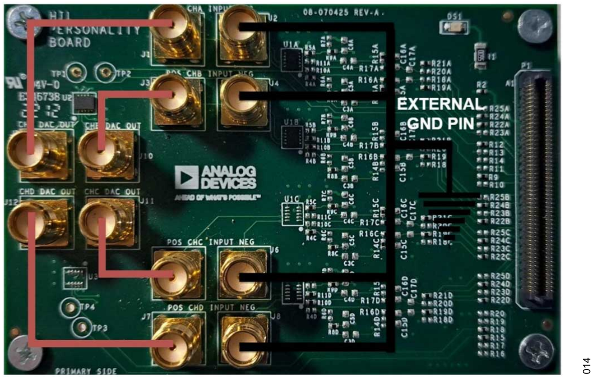
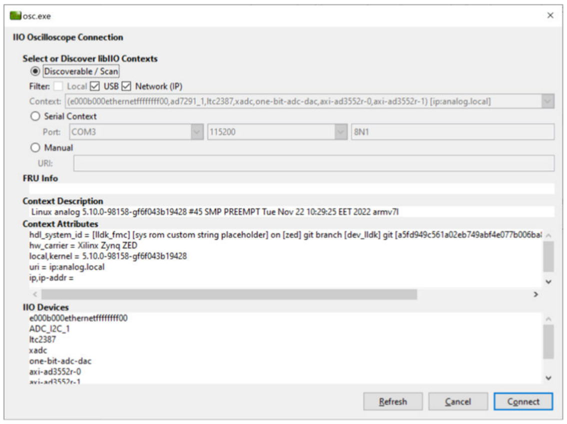


Figure 14. AFE Board I/O Setup

FUNCTIONAL TEST SETUP

1. Open a PuTTY session to the Zedboard's COM port.
2. In the PuTTY terminal, navigate to the /boot folder and run the **setup_adc.sh** script.
3. Launch IIO Oscilloscope and connect to the Zedboard, as shown in Figure 15.



osc.exe

IIO Oscilloscope Connection

Select or Discover libIIO Contexts

● Discoverable / Scan

Filter: □ Local ☑ USB ☑ Network (IP)

Context: (e000b000ethernetffffffff00,ad7291_1,ltc2387,xadc,one-bit-adc-dac,axi-ad3552r-0,axi-ad3552r-1) [ip:analog.local]

○ Serial Context

Port: COM3 115200 8N1

○ Manual

URI:

FRU Info

Context Description

Linux analog 5.10.0-98158-gf6f043b19428 #45 SMP PREEMPT Tue Nov 22 10:29:25 EET 2022 armv7l

Context Attributes

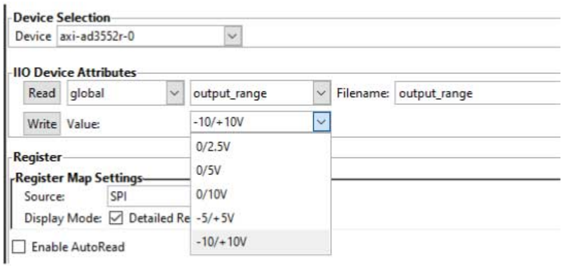
```
hdl_system_id = [lldk_fmc] [sys rom custom string placeholder] on [zed] git branch [dev_lldk] git [a5fd949c561a02eb749abf4e077b006ba
hw_carrier = Xilinx Zynq ZED
local,kernel = 5.10.0-98158-gf6f043b19428
uri = ip:analog.local
ip,ip-addr =
```

IIO Devices

```
e000b000ethernetffffffff00
ADC_I2C_1
ltc2387
xadc
one-bit-adc-dac
axi-ad3552r-0
axi-ad3552r-1
```

Figure 15. IIO Oscilloscope Connection Panel

4. In IIO Oscilloscope, set the AD3552R DAC output ranges to ±10 V and the input source to **dma_input**, as shown in Figure 16.



Device Selection

Device: axi-ad3552r-0

IIO Device Attributes

Read: global, output_range, Filename: output_range

Write: Value: -10/+10V

Register

Register Map Settings

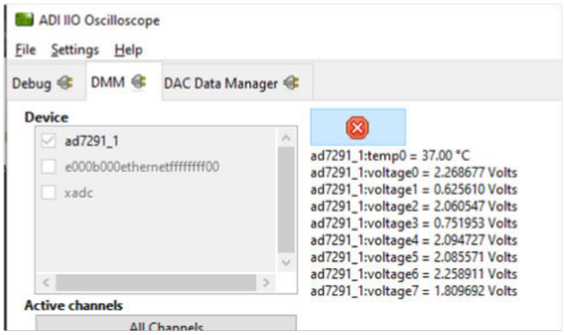
Source: SPI

Display Mode: ☑ Detailed Re

□ Enable AutoRead

Figure 16. IIO Oscilloscope Configuration Panel

5. Navigate to the DMM tab of IIO Oscilloscope and confirm that the voltage monitor values align with those shown in Figure 17.



ADI IIO Oscilloscope

Device

☑ ad7291_1

□ e000b000ethernetffffffff00

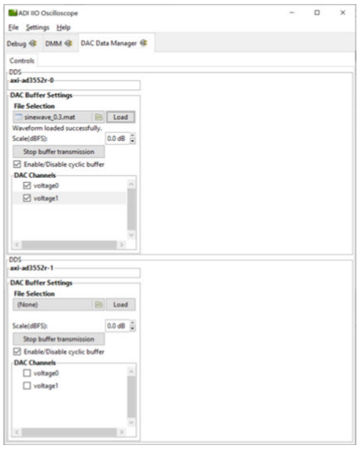
□ xadc

```
ad7291_1:temp0 = 37.00 °C
ad7291_1:voltage0 = 2.268677 Volts
ad7291_1:voltage1 = 0.625610 Volts
ad7291_1:voltage2 = 2.060547 Volts
ad7291_1:voltage3 = 0.751953 Volts
ad7291_1:voltage4 = 2.094727 Volts
ad7291_1:voltage5 = 2.085571 Volts
ad7291_1:voltage6 = 2.258911 Volts
ad7291_1:voltage7 = 1.809692 Volts
```

Active channels

Figure 17. IIO Oscilloscope Voltage Monitor Panel

6. Navigate to the DAC Data Manager and load provided sample waveforms to desired DAC output channels, as shown in Figure 18.



ADI IIO Oscilloscope

DDS

axi-ad3552r-0

DAC Buffer Settings

File Selection: sinewave_0.3.mat Load

Waveform loaded successfully.

Scale(dBFS): 0.0 dB

Stop buffer transmission

☑ Enable/Disable cyclic buffer

DAC Channels

☑ voltage0

☑ voltage1

DDS

axi-ad3552r-1

DAC Buffer Settings

File Selection: (None) Load

Scale(dBFS): 0.0 dB

Stop buffer transmission

☑ Enable/Disable cyclic buffer

DAC Channels

□ voltage0

□ voltage1

Figure 18. IIO Oscilloscope DAC Output Panel

TEST RESULTS

After following the circuit evaluation procedure, the waveforms loaded from the DAC Data Manager tab must appear in the IIO Oscilloscope waveform window, which displays the signals captured at each ADC channel input. Figure 19 shows an example display using the sample waveforms selected, as shown in Figure 18.

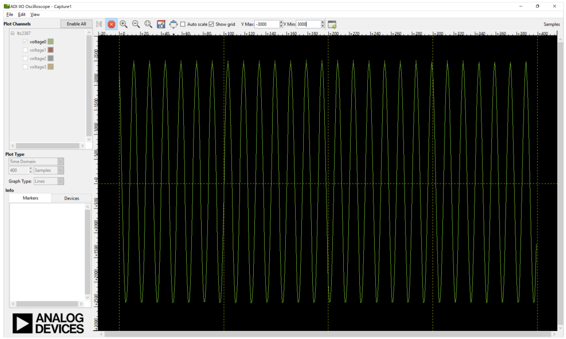


Figure 19. IIO Oscilloscope Waveform Capture