Dual 500mA, Positive/Negative, Ultra-Low Noise, Ultra-High PSRR Low Dropout Linear Regulator

FEATURES

- Ultra-low output RMS noise: 0.8 µV rms (10 Hz to 100 kHz)
- Ultra-low output noise spectral density: 2 nV/√Hz (Positive) and 2.2 nV/√Hz (Negative) at 10 kHz
- Ultra-low 1/f noise: 10 µV p-p (Positive) and 3.2 µV p-p (Negative) (0.1 Hz to 10 Hz)
- Ultra-high PSRR: 76 dB (Positive) and 74 dB (Negative) at 1 MHz
- Output current: 500 mA
- Wide input voltage range: ±1.8 V to ±20 V
- Single capacitor per channel improves noise and PSRR
- SET pin current: 100 µA, ±1% initial accuracy
- Single resistor per channel programs output voltage
- Programmable current limit
- Low-dropout voltage: 260 mV (Positive) and 235 mV (Negative)
- Output voltage range: 0 V to 15 V (Positive) and 0 V to –19.5 V (Negative)
- Programmable power good
- Fast start-up capability
- Precision enable/undervoltage lockout (UVLO)
- Internal current limit with foldback
- Minimum output capacitor: 10 µF ceramic
- Compact, low-profile, 22-lead, 6 mm × 3 mm, Plastic DFN package

APPLICATIONS

- Bipolar very low-noise power supplies
- RF power supplies: phase-locked loops, voltage-controlled oscillators, mixers, low-noise amplifiers, and power amplifiers
- Low-noise instrumentation
- High-speed and high-precision data converters
- Medical applications: imaging and diagnostics
- Precision power supplies
- Postregulator for switching supplies

TYPICAL APPLICATION

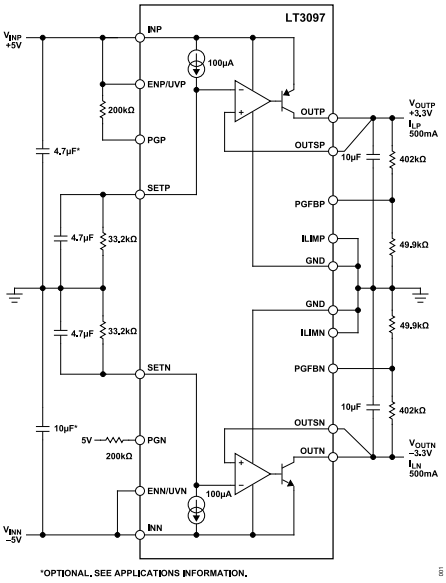

Figure 1. Typical Application

GENERAL DESCRIPTION

The LT3097 is a dual, positive and negative, high-performance, low-dropout linear regulator featuring Analog Devices, Inc., ultra-low noise and ultra-high power supply rejection ratio (PSRR) architecture for powering noise-sensitive applications. Each regulator delivers up to 500 mA with a typical 260 mV/235 mV (positive/negative) dropout voltage.

Operating quiescent current is nominally 2.2 mA/2.35 mA (positive/negative) and drops to 0.3 µA/3 µA (positive/negative) in shutdown. The LT3097 has a wide output voltage range (0 V to 15 V, positive and 0 V to -19.5 V, negative) error amplifier that operates in unity-gain and provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage.

LT3097 is stable with a minimum 10 µF ceramic output capacitor for each channel. Built-in protection includes internal current limit with foldback and thermal limit with hysteresis. The positive regulator also includes reverse-battery protection and reverse-current protection. The LT3097 is available in a thermally enhanced, 22-lead 6 mm × 3 mm, Plastic dual-flat no-leads (DFN) package.

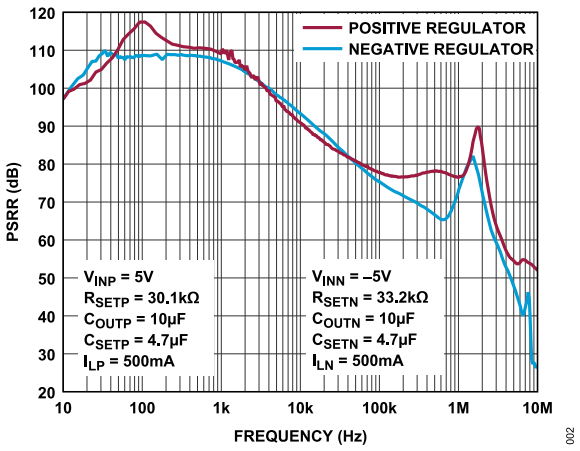

Figure 2. PSRR vs. Frequency

Rev. 0

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REVISION HISTORY

3/2023—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Junction temperature (T_J) = −40°C to +125°C for the minimum and maximum values, ambient temperature (T_A) = 25°C for the typical values, output capacitance (C_{OUT}) = 10 µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7 µF, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POSITIVE INPUT VOLTAGE (V_{INP}) RANGE		2		20	V
NEGATIVE INPUT VOLTAGE (V_{INN}) RANGE		–20		–2.3	V
MINIMUM INP PIN VOLTAGE[1]	Positive Load Current (I_{LP}) = 500 mA, V_{INP} UVLO rising		1.78	2	V
	V_{INP} UVLO hysteresis		75		mV
MINIMUM INN PIN VOLTAGE[2]	Negative Load Current (I_{LN}) = 500 mA, (V_{INN}) UVLO rising	–2.3	–1.8		V
	V_{INN} UVLO hysteresis		130		mV
POSITIVE OUTPUT VOLTAGE (V_{OUTP}) RANGE	$V_{INP} > V_{OUTP}$	0		15	V
NEGATIVE OUTPUT VOLTAGE (V_{OUTN}) RANGE	$V_{INN} < V_{OUTN}$	–19.5		0	V
SETP PIN CURRENT (I_{SETP})	V_{INP} = 2 V, I_{LP} = 1 mA, V_{OUTP} = 1.3 V, T_A = 25°C	99	100	101	µA
	2 V < V_{INP} < 20 V, 0 V < V_{OUTP} < 15 V, 1 mA < I_{LP} < 500 mA[3]	98	100	102	µA
SETN PIN CURRENT (I_{SETN})	V_{INN} = –2.3 V, I_{LN} = 1 mA, V_{OUTN} = –1.5 V, T_A = 25°C	99	100	101	µA
	–20 V < V_{INN} < –2.3 V, –19.5 V < V_{OUTN} < 0 V, 1 mA < I_{LN} < 500 mA[4]	98	100	102	µA
POSITIVE FAST STARTUP I_{SETP}	PGFBP voltage (V_{PGFBP}) = 289 mV, V_{INP} = 2.8 V, SETP voltage (V_{SETP}) = 1.3 V		2		mA
NEGATIVE FAST STARTUP I_{SETN}	PGFBN voltage (V_{PGFBN}) = –286 mV, V_{INN} = –2.3 V, SETN voltage (V_{SETN}) = –1.5 V		1.8		mA
POSITIVE OUTPUT OFFSET VOLTAGE, V_{OSP} (V_{OUTP} – V_{SETP})[5]	V_{INP} = 2 V, I_{LP} = 1 mA, V_{OUTP} = 1.3 V, T_A = 25°C	–1		+1	mV
	2 V < V_{INP} < 20 V, 0 V < V_{OUTP} < 15 V, 1 mA < I_{LP} < 500 mA[3]	–2		+2	mV
NEGATIVE OUTPUT OFFSET VOLTAGE, V_{OSN} (V_{OUTN} – V_{SETN})[6]	V_{INN} = –2.3 V, I_{LN} = 1 mA, V_{OUTN} = –1.5 V, T_A = 25°C	–1		+1	mV
	–20 V < V_{INN} < –2.3 V, –19.5 V < V_{OUTN} < 0 V, 1 mA < I_{LN} < 500 mA[4]	–2		+2	mV
POSITIVE LINE REGULATION					
ΔI_{SETP}	V_{INP} = 2 V to 20 V, I_{LP} = 1 mA, V_{OUTP} = 1.3 V		0.5	±2	nA/V
ΔV_{OSP}	V_{INP} = 2 V to 20 V, I_{LP} = 1 mA, V_{OUTP} = 1.3 V[5]		0.5	±3	µV/V
NEGATIVE LINE REGULATION					
ΔI_{SETN}	V_{INN} = –2.3 V to –20 V, I_{LN} = 1 mA, V_{OUTN} = –1.5 V		0.5	±5	nA/V
ΔV_{OSN}	V_{INN} = –2.3 V to –20 V, I_{LN} = 1 mA, V_{OUTN} = –1.5 V[6]		0.5	±6	µV/V
POSITIVE LOAD REGULATION					
ΔI_{SETP}	I_{LP} = 1 mA to 500 mA, V_{INP} = 2 V, V_{OUTP} = 1.3 V		3		nA
ΔV_{OSP}	I_{LP} = 1 mA to 500 mA, V_{INP} = 2 V, V_{OUTP} = 1.3 V[5]		0.1	0.5	mV
NEGATIVE LOAD REGULATION					
ΔI_{SETN}	I_{LN} = 1 mA to 500 mA, V_{INN} = –2.3 V, V_{OUTN} = –1.5 V		0.1		nA
ΔV_{OSN}	I_{LN} = 1 mA to 500 mA, V_{INN} = –2.3 V, V_{OUTN} = –1.5 V[6]		0.03	0.5	mV
CHANGE IN I_{SETP} WITH V_{SETP}	V_{SETP} = 1.3 V to 15 V, V_{INP} = 20 V, I_{LP} = 1 mA		30	400	nA
	V_{SETP} = 0 V to 1.3 V, V_{INP} = 20 V, I_{LP} = 1 mA		150	600	nA
CHANGE IN I_{SETN} WITH V_{SETN}	V_{SETN} = –1.5 V to –19.5 V, V_{INN} = –20 V, I_{LN} = 1 mA		100	850	nA
	V_{SETN} = 0 V to –1.5 V, V_{INN} = –20 V, I_{LN} = 1 mA		150	500	nA
CHANGE IN V_{OSP} WITH V_{SETP}	V_{SETP} = 1.3 V to 15 V, V_{INP} = 20 V, I_{LP} = 1 mA[5]		0.03	0.6	mV

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{SETP} = 0 V to 1.3 V, V_{INP} = 20 V, I_{LP} = 1 mA[5]		0.3	2	mV
CHANGE IN V_{OSN} WITH V_{SETN}	V_{SETN} = –1.5 V to –19.5 V, V_{INN} = –20 V, I_{LN} = 1 mA[6]		0.02	0.5	mV
	V_{SETN} = 0 V to –1.5 V, V_{INN} = –20 V, I_{LN} = 1 mA[6]		0.15	2	mV
POSITIVE DROPOUT VOLTAGE[7]	I_{LP} = 1 mA and 50 mA, T_A = 25°C		220	275	mV
	I_{LP} = 1 mA and 50 mA			330	mV
	I_{LP} = 300 mA, T_A = 25°C		220	280	mV
	I_{LP} = 300 mA			350	mV
	I_{LP} = 500 mA, T_A = 25°C		260	350	mV
	I_{LP} = 500 mA			450	mV
NEGATIVE DROPOUT VOLTAGE[8]	I_{LN} = 1 mA and 50 mA, T_A = 25°C		185	225	mV
	I_{LN} = 1 mA and 50 mA			275	mV
	I_{LN} = 100 mA, T_A = 25°C		185	230	mV
	I_{LN} = 100 mA			280	mV
	I_{LN} = 500 mA, T_A = 25°C		225	310	mV
	I_{LN} = 500 mA			410	mV
POSITIVE GND PIN CURRENT, V_{INP} = $V_{OUTP\ (NOMINAL)}$[9]	I_{LP} = 10 µA		2.2		mA
	I_{LP} = 1 mA		2.4	4	mA
	I_{LP} = 50 mA		3.5	5.5	mA
	I_{LP} = 100 mA		4.3	7	mA
	I_{LP} = 500 mA		15	25	mA
NEGATIVE GND PIN CURRENT, V_{INN} = $V_{OUTN\ (NOMINAL)}$[10]	I_{LN} = 10 µA		2.35		mA
	I_{LN} = 1 mA		2.4	4	mA
	I_{LN} = 50 mA		3.1	5.5	mA
	I_{LN} = 100 mA		3.8	6.5	mA
	I_{LN} = 500 mA		12	23	mA
POSITIVE OUTPUT NOISE[5, 11]	I_{LP} = 500 mA, frequency = 10 Hz, C_{SETP} = 0.47 µF, V_{OUTP} = 3.3 V		500		nV/√Hz
	I_{LP} = 500 mA, frequency = 10 Hz, C_{SETP} = 4.7 µF, 1.3 V ≤ V_{OUTP} ≤ 15 V		70		nV/√Hz
	I_{LP} = 500 mA, frequency = 10 kHz, C_{SETP} = 0.47 µF, 1.3 V ≤ V_{OUTP} ≤ 15 V		2		nV/√Hz
	I_{LP} = 500 mA, frequency = 10 kHz, C_{SETP} = 0.47 µF, 0 V ≤ V_{OUTP} < 1.3 V		5		nV/√Hz
NEGATIVE OUTPUT NOISE[6, 12]	I_{LN} = 500 mA, frequency = 10 Hz, C_{SETN} = 0.47 µF, V_{OUTN} = –3.3 V		700		nV/√Hz
	I_{LN} = 500 mA, frequency = 10 Hz, C_{SETN} = 4.7 µF, –19.5 V ≤ V_{OUTN} ≤ –1.5 V		70		nV/√Hz
	I_{LN} = 500 mA, frequency = 10 kHz, C_{SETN} = 0.47 µF, –19.5 V ≤ V_{OUTN} ≤ –1.5 V		2.2		nV/√Hz
	I_{LN} = 500 mA, frequency = 10 kHz, C_{SETN} = 0.47 µF, –1.5 V < V_{OUTN} ≤ 0 V		6		nV/√Hz
POSITIVE OUTPUT RMS NOISE[5, 11]	I_{LP} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETP} = 0.47 µF, V_{OUTP} = 3.3 V		2.5		µV rms
	I_{LP} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETP} = 4.7 µF, 1.3 V ≤ V_{OUTP} ≤ 15 V		0.8		µV rms
	I_{LP} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETP} = 4.7 µF, 0 V ≤ V_{OUTP} < 1.3 V		1.8		µV rms
NEGATIVE OUTPUT RMS NOISE[6, 12]	I_{LN} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETN} = 0.47 µF, V_{OUTN} = –3.3 V		3		µV rms

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	I_{LN} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETN} = 4.7 µF, –19.5 V ≤ V_{OUTN} ≤ –1.5 V		0.8		µV rms
	I_{LN} = 500 mA, bandwidth = 10 Hz to 100 kHz, C_{SETN} = 4.7 µF, –1.5 V < V_{OUTN} ≤ 0 V		1.8		µV rms
POSITIVE OUTPUT PEAK-TO-PEAK 1/F NOISE[5, 11]	I_{LP} = 500 mA, bandwidth = 0.1 Hz to 10 Hz, C_{SETP} = 4.7 µF, V_{OUTP} = 3.3 V		27		µV p-p
	I_{LP} = 500 mA, bandwidth = 0.1 Hz to 10 Hz, C_{SETP} = 22 µF, V_{OUTP} = 3.3 V		10		µV p-p
NEGATIVE OUTPUT PEAK-TO-PEAK 1/F NOISE[6, 12]	I_{LN} = 500 mA, bandwidth = 0.1 Hz to 10 Hz, C_{SETN} = 4.7 µF, V_{OUTN} = –3.3 V		6		µV p-p
	I_{LN} = 500 mA, bandwidth = 0.1 Hz to 10 Hz, C_{SETN} = 22 µF, V_{OUTN} = –3.3 V		3.2		µV p-p
POSITIVE REFERENCE CURRENT RMS OUTPUT NOISE[5, 11]	Bandwidth = 10 Hz to 100 kHz		6		nA rms
NEGATIVE REFERENCE CURRENT RMS OUTPUT NOISE[6, 12]	Bandwidth = 10 Hz to 100 kHz		8		nA rms
POSITIVE POWER-SUPPLY REJECTION RATIO (PSRR)					
1.3 V ≤ V_{OUTP} ≤ 15 V (V_{INP} – V_{OUTP} = 2 V (Avg)[5, 11])	Ripple voltage (V_{RIPPLE}) = 500 mV p-p, ripple frequency (f_{RIPPLE}) = 120 Hz, I_{LP} = 500 mA, C_{SETP} = 4.7 µF		117		dB
	V_{RIPPLE} = 150 mV p-p, f_{RIPPLE} = 10 kHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		90		dB
	V_{RIPPLE} = 150 mV p-p, f_{RIPPLE} = 100 kHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		77		dB
	V_{RIPPLE} = 150 mV p-p, f_{RIPPLE} = 1 MHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		76		dB
	V_{RIPPLE} = 80 mV p-p, f_{RIPPLE} = 10 MHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		53		dB
0 V ≤ V_{OUTP} < 1.3 V (V_{INP} – V_{OUTP} = 2 V (Avg)[5, 11])	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 120 Hz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		104		dB
	V_{RIPPLE} = 50 mV p-p, f_{RIPPLE} = 10 kHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		85		dB
	V_{RIPPLE} = 50 mV p-p, f_{RIPPLE} = 100 kHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		72		dB
	V_{RIPPLE} = 50 mV p-p, f_{RIPPLE} = 1 MHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		64		dB
	V_{RIPPLE} = 50 mV p-p, f_{RIPPLE} = 10 MHz, I_{LP} = 500 mA, C_{SETP} = 0.47 µF		54		dB
NEGATIVE POWER-SUPPLY REJECTION RATIO (PSRR)					
–18 V ≤ V_{OUTN} ≤ –1.5 V (V_{INN} – V_{OUTN} = 2 V (Avg)[6, 12])	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 120 Hz, I_{LN} = 500 mA, C_{SETN} = 4.7 µF		108		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 10 kHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		94		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 100 kHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		75		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 1 MHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		74		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 10 MHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		28		dB
–1.5 V < V_{OUTN} ≤ 0 V (V_{INN} – V_{OUTN} = 2 V (Avg)[6, 12])	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 120 Hz, I_{LN} = 500 mA, C_{SETN} = 4.7 µF		108		dB

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 10 kHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		90		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 100 kHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		72		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 1 MHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		78		dB
	V_{RIPPLE} = 500 mV p-p, f_{RIPPLE} = 10 MHz, I_{LN} = 500 mA, C_{SETN} = 0.47 µF		30		dB
ENP/UVP PIN					
Threshold	ENP/UVP trip-point rising (turn-on), V_{INP} = 2 V	1.18	1.24	1.32	V
Hysteresis	ENP/UVP trip-point hysteresis, V_{INP} = 2 V		130		mV
Current ($I_{ENP/UVP}$)	ENP/UVP voltage ($V_{ENP/UVP}$) = 0 V, V_{INP} = 20 V			±1	µA
	$V_{ENP/UVP}$ = 1.24 V, V_{INP} = 20 V		0.03		µA
	$V_{ENP/UVP}$ = 20 V, V_{INP} = 0 V		8	15	µA
ENN/UVN PIN					
Threshold	Positive ENN/UVN trip-point rising (turn-on), V_{INN} = –2.3 V	1.20	1.26	1.35	V
	Negative ENN/UVN trip-point rising (turn-on), V_{INN} = –2.3 V	–1.35	–1.26	–1.20	V
Hysteresis	Positive ENN/UVN trip-point hysteresis, V_{INN} = –2.3 V		200		mV
	Negative ENN/UVN trip-point hysteresis, V_{INN} = –2.3 V		215		mV
Current ($I_{ENN/UVN}$)	ENN/UVN voltage ($V_{ENN/UVN}$) = 0 V, V_{INN} = –20 V			±1	µA
	$V_{ENN/UVN}$ = –1.5 V, V_{INN} = –20 V		–0.5		µA
	$V_{ENN/UVN}$ = –20 V, V_{INN} = –20 V	–35	–18.5		µA
	$V_{ENN/UVN}$ = 1.5 V, V_{INN} = –20 V		8		µA
	$V_{ENN/UVN}$ = 20 V, V_{INN} = 0 V		25	45	µA
POSITIVE QUIESCENT CURRENT IN SHUTDOWN ($V_{ENP/UVP}$ = 0 V)	V_{INP} = 6 V, T_A = 25°C		0.3	1.5	µA
	V_{INP} = 6 V			10	µA
NEGATIVE QUIESCENT CURRENT IN SHUTDOWN ($V_{ENN/UVN}$ = 0 V)	V_{INN} = –6 V, V_{PGN} = Open, T_A = 25°C		3	8	µA
	V_{INN} = –6 V, V_{PGN} = Open			10	µA
POSITIVE CURRENT LIMIT					
Internal[13]	V_{INP} = 2 V, V_{OUTP} = 0 V	570	710	850	mA
	V_{INP} = 12 V, V_{OUTP} = 0 V		700		mA
	V_{INP} = 20 V, V_{OUTP} = 0 V	230	330	430	mA
Programmable	Programming scale factor: 2 V < V_{INP} < 20 V[14]		150		mA × kΩ
	V_{INP} = 2 V, V_{OUTP} = 0 V, R_{ILIMP} = 301 Ω	450	500	550	mA
	V_{INP} = 2V, V_{OUTP} = 0 V, R_{ILIMP} = 1.5 kΩ	90	100	110	mA
NEGATIVE CURRENT LIMIT					
Internal[15]	V_{INN} = –2.3 V, V_{OUTN} = 0 V	550	750		mA
	V_{INN} = –12 V, V_{OUTN} = 0 V		425		mA
	V_{INN} = –20 V, V_{OUTN} = 0 V	40	85	160	mA
Programmable	Programming scale factor: –20 V < V_{INN} < –2.3 V[16]		3.75		A × kΩ
	V_{INN} = –2.3 V, V_{OUTN} = 0 V, R_{ILIMN} = 7.5 kΩ	450	500	560	mA
	V_{INN} = –2.3 V, V_{OUTN} = 0 V, R_{ILIMN} = 37.5 kΩ	90	105	120	mA
PGFBP PIN					
Trip Point	PGFBP trip-point rising	291	300	309	mV
Hysteresis	PGFBP trip-point hysteresis		7		mV
Current (I_{PGFBP})	V_{INP} = 2V, V_{PGFBP} = 300 mV		25		nA

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PGFBN PIN					
Trip Point	PGFBN trip-point rising	288	300	312	mV
Hysteresis	PGFBN trip-point hysteresis		7		mV
Current (I_{PGFBN})	V_{INN} = –2.3 V, V_{PGFBN} = –300 mV		30	100	nA
PGP PIN					
Output Low Voltage	PGP current (I_{PGP}) = 100 µA		30	100	mV
Leakage Current	PGP voltage (V_{PGP}) = 20 V			1	µA
PGN PIN					
Output Low Voltage	PGN current (I_{PGN}) = 100 µA		17	50	mV
Leakage Current	PGN voltage (V_{PGN}) = 20 V			1	µA
POSITIVE MINIMUM LOAD REQUIRED[17]	V_{OUTP} < 1 V	10			µA
NEGATIVE MINIMUM LOAD REQUIRED[18]	V_{OUTN} > –1.5 V			10	µA
POSITIVE THERMAL SHUTDOWN	T_J rising		165		°C
	Hysteresis		8		°C
NEGATIVE THERMAL SHUTDOWN	T_J rising		167		°C
	Hysteresis		8		°C
POSITIVE START-UP TIME	$V_{OUTP(NOM)}$ = 5 V, I_{LP} = 500 mA, C_{SETP} = 0.47 µF, V_{INP} = 6 V, V_{PGFBP} = 6 V		55		ms
	$V_{OUTP(NOM)}$ = 5 V, I_{LP} = 500 mA, C_{SETP} = 4.7 µF, V_{INP} = 6 V, V_{PGFBP} = 6 V		550		ms
	$V_{OUTP(NOM)}$ = 5 V, I_{LP} = 500 mA, C_{SETP} = 4.7 µF, V_{INP} = 6 V, Positive Power-Good 1 resistance (R_{PGP1}) = 50 kΩ, Positive Power-Good 2 resistance (R_{PGP2}) = 700 kΩ (with positive fast start-up to 90% of V_{OUTP})		10		ms
NEGATIVE START-UP TIME	R_{SETN} = 49.9 kΩ, $V_{OUTN(NOM)}$ = –5 V, I_{LN} = 500 mA, C_{SETN} = 0.47 µF, V_{INN} = –6 V, V_{PGFBN} = –6 V		55		ms
	R_{SETN} = 49.9 kΩ, $V_{OUTN(NOM)}$ = –5 V, I_{LN} = 500 mA, C_{SETN} = 4.7 µF, V_{INN} = –6 V, V_{PGFBN} = –6 V		550		ms
	R_{SETN} = 49.9 kΩ, $V_{OUTN(NOM)}$ = –5 V, I_{LN} = 500 mA, C_{SETN} = 4.7 µF, V_{INN} = –6 V, Negative Power-Good 1 resistance (R_{PGN1}) = 50 kΩ, Negative Power-Good 2 resistance (R_{PGN2}) = 700 kΩ (with negative fast start-up to 90% of V_{OUTN})		10		ms
POSITIVE THERMAL REGULATION	10 ms pulse		–0.01		%/W
NEGATIVE THERMAL REGULATION	10 ms pulse		–0.01		%/W
POSITIVE REVERSE CURRENT					
Input	V_{INP} = –20 V, $V_{ENP/UVP}$ = 0 V, V_{OUTP} = 0 V, V_{SETP} = 0 V			150	µA
Output	V_{INP} = 0 V, V_{OUTP} = 5 V, SETP = open, T_A = 25°C		14	25	µA

[1] The ENP/UVP pin threshold must be met to ensure device operation.

[2] The ENN/UVN pin threshold must be met to ensure device operation.

[3] The maximum T_J limits operating conditions. The regulated output-voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current-limit foldback, which starts to decrease current limit at $V_{INP} – V_{OUTP}$ > 12 V. If operating at the maximum output current, limit the input-voltage range. If operating at the maximum input voltage, limit the output-current range.

[4] The maximum T_J limits operating conditions. The regulated output-voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current-limit foldback, which starts to decrease the current limit at $V_{OUTN} – V_{INN}$ > 7 V. If operating at the maximum output current, limit the input-voltage range. If operating at the maximum input voltage, limit the output-current range.

[5] OUTSP connects directly to OUTP.

[6] OUTSN connects directly to OUTN.

SPECIFICATIONS

[7] The dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when $V_{INP} = V_{OUTP\ (NOMINAL)}$. For output voltages less than 1.5 V, the dropout voltage is limited by the minimum input-voltage specification. See Figure 30 for the dropout voltage as a function of output current, measured in a typical application circuit. See Figure 32 for the dropout voltage as a function of temperature, measured in a typical application circuit.

[8] The dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when $V_{INN} = V_{OUTN\ (NOMINAL)}$. For output voltages between 0 V and –1.8 V, the dropout voltage is limited by the minimum input-voltage specification. See Figure 31 for the dropout voltage as a function of output current, measured in a typical application circuit. See Figure 33 for the dropout voltage as a function of temperature, measured in a typical application circuit.

[9] The GND pin current is tested with $V_{INP} = V_{OUTP(NOMINAL)}$ and a current source load. Therefore, the LT3097 is tested while operating in dropout, which is the worst-case GND pin current. The GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SETP pin or the ILIMP pin current; however, quiescent current does include the SETP and ILIMP pin currents.

[10] The GND pin current is tested with $V_{INN} = V_{OUTN(NOMINAL)}$ and a current source load. Therefore, the LT3097 is tested while operating in dropout, which is the worst-case GND pin current. The GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SETN pin or the ILIMN pin current; however, quiescent current does include the SETN and ILIMN pin currents.

[11] Adding a capacitor across the SETP pin resistor decreases the positive output voltage noise. Adding this capacitor bypasses the thermal noise of the resistor on the SETP pin as well as the noise of the positive reference current. The positive output noise then equals the positive error-amplifier noise. The use of a SETP pin bypass capacitor also increases the positive start-up time.

[12] Adding a capacitor across the SETN pin resistor decreases the negative output voltage noise. Adding this capacitor bypasses the thermal noise of the resistor on the SETN pin as well as the noise of the negative reference current. The negative output noise then equals the negative error-amplifier noise. The use of a SETN pin bypass capacitor also increases the negative start-up time.

[13] The positive internal back-up current-limit circuitry incorporates foldback protection that decreases the positive current limit for $V_{INP} – V_{OUTP} > 12$ V. Some level of output current is provided at all $V_{INP} – V_{OUTP}$ differential voltages. See Figure 56 for the current limit as a function of $V_{INP} – V_{OUTP}$.

[14] The positive current-limit programming scale factor is specified while the internal backup current limit is not active. Note that the positive internal current limit has foldback protection for $V_{INP} – V_{OUTP}$ differentials greater than 12 V.

[15] The negative internal back-up current-limit circuitry incorporates foldback protection that decreases the negative current limit for $V_{OUTN} – V_{INN} > 7$ V. Some level of output current is provided at all $V_{OUTN} – V_{INN}$ differential voltages. See Figure 57 for the current limit as a function of $V_{INN} – V_{OUTN}$.

[16] The negative current-limit programming scale factor is specified while the internal backup current limit is not active. Note that the negative internal current limit has foldback protection for $V_{OUTN} – V_{INN}$ differentials greater than 7 V.

[17] For positive output voltages less than 1 V, the positive regulator requires a 10 µA minimum load current for stability.

[18] For negative output voltages between 0 V and –1.5 V, the negative regulator requires a 10 µA minimum load current for stability.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Value
INP Pin Voltage	±22 V
INN Pin Voltage	
with Respect to GND Pin	–22 V to +0.3 V
ENP/UVP Pin Voltage	±22 V
ENN/UVN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V to +30 V
with Respect to GND Pin	±22 V
INP-to-ENP/UVP Differential	±22 V
PGP Pin Voltage[2]	–0.3 V, +22 V
PGN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V to +30 V
with Respect to GND Pin	–0.3 V to +22 V
ILIMP Pin Voltage[2]	–0.3 V, +1 V
ILIMN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V to +22 V
PGFBP Pin Voltage[2]	–0.3 V, +22 V
PGFBN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V to +30 V
with Respect to GND Pin	±22 V
SETP Pin Voltage[2]	–0.3 V, +16 V
SETP Pin Current[3]	±20 mA
SETN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V, +22 V
with Respect to GND Pin	±22 V
SETN Pin Current[4]	±10 mA
OUTSP Pin Voltage[2]	–0.3 V, +16 V
OUTSP Pin Current[3]	±20 mA
OUTSN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V, +22 V
with Respect to GND Pin	±22 V
OUTSN Pin Current[4]	±10 mA
SETN-to-OUTSN Differential[5]	±22 V
OUTP Pin Voltage[2]	–0.3 V, +16 V
OUTN Pin Voltage	
with Respect to INN Pin[1]	–0.3 V, +22 V
with Respect to GND Pin	±22 V
OUTP-to-OUTSP Differential[6]	±1.2 V
OUTN-to-OUTSN Differential[7]	±22 V
INP-to-OUTP Differential	±22 V
INP-to-OUTSP Differential	±22 V
Output Short-Circuit Duration	Indefinite
Temperature	
Operating T_J Range[8], A Grade	–40°C to +125°C
Storage Range	–65°C to +150°C

[1] Parasitic diodes exist internally between the ENN/UVN, ILIMN, PGN, PGFBN, SETN, GND, OUTSN, and OUTN pins and the INN pin. Do not drive the ENN/UVN, ILIMN, PGN, PGFBN, SETN, GND, OUTSN, and OUTN pins more than 0.3 V below the INN pin voltage during a fault condition. The ENN/UVN, ILIMN, PGN, PGFBN, SETN, GND, OUTSN, and OUTN pins must remain at a voltage more positive than INN during normal operation.

[2] Parasitic diodes exist internally between the ILIMP, PGP, PGFBP, SETP, OUTSP, and OUTP pins and the GND pin. Do not drive the ILIMP, PGP, PGFBP, SETP, OUTSP, and OUTP pins more than 0.3 V below the GND pin voltage during a fault condition. The ILIMP, PGP, PGFBP, SETP, OUTSP, and OUTP pins must remain at a voltage more positive than GND during normal operation.

[3] SETP and OUTSP pins are clamped using diodes and two 25 Ω series resistors. For less than 5 ms transients, this clamp circuitry can carry more than the rated current. For more details, see the Figure 122 and the Protection Features section.

[4] SETN and OUTSN pins are clamped using diodes and two 400 Ω series resistors. For less than 5 ms transients, this clamp circuitry can carry more than the rated current. For more details, see the Figure 123 and the Protection Features section.

[5] Maximum SETN and OUTSN pin current requirement must be satisfied.

[6] Maximum OUTP-to-OUTSP differential is guaranteed by design.

[7] Maximum OUTN-to-OUTSN differential is guaranteed by design.

[8] The LT3097 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3097 is tested at T_A = 25°C. Performance of the LT3097 over the full –40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3097 is guaranteed over the full –40°C to 125°C operating T_J range.

Stresses at or above those listed under Absolute Maximum Ratings can cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods can affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

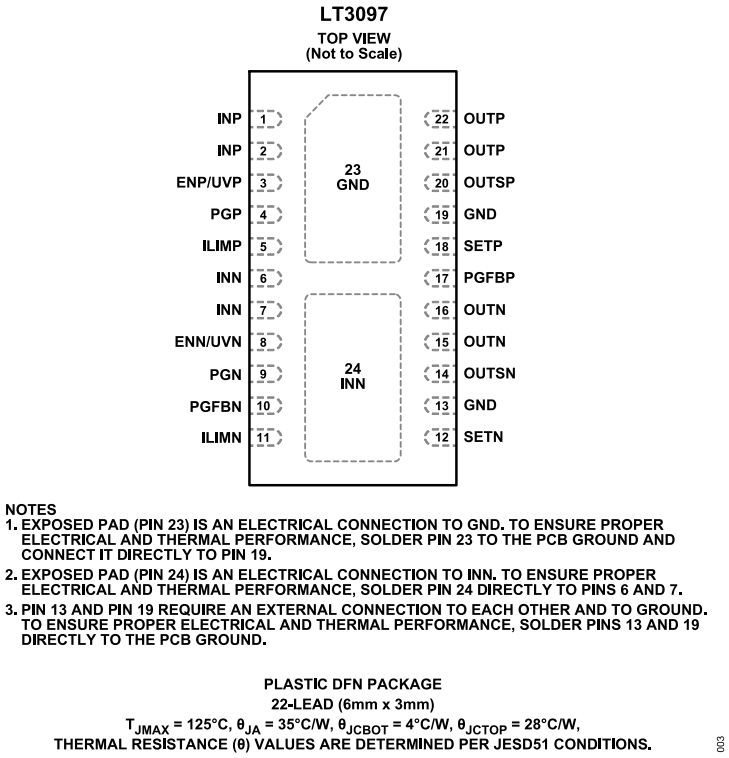

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	INP	Positive Input. The INP pins supply power to the positive regulator. The LT3097 requires a bypass capacitor at the INP pin. In general, the output impedance of a battery rises with frequency; therefore, it is best practice to include a bypass capacitor in battery-powered applications. While a 4.7 µF input bypass capacitor generally suffices, applications with large load transients can require higher input capacitance to prevent input-supply droop. See Stability and Input Capacitance and PSRR and Input Capacitance sections on the proper use of a positive input capacitor and its effect on circuit performance, particularly positive regulator PSRR. The LT3097 withstands reverse voltages on INP for GND, OUTSP, and OUTP. In the case of a reversed input, which occurs if a battery is plugged in backward, the LT3097 positive regulator acts as if a diode is in series with its input. Therefore, no reverse current flows into the LT3097, and no negative voltage appears at the positive load. The positive regulator protects itself and the load.
3	ENP/UVP	Positive Enable and UVLO. Pulling the ENP/UVP pin low moves the LT3097 positive regulator to shutdown mode. The positive quiescent current in shutdown mode drops to less than 1 µA, and the positive output voltage turns off. Alternatively, the ENP/UVP pin can set a positive input-supply UVLO threshold using a resistor-divider between INP, ENP/UVP, and GND. The LT3097 positive regulator typically turns on when the ENP/UVP voltage exceeds 1.24 V on its rising edge, with a 130 mV hysteresis on its falling edge. The ENP/UVP pin can be driven above the positive input voltage and maintain proper functionality. If unused, connect ENP/UVP to INP. Do not float the ENP/UVP pin.
4	PGP	Positive Power Good. PGP is an open-collector flag that indicates positive output-voltage regulation. PGP pulls low if PGFBP is less than 300 mV. If the power-good functionality is not needed, float the PGP pin. The positive power-good functionality is disabled in shutdown. See the Positive Regulator Programmable Power Good section if power-good functionality is needed in shutdown. A parasitic substrate diode exists between the PGP and GND pin of the LT3097; therefore, do not drive PGP more than 0.3 V below GND during normal operation or a fault condition.
5	ILIMP	Positive Regulator Current-Limit Programming Pin. Connecting a resistor between ILIMP and GND programs the current limit. For best accuracy, Kelvin connects this resistor directly to the GND pin of the LT3097. The programming-scale factor is nominally 150 mA × kΩ. The ILIMP pin sources current proportional (1:500) to the positive output current. Therefore, ILIMP also serves as a current-monitoring pin with a 0 V to 300 mV range. If the programmable current-limit functionality is not needed, connect ILIMP to GND. Do not float the ILIMP pin. A parasitic substrate diode exists between the ILIMP and GND pin of the LT3097; therefore, do not drive ILIMP more than 0.3 V below GND during normal operation or a fault condition.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
6, 7	INN	Negative Input. The INN pins supply power to the negative regulator. The LT3097 requires a bypass capacitor at the INN pin. In general, the output impedance of a battery rises with frequency; therefore, it is best practice to include a bypass capacitor in battery-powered applications. While a 10 µF input bypass capacitor generally suffices, applications with large load transients can require higher input capacitance to prevent input-supply droop. See the Stability and Input Capacitance and PSRR and Input Capacitance sections on the proper use of a negative input capacitor and its effect on circuit performance, particularly negative regulator PSRR.
8	ENN/UVN	Negative Enable and UVLO. Pulling the ENN/UVN pin to GND moves the LT3097 negative regulator to shutdown mode. The negative quiescent current in shutdown mode drops to 3 µA, and the negative output voltage turns off. Alternatively, the ENN/UVN pin can set a negative input-supply UVLO threshold using a resistor-divider between INN, ENN/UVN, and GND. The ENN/UVN pin is bidirectional and can be switched with either a positive or negative voltage. For positive voltages on the ENN/UVN pin, the LT3097 negative regulator typically turns on when the ENN/UVN voltage exceeds 1.26 V above ground on its rising edge, with a 200 mV hysteresis on its falling edge. For negative voltages on the ENN/UVN pin, the LT3097 negative regulator typically turns on when the ENN/UVN voltage exceeds 1.26 V below ground on its rising edge, with a 215 mV hysteresis on its falling edge. If unused, connect ENN/UVN to INN. Do not float the ENN/UVN pin.
9	PGN	Negative Power Good. PGN is an open-collector flag that indicates negative output-voltage regulation. PGN pulls to GND if PGFBN is between 0 V and –300 mV. If the power-good functionality is not needed, float the PGN pin. The PGN flag status is valid even if the LT3097 negative regulator is in shutdown, with the PGN pin being pulled to GND.
10	PGFBN	Negative Power-Good Feedback. The PGN pin pulls high if PGFBN is below –300 mV on its rising edge, with 7 mV hysteresis on its falling edge. Connecting an external resistor-divider between OUTN, PGFBN, and GND sets the programmable power-good threshold with the following transfer function: $–0.3\ V \times (1 + R_{PGN2}/R_{PGN1})$. In the Fast Startup section, PGFBN also activates the fast start-up circuitry. Connect PGFBN to INN if the power-good and fast start-up functions are not needed.
11	ILIMN	Negative Regulator Current-Limit Programming Pin. Connecting a resistor between ILIMN and GND programs the current limit. For best accuracy, Kelvin connects this resistor directly to the GND pin of the LT3097. The programming-scale factor is nominally 3.75 A × kΩ. If the programmable current-limit functionality is not needed, connect ILIMN to GND. Do not float the ILIMN pin.
12	SETN	The Inverting Input of the Error Amplifier and the Regulation Set Point for the LT3097 Negative Regulator. SETN sinks precision 100 µA current that flows through an external resistor connected between SETN and GND. The negative output voltage of the LT3097 is determined by $V_{SETN} = I_{SETN} \times$ SETN resistance (R_{SETN}). The negative output voltage range is from 0 V to –19.5 V. Adding a capacitor from SETN to GND improves noise, PSRR, and transient response at the expense of an increased start-up time. Using the fast start-up capability through the PGFBN pin mitigates this increase in start-up time. For optimum negative load regulation, Kelvin connects the ground side of the SETN pin resistor directly to the negative load.
13	GND	Ground. Pin 13 is negative regulator ground.
14	OUTSN	Negative Output Sense. The OUTSN pin is the noninverting input to the error amplifier of the negative regulator. For optimal transient performance and load regulation, Kelvin connects OUTSN directly to the negative output capacitor and the negative load. In addition, connect the GND connections of the negative output capacitor and the SETN pin capacitor directly together. Exercise care regarding placement of negative input capacitors relative to negative output capacitors due to potential PSRR degradation from magnetic coupling effects. See PSRR and Input Capacitance for further information on capacitor placement and board layout. A parasitic-substrate diode exists between the OUTSN and INN pins of the LT3097; therefore, do not drive OUTSN more than 0.3 V below INN during normal operation or during a fault condition.
15, 16	OUTN	Negative Output. The OUTN pins supply power to the negative load. For stability, use a minimum 10 µF output capacitor with an equivalent series resistance (ESR) of less than 30 mΩ and an effective series inductance (ESL) of less than 1.5 nH. Large load transients require larger output capacitance to limit peak-voltage transients. See the Stability and Output Capacitance section for more information on negative output capacitance. A parasitic-substrate diode exists between the OUTN and INN pins of the LT3097; therefore, do not drive OUTN more than 0.3 V below INN during normal operation or a fault condition.
17	PGFBP	Positive Power-Good Feedback. The PGP pin pulls high if PGFBP increases beyond 300 mV on its rising edge, with 7 mV hysteresis on its falling edge. Connecting an external resistor-divider between OUTP, PGFBP, and GND sets the programmable power-good threshold with the following transfer function: $0.3\ V \times (1 + R_{PGP2}/R_{PGP1})$.In the Fast Startup section, PGFBP also activates the fast start-up circuitry. Connect PGFBP to INP if the power-good and fast start-up functions are not needed. In addition, if reverse-input protection is additionally required, connect the anode of a 1N4148 diode to INP and its cathode to PGFBP. A parasitic-substrate diode exists between the PGFBP and GND pin of the LT3097; therefore, do not drive PGFBP more than 0.3 V below GND during normal operation or a fault condition.
18	SETP	The Inverting Input of the Error Amplifier and the Regulation Set Point for the LT3097 Positive Regulator. SETP sources precision 100 µA current that flows through an external resistor connected between SETP and GND. The positive output voltage of the LT3097 is determined by $V_{SETP} = I_{SETP} \times$ SETP resistance (R_{SETP}). The positive output voltage range is from 0 V to 15 V. Adding a capacitor from SETP to GND improves noise, PSRR, and transient response at the expense of an increased start-up time. Using the fast start-up capability through the PGFBP pin mitigates this increase in start-up time. For optimum positive load regulation, Kelvin connects the ground side of the SETP pin resistor directly to the positive load. A parasitic-substrate diode exists between the SETP and GND pins of the LT3097; therefore, do not drive SETP more than 0.3 V below GND during normal operation or a fault condition.
19	GND	Ground. Pin 19 is positive regulator ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 3. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
20	OUTSP	Positive Output Sense. The OUTSP pin is the noninverting input to the error amplifier of the positive regulator. For optimal transient performance and load regulation, Kelvin connects OUTSP directly to the positive output capacitor and the positive load. In addition, connect the GND connections of the positive output capacitor and the SETP pin capacitor directly together. Exercise care with regard to the placement of positive input capacitors relative to positive output capacitors due to potential PSRR degradation from magnetic coupling effects; see PSRR and Input Capacitance for further information on capacitor placement and board layout. A parasitic-substrate diode exists between the OUTSP and GND pins of the LT3097; therefore, do not drive OUTSP more than 0.3 V below GND during normal operation or a fault condition.
21, 22	OUTP	Positive Output. The OUTP pins supply power to the positive load. For stability, use a minimum 10 µF output capacitor with an ESR of less than 20 mΩ and an ESL of less than 2 nH. Large load transients require larger output capacitance to limit peak-voltage transients. See the Stability and Output Capacitance section for more information on positive output capacitance. A parasitic-substrate diode exists between the OUTP and GND pins of the LT3097; therefore, do not drive OUTP more than 0.3 V below GND during normal operation or a fault condition.
23	EPAD (GND)	Ground Exposed Pad. The ground exposed pad is an electrical connection to pin 19 GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and connect it directly to the pin 19 GND.
24	EPAD (INN)	INN Exposed Pad. The INN exposed pad is an electrical connection to INN. To ensure proper electrical and thermal performance, solder the INN exposed backside directly to the INN pins 6 and 7.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

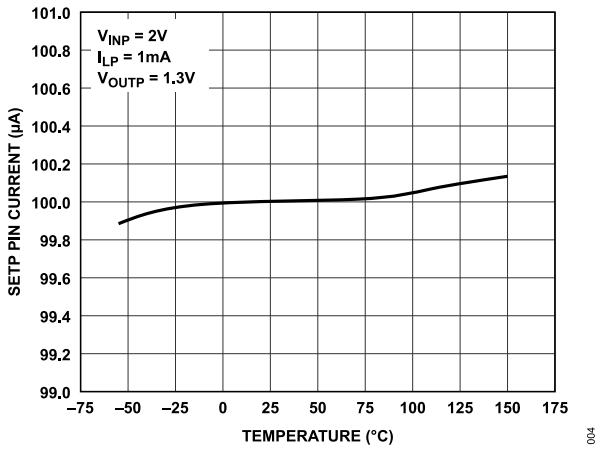

Figure 4. SETP Pin Current vs. Temperature

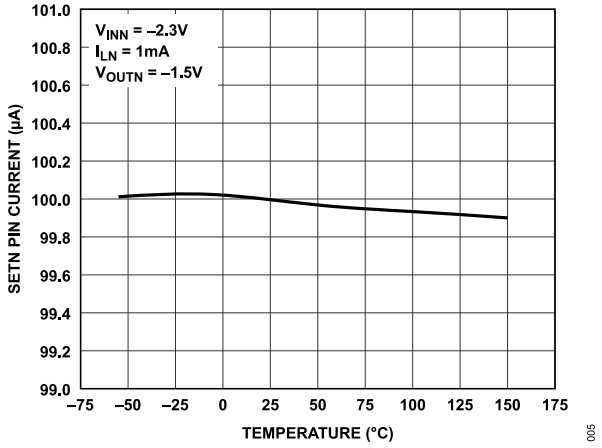

Figure 5. SETN Pin Current vs. Temperature

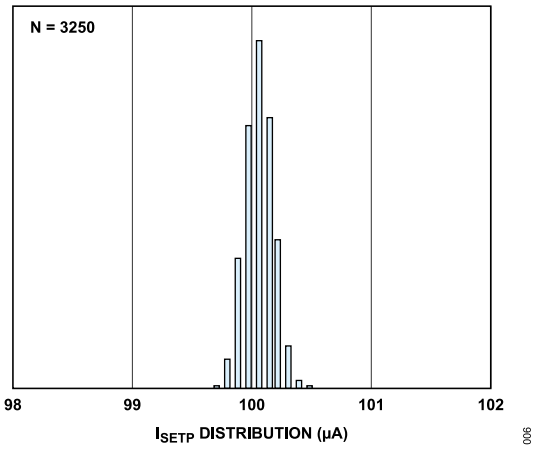

Figure 6. I_{SETP} Distribution

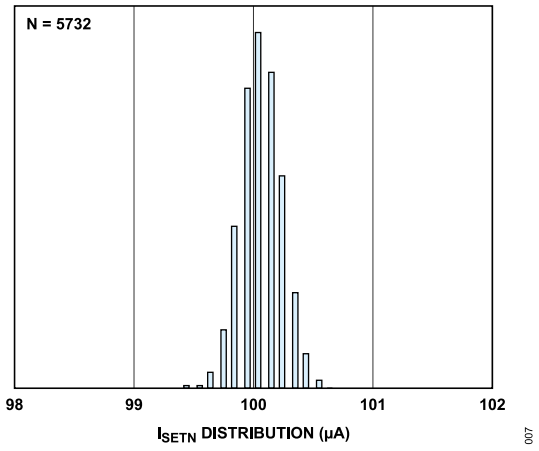

Figure 7. I_{SETN} Distribution

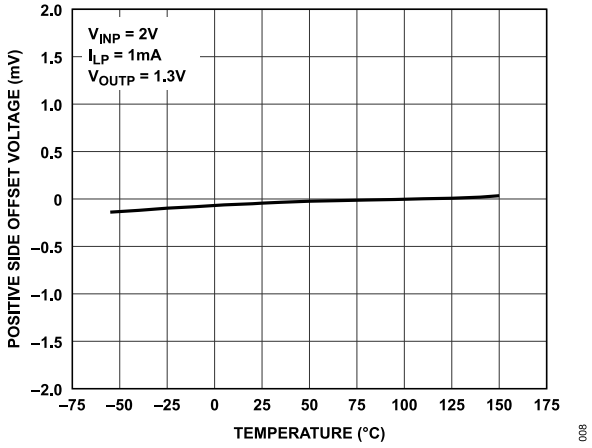

Figure 8. Positive Side Offset Voltage (V_{OUTP} – V_{SETP}) vs. Temperature

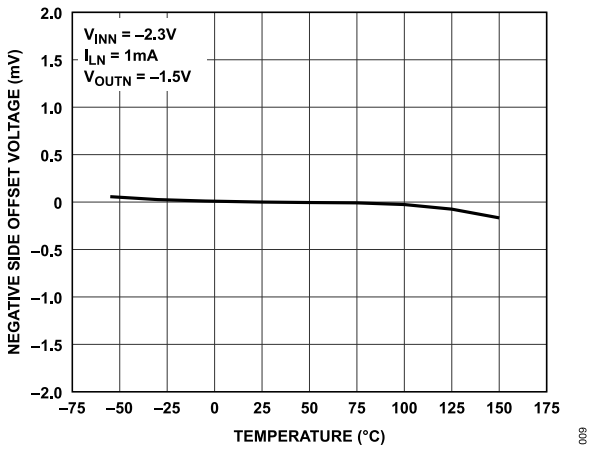

Figure 9. Negative Side Offset Voltage (V_{OUTN} – V_{SETN}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

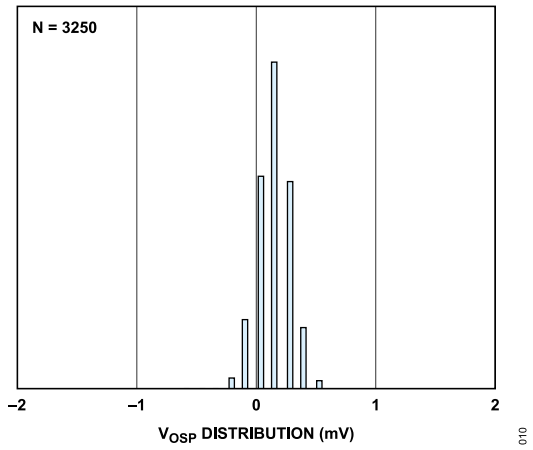

Figure 10. Positive Offset Voltage (V_{OSP}) Distribution

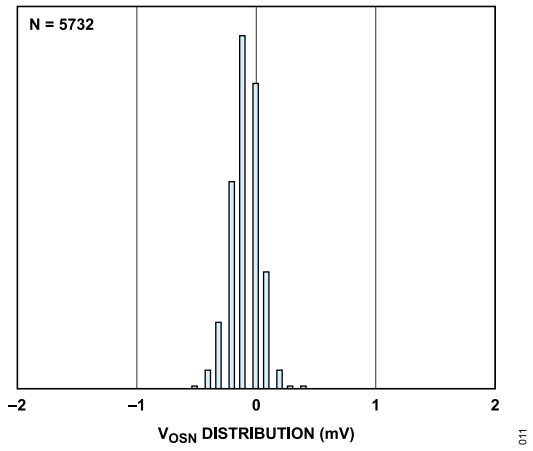

Figure 11. Negative Offset Voltage (V_{OSN}) Distribution

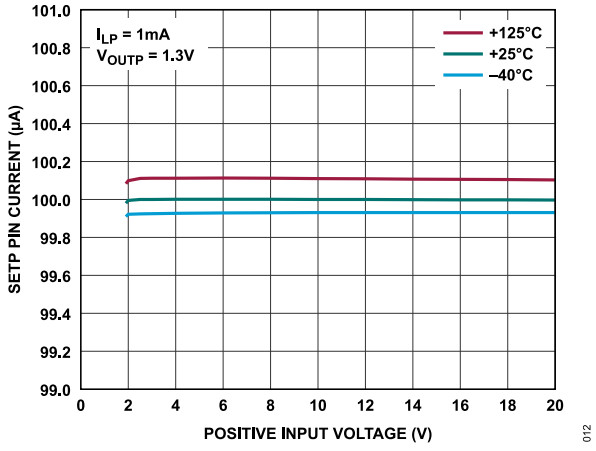

Figure 12. SETP Pin Current vs. Positive Input Voltage

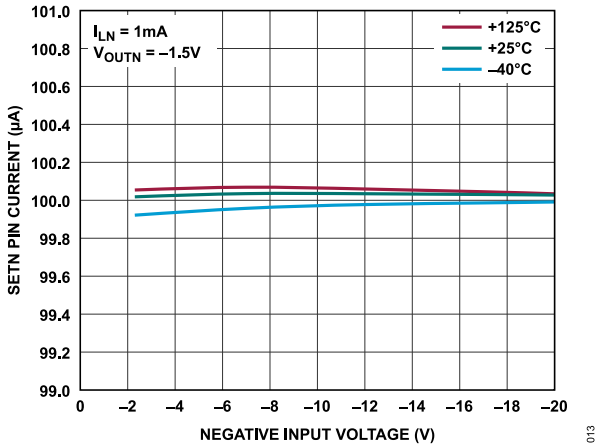

Figure 13. SETN Pin Current vs. Negative Input Voltage

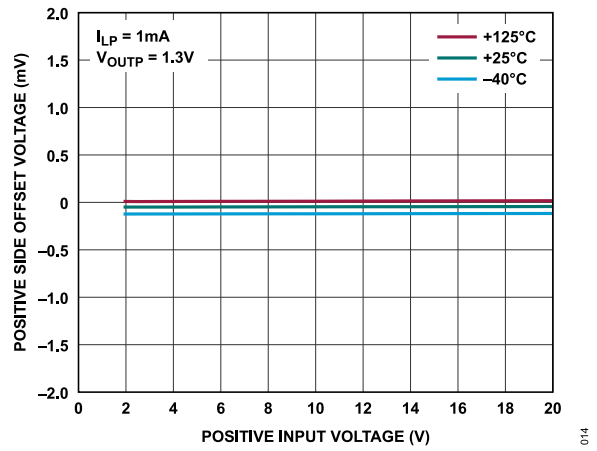

Figure 14. Positive Side Offset Voltage (V_{OUTP} – V_{SETP}) vs. Positive Input Voltage

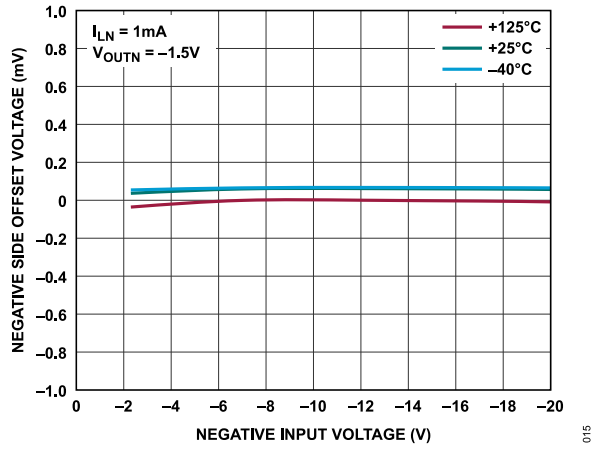

Figure 15. Negative Side Offset Voltage (V_{OUTN} – V_{SETN}) vs. Negative Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

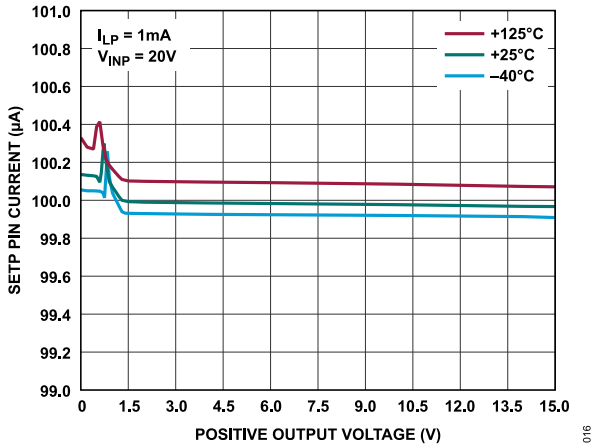

Figure 16. SETP Pin Current vs. Positive Output Voltage

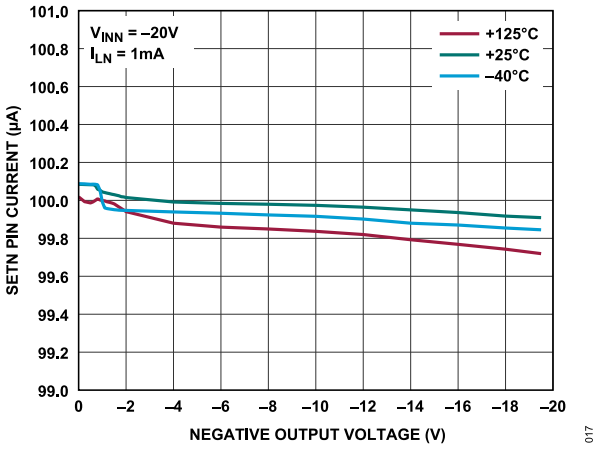

Figure 17. SETN Pin Current vs. Negative Output Voltage

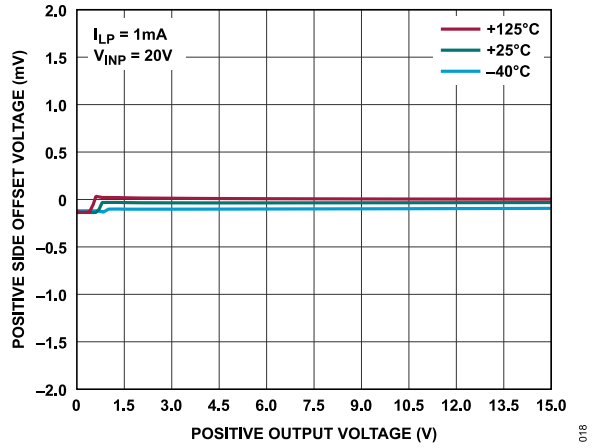

Figure 18. Positive Side Offset Voltage (V_{OUTP} – V_{SETP}) vs. Positive Output Voltage

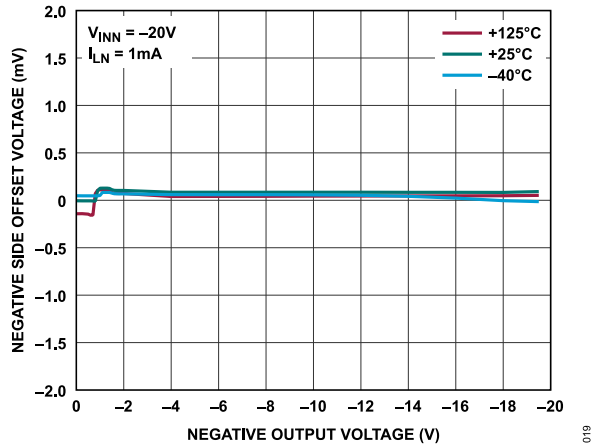

Figure 19. Negative Side Offset Voltage (V_{OUTN} – V_{SETN}) vs. Negative Output Voltage

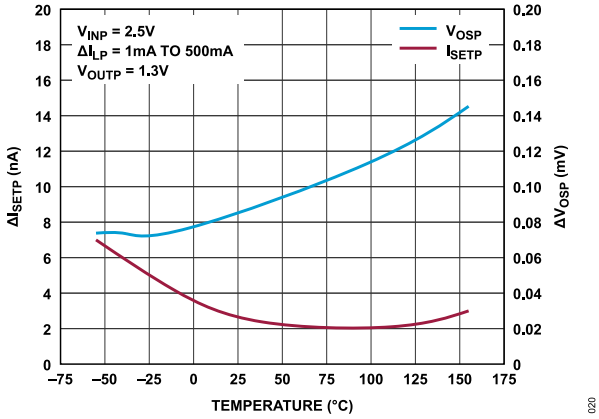

Figure 20. I_{SETP} and V_{OSP} Load Regulation vs. Temperature

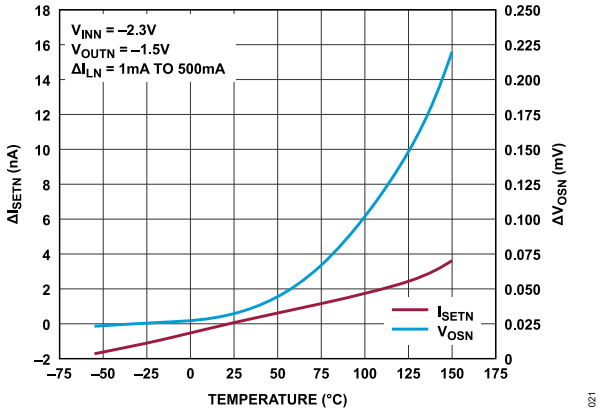

Figure 21. I_{SETN} and V_{OSN} Load Regulation vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

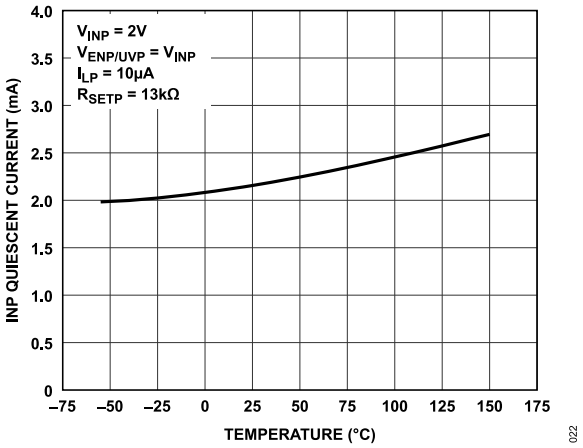

Figure 22. INP Quiescent Current vs. Temperature ($V_{ENP/UVP}$ = V_{INP})

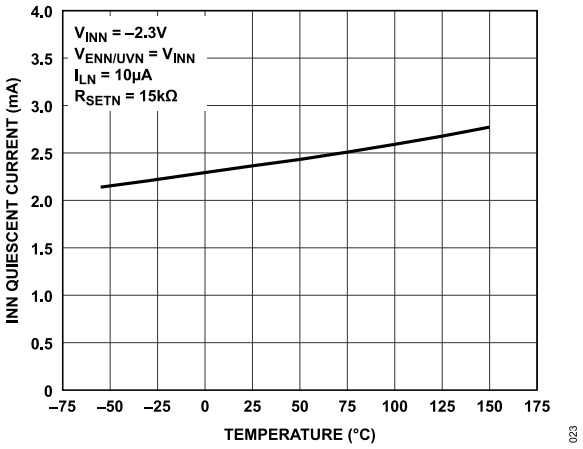

Figure 23. INN Quiescent Current vs. Temperature ($V_{ENN/UVN}$ = V_{INN})

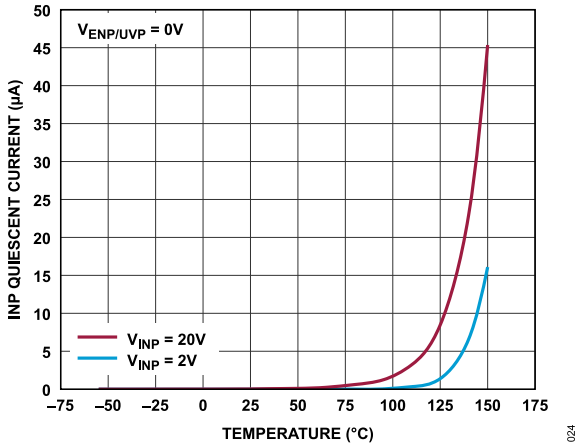

Figure 24. INP Quiescent Current vs. Temperature ($V_{ENP/UVP}$ = 0 V)

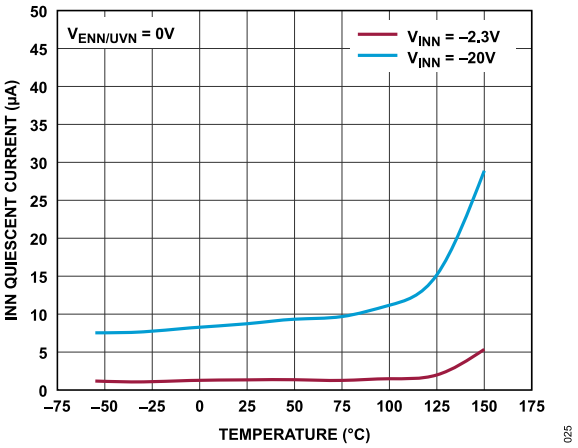

Figure 25. INN Quiescent Current vs. Temperature ($V_{ENN/UVN}$ = 0 V)

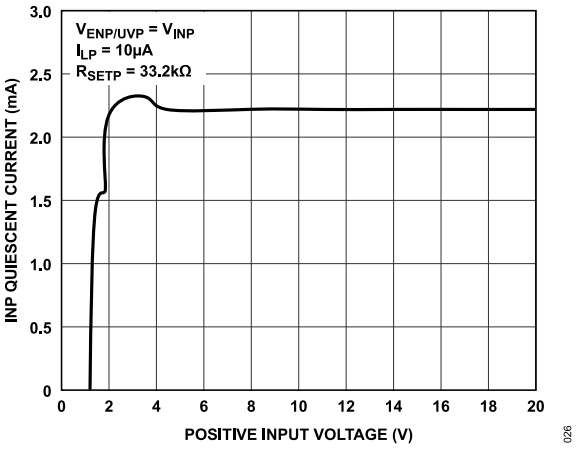

Figure 26. INP Quiescent Current vs. Positive Input Voltage

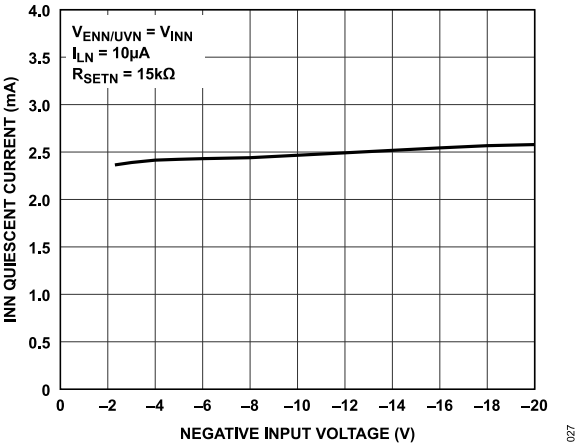

Figure 27. INN Quiescent Current vs. Negative Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

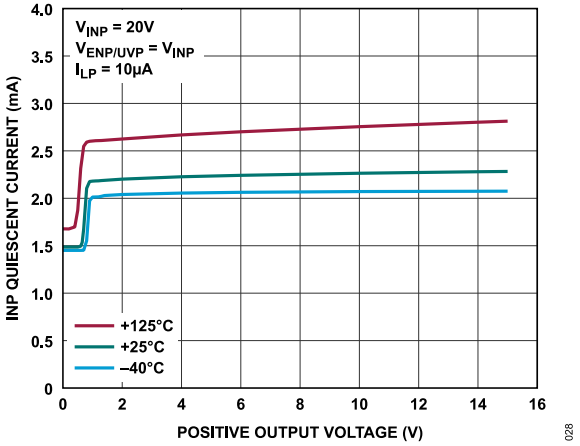

Figure 28. INP Quiescent Current vs. Positive Output Voltage

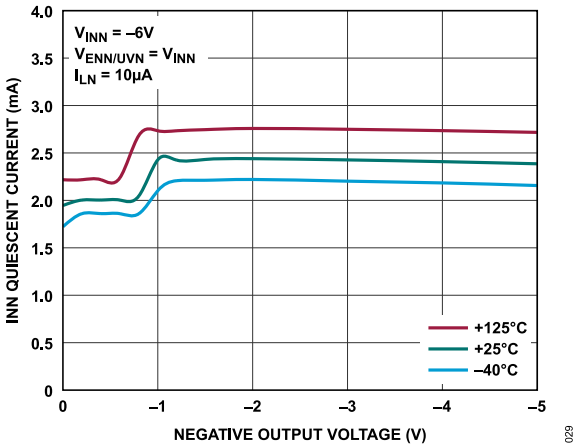

Figure 29. INN Quiescent Current vs. Negative Output Voltage

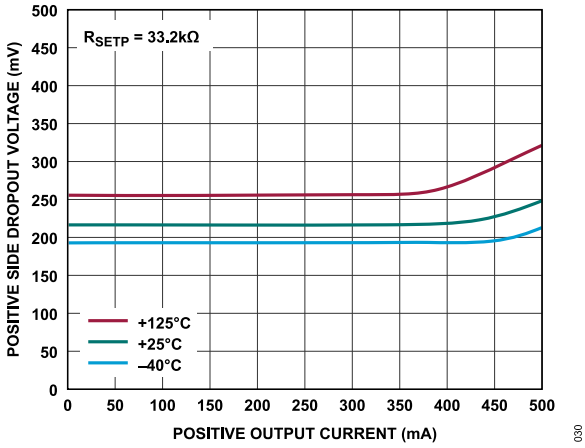

Figure 30. Positive Side Dropout Voltage vs. Positive Output Current

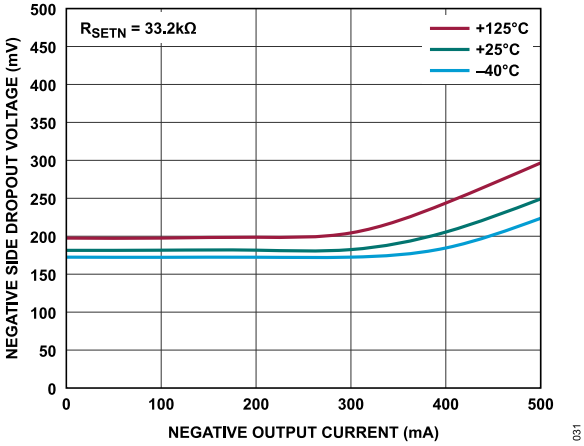

Figure 31. Negative Side Dropout Voltage vs. Negative Output Current

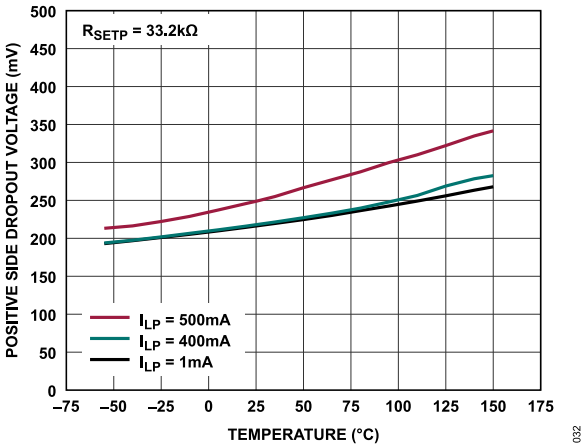

Figure 32. Positive Side Dropout Voltage vs. Temperature

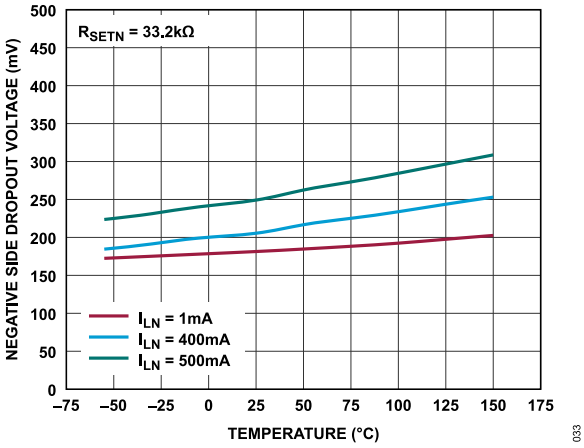

Figure 33. Negative Side Dropout Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

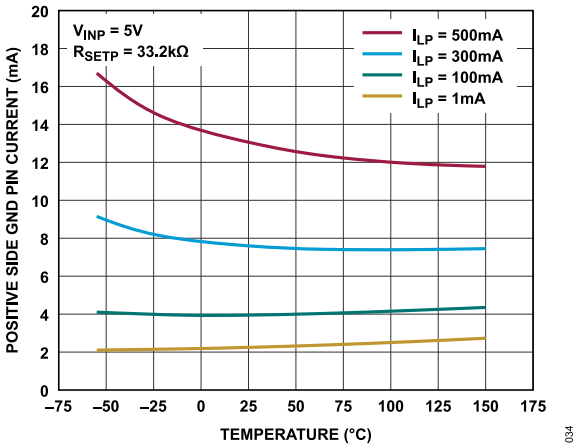

Figure 34. Positive Side GND Pin Current vs. Temperature

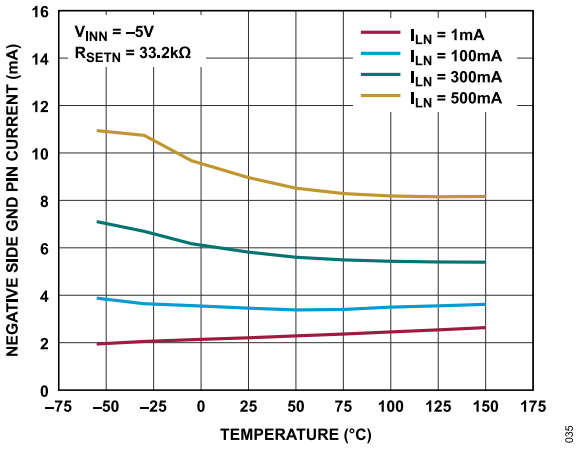

Figure 35. Negative Side GND Pin Current vs. Temperature

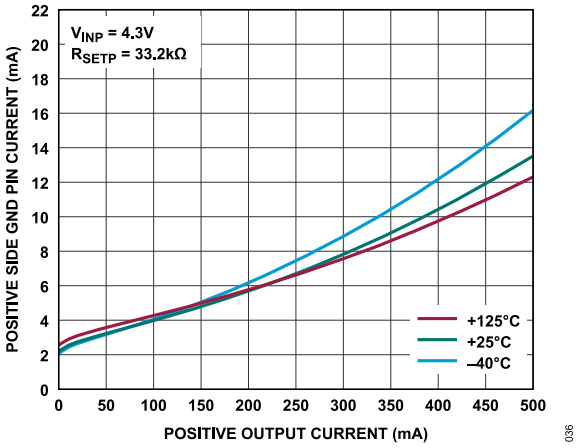

Figure 36. Positive Side GND Pin Current vs. Positive Output Current

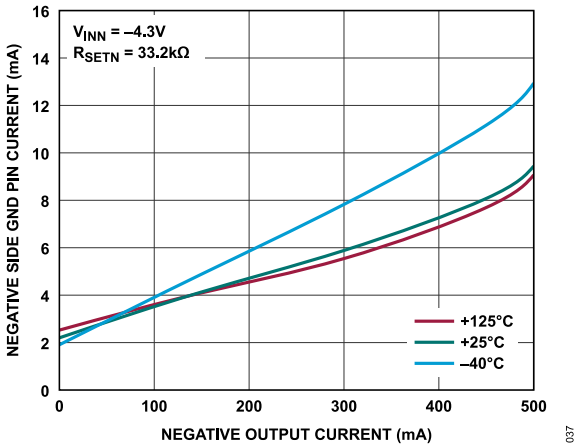

Figure 37. Negative Side GND Pin Current vs. Negative Output Current

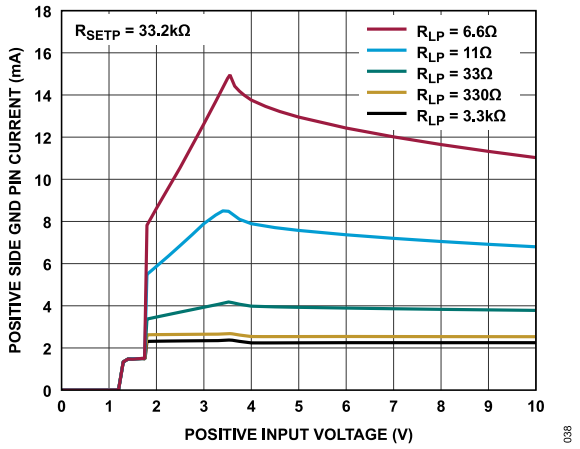

Figure 38. Positive Side GND Pin Current vs. Positive Input Voltage (R_{LP} is the Positive Load Resistance)

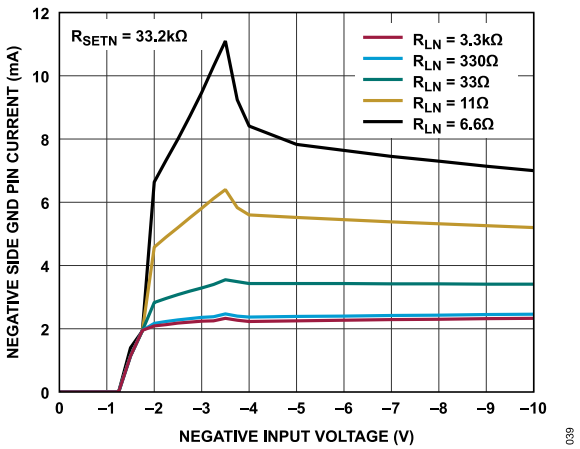

Figure 39. Negative Side GND Pin Current vs. Negative Input Voltage (R_{LN} is the Negative Load Resistance)

TYPICAL PERFORMANCE CHARACTERISTICS

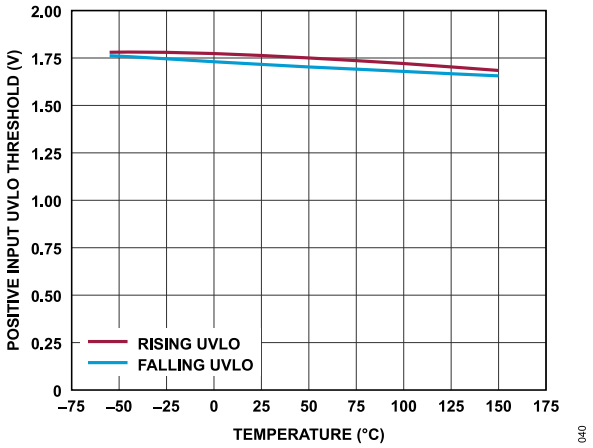

Figure 40. Positive Input UVLO Threshold vs. Temperature

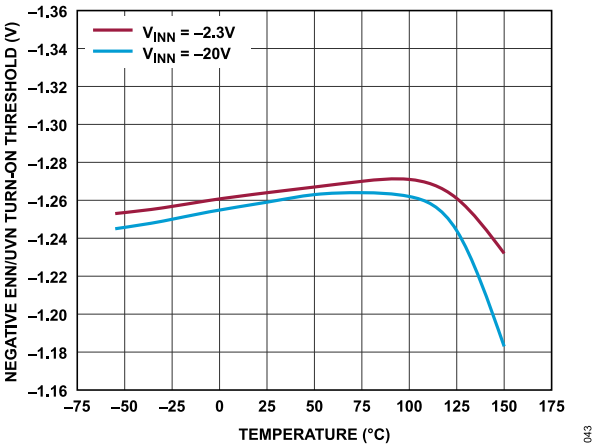

Figure 43. Negative ENN/UVN Turn-On Threshold vs. Temperature

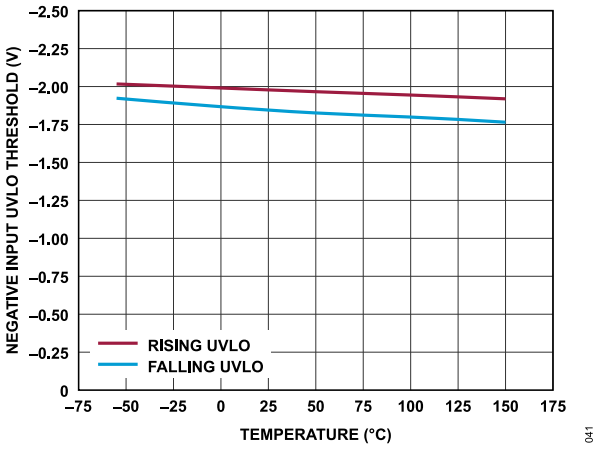

Figure 41. Negative Input UVLO Threshold vs. Temperature

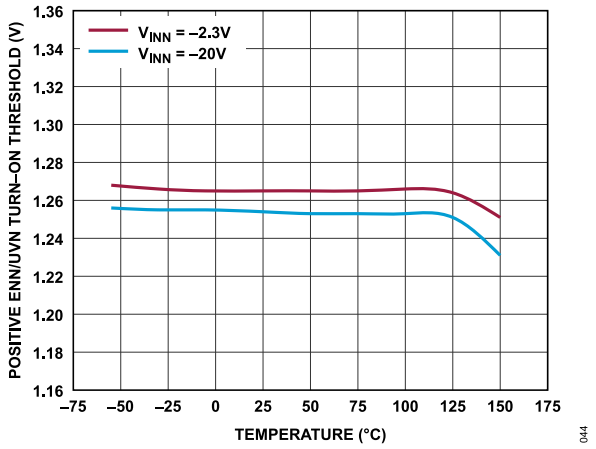

Figure 44. Positive ENN/UVN Turn-On Threshold vs. Temperature

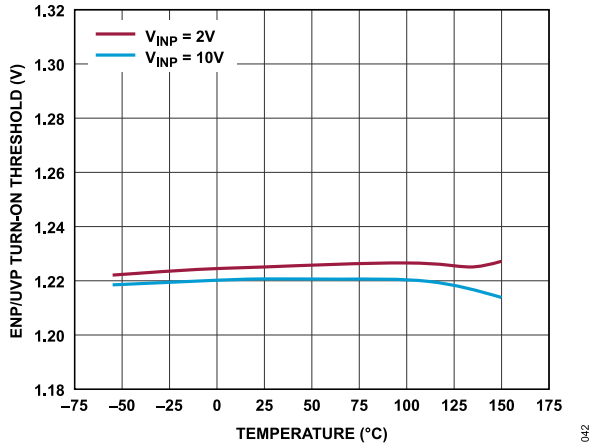

Figure 42. ENP/UVP Turn-On Threshold vs. Temperature

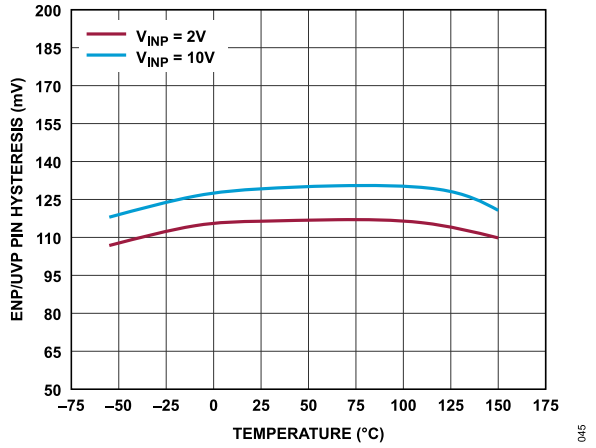

Figure 45. ENP/UVP Pin Hysteresis vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

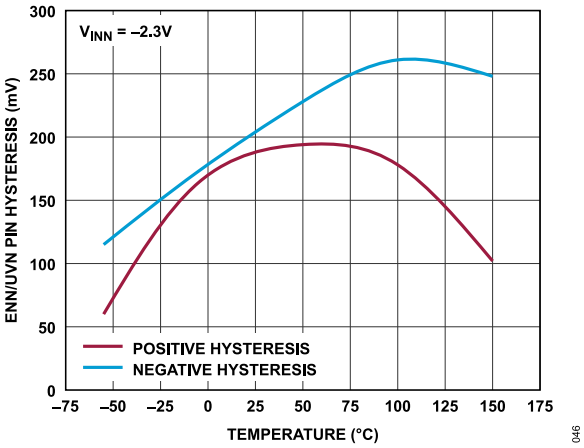

Figure 46. ENN/UVN Pin Hysteresis vs. Temperature

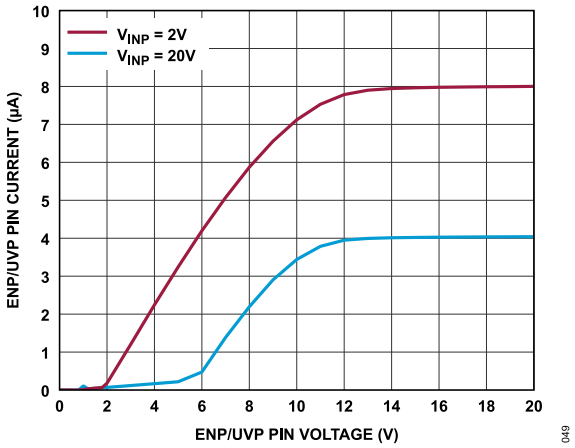

Figure 49. ENP/UVP Pin Current vs. ENP/UVP Pin Voltage (V_{INP} Steps)

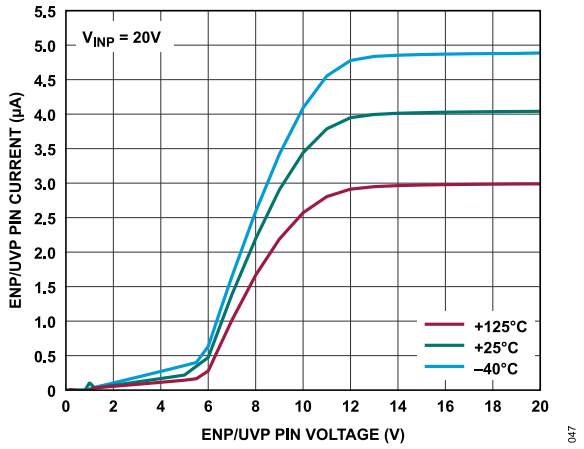

Figure 47. ENP/UVP Pin Current vs. ENP/UVP Pin Voltage (Temperature Steps)

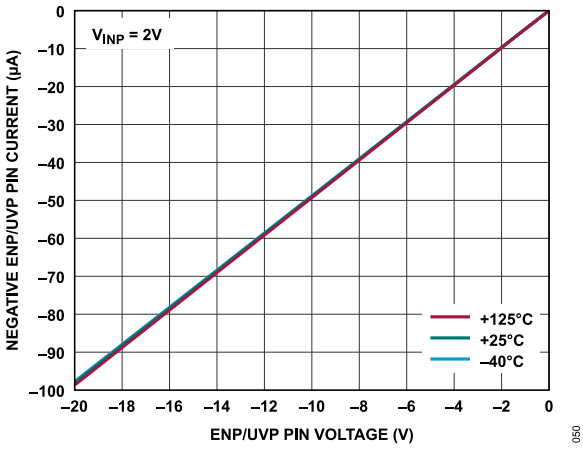

Figure 50. Negative ENP/UVP Pin Current vs. ENP/UVP Pin Voltage

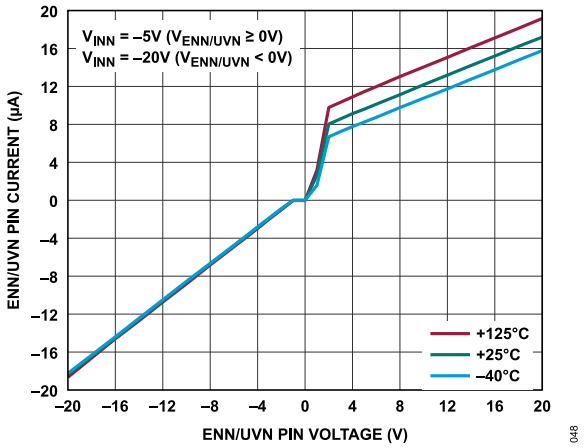

Figure 48. ENN/UVN Pin Current vs. ENN/UVN Pin Voltage (Temperature Steps)

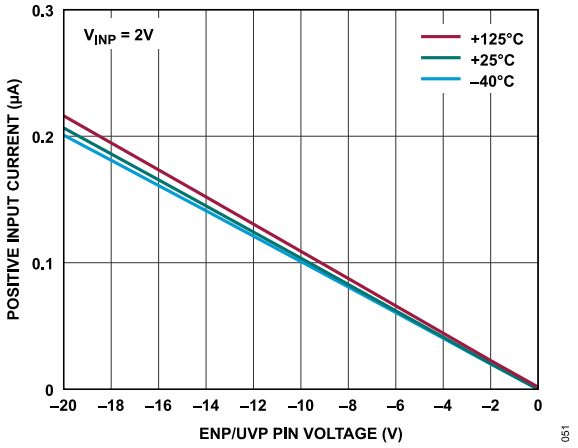

Figure 51. Positive Input Current vs. ENP/UVP Pin Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

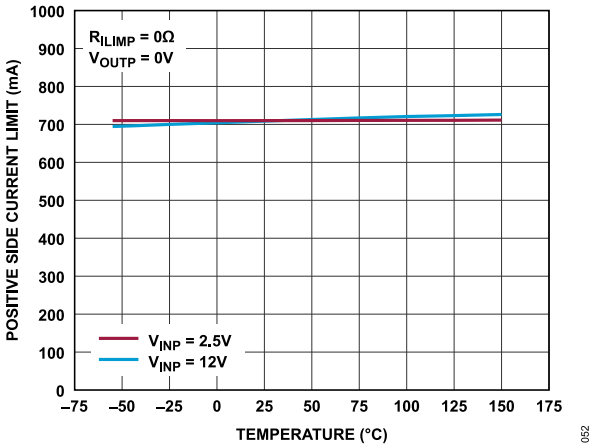

Figure 52. Positive Side Internal Current Limit vs. Temperature

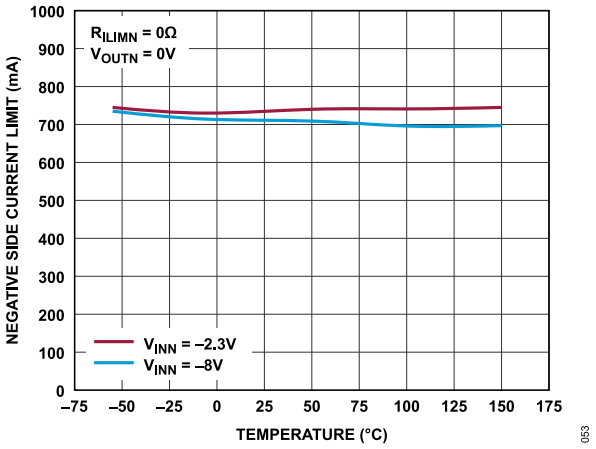

Figure 53. Negative Side Internal Current Limit vs. Temperature

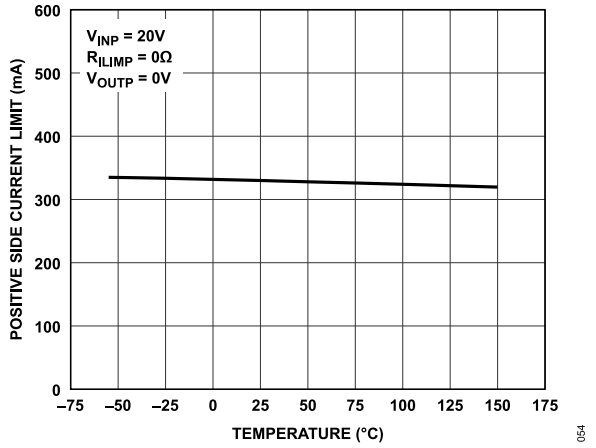

Figure 54. Positive Side Internal Current Limit vs. Temperature (Foldback)

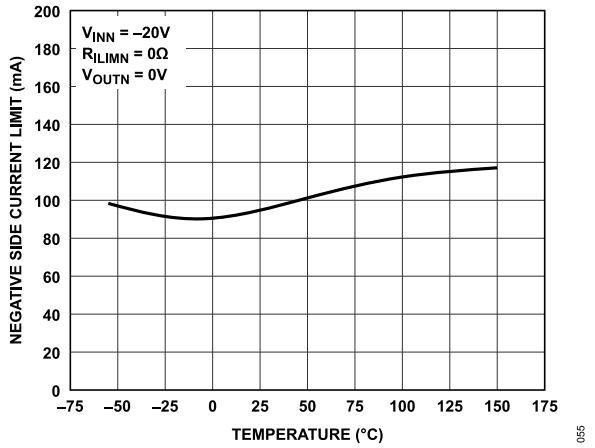

Figure 55. Negative Side Internal Current Limit vs. Temperature (Foldback)

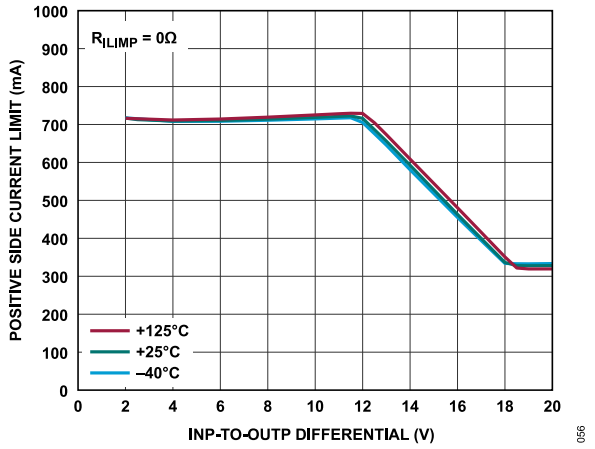

Figure 56. Positive Side Internal Current Limit vs. Positive Input-to-Output Differential

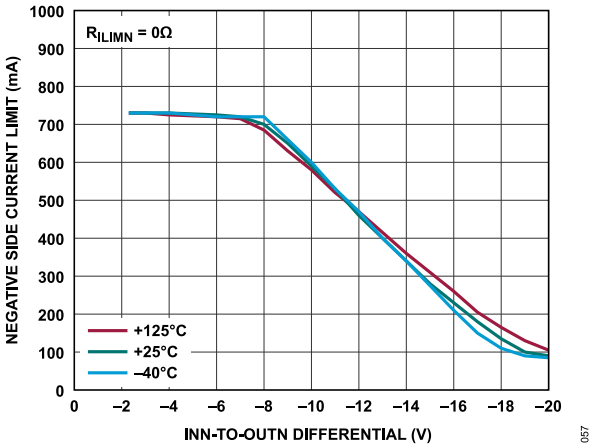

Figure 57. Negative Side Internal Current Limit vs. Negative Input-to-Output Differential

TYPICAL PERFORMANCE CHARACTERISTICS

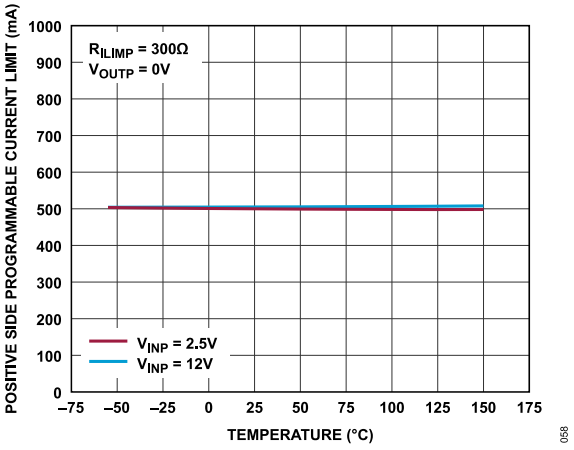

Figure 58. Positive Side Programmable Current Limit vs. Temperature (500 mA)

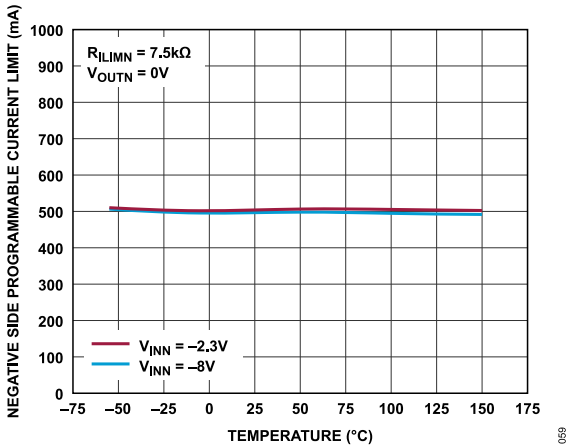

Figure 59. Negative Side Programmable Current Limit vs. Temperature (500 mA)

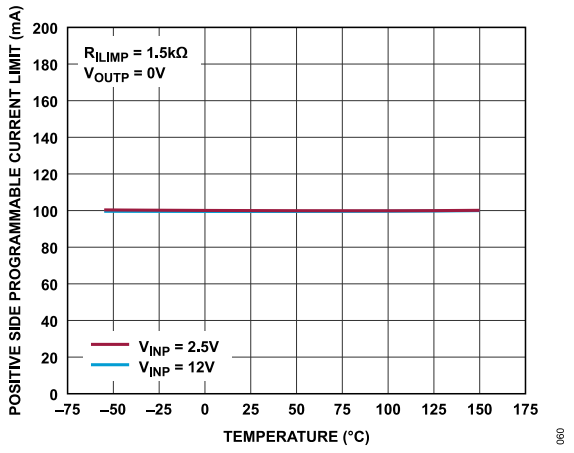

Figure 60. Positive Side Programmable Current Limit vs. Temperature (100 mA)

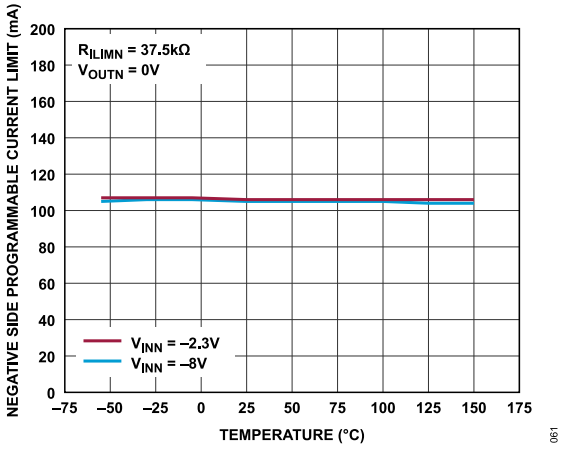

Figure 61. Negative Side Programmable Current Limit vs. Temperature (100 mA)

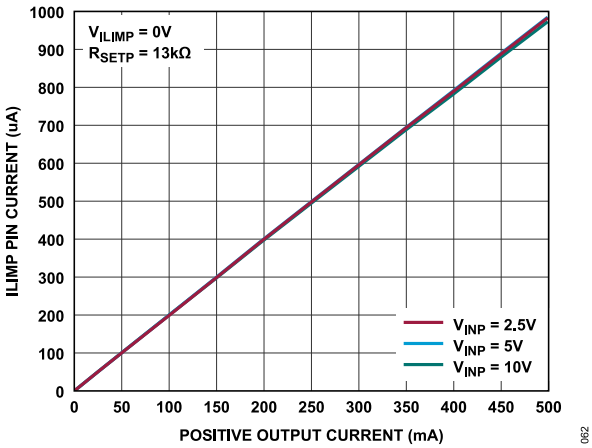

Figure 62. ILIMP Pin Current vs. Positive Load Current

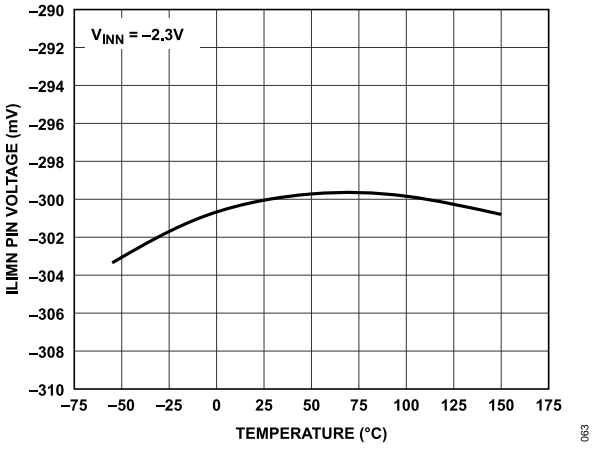

Figure 63. ILIMN Pin Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

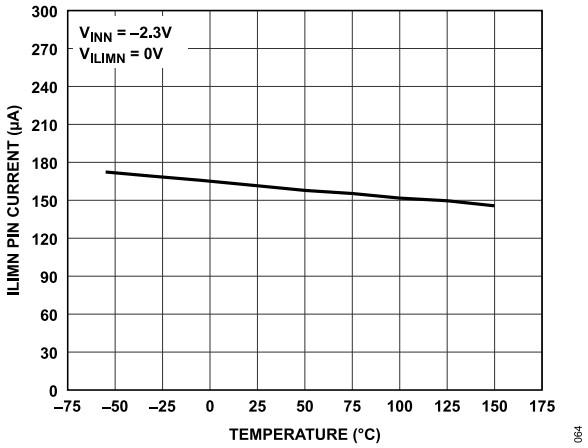

Figure 64. ILIMN Pin Current vs. Temperature

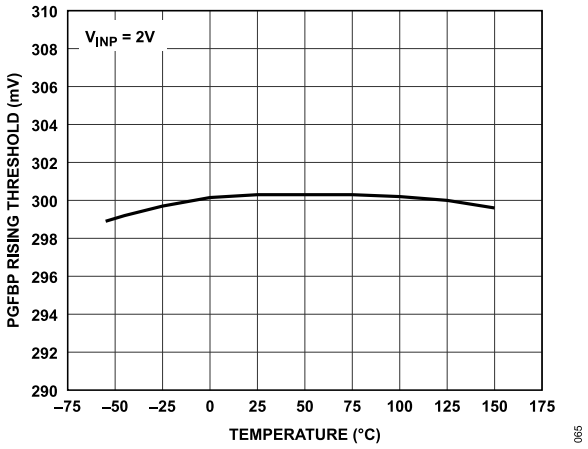

Figure 65. PGFBP Rising Threshold vs. Temperature

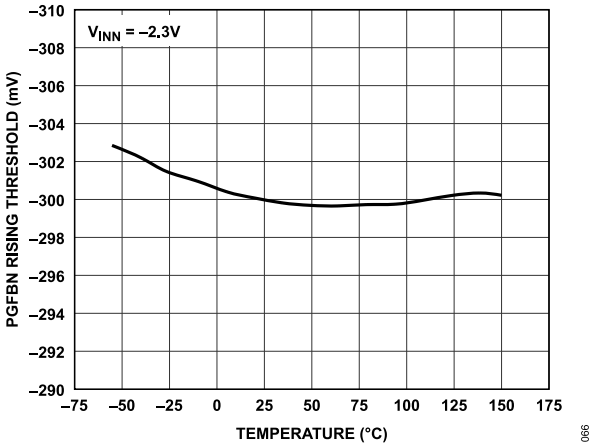

Figure 66. PGFBN Rising Threshold vs. Temperature

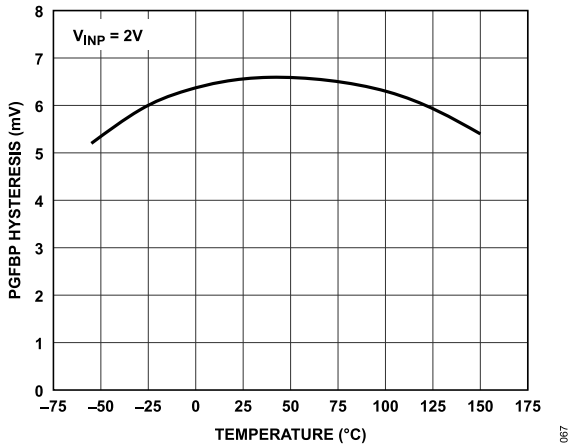

Figure 67. PGFBP Hysteresis vs. Temperature

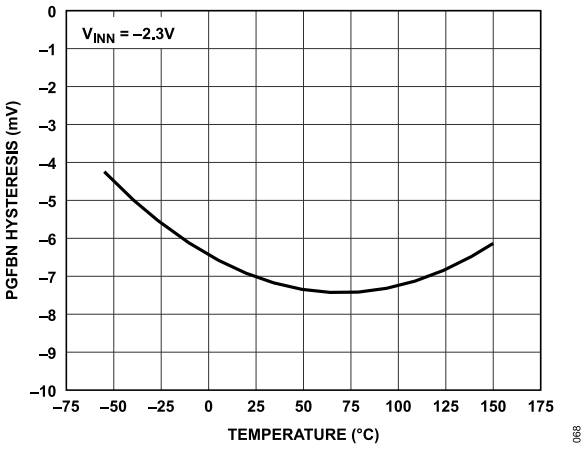

Figure 68. PGFBN Hysteresis vs. Temperature

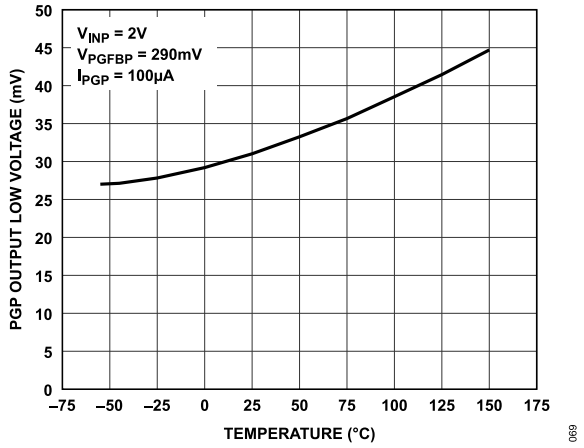

Figure 69. PGP Output Low Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

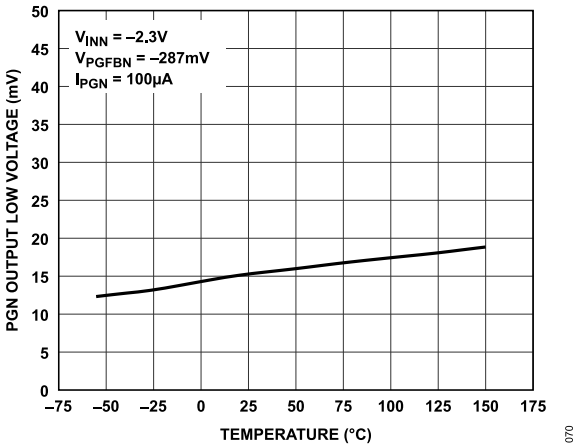

Figure 70. PGN Output Low Voltage vs. Temperature

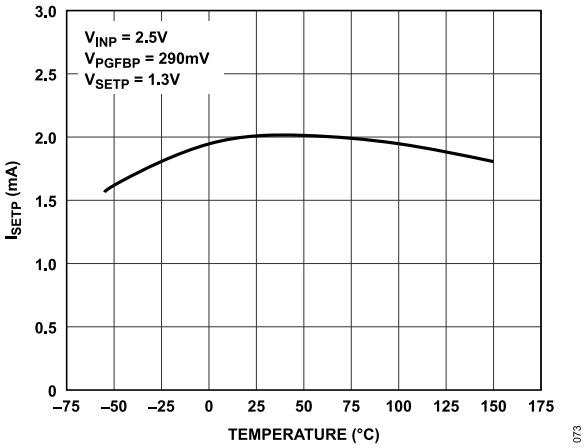

Figure 73. I_{SETP} during Start-Up with Fast Start-Up Enabled vs. Temperature

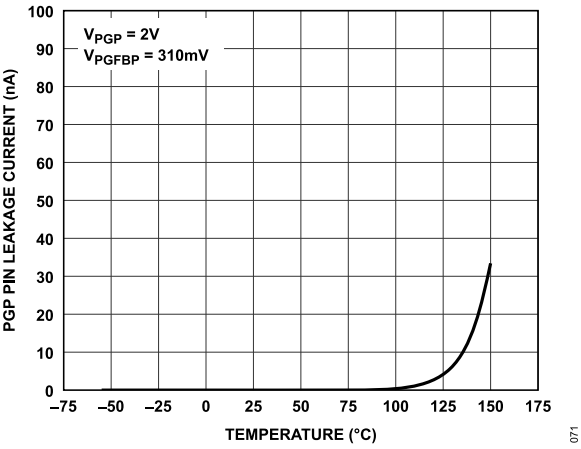

Figure 71. PGP Pin Leakage Current vs. Temperature

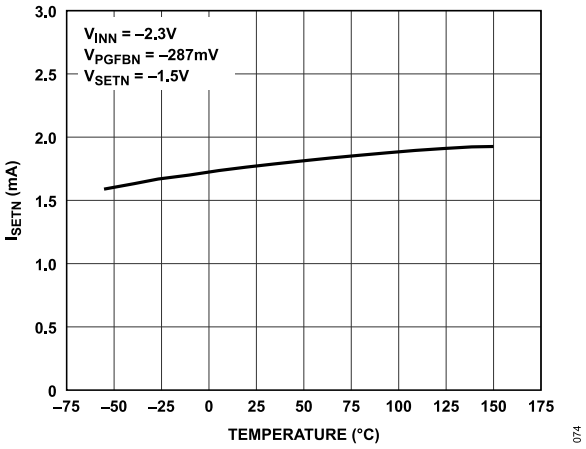

Figure 74. I_{SETN} during Start-Up with Fast Start-Up Enabled vs. Temperature

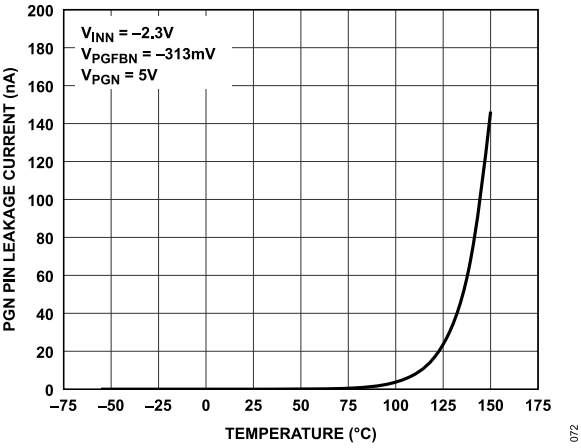

Figure 72. PGN Pin Leakage Current vs. Temperature

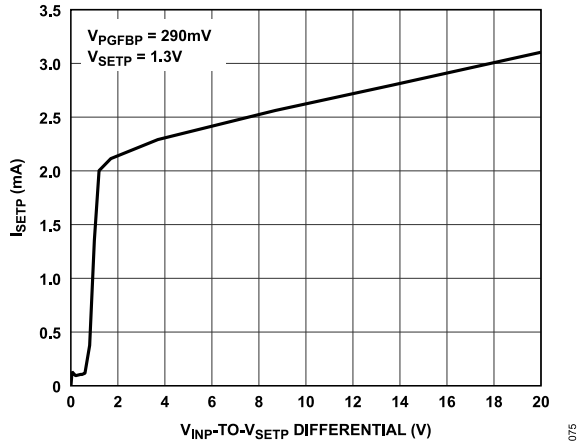

Figure 75. I_{SETP} during Start-Up with Fast Start-Up Enabled vs. V_{INP}-to-V_{SETP} Differential

TYPICAL PERFORMANCE CHARACTERISTICS

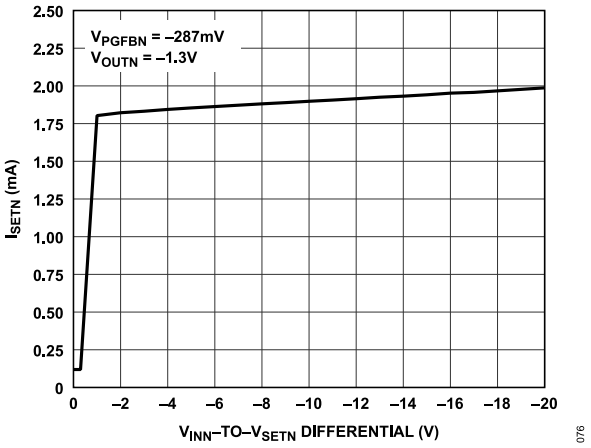

Figure 76. I_{SETN} during Start-Up with Fast Start-Up Enabled vs. V_{INN}-to-V_{SETN} Differential

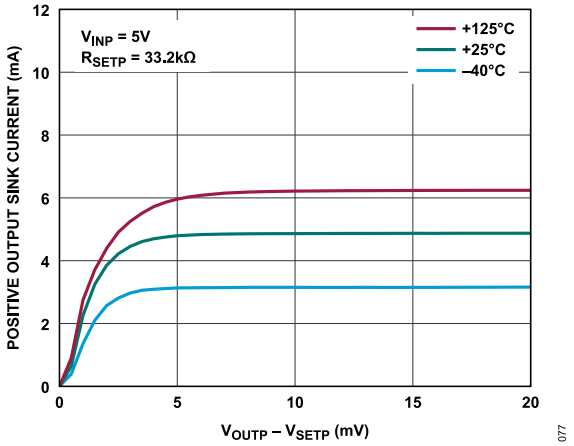

Figure 77. Positive Output Overshoot Recovery Sink Current vs. V_{OUTP} – V_{SETP}

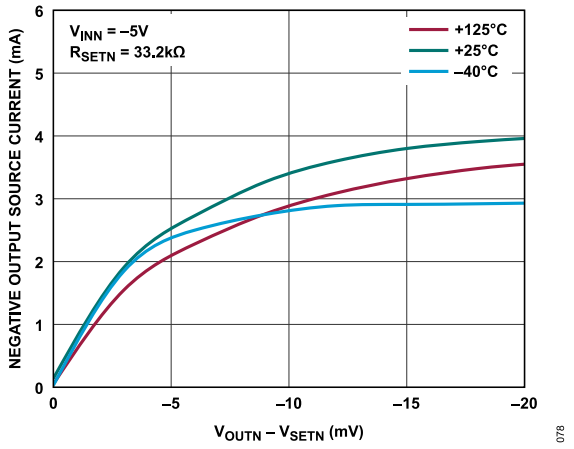

Figure 78. Negative Output Overshoot Recovery Source Current vs. V_{OUTN} – V_{SETN}

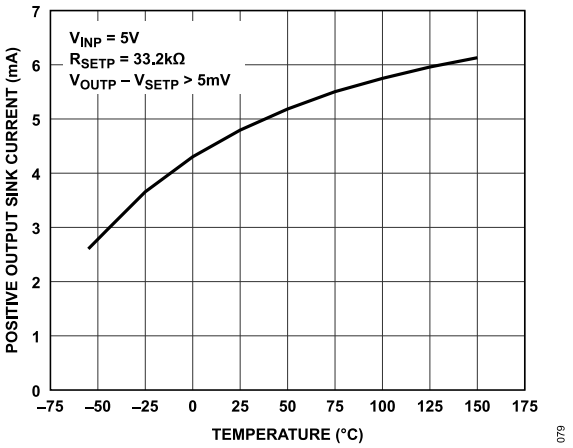

Figure 79. Positive Output Overshoot Recovery Sink Current vs. Temperature

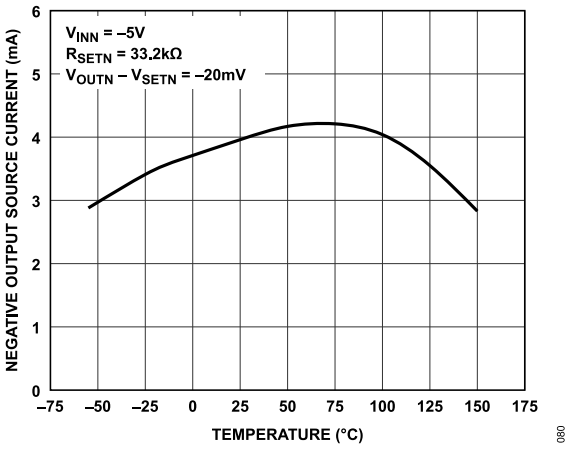

Figure 80. Negative Output Overshoot Recovery Source Current vs. Temperature

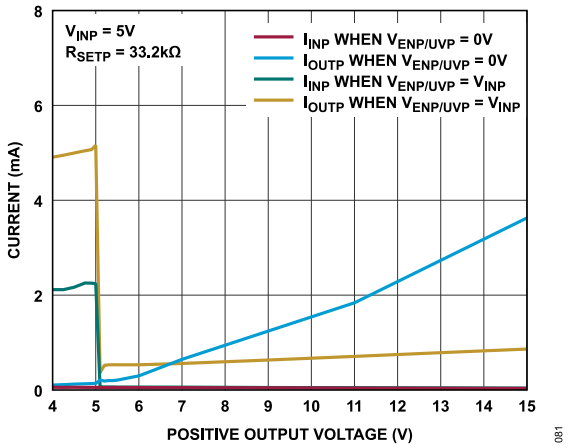

Figure 81. Current when V_{OUTP} Forced above $V_{OUTP(NOMINAL)}$ vs. Positive Output Voltage (I_{INP} is the Positive Input Current, and I_{OUTP} is the Positive Output Current)

TYPICAL PERFORMANCE CHARACTERISTICS

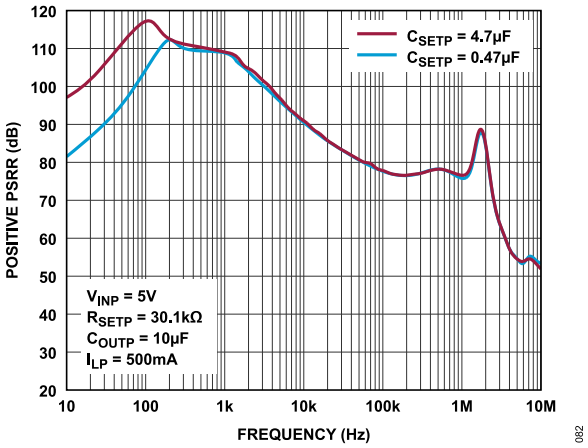

Figure 82. Positive PSRR vs. Frequency (C_{SETP} Steps)

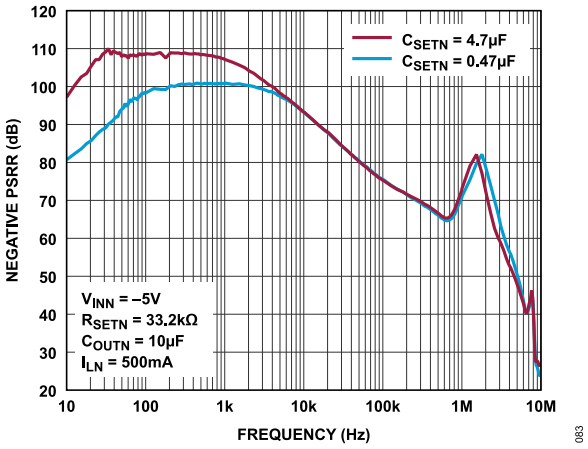

Figure 83. Negative PSRR vs. Frequency (C_{SETN} Steps)

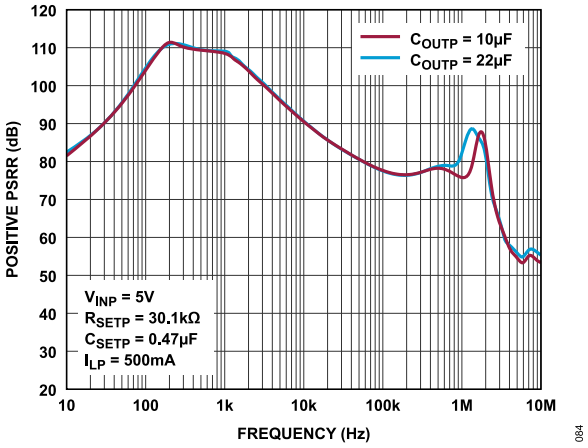

Figure 84. Positive PSRR vs. Frequency (C_{OUTP} Steps)

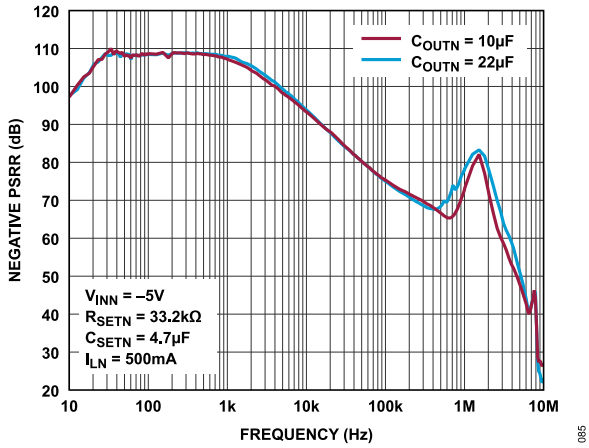

Figure 85. Negative PSRR vs. Frequency (C_{OUTN} Steps)

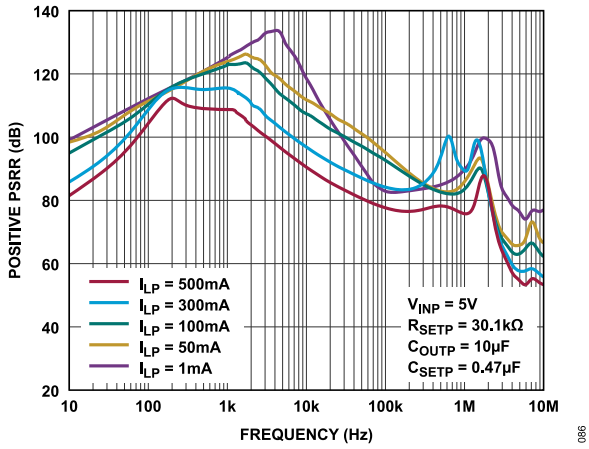

Figure 86. Positive PSRR vs. Frequency (I_{LP} Steps)

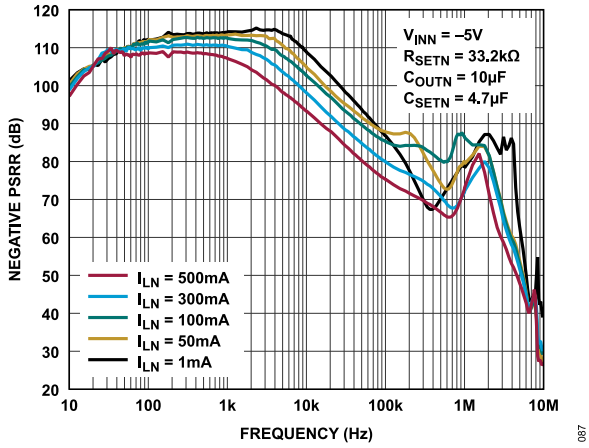

Figure 87. Negative PSRR vs. Frequency (I_{LN} Steps)

TYPICAL PERFORMANCE CHARACTERISTICS

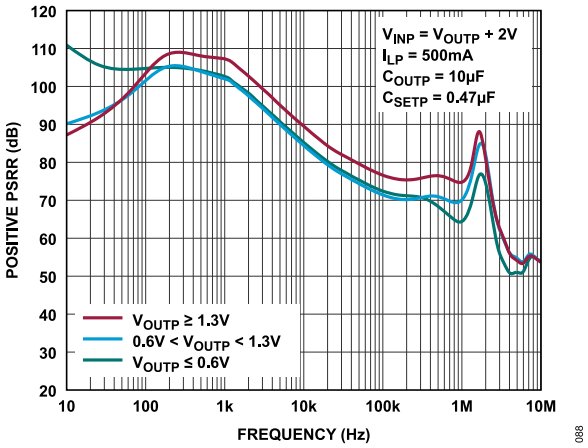

Figure 88. Positive PSRR as a Function of the Positive Error-Amplifier Input Pair vs. Frequency

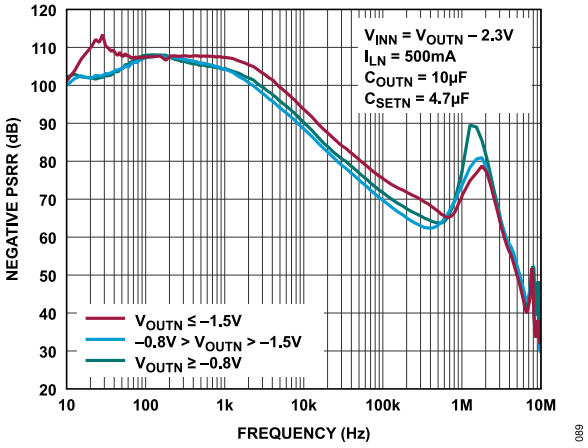

Figure 89. Negative PSRR as a Function of the Negative Error-Amplifier Input Pair vs. Frequency

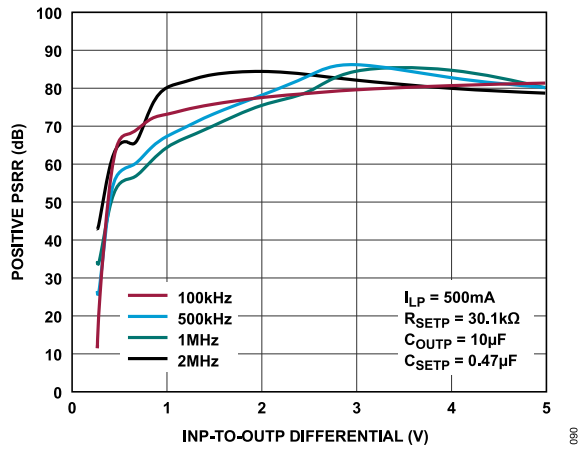

Figure 90. Positive PSRR vs. V_{INP}-to-V_{OUTP} Differential

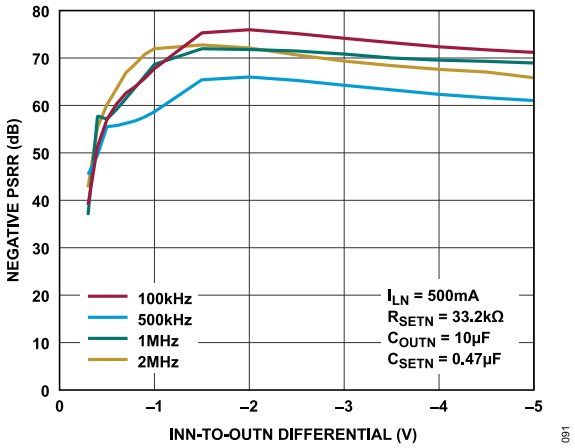

Figure 91. Negative PSRR vs. V_{INN}-to-V_{OUTN} Differential

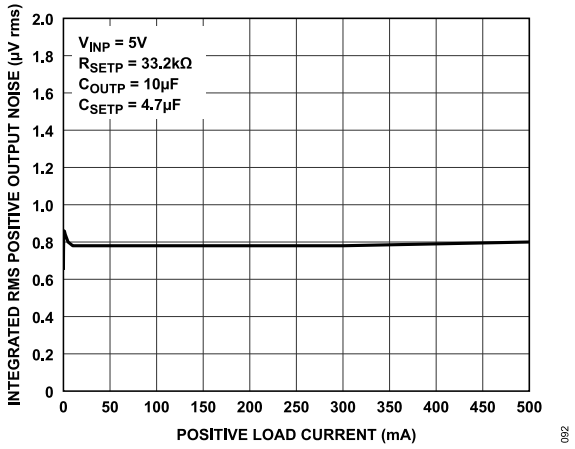

Figure 92. Integrated RMS Positive Output Noise (10 Hz to 100 kHz) vs. Positive Load Current

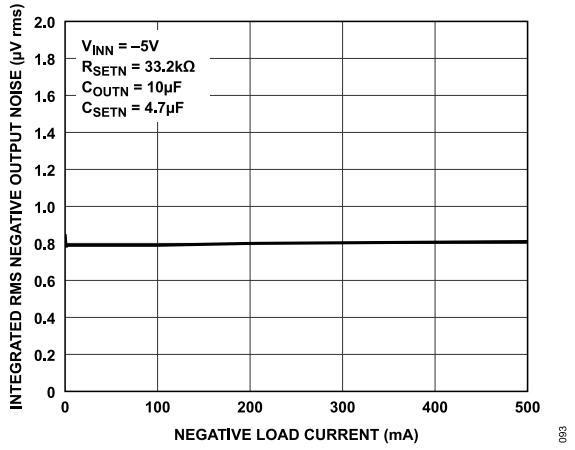

Figure 93. Integrated RMS Negative Output Noise (10 Hz to 100 kHz) vs. Negative Load Current

TYPICAL PERFORMANCE CHARACTERISTICS

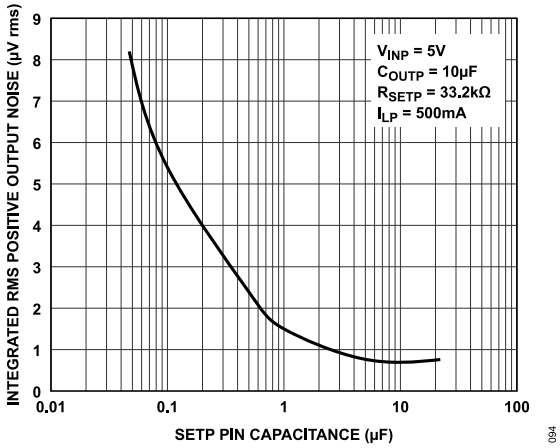

Figure 94. Integrated RMS Positive Output Noise (10 Hz to 100 kHz) vs. SETP Pin Capacitance

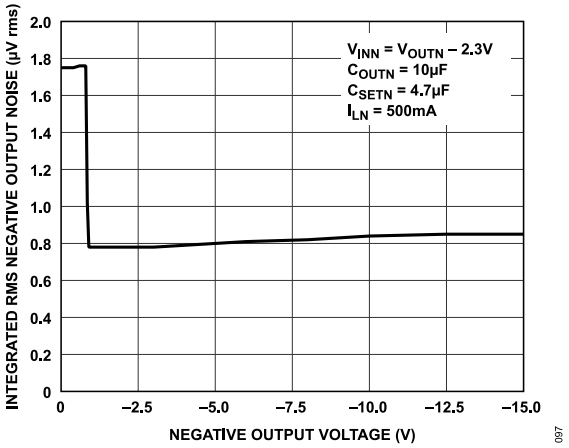

Figure 97. Integrated RMS Negative Output Noise (10 Hz to 100 kHz) vs. Negative Output Voltage

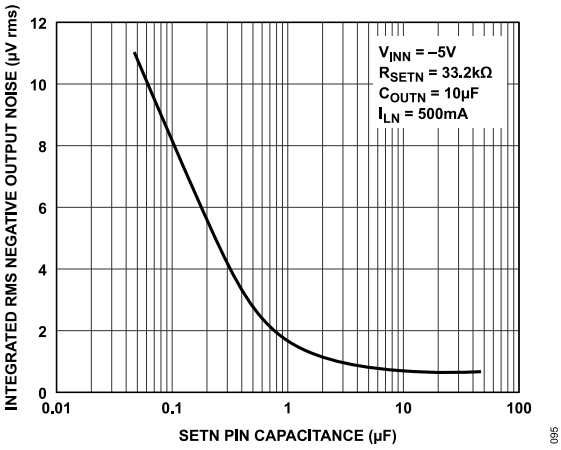

Figure 95. Integrated RMS Negative Output Noise (10 Hz to 100 kHz) vs. SETN Pin Capacitance

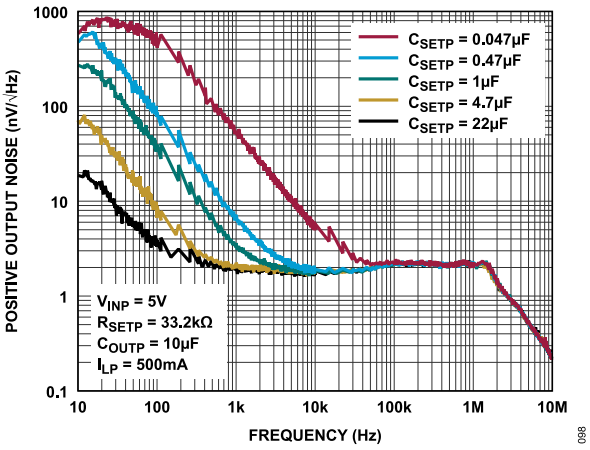

Figure 98. Positive Output Noise vs. Frequency (C_{SETP} Steps)

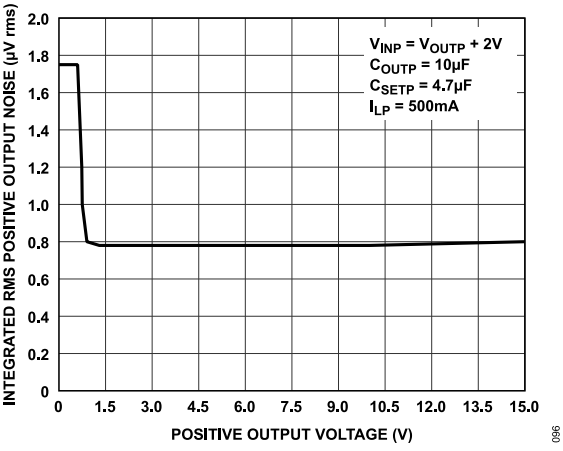

Figure 96. Integrated RMS Positive Output Noise (10 Hz to 100 kHz) vs. Positive Output Voltage

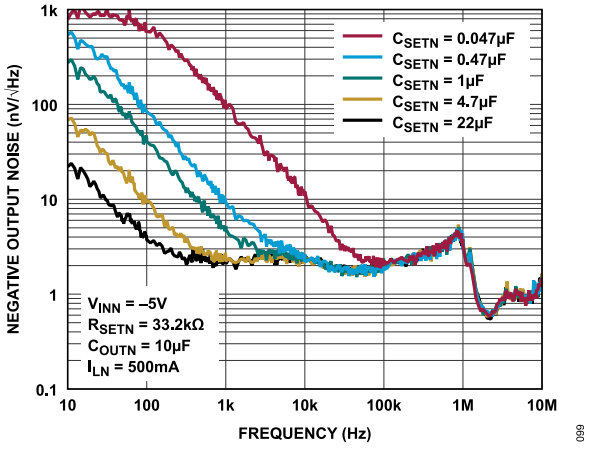

Figure 99. Negative Output Noise vs. Frequency (C_{SETN} Steps)

TYPICAL PERFORMANCE CHARACTERISTICS

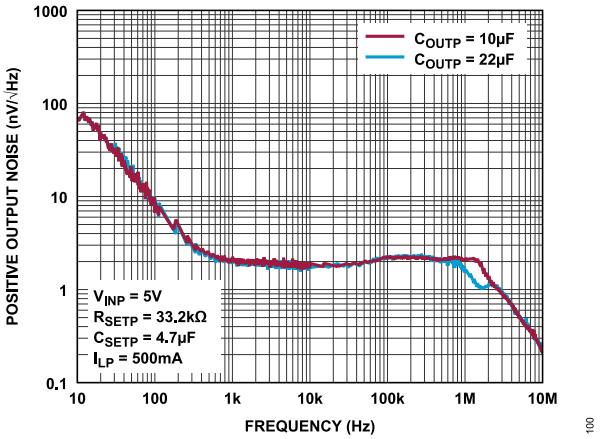

Figure 100. Positive Output Noise vs. Frequency (C_{OUTP} Steps)

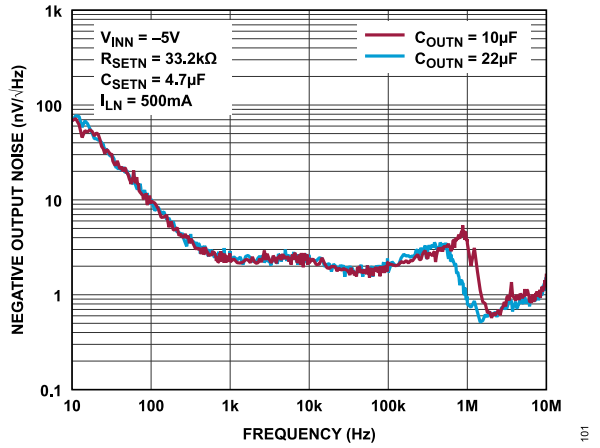

Figure 101. Negative Output Noise vs. Frequency (C_{OUTN} Steps)

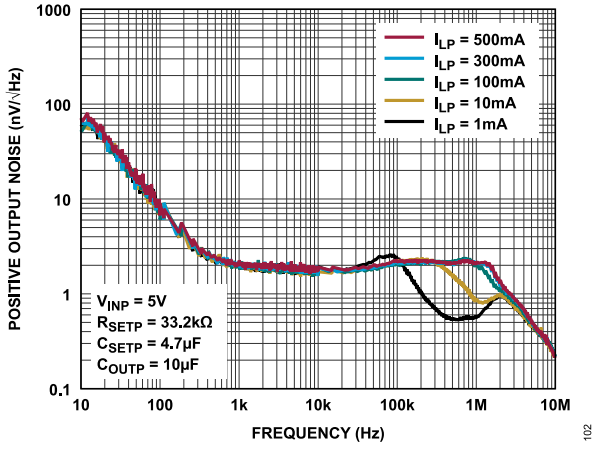

Figure 102. Positive Output Noise vs. Frequency (I_{LP} Steps)

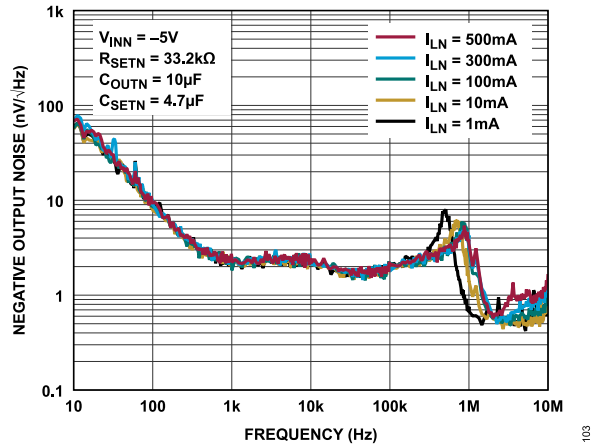

Figure 103. Negative Output Noise vs. Frequency (I_{LN} Steps)

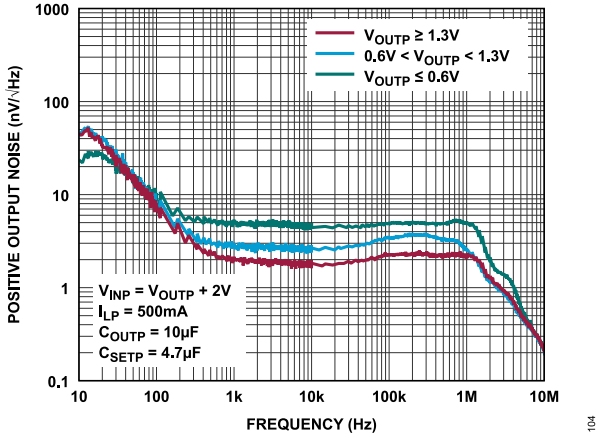

Figure 104. Positive Output Noise as a Function of the Positive Error-Amplifier Input Pair vs. Frequency

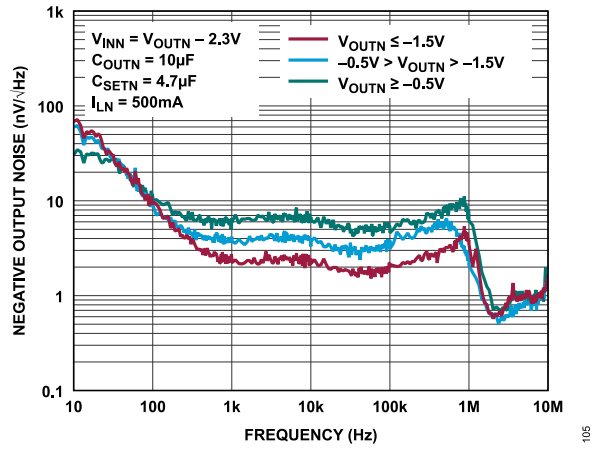

Figure 105. Negative Output Noise as a Function of the Negative Error-Amplifier Input Pair vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

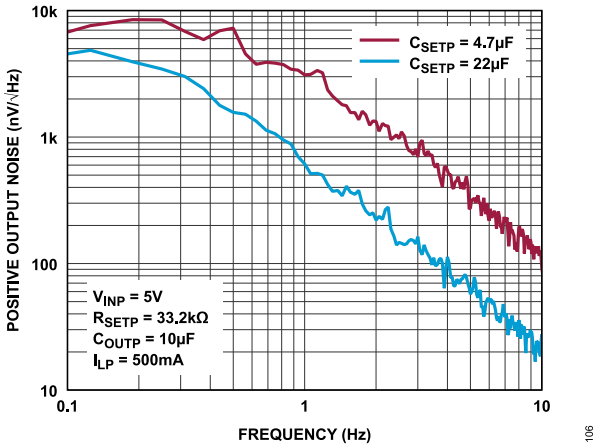

Figure 106. Positive Output Noise (0.1 Hz to 10 Hz) vs. Frequency

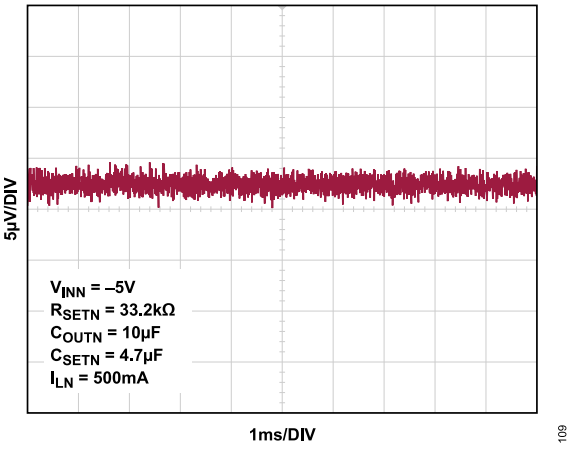

Figure 109. Negative Output Noise: 10 Hz to 100 kHz

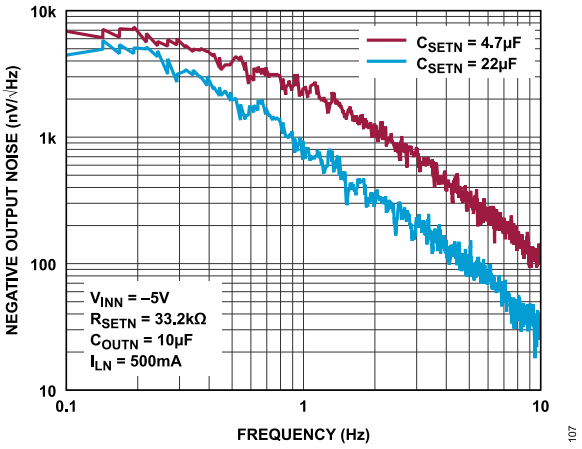

Figure 107. Negative Output Noise (0.1 Hz to 10 Hz) vs. Frequency

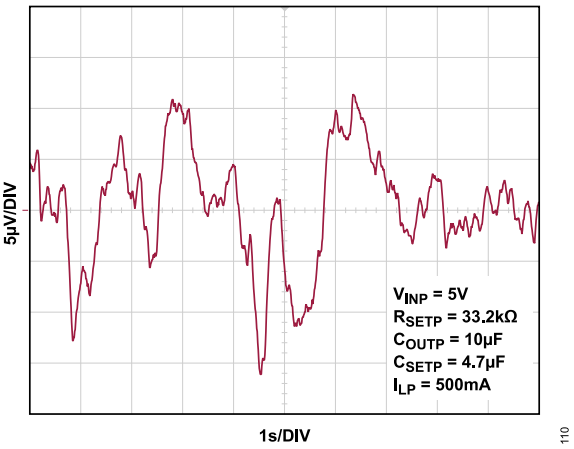

Figure 110. Positive Output Noise: 0.1 Hz to 10 Hz (C_{SETP} = 4.7 µF)

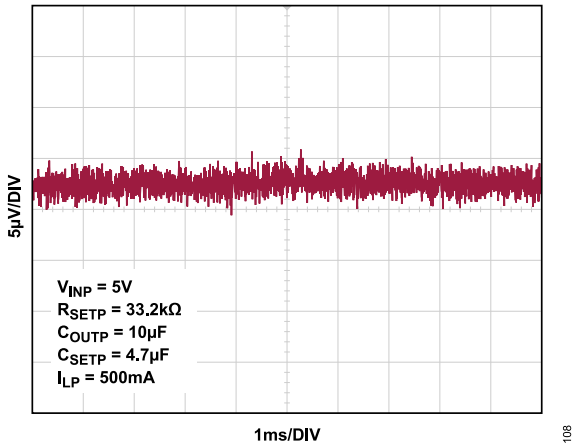

Figure 108. Positive Output Noise: 10 Hz to 100 kHz

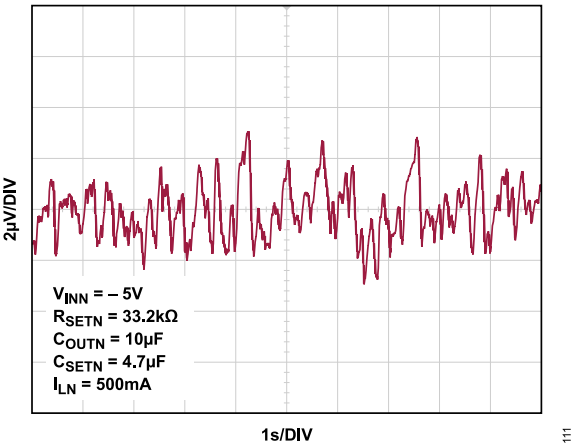

Figure 111. Negative Output Noise: 0.1 Hz to 10 Hz (C_{SETN} = 4.7 µF)

TYPICAL PERFORMANCE CHARACTERISTICS

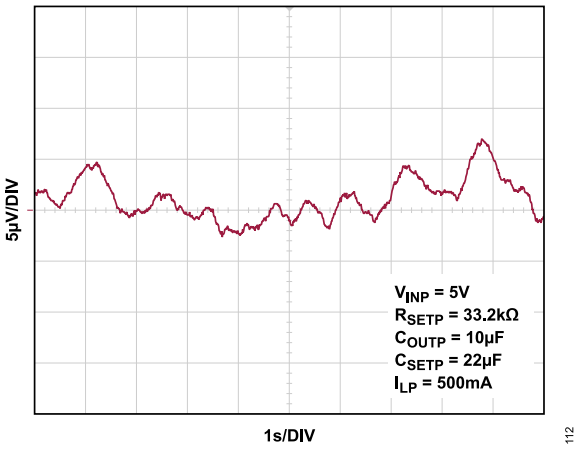

Figure 112. Positive Output Noise: 0.1 Hz to 10 Hz (C_{SETP} = 22 µF)

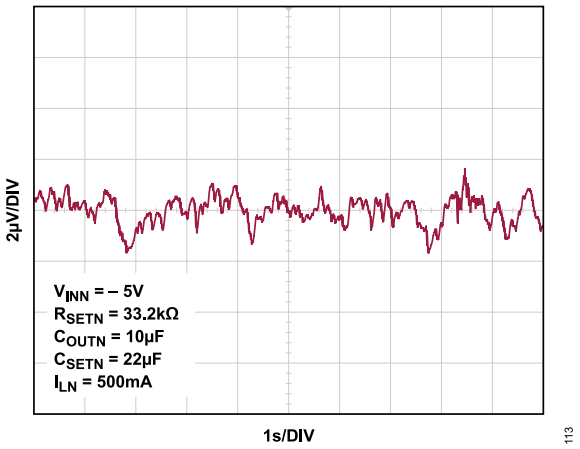

Figure 113. Negative Output Noise: 0.1 Hz to 10 Hz (C_{SETN} = 22 µF)

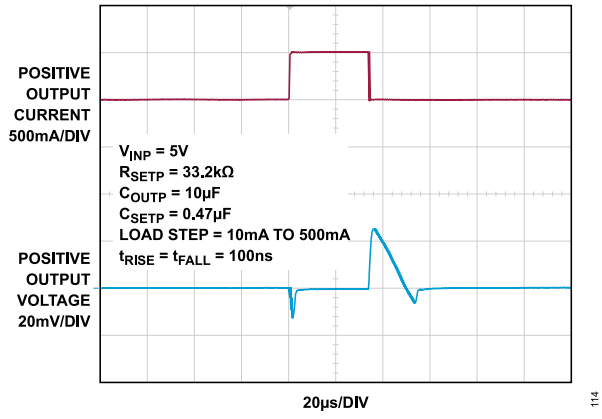

Figure 114. Positive Load-Transient Response

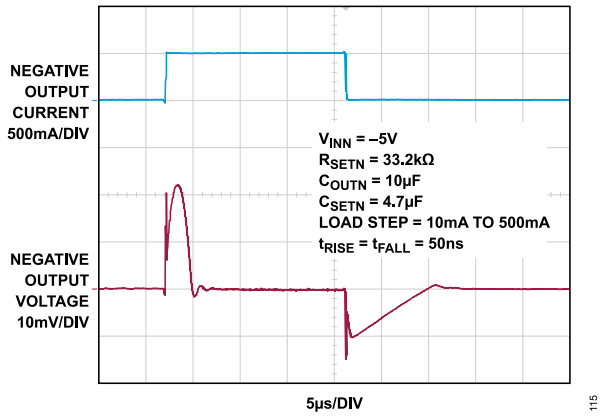

Figure 115. Negative Load-Transient Response

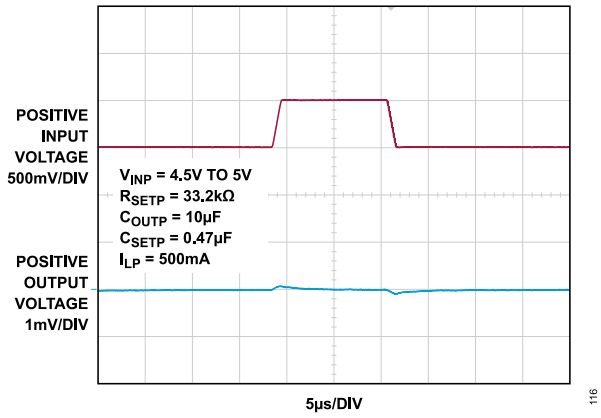

Figure 116. Positive Line-Transient Response

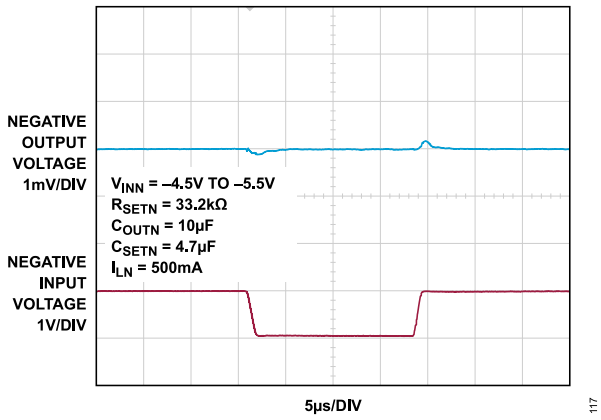

Figure 117. Negative Line-Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS

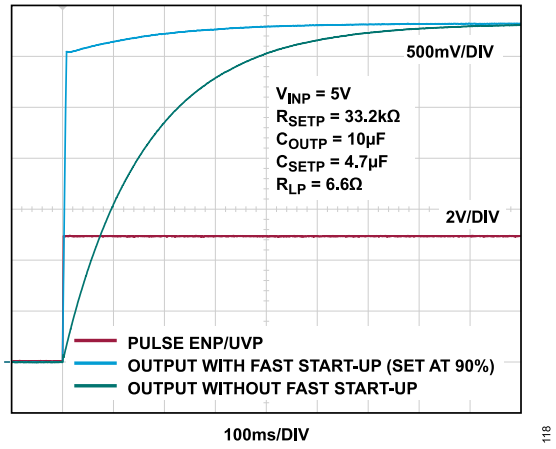

Figure 118. Positive Start-Up Time with and Without Fast Start-Up Circuitry for Large C_{SETP}

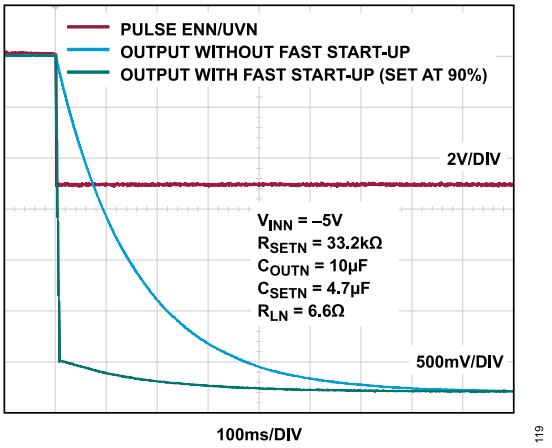

Figure 119. Negative Start-Up Time with and Without Fast Start-Up Circuitry for Large C_{SETN}

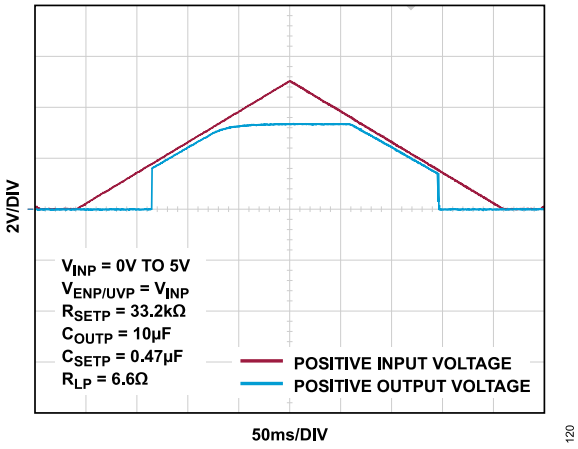

Figure 120. Positive Input Supply Ramp-Up and Ramp-Down

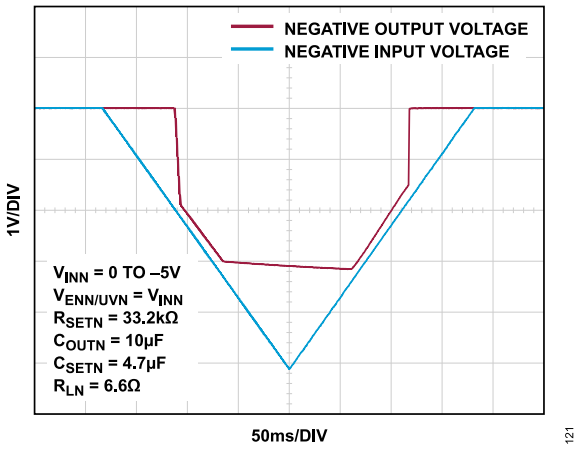

Figure 121. Negative Input Supply Ramp-Up and Ramp-Down

THEORY OF OPERATION

Figure 122 shows the functional block diagram for the positive regulator of the LT3097. Figure 123 shows the functional block diagram for the negative regulator of the LT3097.

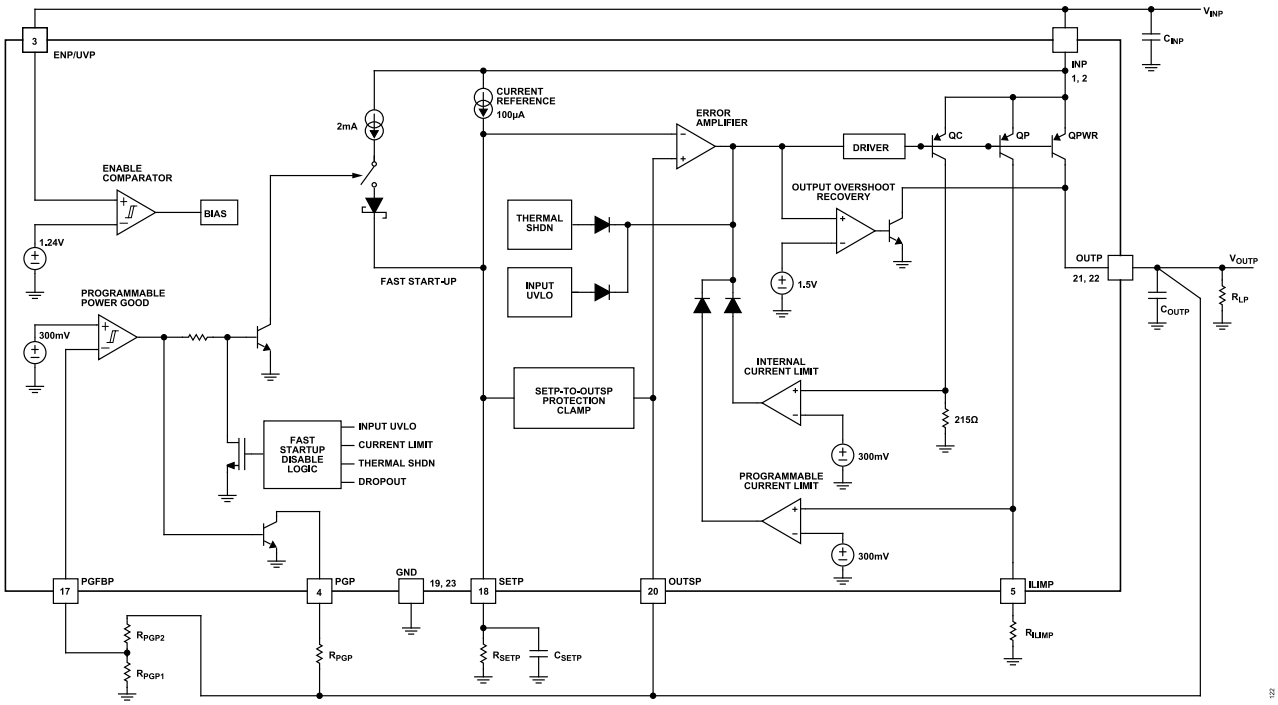

Figure 122. Positive Regulator Functional Block Diagram

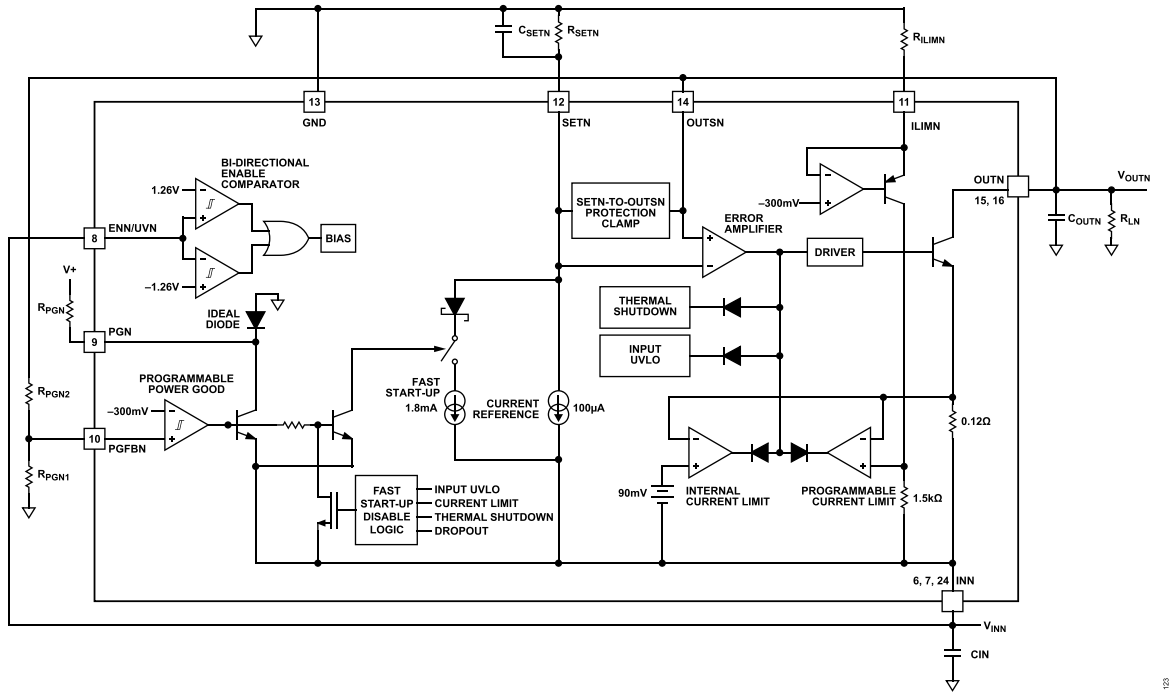

Figure 123. Negative Regulator Functional Block Diagram

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The LT3097 is a dual, positive and negative, high-performance, low-dropout, linear regulator that features Analog Devices, Inc., ultra-low noise and ultra-high PSRR architecture for powering noise-sensitive applications. Designed as a precision-current source followed by a high-performance, rail-to-rail voltage buffer, the LT3097 can provide rail-to-rail output voltages, 0 V to 15 V for the positive output and 0 V to –19.5 V for the negative output. The LT3097 also features a programmable current limit, fast start-up capability, and programmable power good for both positive and negative sides.

The LT3097 is simple to use and incorporates all the protection features expected in high-performance regulators. Short-circuit protection, safe-operating area protection, and thermal shutdown with hysteresis for both positive and negatives sides are included. The positive regulator also includes reverse-battery protection and reverse-current protection.

The LT3097 is available in a thermally enhanced, low-profile 22-lead 6 mm × 3 mm, Plastic DFN package with exposed backside pads for each regulator, providing optimum thermal performance.

OUTPUT VOLTAGE

The LT3097 positive regulator incorporates a precision 100 µA current reference flowing out of the SETP pin, which also connects to the inverting input of the error amplifier of the positive regulator. Similarly, the LT3097 negative regulator incorporates precision 100 µA current reference flowing into the SETN pin, which also connects to the inverting input of the error amplifier of the negative regulator. Figure 124 illustrates that connecting resistors from SETP to the ground and from SETN to the ground generates reference voltages for the respective error amplifiers. These reference voltages are the product of the SETP pin current and the SETP pin resistor for the positive regulator, and the product of the SETN pin current and the SETN pin resistor for the negative regulator. The unity-gain configuration of the error amplifiers produces low-impedance versions of these voltages on the noninverting inputs of the error amplifiers, that are, the OUTSP pin, which is externally connected to the OUTP pin for the positive regulator; and the OUTSN pin, which is externally connected to the OUTN pin for the negative regulator.

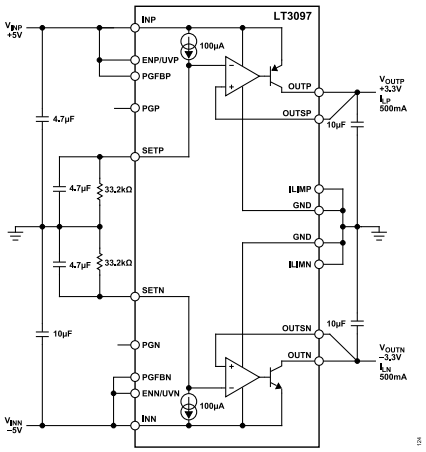

Figure 124. Basic Adjustable Regulator

The rail-to-rail error amplifier and current reference of the positive regulator allow for a wide output voltage range from 0 V (using a 0 Ω resistor) to V_{INP} minus dropout, up to 15 V. A PNP-based input pair is active for a 0 V to 0.6 V output and an NPN-based input pair is active for output voltages greater than 1.3 V, with a smooth transition between the two input pairs from 0.6 V to 1.3 V output. While the NPN-based input pair is designed to offer the best overall performance for the positive regulator, see the Table 1 for details on the offset voltage, SETP pin current, output noise, and PSRR variation with the error-amplifier input pair. The rail-to-rail error amplifier and current reference of the negative regulator allow for a wide output voltage range from 0 V (using a 0 Ω resistor) to V_{INN} minus dropout, up to –19.5 V. An NPN-based input pair is active for a 0 V to –0.8 V output and a PNP-based input pair is active for output voltages less than –1.5 V, with a smooth transition between the two input pairs from –0.8 V to –1.5 V output. While the PNP-based input pair is designed to offer the best overall performance for the negative regulator, see the Table 1 for details on the offset voltage, SETN pin current, output noise, and PSRR variation with the error-amplifier input pair. Table 4 lists many common output voltages and their corresponding 1% R_{SETP} and R_{SETN} resistors.

Table 4. 1% Resistor for Common Output Voltages

R_{SETP}/R_{SETN} (kΩ)	V_{OUTP} (V)	V_{OUTN} (V)
24.9	2.5	–2.5
33.2	3.3	–3.3
49.9	5	–5
121	12	–12
150	15	–15

The benefit of using a current reference compared to the typical voltage reference used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This configuration allows the positive and the negative regulators of the LT3097 to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with output voltage. Moreover, because none of the er-

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ror-amplifier gain is needed to amplify the SETP/SETN pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Because the zero temperature-coefficient current source is highly accurate, the SETP/SETN pin resistor can become a limiting factor in achieving high accuracy. Therefore, the SETP/SETN pin resistor must be a precision resistor. Additionally, any leakage paths to or from the SETP/SETN pin create errors in the output voltage. Use high-quality insulation (for example, Teflon or Kel-F) if necessary. Moreover, cleaning of all insulating surfaces to remove fluxes and other residues can be required. High-humidity environments can require a surface coating at the SETP/SETN pin to provide a moisture barrier.

Minimize board leakage by encircling the SETP/SETN pin with a guard ring that operates at a potential close to itself, ideally connected to the OUTP/OUTN pins. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard-ring width. Leakages of 100 nA into or out of the SETP/SETN pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. Figure 125 illustrates a typical guard-ring layout technique.

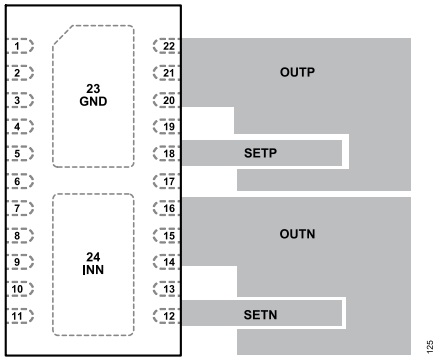

Figure 125. Guard Ring Layout

Because the SETP/SETN pin is a high-impedance node, unwanted signals can couple into the SETP/SETN pin and cause erratic behavior, which is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SETP/SETN pin with a small capacitance to ground resolves this issue, 10 nF is sufficient. For applications requiring higher accuracy or an adjustable output voltage, the SETP/SETN pin can be actively driven by an external voltage source capable of sinking/sourcing 100 µA. Connecting a precision-voltage reference to the SETP/SETN pin eliminates any errors in the output voltage due to the reference current and SETP/SETN pin resistor tolerances.

OUTPUT SENSING AND STABILITY

The OUTSP/OUTSN pin of the LT3097 provides a Kelvin-sense connection to the output. The GND side of the SETP/SETN pin resistor provides a Kelvin-sense connection to the GND side of the load.

Additionally, for ultra-high PSRR, the LT3097 bandwidth of the positive and negative regulator is made quite high (~1 MHz), making it close to the self-resonance frequency (~1.6 MHz) of a typical 10 µF (1206 case size), ceramic-output capacitor. Therefore, avoiding adding extra impedance (ESR and ESL) outside the feedback loop is important. To that end, as shown in Figure 126, minimize the effects of PCB trace and solder inductance by connecting the OUTSP/OUTSN pin directly to C_{OUTP}/C_{OUTN} and the GND side of C_{SETP}/C_{SETN} directly to the GND side of C_{OUTP}/C_{OUTN}, as well as keeping the GND sides of C_{INP}/C_{INN} and C_{OUTP}/C_{OUTN} reasonably close. Refer to the LT3097 evaluation board user guide (EVAL-LT3097-AZ) for more information on the recommended layout that meets these requirements. While the LT3097 is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase and gain margin, noise, and PSRR performance can degrade.

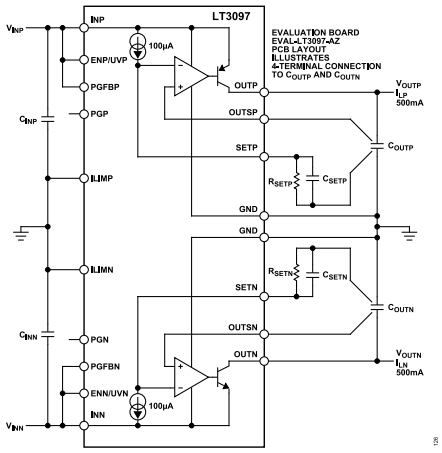

Figure 126. C_{OUTP}/C_{OUTN} and C_{SETP}/C_{SETN} Connections for Best Performance

STABILITY AND OUTPUT CAPACITANCE

The LT3097 requires an output capacitor for stability. Given its high bandwidth, Analog Devices, Inc., recommends low ESR and ESL ceramic capacitors. For the positive regulator, a minimum of 10 µF capacitance with an ESR of less than 20 mΩ and an ESL of less than 2 nH is required for stability. For the negative regulator, a minimum of 10 µF capacitance with an ESR of less than 30 mΩ and an ESL of less than 1.5 nH is required for stability.

Given the high PSRR and low-noise performance attained using a single 10 µF ceramic-output capacitor, larger values of output capacitor only marginally improve the performance because the regulator bandwidth decreases with increasing output capacitance — hence, there is little to be gained by using larger than the minimum 10µF output capacitor. Nonetheless, larger values of out-

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put capacitance do decrease peak output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3097 increase the effective output capacitance.

Give extra consideration to the type of ceramic capacitors used. The capacitors are manufactured with a variety of dielectrics, each with different behaviors across temperature and applied voltage. The most common dielectrics used are specified with Electronic Industries Alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in the small packages, but these dielectrics tend to have stronger voltage and temperature coefficients, as shown in Figure 127 and Figure 128. When used with a 5 V regulator, a 16 V, 10 µF Y5V capacitor can exhibit an effective value as low as 1 µF to 3 µF for the DC bias voltage applied over the operating temperature range.

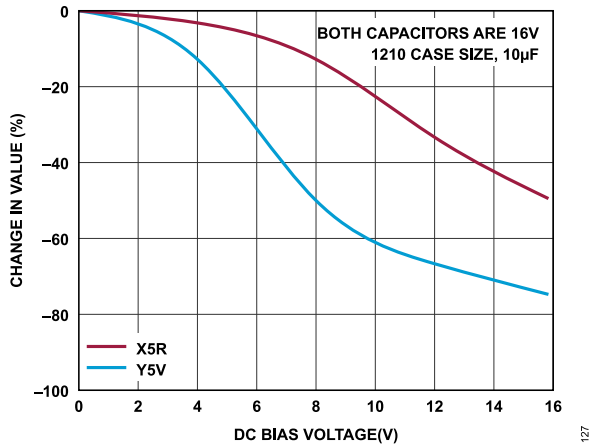

Figure 127. Ceramic Capacitor DC Bias Characteristics

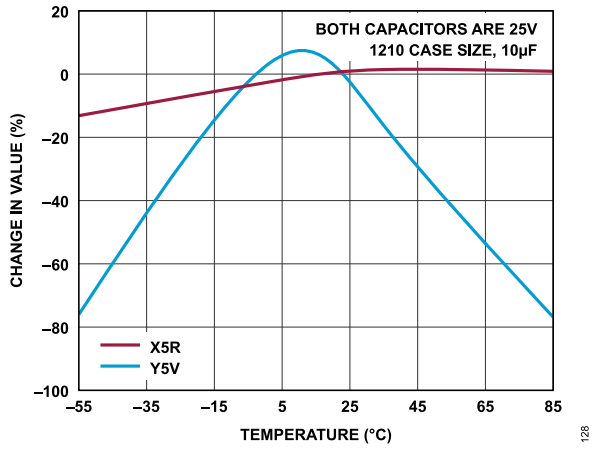

Figure 128. Ceramic Capacitor Temperature Characteristics

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for the LT3097. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify the operating temperature range and the maximum capacitance change over temperature. While capacitance changes due to DC bias for X5R and X7R are better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in Figure 129, capacitor DC bias characteristics tend to improve as component case size increases. However, verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, Analog Devices, Inc., recommends using the Murata GCM series ceramic capacitors.

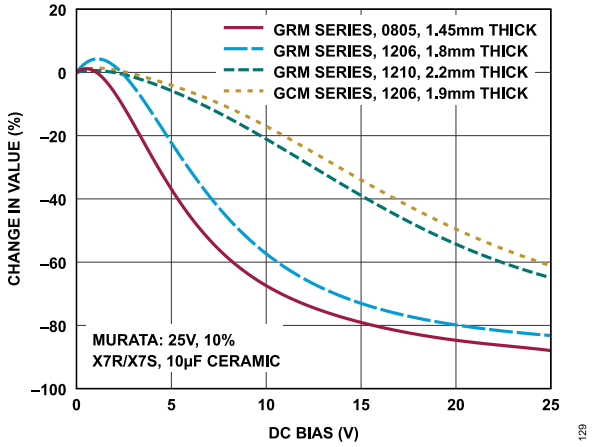

Figure 129. Capacitor Voltage Coefficient for Different Case Sizes

HIGH VIBRATION ENVIRONMENTS

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3097 applications in high-vibration environments have three distinct, piezoelectric noise generators: ceramic output, input, and SETP/SETN pin capacitors. However, due to the low output impedance over a wide frequency range of the LT3097, negligible output noise is generated using a ceramic-output capacitor. Similarly, due to the ultrahigh PSRR of the LT3097, negligible output noise is generated using a ceramic-input capacitor. Nonetheless, given the high SETP/SETN pin impedance, any piezoelectric response from a ceramic SETP/SETN pin capacitor generates significant output noise, and peak-to-peak excursions of hundreds of mV. However, due to the high ESR and ESL tolerance of the SETP/SETN pin capacitor, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SETP/SETN pin, although electrolytic capacitors tend to have high 1/f noise. In any case, the use of a surface-mount capacitor is highly recommended.

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STABILITY AND INPUT CAPACITANCE

The LT3097 is stable with a minimum 4.7 µF INP pin capacitor for the positive regulator and 10 µF INN pin capacitor for the negative regulator. Analog Devices, Inc., recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the input and ground terminals of the LT3097, the use of low-value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause of this instability and not the LT3097.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465 nH of self-inductance.

Several methods exist to reduce the self-inductance of a wire. One method divides the current flowing toward the LT3097 between the two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connect two equal inductors in parallel. However, when placed close to each other, their mutual inductance adds to the overall self-inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) close. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted close powers the LT3097, a 4.7 µF/10 µF input capacitor suffices for stability for the positive/negative regulator. However, if a distantly located supply powers the LT3097, use a larger value input capacitor. Use a rough guideline of 1 µF (in addition to the 4.7 µF/10 µF minimum) per 6" of wire length. The minimum input capacitance required to stabilize the application also varies with the output capacitance as well as the load current. Place additional capacitance on the output of the LT3097 to help with this issue. However, this approach requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the input of the LT3097 also helps stabilize the application; as little as 0.1 Ω to 0.5 Ω suffices. This impedance dampens the LC tank circuit at the expense of the dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the input of the LT3097 in parallel with a 4.7 µF/10 µF ceramic capacitor for the positive/negative regulator.

PSRR AND INPUT CAPACITANCE

For applications using the LT3097 for post-regulating switching converters, placing a capacitor directly at the input of the LT3097 results in AC current (at the switching frequency) flowing near the LT3097. This relatively high-frequency switching current generates a magnetic field that couples to the output of the LT3097, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, and the input capacitance, among other factors, the PSRR degradation can easily be more than 30 dB at 1 MHz. This degradation is present even if the LT3097 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional, low PSRR, LDO regulators, the ultra-high PSRR of the LT3097 requires careful attention to higher-order parasitics to extract the full performance offered by the regulator.

To mitigate the flow of the high-frequency switching current near the LT3097, as long as the output capacitor of the switching converter is located more than an inch away from the LT3097, remove the input capacitor of the LT3097. Magnetic coupling rapidly decreases with increasing distance. Nonetheless, if the switching preregulator is placed too far away (conservatively more than a couple of inches) from the LT3097, with no input capacitor present, as with any regulator, the input of the LT3097 oscillates at the parasitic LC resonance frequency. In addition, it is generally a common (and preferred) practice to bypass the regulator input with some capacitance. Therefore, this option is fairly limited in its scope and not the most palatable solution.

To that end, Analog Devices, Inc., recommends using the LT3097 demonstration board layout for achieving the best possible PSRR performance. For more details refer to the LT3097 evaluation board user guide (EVAL-LT3097-AZ. The LT3097 evaluation board layout uses magnetic-field cancellation techniques to prevent PSRR degradation caused by this high-frequency current flow, while using the input capacitor.

FILTERING HIGH-FREQUENCY SPIKES

For applications where the LT3097 is used to post-regulate a switching converter, its high PSRR effectively suppresses any noise present at the switching frequency of the switching converter, typically 100 kHz to 4 MHz. However, the high-frequency (hundreds of MHz) spikes, beyond the bandwidth of the LT3097, associated with the power-switch transition times of the switching converter almost directly pass through the LT3097. While the output capacitor is intended partly to absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or even the inductance associated with a short (for example, 0.5”) PCB trace between the output of the switching converter and the input of the LT3097 can serve as an LC filter to suppress these high-frequency spikes.

OUTPUT NOISE

The LT3097 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor-divider network used for setting the output voltage, and the noise gain created by this resistor-divider. Many low-noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

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Unlike most linear regulators, the LT3097 does not use a voltage reference. Instead, the LT3097 uses a 100 µA current reference each for the positive regulator and the negative regulator. The current reference of the positive regulator operates with a typical noise-current level of 20 pA/√Hz (6 nA rms over a 10 Hz to 100 kHz bandwidth). The resultant positive voltage noise equals the current noise multiplied by the SETP resistor value, which, in turn, is RMS summed with the noise of the error amplifier of the positive regulator and the thermal noise of the SETP resistor, $\sqrt{4kTR_{SETP}}$, where k = Boltzmann's constant (1.380649×10^{-23}J/K), and T is the absolute temperature. The current reference of the negative regulator operates with a typical noise-current level of 27 pA/√Hz (8 nA rms over a 10 Hz to 100 kHz bandwidth). The resultant negative voltage noise equals the current noise multiplied by the SETN resistor value, which, in turn, is RMS summed with the noise of the error amplifier of the negative regulator and the thermal noise of the SETN resistor, $\sqrt{4kTR_{SETN}}$, where k = Boltzmann's constant (1.380649×10^{-23}J/K), and T is the absolute temperature.

One problem that conventional linear regulators face is that the resistor-divider setting the output voltage gains up the reference noise. In contrast, the unity-gain follower architecture of the LT3097 presents no gain from the SETP/SETN pin to the positive/negative output. Therefore, if a capacitor bypasses the SETP/SETN pin resistor, the positive/negative output noise is independent of the programmed positive/negative output voltage. The resultant positive output noise is set just by the noise of the error amplifier of the positive regulator, typically 2 nV/√Hz from a 10 kHz to 1 MHz bandwidth and 0.8 µV rms from a 10 Hz to 100 kHz bandwidth using a 4.7 µF SETP pin capacitor. The resultant negative output noise is set just by the noise of the error amplifier of the negative regulator, typically 2.2 nV/√Hz from a 10 kHz to 1 MHz bandwidth and 0.8 µV rms from a 10 Hz to 100 kHz bandwidth using a 4.7 µF SETN pin capacitor.

See the Figure 92, Figure 93, Figure 94, Figure 95, Figure 98, Figure 99, Figure 102, Figure 103, Figure 106, and Figure 107 for the noise spectral density (for the 10 Hz to 10 MHz frequency range and for the 0.1 Hz to 10 Hz 1/f noise frequency range) and RMS integrated noise over various load currents and SET pin capacitance information.

SETP/SETN PIN (BYPASS) CAPACITANCE: NOISE, PSRR, TRANSIENT RESPONSE, AND SOFT-START

In addition to reducing output noise, using a SETP/SETN pin bypass capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the DC regulation of the LT3097. Capacitor leakage of even 100 nA is a 0.1% DC error. Therefore, Analog Devices, Inc., recommends using a good quality, low-leakage ceramic capacitor.

Using a SETP/SETN pin bypass capacitor also soft starts the output and limits inrush current. The RC time constant, formed by the SETP/SETN pin resistor and capacitor, controls the soft-start time. The ramp-up rate from 0% to 90% of nominal VOUT is the following:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \quad (Fast \quad Start-Up \quad Disabled) \tag{1}$$

FAST STARTUP

For ultra-low noise applications that require low 1/f noise (that is, at frequencies below 100 Hz), a larger value, SETP/SETN pin capacitor is required of up to 22 µF. Typically, this larger value significantly increases the start-up time of the regulator. However, the LT3097 incorporates fast start-up circuitry that increases the SETP/SETN pin current to approximately 2 mA/1.8 mA during startup.

As shown in the Figure 122/Figure 123, the 2 mA/1.8 mA current source remains engaged while PGFBP/PGFBN is less than 300 mV/-300 mV, unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is less than the minimum V_{INP}/V_{INN}.

If the fast start-up capability is not used, connect PGFBP/PGFBN to INP/INN or to OUTP/OUTN for output voltages more than 300 mV/-300 mV, and note that this also disables the power-good functionality.

See the Positive Regulator Programmable Power Good and Negative Regulator Programmable Power Good sections for more information.

ENP/UVP

The ENP/UVP pin is used to put the positive regulator into a micropower shutdown state. The positive regulator of the LT3097 has an accurate 1.24 V turn-on threshold on the ENP/UVP pin with 130 mV of hysteresis. This threshold can be used with a resistor-divider from the positive input supply to define an accurate UVLO threshold for the positive regulator, as shown in the Figure 131. The ENP/UVP pin current ($I_{ENP/UVP}$) at the threshold from Table 1 must be considered when calculating the resistor-divider network as follows:

$$V_{INP\,(UVLO)} = 1.24 \quad V \times \left(1 + \frac{R_{ENP2}}{R_{ENP1}}\right) + I_{ENP/UVP} \times R_{ENP2} \tag{2}$$

Where:
R_{ENP1} and R_{ENP2} are the resistors from the ENP/UVP pin to GND and the ENP/UVP pin to INP, respectively.
$I_{ENP/UVP}$ can be ignored if R_{ENP1} is less than 100 kΩ. If unused, connect the ENP/UVP pin to INP.

ENN/UVN

The ENN/UVN pin is used to put the negative regulator into a micropower shutdown state. The negative regulator of the LT3097 has an accurate -1.26 V turn-on threshold on the ENN/UVN pin with 215 mV of hysteresis. This threshold can be used with a resistor-divider from the negative input supply to define an accurate UVLO

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threshold for the negative regulator as illustrated in the Figure 131. The ENN/UVN pin current ($I_{ENN/UVN}$) at the threshold from Table 1 must be considered when calculating the resistor-divider network as follows:

$$V_{INN\ (UVLO)} = -1.26\ \ V \times \left(1 + \frac{R_{ENN2}}{R_{ENN1}}\right) - I_{ENN/UVN} \times R_{ENN2} \quad (3)$$

where:
R_{ENN1} and R_{ENN2} are the resistors from the ENN/UVN pin to GND and the ENN/UVN pin to INN, respectively.
$I_{ENN/UVN}$ can be ignored if R_{ENN1} is less than 100 kΩ. If unused, connect the ENP/UVP pin to INP.

Since the ENN/UVN pin is bidirectional, it can also be pulled more than 1.26V to turn on the negative regulator of the LT3097. In bipolar supply applications, the positive ENN/UVN threshold can be used to sequence the turn-on of the negative regulator of the LT3097 after the positive regulator of the LT3097 has turned on. If unused, connect the ENN/UVN pin to INN.

POSITIVE REGULATOR PROGRAMMABLE POWER GOOD

As shown in the Figure 122 and discussed in the Fast Startup section, the positive side power-good threshold is user-programmable using the ratio of two external resistors, R_{PGP1} and R_{PGP2}:

$$V_{OUTP(PG\_THRESHOLD)} = 0.3V \times \left(1 + \frac{R_{PGP2}}{R_{PGP1}}\right) + I_{PGFBP} \times R_{PGP2} \quad (4)$$

If the PGFBP pin increases to more than 300 mV, the open-collector PGP pin deasserts and becomes high impedance. The power-good comparator has 7 mV hysteresis and 5 µs of deglitching. The I_{PGFBP} from Table 1 must be considered when determining the resistor-divider network. The I_{PGFBP} can be ignored if R_{PGP1} is less than 30 kΩ. If the power-good functionality is not used, float the PGP pin. Note that programmable power good and fast start-up capabilities are disabled for positive output voltages less than 300 mV.

The power-good functionality is disabled in shutdown, i.e. when ENP/UVP is set to 0V. If power-good functionality is desired in shutdown, connect the power-good resistor (i.e. R_{PGP} in the Figure 122) between the PGP pin and either the ENP/UVP pin or OUTP pin.

NEGATIVE REGULATOR PROGRAMMABLE POWER GOOD

As shown in the Figure 123 and discussed in the Fast Startup section, the negative side power-good threshold is user-programmable using the ratio of two external resistors, R_{PGN1} and R_{PGN2}:

$$V_{OUTN(PG\_THRESHOLD)} = -0.3V \times \left(1 + \frac{R_{PGN2}}{R_{PGN1}}\right) - I_{PGFBN} \times R_{PGN2} \quad (5)$$

If the PGFBN pin decreases to less than −300 mV, the open-collector PGN pin deasserts and becomes high impedance. The power-good comparator has 7 mV hysteresis and 5 µs of deglitching. The I_{PGFBN} from Table 1 must be considered when determining the resistor-divider network. The I_{PGFBN} can be ignored if R_{PGP1} is less than 30 kΩ. If the power-good functionality is not used, float the PGN pin. Note that programmable power good and fast start-up capabilities are disabled for negative output voltages between 0 V and −300 mV.

Take care when laying out traces for PGN and PGFBN on a PCB. If the PGN and PGFBN pins are run close to each other for a distance (typically greater than two inches), stray capacitance from trace-to-trace couples the PGN signal into the high-impedance PGFBN signal. Since PGN is out of phase relative to PGFBN, this results in oscillation. To avoid this, minimize the distance the two traces run close to each other; lowering the impedance seen at the PGFBN pin by using lower value resistors for the PGFBN divider also helps.

POSITIVE REGULATOR EXTERNALLY PROGRAMMABLE CURRENT LIMIT

The current-limit threshold of the ILIMP pin is 300 mV. Connecting a resistor from ILIMP to GND sets the maximum current flowing out of the ILIMP pin, which, in turn, programs the current limit of the positive regulator of the LT3097. With a 150 mA × kΩ programming scale factor, calculate the current limit as follows:

$$Positive\ \ Side\ \ Current\ \ Limit = \frac{150\ \ mA \times k\Omega}{R_{ILIMP}} \quad (6)$$

For example, a 1 kΩ resistor programs the current limit to 150 mA, and a 2 kΩ resistor programs the current limit to 75 mA. For good accuracy, Kelvin connect this resistor to the GND pin (pin 19) of the LT3097.

When the INP-to-OUTP differential is greater than 12 V, the foldback circuitry of the positive regulator of the LT3097 decreases the internal current limit. As a result, the internal current limit can override the externally programmed current-limit level to keep the LT3097 within its safe-operating area (SOA). See Figure 56.

As shown in the Figure 122, the ILIMP pin sources current proportional (1:500) to the output current; therefore, it also serves as a current monitoring pin with a 0 V to 300 mV range. If external current limit or current monitoring is not used, connect ILIMP to GND.

NEGATIVE REGULATOR EXTERNALLY PROGRAMMABLE CURRENT LIMIT

The ILIMN pin internally regulates to −300 mV. Connecting a resistor from GND to ILIMN sets the current flowing into the ILIMN pin, which, in turn, programs the current limit of the negative regulator of the LT3097. With a 3.75 A × kΩ programming scale factor, calculate the current limit as follows:

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$$Negative\ \ Side\ \ Current\ \ Limit = \frac{3.75\ \ A \times k\Omega}{R_{ILIMN}} \quad (7)$$

For example, a 7.5 kΩ resistor programs the current limit to 500 mA, and a 15 kΩ resistor programs the current limit to 250 mA. For good accuracy, Kelvin connect this resistor to the GND pin (pin 13) of the LT3097.

When the INN-to-OUTN differential is greater than 7 V, the foldback circuitry of the negative regulator of the LT3097 decreases the internal current limit. As a result, the internal current limit can override the externally programmed current-limit level to keep the LT3097 within its SOA. See Figure 57.

ILIMN is not designed to serve as a current monitoring pin. If the external current limit is not used, connect ILIMN to GND.

POSITIVE OUTPUT OVERSHOOT RECOVERY

During a load-step change from full load to no load (or light load), the positive output voltage overshoots before the regulator responds to turn the power transistor off. Given that there is no load (or a light load) present at the positive output, it takes a long time to discharge the output capacitor.

As shown in the Figure 122, the LT3097 incorporates an overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event OUTSP is higher than SETP. This current is typically about 4 mA. No load recovery is disabled for positive input voltages less than 2.5 V or positive output voltages less than 1.5 V.

If OUTSP is externally held more than SETP, the current sink turns on in an attempt to restore OUTSP to its programmed voltage. The current sink remains on until the external circuitry releases OUTSP.

NEGATIVE OUTPUT OVERSHOOT RECOVERY

During a load-step change from full load to no load (or light load), the negative output voltage overshoots before the regulator responds to turn the power transistor off. Given that there is no load (or a light load) present at the negative output, it takes a long time to discharge the output capacitor.

As illustrated in the Figure 123, the LT3097 incorporates an overshoot recovery circuitry that turns on a current source to discharge the output capacitor in the event OUTSN is higher than SETN. This current is typically about 3.5 mA.

If OUTSN is externally held more than SETN, the current source turns on in an attempt to restore OUTSN to its programmed voltage. The current source remains on until the external circuitry releases OUTSN.

PCB LAYOUT CONSIDERATIONS

Given the high bandwidth and ultra-high PSRR of the LT3097, a careful PCB layout must be employed to achieve full device performance. Figure 130 shows the EVAL-LT3097-AZ evaluation board with a layout that delivers the full performance of the regulator. For more details refer to the LT3097 evaluation board user guide (EVAL-LT3097-AZ).

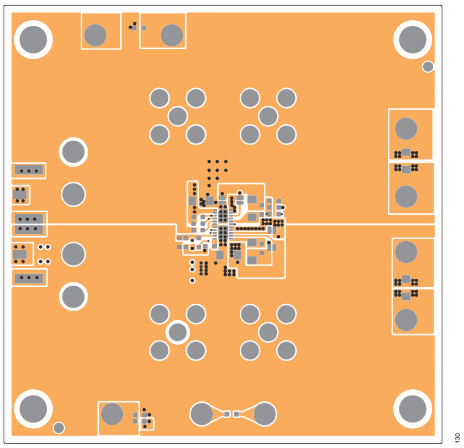

Figure 130. EVAL-LT3097-AZ Evaluation Board

THERMAL CONSIDERATIONS

The positive and negative regulators of the LT3097 have internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 165°C for the positive regulator and 167 °C for the negative regulator, with about 8°C of hysteresis for each regulator. For continuous normal load conditions, do not exceed the maximum junction temperature of 125°C. It is important to consider all sources of thermal resistance from junction to ambient, which includes junction to case, case to heatsink interface, heatsink resistance, or circuit board to ambient as the application dictates. Additionally, consider all heat sources close to the LT3097.

The underside of the DFN package has exposed metal from the lead frame to the die attachment. Note that the exposed-pad pin 23 is electrically connected to the ground (pin 19), and the exposed-pad pin 24 is electrically connected to INN (pins 6 and 7). This package allows heat to directly transfer from the die junction to the PCB metal to limit the maximum operating junction temperature. The dual, inline pin arrangement allows the metal to extend beyond the ends of the package on the topside (component side) of the PCB.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by the LDO regulator.

Table 5 lists the thermal resistance as a function of the copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR4 board with 1 oz solid internal planes and 2 oz top and bottom planes with a total board thickness of 1.6 mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information

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on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD-51, JESD51-7, and JESD51-12. Achieving low thermal resistance necessitates careful PCB layout.

Table 5. Measured Thermal Resistance for DFN Package

Copper Area			
Top Side[1]	Bottom Side	Board Area	Thermal Resistance (θ_{JA})
2500 mm^2	2500 mm^2	2500 mm^2	34°C/W
1000 mm^2	2500 mm^2	2500 mm^2	35°C/W
225 mm^2	2500 mm^2	2500 mm^2	36°C/W

[1] The device is mounted on the topside.

CALCULATING JUNCTION TEMPERATURE

For example, given a positive output voltage of 3.3 V, a positive input voltage of 5 V ± 5%, a positive output current range from 1 mA to 500 mA, a negative output voltage of −3.3 V, a negative input voltage of −5 V ± 5%, a negative output current range from 1 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The power dissipation of the positive side of the LT3097 is the following:

$$I_{OUTP(MAX)} \times \left(V_{INP(MAX)} - V_{OUTP}\right) + I_{GNDP} \times V_{INP(MAX)} \quad (8)$$

where:
$I_{OUTP(MAX)}$ = 500 mA.
$V_{INP(MAX)}$ = 5.25 V.
I_{GNDP} (at I_{OUTP} = 500 mA and V_{INP} = 5.25 V) = 12.5 mA.

Therefore, $P_{DISS\text{-}POSITIVE}$ = 0.5 A × (5.25 V − 3.3 V) + 12.5 mA × 5.25 V = 1 W.

The power dissipation of the negative side of the LT3097 is the following:

$$I_{OUTN(MAX)} \times \left(V_{INN(MAX)} - V_{OUTN}\right) + I_{GNDN} \times V_{INN(MAX)} \quad (9)$$

where:
$I_{OUTN(MAX)}$ = 500 mA.
$V_{INN(MAX)}$ = −5.25 V.
I_{GNDN} (at I_{OUTN} = 500 mA and V_{INN} = −5.25 V) = 9 mA.

Therefore, $P_{DISS\text{-}NEGATIVE}$ = −0.5 A × (−5.25 V + 3.3 V) + 9 mA × 5.25 V = 1.02 W.

The total power equals $P_{TOTAL} = P_{DISS\text{-}POSITIVE} + P_{DISS\text{-}NEGATIVE}$, which is 2.02W.

Using a DFN package, the thermal resistance is in the range of 34°C/W to 37°C/W, depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals 2.02 W × 35°C/W = 70.7°C.

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient, which calculates as follows:

$$T_{JMAX} = 50°C + 70.7°C = 120.7°C \quad (10)$$

OVERLOAD RECOVERY

Like many IC power regulators, the LT3097 incorporates SOA protection. The SOA protection activates at input-to-output differential voltages greater than 12 V for the positive regulator and 7V for the negative regulator. The SOA protection decreases the current limit because the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the Absolute Maximum Ratings of the LT3097. The LT3097 provides some level of output current for all values of input-to-output differentials. See the Figure 56/Figure 57. When power is first applied, and the input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the LDO regulator to supply the large output current and startup into high-current loads.

Due to current-limit foldback, however, at high-input voltages, a problem can occur if the output voltage is low, and the load current is high. Such situations occur after the removal of a short-circuit or if the ENP/UVP or ENN/UVN pins are pulled high after the input voltage is already turned on. The load-line, in such cases, intersects the output-current profile at two points. As a result, the regulator now has two stable operating points. With this double intersection, the input-power supply may need to be cycled down to zero and brought back up again to allow the output to recover. Other LDO regulators with foldback current-limit protection (such as the LT3042 and LT3093) also exhibit this phenomenon; therefore, it is not unique to the LT3097.

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PROTECTION FEATURES

The LT3097 incorporates several protection features for sensitive applications. Precision current-limit and thermal-overload protection protect the LT3097 against overload and fault conditions at the output of the device. For normal operation, do not allow the junction temperature to exceed 125°C.

To protect the low-noise error amplifier of the positive regulator of the LT3097, the SETP-to-OUTSP protection clamp limits the maximum voltage between SETP and OUTSP with a maximum DC current of 20 mA through the clamp. Therefore, for applications where SETP is actively driven by a voltage source, the voltage source must be current-limited to 20 mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SETP pin capacitor (C_{SETP}) to 22 µF.

To protect the low-noise error amplifier of the negative regulator of the LT3097, the SETN-to-OUTSN protection clamp limits the maximum voltage between SETN and OUTSN with a maximum DC current of 10 mA through the clamp. Therefore, for applications where SETN is actively driven by a voltage source, the voltage source must be current-limited to 10 mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SETN pin capacitor (C_{SETN}) to 22 µF.

The positive regulator of the LT3097 also incorporates reverse-input protection whereby the INP pin withstands reverse voltages of up to –20 V without causing any input-current flow and without developing negative voltages at the OUTP pin. The positive regulator protects both itself and the load against batteries that are plugged in backwards.

In circuits where a backup battery is required, several different input and output conditions can occur for the positive regulator. The positive output voltage can be held up while the positive input is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all cases, the reverse-current protection circuitry prevents current flow from the positive output to the positive input. Nonetheless, due to the OUTSP-to-SETP clamp, unless the SETP pin is floating, current can flow to GND through the SETP pin resistor as well as up to 15 mA to GND through the positive output overshoot recovery circuitry. This current flow through the positive output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between the OUTSP and SETP pins, with its anode at the OUTSP pin.

Pulling the negative output of the LT3097 above ground induces no damage to the part. If INN is left open circuit or grounded, OUTN can be pulled 20V above GND. In this condition, a maximum current of 25mA flows into the OUTN pin and out of the GND pin (pin 13). If INN is powered by a voltage source, OUTN sinks the short circuit current of the negative regulator of the LT3097 and protects itself by thermal limiting. In this case, however, grounding the ENN/UVN pin turns off the negative regulator and stops OUTN from sinking the short-circuit current.

TYPICAL APPLICATIONS

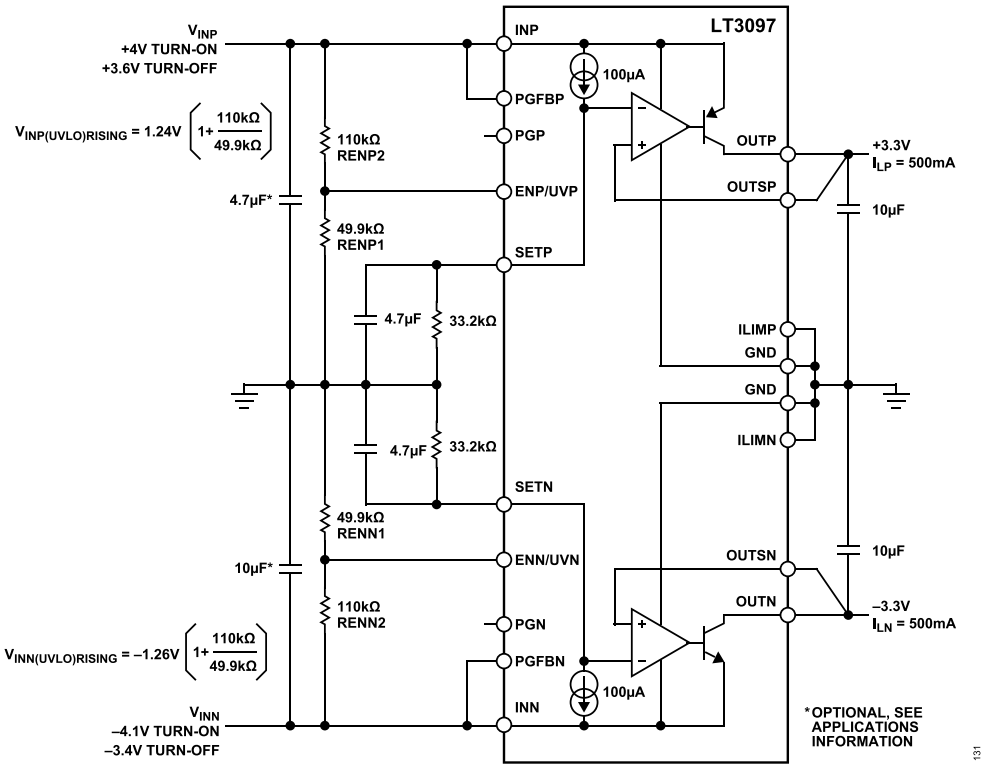

Figure 131. Programming Undervoltage Lockout

RELATED PRODUCTS

Table 6. Related Products

Model	Description	Comments
LT3032	Dual 150 mA Positive/Negative Low Noise Low Dropout Linear Regulator	20 µV rms noise (positive) and 30 µV rms noise (negative), V_{IN} = ±2.3 V to ±20 V, 300 mV dropout voltage per channel, 4 mm × 3 mm DFN package
LT3045	20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator	0.8 µV rms noise and 76 dB PSRR at 1 MHz, V_{IN} = 1.8 V to 20 V, 260 mV dropout voltage, 3 mm × 3 mm DFN and MSOP packages
LT3094	−20 V, 500 mA, ultralow noise, ultrahigh PSRR negative linear regulator	0.8 µV rms noise and 74 dB PSRR at 1 MHz, V_{IN} = –1.8 V to –20 V, 235 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages
LT3045-1	20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator with VIOC control	0.8 µV rms noise and 75 dB PSRR at 1 MHz, V_{IN} = 1.8 V to 20 V, 260 mV dropout voltage, 3 mm × 3 mm DFN and MSOP packages
LT3042	20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator	0.8 µV rms noise and 79 dB PSRR at 1 MHz, V_{IN} = 1.8 V to 20 V, 350 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages
LT3041	20 V, 1 A, ultra-low noise, ultra-high PSRR linear regulator with VIOC control	1 µV rms noise and 80 dB PSRR at 1 MHz, V_{IN} = 2.2 V to 20 V, 310 mV dropout voltage, programmable current limit and power good, 4 mm × 3 mm DFN package
LT3040	20 V, 200 mA, ultralow noise, ultrahigh PSRR precision DAC/ reference buffer	1.2 µV rms noise and 73dB PSRR at 1 MHz, V_{IN} = 1.8 V to 20 V, 350 mV dropout voltage, 3 mm × 3 mm DFN and MSOP Packages
LT3093	−20 V, 200 mA, ultralow noise, ultrahigh PSRR negative linear regulator	0.8 µV rms noise and 73 dB PSRR at 1 MHz, V_{IN} = –1.8 V to –20 V, 190 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages
ADP1761	1 A, Low V_{IN}, low noise, CMOS linear regulator	2 µV rms noise and 41 dB PSRR at 1 MHz, VIN = 1.10 V to 1.98 V, 30 mV dropout voltage, soft-start and power good, 3 mm x 3 mm LFCSP package
ADP7156	1.2 A, ultralow noise, high PSRR, fixed output, RF linear regulator	1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 2.3 V to 5.5 V, 120 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages
ADP7157	1.2 A, ultralow noise, high PSRR, adjustable output, RF linear regulator	1.6 µV rms noise and 55 dB PSRR at 1 MHz, VIN = 2.3 V to 5.5 V, 120 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages
ADM7150	800 mA, ultralow noise, high PSRR, fixed output, RF linear regulator	1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 4.5 V to 16 V, 600 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages
ADM7151	800 mA, ultralow noise, high PSRR, adjustable output, RF linear regulator	1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 4.5 V to 16 V, 600 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages
MAX38913	4 µV rms, ultra-low noise, 1 A, LDO with two-level, output-voltage selection	4 µV rms noise and 50 dB PSRR at 1 MHz, VIN = 1.8 V to 5.5 V, 28 mV dropout voltage, fast active discharge and power-OK, 3 mm × 3 mm TDFN and WLP packages