# 100$V_{IN}$/120$V_{OUT}$ LED Controller with Exponential PWM and Scalable Dimming

## FEATURES

- **128:1 Internal Exponential PWM Dimming**
- **Two-Pin Multiplying Analog Dimming**
- **Internal Spread Spectrum Frequency Modulation**
- **20,000:1 External PWM Dimming at 100Hz**
- **Rail-to-Rail LED Current Sensing: 0V to 120V**
- **±2% LED Current Regulation**
- **±2% Output Voltage Regulation**
- **LED Short/Open Protection and Indication**
- **Wide Input Voltage Range (5V to 100V)**
- **PMOS Switch Driver for PWM and Output Disconnect**
- Constant-Voltage and Constant-Current Regulation
- Adjustable Switching Frequency Up to 2MHz
- Programmable $V_{IN}$ UVLO with Hysteresis
- Side Solderable 20-Lead 3mm × 4mm QFN Package
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- High Voltage LED Applications
- Automotive Head Lamps/Running Lamps
- Accurate Current Limited Voltage Regulator

## DESCRIPTION

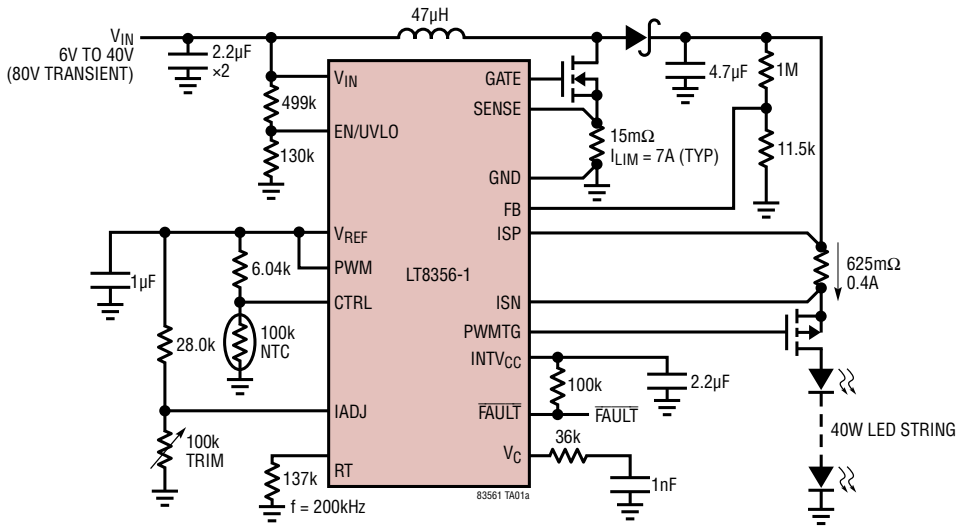
The LT®8356-1 is a DC/DC controller designed to drive high current LEDs. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. A voltage feedback pin serves as the input for several LED protection features and makes it possible for the converter to operate as a constant-voltage source. The LT8356-1 can implement boost, boost-to-battery, buck-mode, SEPIC, and flyback LED drivers.

The LT8356-1 senses output current at the high or low side of the load. The product of CTRL and IADJ inputs provides analog programming of the output current. The PWM input and PWMTG high side PMOS driver provides precision time-based LED dimming capability. When driven by an external digital signal, the PWM input provides LED dimming ratios of up to 20,000:1 at 100Hz. When driven by a constant voltage, the PWM input selects from one of 128 internally generated, precision, exponentially spaced dimming ratios ranging from 0.78% up to 100%.

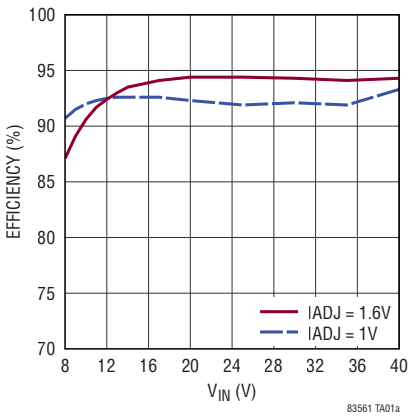


## TYPICAL APPLICATION

**40W Boost LED Driver with Thermal Derating and Trim**




**Efficiency vs $V_{IN}$**

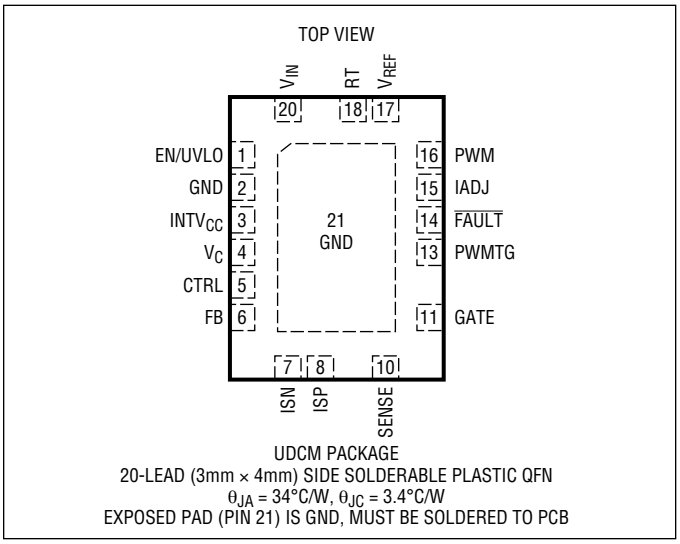


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$ ..... 100V
EN/UVLO ..... 100V
ISP and ISN ..... 120V
ISP–ISN ..... ±1V, (Note 2)
CTRL, IADJ, PWM and FB ..... 15V
$\overline{FAULT}$ ..... 40V
$INTV_{CC}$ ..... $V_{IN}$ + 0.3V, 8V
SENSE ..... 0.5V
RT, GATE and PWMTG ..... (Note 3)
$V_C$, and $V_{REF}$ ..... (Note 3)
Operating Junction Temperature Range (Notes 4, 5)
LT8356I-1 ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




UDCM PACKAGE
20-LEAD (3mm × 4mm) SIDE SOLDERABLE PLASTIC QFN
$\theta_{JA}$ = 34°C/W, $\theta_{JC}$ = 3.4°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| **AUTOMOTIVE PRODUCTS*** | | | | |
| LT8356IUDCM-1#WPBF | LT8356IUDCM-1#WTRPBF | LHNV | 20-Lead (3mm × 4mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C (Note 3). Unless otherwise noted, $V_{IN}$ = EN/UVLO = 12V, ISP = ISN = 60V, CTRL = IADJ = 2V, PWM = $INTV_{CC}$, FB = 1V.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Operating Supply Range | | ● | 5 | | 100 | V |
| Input ($V_{IN}$) Quiescent Current | PWM = 0V | | | 3 | | mA |
| Input ($V_{IN}$) Shutdown Current | EN/UVLO = 0V<br>EN/UVLO = 1.1V, EN/UVLO Rising | | | 0<br>12 | 6<br>20 | µA<br>µA |
| EN/UVLO Shutdown Threshold | EN/UVLO Falling | ● | 1.150 | 1.250 | 1.350 | V |
| EN/UVLO Rising Hysteresis | EN/UVLO Rising | | | 60 | | mV |
| EN/UVLO Pin Current (Device Off) | EN/UVLO = 1.1V, EN/UVLO Rising | | | 2.3 | | µA |
| EN/UVLO Pin Current (Device On) | EN/UVLO = 1.35V | | | 0 | | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C (Note 3). Unless otherwise noted, $V_{IN}$ = EN/UVLO = 12V, ISP = ISN = 60V, CTRL = IADJ = 2V, PWM = $INTV_{CC}$, FB = 1V.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Internal Voltage Regulator** | | | | | | |
| $INTV_{CC}$ Regulation Voltage | PWM = 0V, 12V < $V_{IN}$ < 100V, $I_{INTVCC}$ =1mA | | 7.35 | 7.5 | 7.65 | V |
| $INTV_{CC}$ Line Regulation | PWM = 0V, 10 < $V_{IN}$ < 100V | | | 0.75 | 3.0 | mV/V |
| $INTV_{CC}$ Load Regulation | PWM = 0V, 1mA < $I_{INTVCC}$ < 30mA | | | 2.25 | 4.5 | mV/mA |
| $INTV_{CC}$ Current Limit | PWM = 0V, $V_{IN}$ = 12V, $INTV_{CC}$ = 7V<br>PWM = 0V, $V_{IN}$ = 100V, $INTV_{CC}$ = 7V | | 65<br>45 | 90<br>60 | 115<br>75 | mA<br>mA |
| $INTV_{CC}$ Dropout Voltage | PWM = 0V, $V_{IN}$ = 7.5V, $I_{LOAD}$ = 10mA | | | 150 | | mV |
| $INTV_{CC}$ Undervoltage Lockout Threshold | PWM = 0V, $INTV_{CC}$ Falling | | | 4.3 | | V |
| $V_{REF}$ Voltage | $I_{VREF}$ = 0.5mA | ● | 1.96 | 1.99 | 2.02 | V |
| $V_{REF}$ Load Regulation | $I_{VREF}$ = 0.1mA to 1mA | | | 5 | 8 | mV/mA |
| $V_{REF}$ Current Limit | $V_{REF}$ = 1.8V | | 4 | 6 | 8 | mA |
| **Current Regulation (Note 6)** | | | | | | |
| ISP, ISN Common Mode Voltage Range | | ● | 0 | | 110 | V |
| LED Current Sense Threshold ($V_{ISP}$–$V_{ISN}$) | CTRL = 2V, IADJ = 2V (100%), ISP = 100V<br>CTRL = 1V, IADJ = 2V (50%), ISP = 100V<br>CTRL = 0.6V, IADJ = 2V (10%), ISP = 100V<br>CTRL = 2V, IADJ = 2V (100%), ISN = 0V | ●<br>●<br>● | 245<br>120<br>20<br>240 | 250<br>125<br>25<br>250 | 255<br>130<br>30<br>260 | mV<br>mV<br>mV<br>mV |
| LED Current Sense Threshold ($V_{ISP}$–$V_{ISN}$) | CTRL = 2V, IADJ = 1V (50%), ISP = 100V | ● | 118 | 125 | 134 | mV |
| SENSE Current Limit Threshold | 50% Duty Cycle at GATE (Note 7) | ● | 95 | 105 | 115 | mV |
| CTRL Off Threshold (Falling) | | ● | 280 | 300 | 320 | mV |
| CTRL Off Hysteresis | | | | 30 | | mV |
| IADJ Off Threshold (Falling) | | | | 500 | | mV |
| IADJ Off Hysteresis | | | | 20 | | mV |
| CTRL Pin Current | Current Out of Pin, CTRL = 0V | | | 20 | | nA |
| IADJ Pin Current | IADJ = 1.5V | | | 0 | | nA |
| ISP, ISN Pin Current (Combined) | PWM = $INTV_{CC}$, ISP = 100V (Active)<br>PWM = 0V, ISP = 100V (Standby) | | | 600<br>20 | <br>25 | µA<br>µA |
| Error Amp Transconductance | CTRL = 2V, IADJ = 2V (Full-Scale) | | | 65 | | µs |
| Error Amp Output Resistance | | | | 15 | | MΩ |
| **Output Voltage Regulation** | | | | | | |
| FB Regulation Voltage ($V_{FB}$) | CTRL = 2V, IADJ = 2V<br>CTRL = 2V, IADJ = 2V | <br>● | 1.188<br>1.176 | 1.200<br>1.200 | 1.212<br>1.224 | V<br>V |
| FB Pin Current | Current Out of Pin, $V_{FB}$ = 1.18V | | | 20 | | nA |
| FB Amplifier Transconductance | | | | 380 | | µs |
| **Oscillator** | | | | | | |
| Programmed Switching Frequency ($f_{SW}$) | $R_T$ = 8.66kΩ<br>$R_T$ = 63.4kΩ<br>$R_T$ = 137kΩ | <br>● | 1800<br>380<br>185 | 1950<br>400<br>200 | 2100<br>420<br>215 | kHz<br>kHz<br>kHz |
| Spread Spectrum Frequency Range | | | 100 | | 125 | $\%f_{SW}$ |
| Minimum Off-Time | $R_T$ = 63.4kΩ | ● | 40 | 60 | 80 | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C (Note 3). Unless otherwise noted, $V_{IN}$ = EN/UVLO = 12V, ISP = ISN = 60V, CTRL = IADJ = 2V, PWM = $INTV_{CC}$, FB = 1V.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Minimum On-Time | $C_{GATE}$ = 3.3nF, $R_T$ = 63.4kΩ (Note 8)<br>$C_{GATE}$ = 10nF, $R_T$ = 63.4kΩ (Note 8) | | | 100<br>180 | | ns<br>ns |
| **External NMOS Power Switch Driver** | | | | | | |
| Pull-Up Device On-Resistance | | | | 5 | | Ω |
| Pull-Down Device On-Resistance | | | | 3 | | Ω |
| GATE Rise Time (Note 9) | $C_{GATE}$ = 3.3nF, 10% to 90% | | | 45 | | ns |
| GATE Fall Time (Note 9) | $C_{GATE}$ = 3.3nF, 90% to 10% | | | 40 | | ns |
| **External PMOS Driver** | | | | | | |
| PWMTG ON Voltage ($V_{ISP}$–$V_{PWMTG}$) | $V_{ISP}$ = 100V | | 7.5 | 8.5 | 9.5 | V |
| PWMTG OFF Voltage ($V_{ISP}$–$V_{PWMTG}$) | $V_{ISP}$ = 100V | | | 0 | 0.3 | V |
| PWMTG Turn-On Time | $C_L$ = 470pF, $V_{ISP}$ = 100V | | | 150 | | ns |
| PWMTG Turn-Off Time | $C_L$ = 470pF, $V_{ISP}$ = 100V | | | 180 | | ns |
| **Fault Detection** | | | | | | |
| FB LED Open Threshold | $V_{ISP}$–$V_{ISN}$ = 0V, FB rising | | 1.116 | 1.140 | 1.164 | V |
| FB Overvoltage Threshold | FB rising | | 1.235 | 1.260 | 1.285 | V |
| FB Shorted LED Threshold | FB Falling | | | 300 | 330 | mV |
| LED Overcurrent Protection Threshold ($V_{ISP}$–$V_{ISN}$) | | <br>● | 610<br>450 | 670 | 730<br>850 | mV<br>mV |
| $\overline{FAULT}$ Pins Pull-Down Current | $V_{\overline{FAULT}}$ = 0.3V, $V_{FB}$ = 1.3V | | 0.5 | | | mA |
| $\overline{FAULT}$ Pin Leakage Current | $V_{\overline{FAULT}}$ = 40V, $V_{FB}$ = 0.7V | | | | 100 | nA |
| **Internal PWM Generator** | | | | | | |
| PWM Pin Voltage for Max Duty Ratio | | | | 1.5 | | V |
| PWM Pin Voltage for Min Duty Ratio | | | | 0.5 | | V |
| PWM Off Threshold (Falling) | | | | 0.4 | | V |
| PWM On Threshold (Rising) | | | | 1.6 | | V |
| Minimum Duty Ratio | $V_{PWM}$ = 0.5V, $R_T$ = 63.4kΩ | | | 0.78 | | % |
| Maximum Duty Ratio | $V_{PWM}$ = 1.5V, $R_T$ = 63.4kΩ | | | 100 | | % |
| PWM Voltage Step per Duty Ratio Setting | (Note 9) | | | 7.8 | | mV |
| PWM Pin Current | PWM = 1V | | | 0 | | nA |
| PWM Clock Frequency | | | | $f_{SW}$/1000 | | Hz |
| Fraction of $V_{REF}$ for 10% Duty | $R_T$ = 63.4kΩ | | | 0.511 $V_{REF}$ | | V |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** ISP–ISN may exceed 1V transiently. Do not exceed ISP–ISN = 10V for more than 1ms.

**Note 3:** Do not apply a positive or negative voltage to the PWMTG, RT, $V_{REF}$, $V_C$ or GATE pin, otherwise permanent damage may occur. Use these pins only as directed in the Pin Functions and Applications Information sections.

**Note 4:** LT8356I-1 is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. Operation lifetime is derated at junction temperatures greater than 125°C.

**Note 5:** This IC include overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 6:** LED voltage and current sense amplifier parameters are measured in a servo loop with $V_C$.

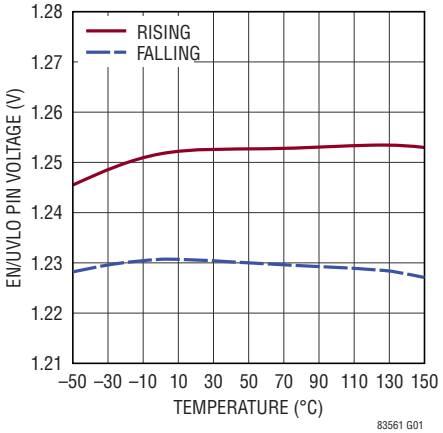
**Note 7:** Tested in a non-switching setup and correlated by design.

**Note 8:** Tested at $R_T$ = 63.4kΩ, guaranteed for all $R_T$ by design.

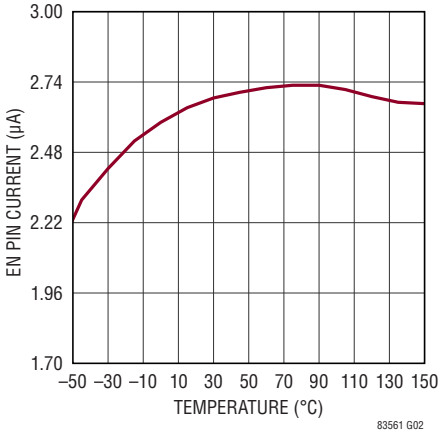
**Note 9:** GATE rise and fall time as well as the step size for the PWM ADC are guaranteed by design and not tested.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

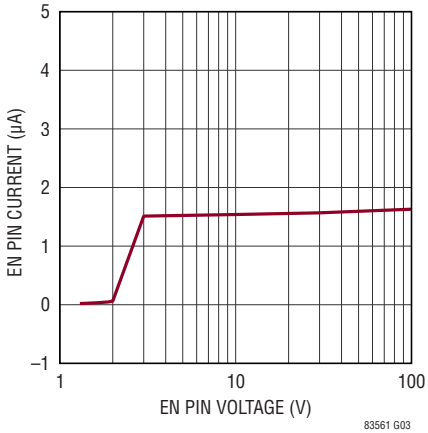
### EN/UVLO Thresholds vs Temperature



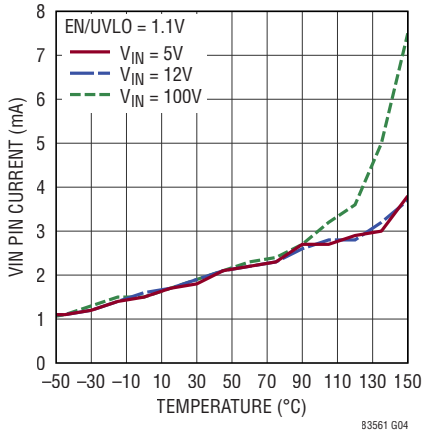

### EN/UVLO Hysteresis Current vs Temperature



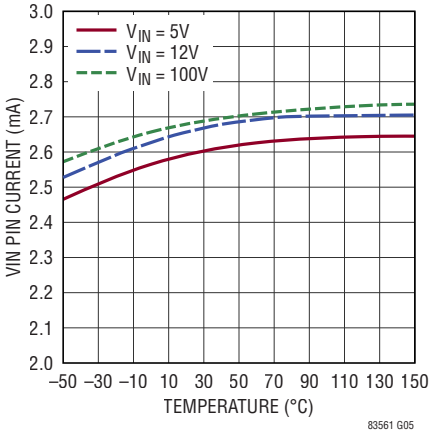

### EN/UVLO Current vs Voltage Above Turn-On Threshold



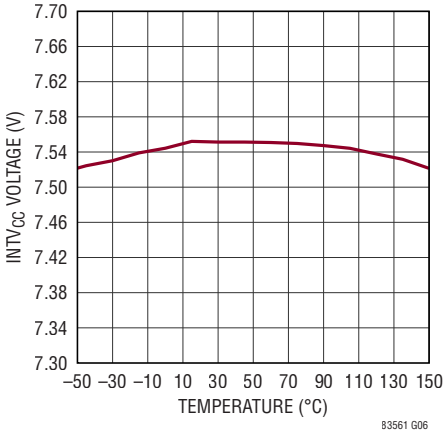

### $V_{IN}$ Shutdown Current vs Temperature



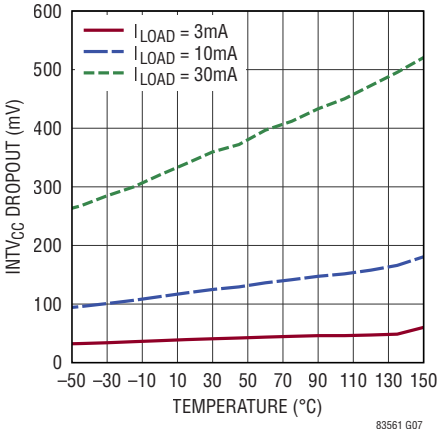

### $V_{IN}$ Quiescent Current vs Temperature



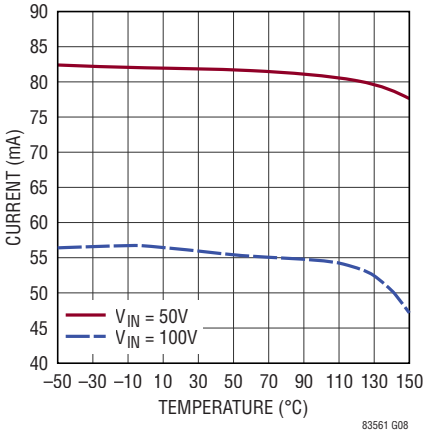

### $INTV_{CC}$ Voltage vs Temperature



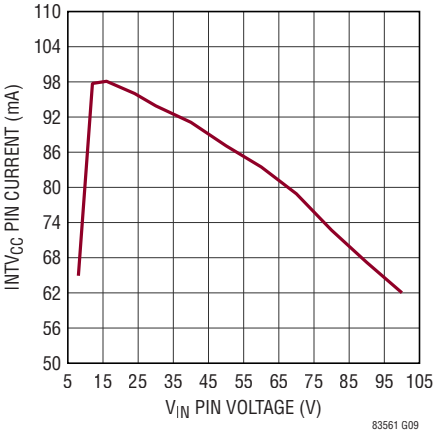

### $INTV_{CC}$ Dropout vs Temperature




### $INTV_{CC}$ Current Limit vs Temperature

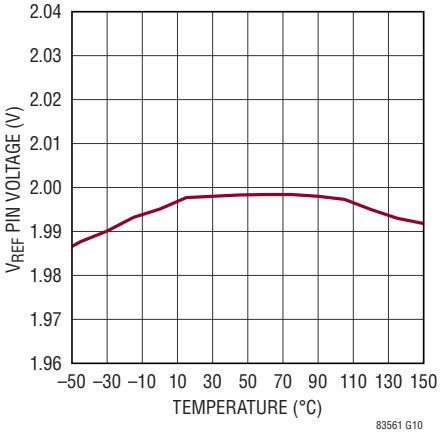



### $INTV_{CC}$ Current Limit vs $V_{IN}$

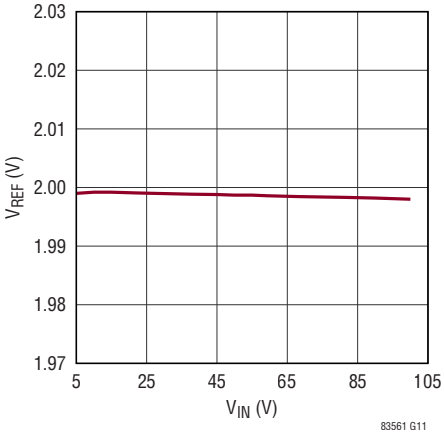


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

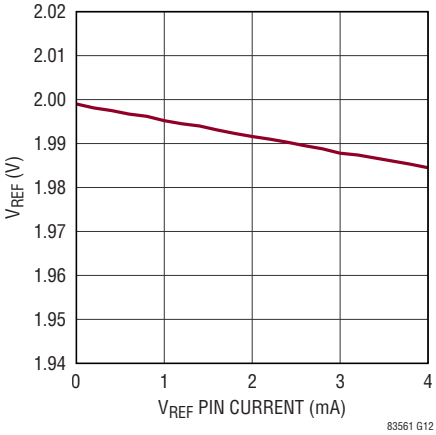
### $V_{REF}$ Voltage vs Temperature



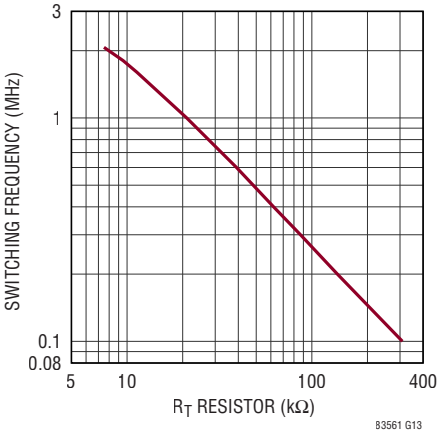

### $V_{REF}$ Line Regulation



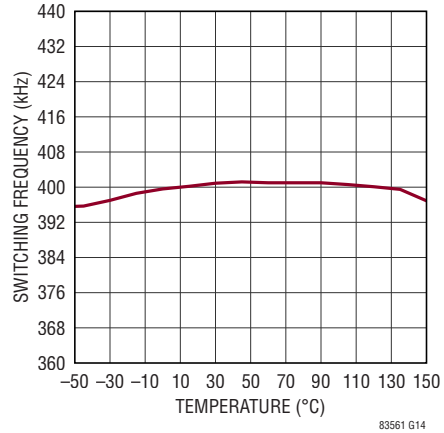

### $V_{REF}$ Load Regulation



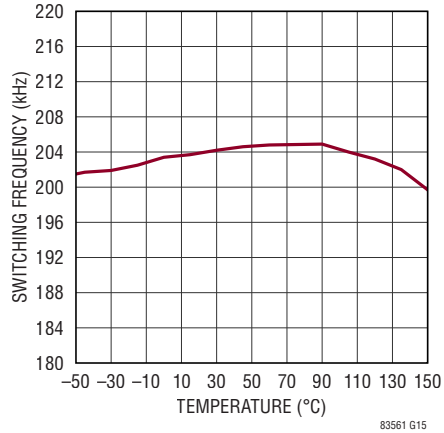

### Switching Frequency vs $R_T$ Resistor



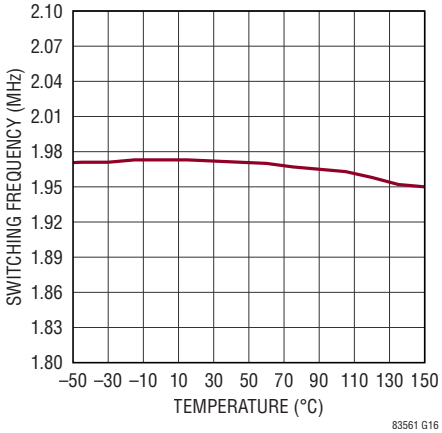

### Switching Frequency (400kHz) vs Temperature



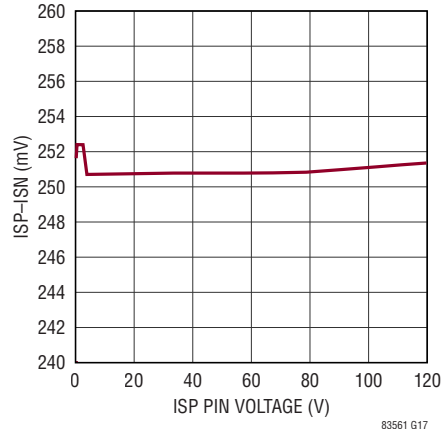

### Switching Frequency (200kHz) vs Temperature



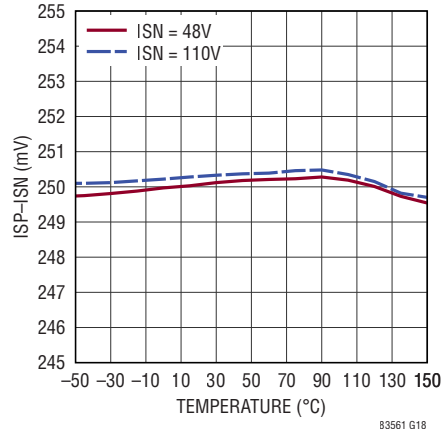

### Switching Frequency (2MHz) vs Temperature




### ISP–ISN Voltage vs ISP Voltage

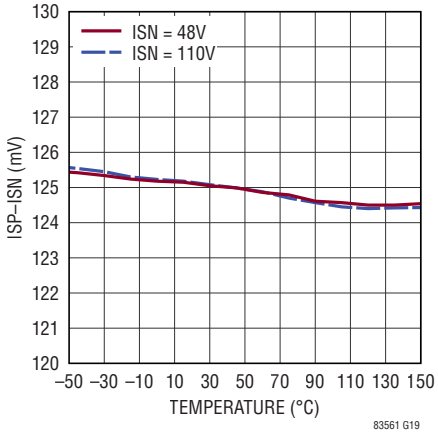



### ISP–ISN Full Scale Threshold vs Temperature

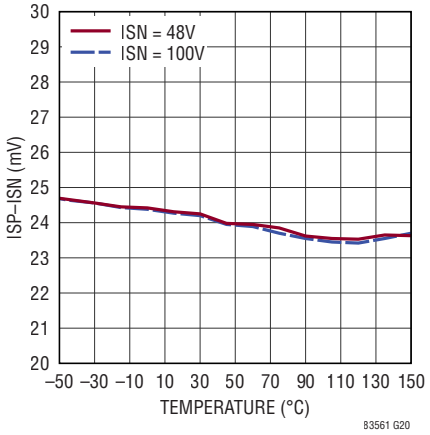


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

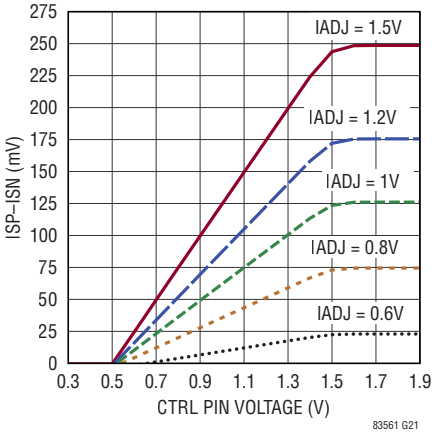
### ISP–ISN Threshold at CTRL = 1V vs Temperature



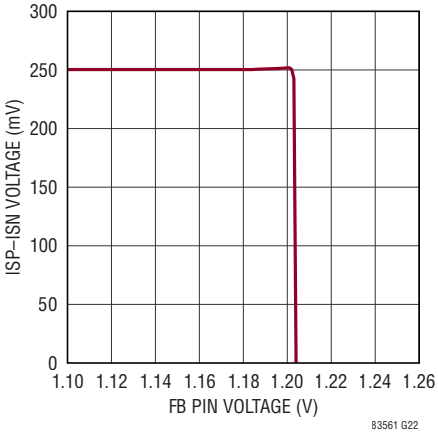

### ISP–ISN Threshold at CTRL = 0.6V vs Temperature



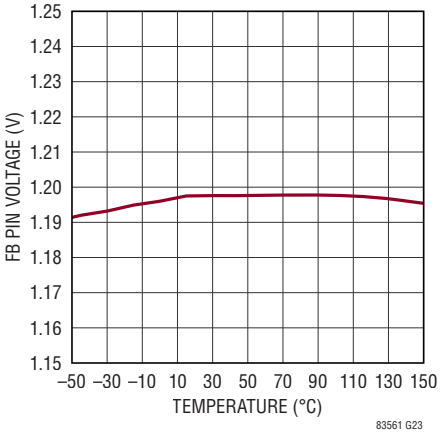

### ISP–ISN Threshold vs CTRL, IADJ Pin Voltage



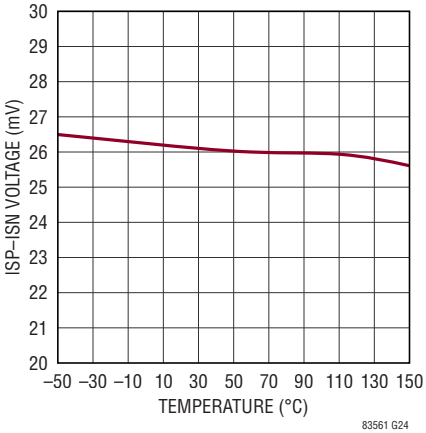

### ISP–ISN Voltage vs FB Pin Voltage



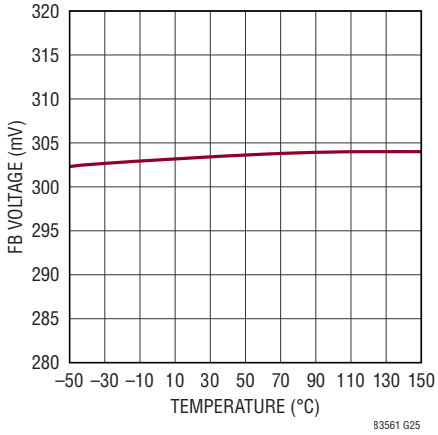

### Output Voltage Regulation vs Temperature



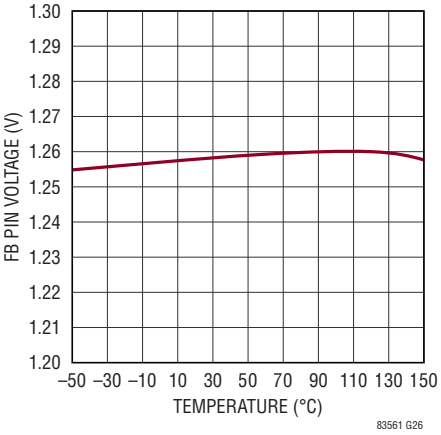

### C/10 Threshold vs Temperature



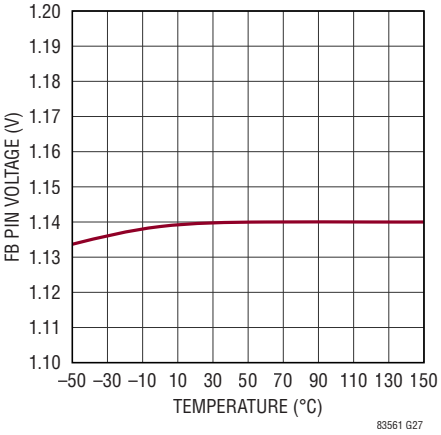

### FB Short LED Threshold vs Temperature




### FB Overvoltage Threshold vs Temperature

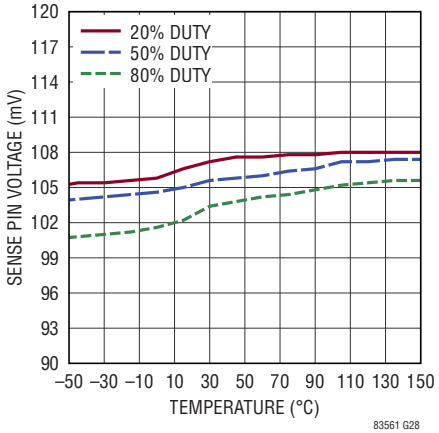



### FB Open LED Threshold vs Temperature

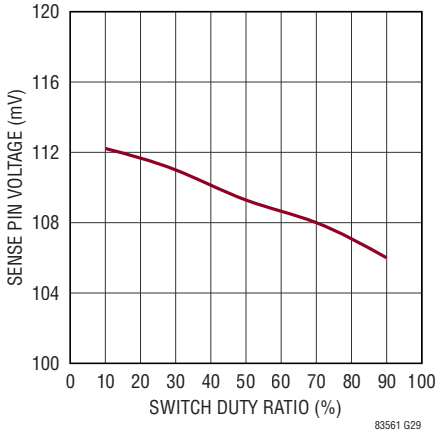


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

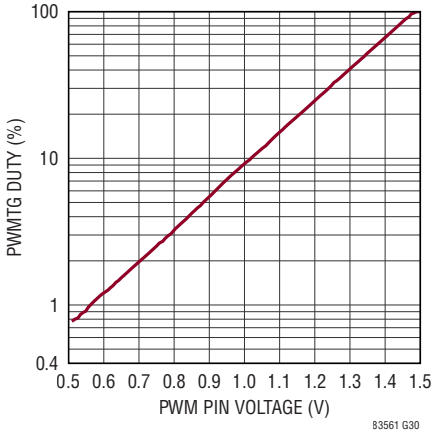
### SENSE Current Limit vs Temperature



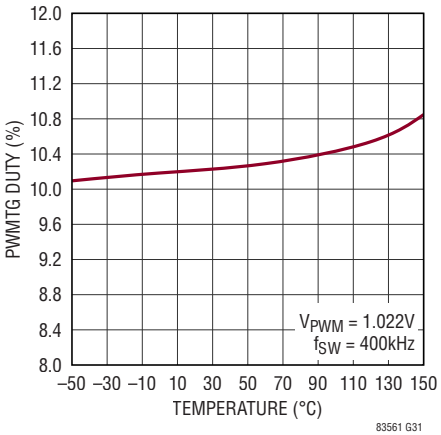

### SENSE Current Limit vs Duty Ratio



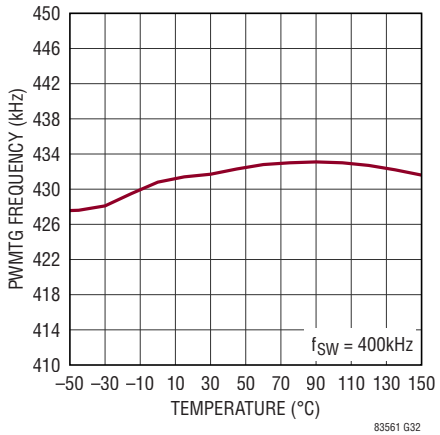

### PWMTG Duty vs PWM Pin Voltage



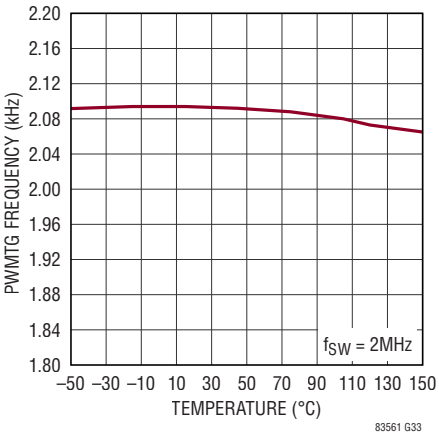

### PWMTG Duty vs Temperature



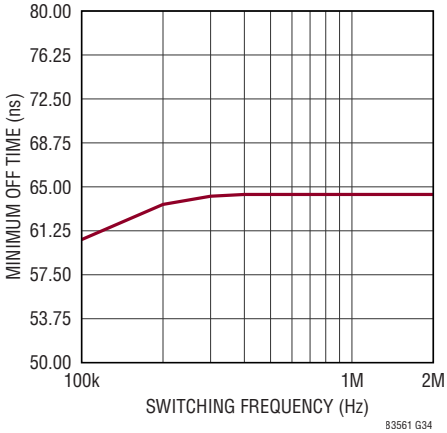

### PWMTG Frequency vs Temperature



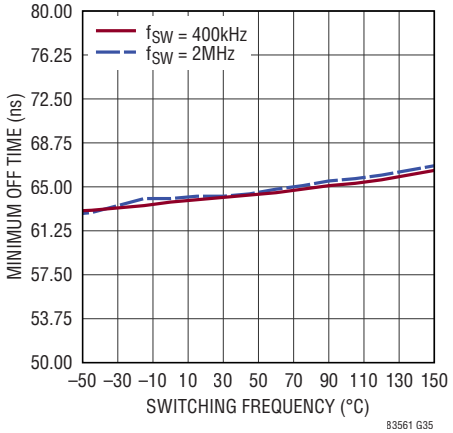

### PWMTG Frequency vs Temperature



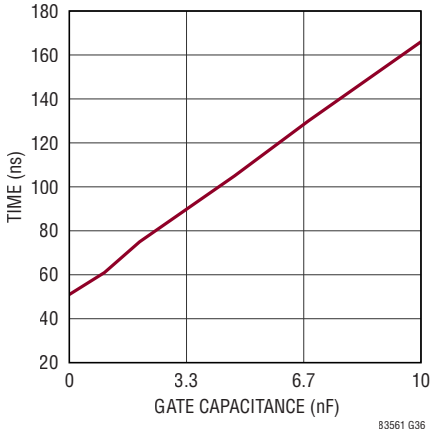

### Minimum Off-Time vs Switching Frequency




### Minimum Off-Time vs Temperature

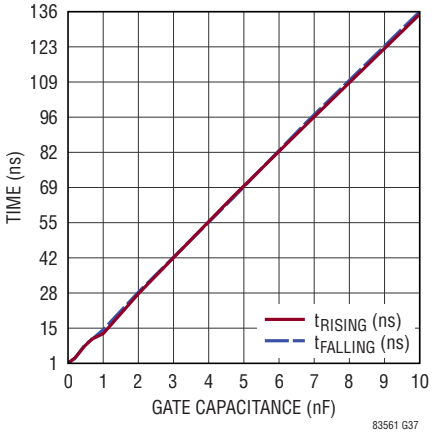



### Minimum On-Time vs Gate Capacitance

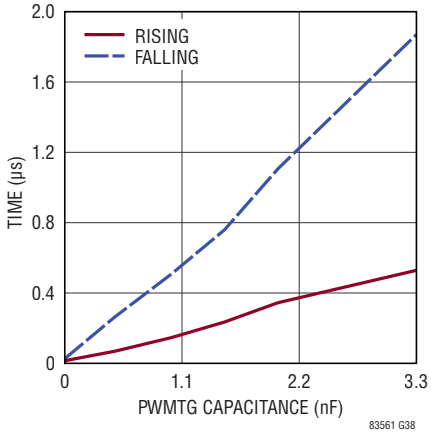


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

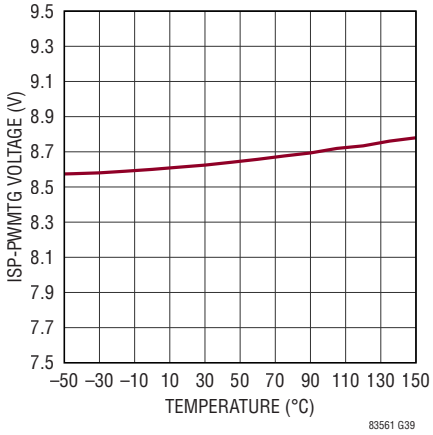
**GATE Rise/Fall Time vs GATE Capacitance**



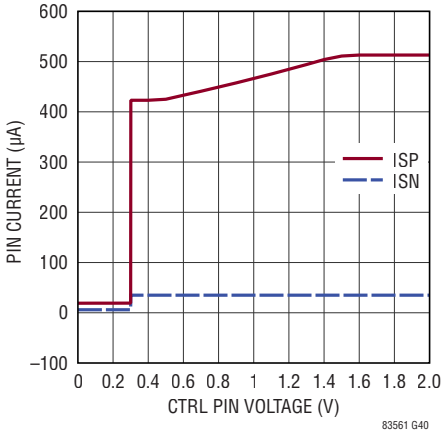

**PWMTG Driver Rise/Fall Time vs PWMTG Capacitance**



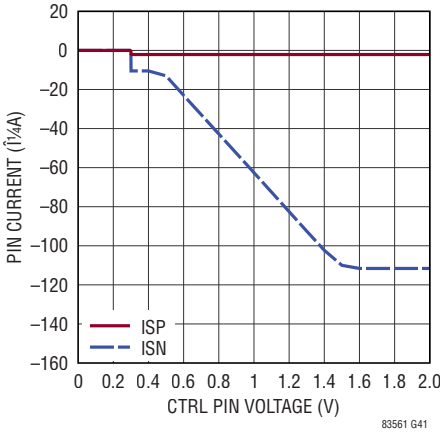

**PWMTG ON Voltage vs Temperature**




**ISP/ISN Pin Current vs CTRL Voltage at ISP = 100V**




**ISP/ISN Pin Current vs CTRL Voltage at ISN = 0V**



## PIN FUNCTIONS

**EN/UVLO (Pin 1):** When the voltage at this pin falls below 1.25V (typical), switching stops and the part shuts down. A hysteresis of approximately 60mV is included when returning over 1.25V. Drive this pin high with a logic level greater than 1.4V or low with a logic level below 0.3V for simple ON/OFF functionality or tie it through a resistive voltage divider to $V_{IN}$ for a precise input undervoltage shutdown threshold.

**GND (Pin 2, Pin 21 Exposed Pad):** Ground. Solder the exposed pad directly to the ground plane. Do not rely only on pin 2 for ground. Ensure the exposed pad is not left open.

**$INTV_{CC}$ (Pin 3):** Voltage Supply Used by Internal Circuits. Tie a capacitor from this pin to ground. It requires a minimum capacitance of 2.2µF; but considering temperature and voltage coefficients, 4.7µF is recommended. The typical $INTV_{CC}$ voltage is 7.5V, and a 16V rated capacitor will usually be appropriate. This pin is not intended for use as a power source for external loads and connecting it to certain external loads may interfere with operation of the device. Using the $INTV_{CC}$ pin for any purpose other than those described in the Applications Information section is not recommended.

**$V_C$ (Pin 4):** An Internal Error Amplifier Node Used for Compensation. Stabilize the loop by connecting a capacitor or RC network between this pin and ground. Read more in the Applications Information section for details about compensation.

**CTRL, IADJ (Pins 5, 15):** Two-Pin Analog Alternative to PWM Dimming. Tie CTRL and IADJ to $V_{REF}$ or $INTV_{CC}$ to set $R_{ILED}$ current to full-scale. The product of the offset CTRL and IADJ pin voltages sets the current in $R_{ILED}$ as $[(CTRL – 0.48V) • (IADJ – 0.5V) – 0.02V]/(4R_{ILED})$ when the voltages at CTRL and IADJ pins vary between 0.5V to 1.5V.

**FB (Pin 6):** Output Voltage Feedback Pin. This pin is used for output voltage regulation and limiting. Tie this pin to a resistive voltage divider from the output voltage. When the voltage at FB reaches 1.2V (typical), the control loop will reduce the switch current to regulate the output voltage such that FB remains around 1.2V. If the voltage at FB exceeds 1.26V (typical), PWMTG is driven high and switching briefly stops. If the voltage at FB falls below 300mV (typical) after soft-start has finished, PWMTG is driven high, soft-start resets, and switching stops. After a cooldown period, the part will re-enter soft-start. See the Applications Information section for more info on the use of the FB pin for general applications.

**ISN (Pin 7):** Kelvin connects this pin to the low side of the LED current feedback sense resistors $R_{ILED}$. Current through sense resistor, $R_{ILED}$ is 250mV/$R_{ILED}$ while CTRL > 1.5V and IADJ > 1.5V. It varies as $(CTRL – 500mV) • (IADJ – 500mV)/4R_{ILED})$ if the voltage at the CTRL and IADJ pins vary between 0.5V to 1.5V.

**ISP (Pin 8):** Kelvin connects this pin to the high side of the LED current feedback sense resistor $R_{ILED}$, see ISN for more details. If the voltage difference $V_{ISP}–V_{ISN}$ ever exceeds around 670mV (typical), switching stops, PWMTG goes high to disconnect the load, and soft-start resets. After a cooldown period, the part will re-enter soft-start. See the Applications Information section for more details.

**SENSE (Pin 10):** Kelvin connects this pin to the positive side of the grounded switch current sense resistor. Kelvin connects the negative side of the same resistor to the exposed pad of the IC. For more information about this, see the PCB Layout Guidelines and Information guidelines in the Applications Information section.

**GATE (Pin 11):** External NMOS Power Switch Gate Driver. Connect this pin to the gate of an NMOS whose source is connected to the switch current sense resistor.

**PWMTG (Pin 13):** High Side Gate Driver for the External Series PMOS Switch. Use these pins to disconnect the load for PWM dimming as well as fault events. PWMTG drives the PMOS gate between ISP–8.5V and ISP (typical) to cut off the flow of residual charge from the output capacitor when the LED load should be disconnected, as well as to prevent the long transient that would result from needing to recharge the output capacitor at the end of a long PWM off period. Leave open if unused. The voltage

## PIN FUNCTIONS

at PWMTG is limited to 8.5V (typical) below the voltage at ISP to protect the gate of the PMOS switch.

**$\overline{\text{FAULT}}$ (Pin 14):** Open-Drain Fault Indication Pin Indicating Short LED, Open LED, Overvoltage and Overcurrent Faults. Tie this pin through a 100k resistor to $INTV_{CC}$ or any suppl less than 40V or use it as an open-drain signal. LT8356-1 pulls these pins low to signal all reported fault events.

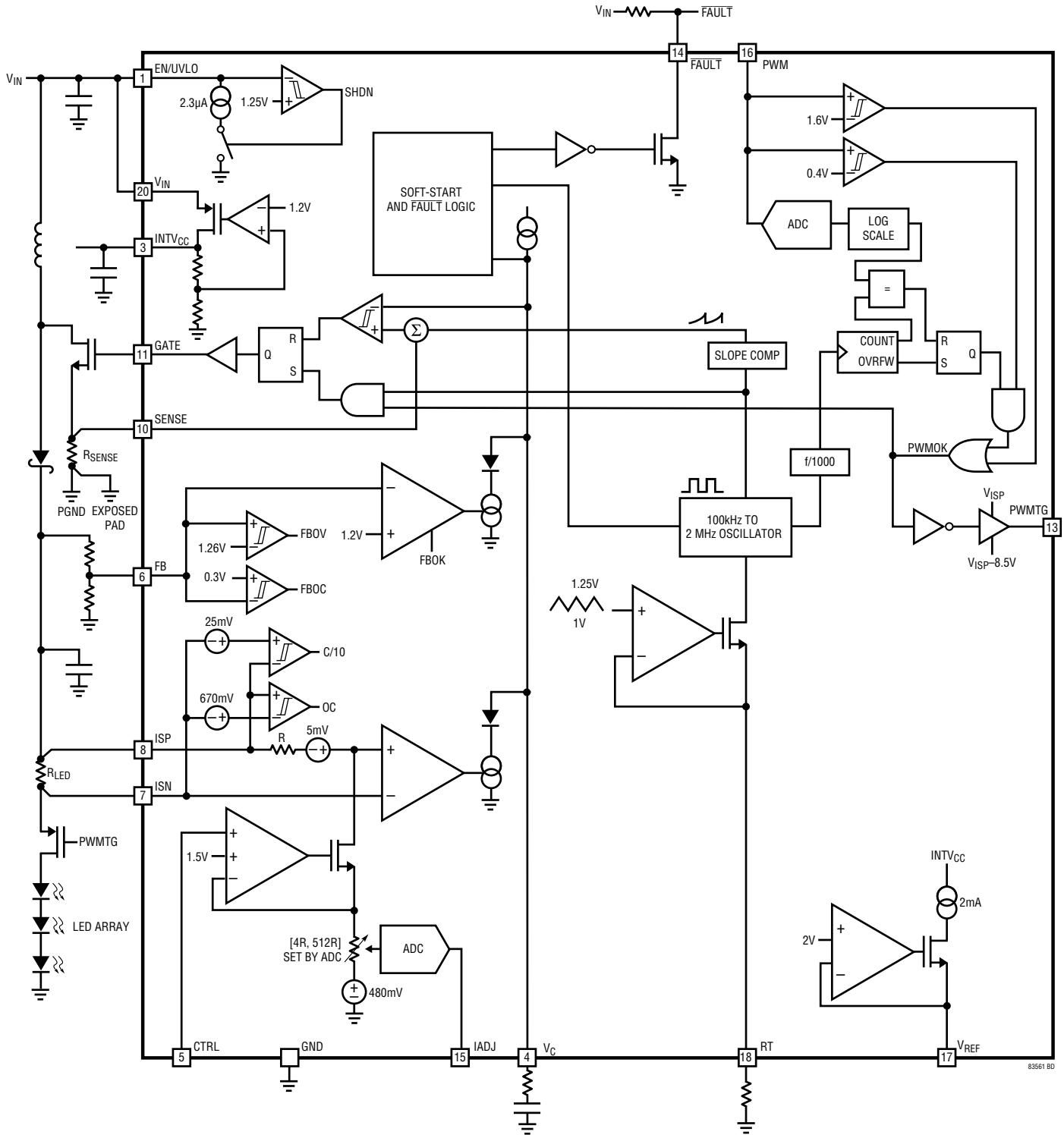
**PWM (Pin 16):** Pulse Width Modulation (PWM) Dimming Generation Control Pin. Connect an analog signal to this pin to use the internal exponential PWM dimming generator. When the voltage at this pin remains between 0.5V and 1.5V, the duty ratio of the internal dimming PWM generator will vary with the pin voltage. A linear ramp of voltage on the PWM pin between 0.5V and 1.5V lasting many PWMTG cycles at $f_{SW}$/1000 will result in an exponentially increasing PWM duty ratio. An external PWM signal can also drive this pin directly if the ON and OFF voltages are above 1.6V and below 0.4V, respectively. If PWM dimming is not used, tie this pin to $INTV_{CC}$ or $V_{REF}$.

**$V_{REF}$ (Pin 17):** A 2V (Typical) Reference Voltage. It can supply a maximum of 2.5mA at room temperature, useful for resistor networks that set voltages across CTRL, IADJ and PWM pins. The output is stable without a local bypass but, if needed, bypass this pin to ground with a 1µF capacitor. If no load is connected or unused, leave pin floating.

**RT (Pin 18):** Connect a resistor between this pin and ground to set the switching frequency and PWM dimming frequency. Do not connect anything but a resistor to this pin or the device may not function correctly.

**$V_{IN}$ (Pin 20):** Input Supply Pin. Must be locally bypassed.

## BLOCK DIAGRAM



## OPERATION

The LT8356-1 is a constant-frequency, constant-current/ constant-voltage (CC/CV) boost power stage controller. The operation of the part can be best understood by looking at the Block Diagram. The controller can implement boost, SEPIC, buck mode or buck-boost mode LED drivers. At the beginning of every clock cycle, the clock signal sets an SR-latch controlling the gate driver. The external NMOS switch turns on and connects the inductor to ground. The positive voltage drops across the inductor results in linearly increasing current in the inductor. The switch will remain on until the current comparator resets it. This reset will occur when the switch current, as measured by the switch current sense resistor, exceeds the internal demand current. This demand current comes from the error amplifier. The external LED current sense resistor used to program load current drives the error amplifier. The voltage drop across the sense resistor multiplied by the amplifier's transconductance establishes the demand current. Without a forced offset, the error amplifier regulates the load to zero current based on the voltage across the LED current sense resistor.

To establish the positive offset in the error amplifier needed to program the LED current, a small current is intentionally pulled from only one input of the amplifier through an internal series resistor. The CTRL and IADJ pins establish this offset current by varying the voltage dropped across a second internal resistor to GND. Changing the CTRL pin voltage will vary the voltage dropped across the second internal resistor, while changing the IADJ pin voltage will change the value of that resistor. This varies the LED current sense resistor regulation voltage between true zero and 250mV.

During constant-current operation, the FB pin provides overvoltage protection. When the FB pin voltage is below its regulation threshold, the FB amplifier has little effect on demand current. However, as the FB pin voltage approaches 1.2V, the FB amplifier has an increasingly pronounced effect, until it eventually dominates the demand current. If the FB pin voltage exceeds the regulation threshold by 60mV (typical), the part detects an overvoltage event. Similarly, if the voltage at the FB pin ever falls below 300mV (typical, excluding startup) then the part detects a short LED event.

Fast overcurrent protection relies on a separate signal path than the main LED current sense amplifier. If the LED current sense resistor voltage ($V_{ISP}$–$V_{ISN}$) exceeds 670mV (typical), switching stops. This event causes a brief interruption of switching while soft-start is reset, followed by a soft-start of the switching.

Four different methods for dimming the LED load are provided with LT8356-1. First, the voltages at the CTRL and IADJ pins, which set the LED current sense resistor regulation threshold , provide continuous, analog dimming of the LED load. In addition, two methods of PWM dimming exist. The first, external PWM, relies on a user-provided PWM signal. This signal drives the PWM pin, directly turning on and off the LED load. This method can achieve dimming ratios of 20,000:1 at 100Hz PWM frequency. Alternatively, the part can generate the PWM signal internally from an analog control signal at the PWM pin.

The internal dimming PWM generator selects one of 128 predetermined duty ratio values based on the analog voltage at the PWM pin. An exponential relationship exists between the PWM pin voltage and these duty ratio values. For example, consider a voltage at the PWM pin starting at 0V. When the voltage increases until the duty ratio is 9.6%, further increasing by 7.8mV (typical) will change the duty ratio to 10%. By the time the voltage is high enough to set 96% duty, the same 7.8mV (typical) increase will move the duty ratio up to 100%. A straight ramp at the PWM pin lasting many PWMTG dimming periods as set by $R_T$ will create an exponentially increasing PWM duty ratio for the LED load.

# APPLICATIONS INFORMATION

## INTRODUCTION

LT8356-1 provides a variety of features to enable a wide range of application options. Due to the small package size and pin count, many pins perform more than one function. The simplest LT8356-1 application is realizable in only a few off-chip components and with very few design choices on the part of the user. To fully utilize the capability of the part, however, requires a good understanding of how the individual features play together. The detailed explanations of each feature below along with several example application circuits will help with developing a good understanding of the part.

## PROGRAMMING THE LED CURRENT

Full-scale current through the LED string is easily programmed using a single resistor ($R_{ILED}$) connected in series with the LED string. For most applications, the LED current sense resistor should be placed on the high-side of the LED string; and Kelvin connected to LED current sense pins ISP and ISN. The loop will regulate a drop of 250mV across the LED current sense resistor, scaled by the voltage at the CTRL and IADJ pins, as discussed later. Choose a resistor with sufficient power dissipation capability for the programmed LED current. For LED currents less than 1.5A, a 0.5W resistor will usually suffice. Since the loop regulates the voltage across $R_{ILED}$, typical full-scale load current (IFS) is defined in Equation 1.

$$IFS = \frac{1}{4R_{ILED}} A \quad (1)$$

For the best performance and protection, sense at the highest potential in the LED string, and tie the source of the external PWM dimming PMOS to ISN. More details on the PWM dimming PMOS will be discussed later. Note that the loop can regulate LED current when the voltage at ISP is 0V, but a ground sensing configuration is not desirable for many applications. For more information see the Low Voltage (SEPIC) Start-Up.

## ADJUSTING LED CURRENT WITH CTRL AND IADJ PINS

The CTRL and IADJ pins provide an analog alternative to PWM dimming. The value of the voltage regulated across the LED current sense resistor can be adjusted with the CTRL and/or IADJ pins. As the voltage present at either pin is independently varied, the regulated voltage drop across the LED current sense resistor varies from 0V to 250mV. The system will supply no current if the CTRL pin voltage falls below 500mV or the IADJ pin voltage falls below 500mV, and will continue to supply full-scale current if the voltage at the CTRL pins exceed 1.5V and the IADJ pin exceeds 1.5V. The total LED current, $I_{LED}$, taking the effects of the CTRL and IADJ pins into account is shown in Equation 2.

$$I_{LED} = \frac{(V_{CTRL} - 0.48)(V_{IADJ} - 0.5) - 0.02}{4R_{ILED}} A, \quad 0.5V < V_{CTRL}, V_{IADJ} < 1.5V \quad (2)$$

The IADJ feature intentionally adds a small offset to ensure that true zero can be reached for LED current regulation. As a result, some combinations of CTRL and IADJ near the bottom of the range will result in no current flowing in the load. Note that the CTRL and IADJ pins can also be used for PWM by driving either with a digital signal whose low value is below 300mV; and whose high value is above 1.6V. Figure 1 shows how CTRL pin voltage affects LED current for varying values of IADJ.

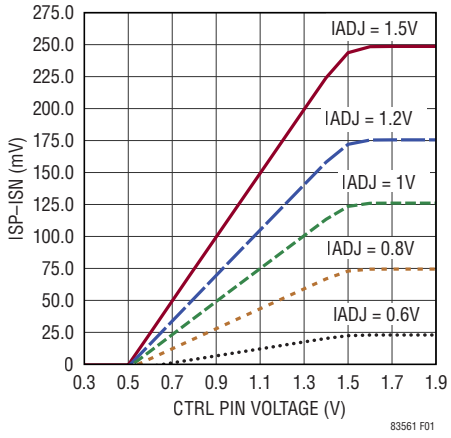



**Figure 1. $V_{ISP}$–$V_{ISN}$ vs CTRL and $V_{IADJ}$ Pin Voltage**

# APPLICATIONS INFORMATION

## SETTING THE OUTPUT REGULATION VOLTAGE

In addition to output current regulation, LT8356-1 can also provide output voltage regulation. The loop will go into voltage regulation mode when the voltage at the FB pin approaches 1.2V, regulating output voltage will reduce LED current below its programmed value. Voltage regulation mode is primarily included as a protection feature, allowing the part to gracefully manage some faults such as an open LED string. To set the output regulation voltage, connect a resistive voltage divider from the output voltage to FB as shown in Figure 2. Choose $R_{FB1}$ and $R_{FB2}$ to set the output voltage according to Equation 3.

$$V_{OUT} = \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \bullet 1.2V \quad (3)$$

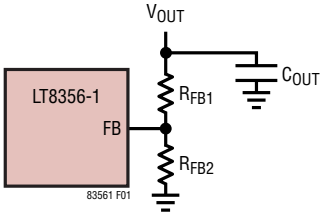



**Figure 2. Voltage Feedback Network**

It is important that the divider should be Kelvin connected to the output capacitor, as shown in Figure 2. The resistors $R_{FB1}$ and $R_{FB2}$ should be chosen such that their total value is between 1k and 1M. Be sure to keep resistor power dissipation capabilities in mind with higher output voltages.

In some configurations, such as buck mode, where the load voltage is not directly referred to ground, a level shifter may be needed to use constant-voltage mode control. Figure 3 shows an example circuit to accomplish output voltage control for buck and buck-boost topologies. Note the use of R1 in buck mode operation to keep PNP properly biased.

If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB pin should never exceed 1.12V when LEDs are connected.

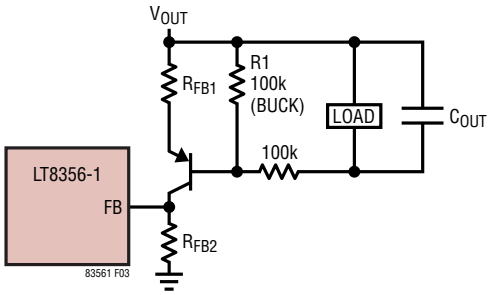



**Figure 3. Voltage Feedback Network with Level Shifter**

## SETTING SWITCHING AND PWM FREQUENCY

To program LT8356-1's switching frequency, connect a single resistor to ground from the RT pin. Use Equation 4 to approximate a starting value for the RT pin resistor, or Table 1 to use suggested values. It is important to connect only a resistor to GND on the RT pin.

$$R_T = \frac{3.15 \bullet 10^{11}}{(f_{SW})^{1.2}} \quad (4)$$

**Table 1. RT Values for Selected Switching Frequencies**

| SWITCHING FREQUENCY | $R_T$ VALUE (kΩ) |
|---|---|
| 100kHz | 309 |
| 200kHz | 137 |
| 300kHz | 86.6 |
| 400kHz | 63.4 |
| 500kHz | 48.7 |
| 1MHz | 21 |
| 1.95MHz | 8.66 |

During start-up, the switching frequency is reduced to allow sufficient switch OFF time, especially for 2MHz operation, so that inductor current can ramp below current limit when there is minimal voltage across the inductor during the OFF time. This condition is encountered at start-up or after faults when the output is still low. During start-up, or when restarting after faults, switching frequency will drop to around 20% of its nominal value, and step-up over the duration of around 256 times the nominal switching period. For more information about this, see the Soft-Start section.

## APPLICATIONS INFORMATION

The internal dimming PWM generator clock runs at approximately $f_{SW1}/1000$.

### PULSE WIDTH MODULATION (PWM) DIMMING

Pulse width modulation (PWM) allows high dynamic range dimming of the LED load. When using PWM dimming, a pulse train with duty ratio proportional to desired LED current controls the load. During ON periods, the part operates normally. During OFF periods the part stops switching. While the part is not switching, the compensation node is high impedance to minimize changes to the compensation capacitor voltage. This reduces transient settling time when the next ON period arrives. In addition to this, the LT8356-1 provides an optional load disconnect. Disconnecting the load makes turn-off much faster, as the output capacitor does not continue to conduct current into the load. Transient settling time is also shorter when turning back ON, as the output capacitor's state is less affected by the load. To use the external load, tie a disconnect PMOS in series with the load such that the source of the PMOS connects to the ISN node, and the drain to the LED load. Connect the gate of the PMOS to the PWMTG pin. The voltage at the PWMTG pin will vary between $V_{ISP}$ and $V_{ISP}$–8.5V (typical) to turn the PMOS off and on. Note that this configuration works for any of the supported power stage topologies. For more information on power stage topologies, see the Typical Application section.

The PWM pin allows two modes of PWM dimming. The first mode is external PWM. In this mode, a digital signal created by some other device, such as a microprocessor, drives the PWM pins. This PWM signal directly controls the part: when this signal is high, the part runs, when this signal is low, the part does not run, and disconnects the load if an external PMOS is used. Tying the PWM pin to $INTV_{CC}$ or $V_{REF}$ results in continuous, uninterrupted operation. Conversely, tying the PWM pin to ground results in the system remaining idle indefinitely. External PWM dimming can support ON periods shorter than 500ns, allowing a PWM dimming dynamic range of 20,000:1 at 100Hz. Careful design of the wiring, including short cabling to reduce parasitic inductance, to the LED load improves turn on speed and regulation accuracy for brief (<1µs), high current (>0.5A) pulses. While sub-microsecond PWM dimming on times are supported by LT8356-1, very brief off times (<0.3µs) are not supported. This means that negative going glitches on the CTRL, IADJ, and PWM pins should be avoided. The second mode of PWM dimming is internal.

When using internal PWM dimming, the analog voltage at the PWM pin control the duty ratio of the PWMTG signal. The voltage range for internal PWM dimming is from 0.5V to 1.5V at the PWM pin. The internal PWM generator converts the voltage at the PWM pin to a 7-bit digital representation. The analog-to-digital converter responsible for this uses a linear scale, each code is around 7.8mV wide. Each 7-bit code corresponds to a unique duty ratio value. The values of duty ratio are separated exponentially. Refer to Figure 4 for a graphical representation of this relationship and Table 2 for recommended PWM voltage for selected PWM Duties.

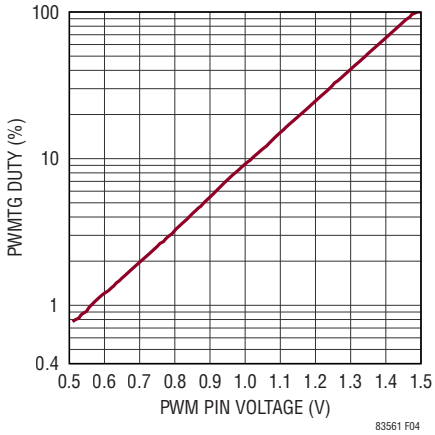



**Figure 4. PWM Duty vs PWM Pin Voltages**

**Table 2. Recommended PWM Voltage for Selected PWM Duties**

| PWM DUTY (%) | FRACTION OF $V_{REF}$ VOLTAGE AT PWM |
|---|---|
| 1 | 0.282 |
| 5 | 0.413 |
| 10 | 0.511 |
| 15 | 0.55 |
| 20 | 0.581 |
| 25 | 0.6 |
| 33.3 | 0.631 |
| 50 | 0.702 |
| 76.5 | 0.713 |
| 100 | >0.8 |

# APPLICATIONS INFORMATION

## SPREAD SPECTRUM SWITCHING FREQUENCY

The internal spread-spectrum frequency modulation is always enabled in the LT8356-1. The modulating waveform is a triangle wave with steps at the positive and negative peaks. The modulation frequency is around 3kHz, and the switching frequency range is from 100% to 125% of the programmed value. If spread spectrum frequency modulation does not provide sufficient EMI attenuation even with good PCB design, consider slowing the switch turn-on speed by placing a 5Ω to 10Ω resistor between the GATE pin and the external NMOS switch. Please contact the factory for a reference design.

## MAXIMUM DUTY RATIO

Since LT8356-1 uses a switch to connect an inductor from $V_{IN}$ to ground, having a duty ratio of 100% would result in zero current flowing to the load. To prevent this situation, the part enforces a minimum off time. During this time, irrespective of load or demand, the switch turns off and allows the inductor current to flow into the load. The duty ratio can, therefore, never reach 100%. The maximum duty ratio varies with frequency. Consider adding margin to account for variations in component values and LT8356-1 switching frequencies variations.

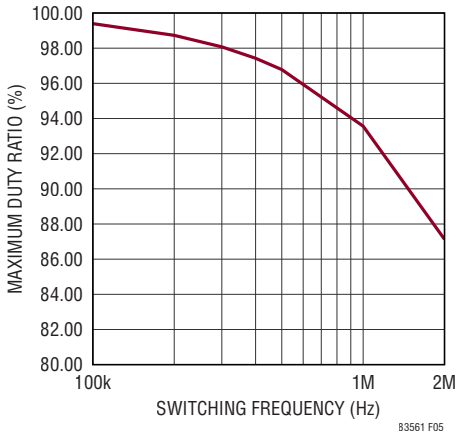



**Figure 5. Maximum Duty as a Function of Switching Frequency**

## MAXIMUM SWITCH CURRENT

An important system parameter is the current limit. This prevents damage to system components by limiting the maximum instantaneous current conducting through the power switch. In a well-designed system, there will be margin between the maximum switch current to drive the LED load and the switch current limit. The LT8356-1 offers a current limit that has sufficient slope compensation so that reaching the current limit during line and load transients does not result in subharmonic oscillations. The switch current sense resistor programs the switch current limit as $0.1/R_{SENSE}$. Normally, the loop limits switch current based on the value of the sense resistor.

The loop will not typically command a voltage $V_{SENSE}$ of more than 105mV. A good rule of thumb for setting maximum LED current for boost and buck-boost power stages appears in Equation 5. This equation assumes that the inductor selection used limits current ripple to around 20% of average current. For more information, see the Inductor Selection section.

$$I_{LED,MAX(20\%\ Ripple)} = \frac{0.9\ (100mV)}{R_{SENSE}} \bullet \frac{V_{IN}}{V_{ISP}} \quad (5)$$

In the boost and buck-boost topologies, average switch current is related to average LED current by the ratio of $V_{IN}$ to $V_{ISP}$. In the buck topology, average LED current approximately equals average inductor current. For this reason, the buck topology provides the highest possible LED current capability. The peak instantaneous switch current is thus the average LED current plus half of the peak-to-peak ripple current. This leads to the result in Equation 6 for buck mode current limit.

$$I_{LED,MAX(BUCK)} = \frac{100mV}{R_{SENSE}} \bullet \frac{V_{LED}\ (V_{IN} - V_{LED})}{2 \bullet V_{IN} \bullet L \bullet f_{SW}} \quad (6)$$

For more information about power stage topologies, review the Typical Application section. Since LT8356-1 offers a switch current limit that does not significantly change with duty ratio, the switch current limit can also limit the input current. Like the load current, the average input current and average switch current are not always the same. However, while the switch is on, the same instantaneous current flows in the switch and inductor. Because the inductor connects directly to the input, the peak input current, which is also the peak inductor current, cannot exceed the programmed switch current limit.

## APPLICATIONS INFORMATION

Note that average input and load current will be strictly less than maximum peak switch current.

### LOOP COMPENSATION

To ensure stable operation of the control loop realized by LT8356-1 it is necessary to limit the loop bandwidth. To do this, connect an RC network between the $V_C$ pin and ground. A single capacitor can fulfill stability requirements if PCB area is extremely limited. The addition of a series resistor, however, will increase response speed and can also recover phase margin. A schematic diagram of the typical compensation scheme is illustrated in Figure 6. For many cases, a 1nF capacitor and 47k resistor will suffice. These are good values to start with for all applications. If settling time is unacceptable, ringing is too large, or the loop remains unstable the following steps can help. First, try reducing to 10k or eliminating the compensation resistor, $R_C$, especially if transient response is ringing or underdamped. Reducing the compensation resistor will cause longer settling time and larger deviation from load-steps such as PWM dimming. Next, increase the size of the compensation capacitor, $C_C$. This will reduce the frequency of the dominant (low frequency) pole and thereby the unity gain frequency. It will usually be possible to stabilize the loop given a big enough compensation capacitor. Increasing the compensation capacitor slows down the transient response to line and load activity. If the compensation capacitor cannot change by a small amount to achieve stability, consider instead decreasing the output capacitor or decreasing the inductor to separate the load pole and right half plane zero (for boost and SEPIC topologies).

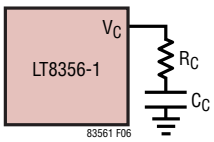



**Figure 6. LT8356-1 Compensation Network**

### INPUT AND OUTPUT CAPACITOR SELECTION

The input and output capacitors supply the transient current for the power stage and should be placed and chosen according to the transient current requirements. An X7R type ceramic capacitor is usually a good choice for both input and output capacitor. Ceramic capacitors have a large voltage coefficient (i.e., lower capacitance when biased near their rated voltage). It is generally a good rule of thumb to choose a capacitance 60% higher to compensate for the voltage coefficient. Consult the capacitor manufacturer to ensure capacitance is sufficient at the operating voltage.

The switching frequency, output current, inductor ripple current, and tolerable input voltage ripple are key parameters to consider when determining the value of the input capacitor. Typically, boost and SEPIC converters require a lower value input capacitor than buck mode converters. Use Equation 7 to estimate the value of the input capacitor. If the inductor is selected according to the directions in the Inductor Selection section, the input capacitance value can be calculated.

$$C_{IN(BOOST)} = \frac{20mV}{0.8 \bullet \Delta V_{IN} \bullet R_{SENSE} \bullet f_{SW}} \quad (7)$$

For a boost converter switching at 200kHz, a 10µF input capacitor will often be sufficient. In the buck mode configuration, the input capacitor has large, pulsed currents due to the current returned through the Schottky diode when the switch is off. The minimum input capacitance can be estimated with Equation 8.

$$C_{IN(BUCK)} = \frac{I_{LED}}{\Delta V_{IN} \bullet f_{SW}} \quad (8)$$

For the buck case at 2MHz, a 10µF input capacitor would be appropriate to ensure less than 100mV of input voltage ripple with $I_{LED}$ = 1.5A. Additional margin is recommended. In the buck converter case, it is important to place the capacitor as close as possible to the Schottky diode, external NMOS switch and the sense resistor. It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. Use Equation 9 to estimate the RMS input capacitor current for the buck converter case.

$$I_{CIN(BUCK)} = I_{LED} \sqrt{\frac{V_{LED}}{V_{IN}} \left(1 - \frac{V_{LED}}{V_{IN}}\right)} \quad (9)$$

## APPLICATIONS INFORMATION

The selection of the output capacitor depends on load and power stage configuration. For example, a boost or buck-boost mode converter will require a much larger output capacitor than a buck mode converter for the same conditions. The boost and buck-boost mode configurations will also require similar low ESR and low ESL capacitors like the input capacitor of the buck mode case. Capacitor values will increase proportionally with decreasing switching frequency for the same ripple voltage. The equivalent resistance presented by an LED load is frequently low, so larger capacitors may be needed to further reduce voltage ripple. It is likely that the appropriate output capacitor value will fall between 10µF and 47µF. Use the example applications as a starting point for output capacitor selection.

### SCHOTTKY RECTIFIER SELECTION

Choose a Schottky diode with reverse breakdown voltage greater than the maximum programmed output voltage and a current rating greater than the peak inductor current. Be sure to set the programmable switch current limit lower than the maximum forward current of the Schottky rectifier chosen. It is best to find a rectifier with low equivalent capacitance, around or below 500pF. Pay attention to reverse leakage current if the part is to be used in low frequency PWM dimming situations. The reverse leakage current can discharge the output capacitor. This can lead to lengthy turn-on transient effects that degrade maximum PWM dimming dynamic range. Not all applications will require the combination of high reverse voltage and forward current of this rectifier.

### INDUCTOR SELECTION

Select an inductor for use with LT8356-1 that has a saturation current greater than the switch current limit set by the switch current sense resistor as $0.1V/R_{SENSE}$. Include some margin for the saturation current. Choose the inductor value based on desired ripple current given input and output voltage and switching frequency. Use Equation 10 to select an inductor with around 20% ripple.

$$L_{BOOST} = \frac{R_{SENSE} \bullet V_{IN}}{0.02V \bullet f_{SW}} \left(1 - \frac{V_{IN}}{V_{ISP}}\right)$$
$$L_{BUCK} = \frac{R_{SENSE} \bullet V_{LED}}{0.02V \bullet f_{SW}} \left(1 - \frac{V_{LED}}{V_{IN}}\right) \quad (10)$$

Table 3 provides some recommended inductor vendors.

**Table 3. Recommended Inductor Vendors**

| VENDOR | WEB |
|---|---|
| Sumida | www.sumida.com |
| Wurth Elektronik | www.we-online.com |
| Coiltronics | www.cooperet.com |
| Vishay | www.vishay.com |
| Coilcraft | www.coilcraft.com |

### POWER PMOS SELECTION

For the PMOS to be used with PWMTG, select a device with drain-source voltage rating higher than the external NMOS switch and Schottky rectifier. The gate-source voltage rating should be higher than 12V. The drain current rating should be sufficient to conduct the full programmed LED current with some margin. Ensure that the PWMTG drive voltage of 8.5V will fully enhance the PMOS device. Be careful when selecting a PMOS to consider the effect that higher current ratings have on gate charge (Qg). A very high Qg PMOS will slow turn-on and turn-off times and can lead to offsets for very brief on-time PWM dimming (shorter than 500ns). A clamping diode might be necessary near PMOS's drain to prevent the drain ringing well below ground when being shorted to ground through a long cable.

### POWER NMOS SELECTION

Choose an external NMOS switch with breakdown voltage higher than the programmed output voltage by at least 20%. Select the forward current rating based on the load requirements and maximum current through the switch. Be sure to set the programmable switch current limit lower than the maximum rated forward current of the switch. Like the power PMOS, the gate charge of the external NMOS can impact performance. Very low Qg MOSFETs

## APPLICATIONS INFORMATION

(<1nC) can turn on quickly, potentially negatively impacting EMI performance. Conversely, very high Qg MOSFETs (>100nC) can draw excessive current from the part's internal LDO regulator at higher switching frequencies.

### SENSE RESISTORS SELECTION

Select the LED and switch current sense resistors for power dissipation limits and PCB footprint convenience. The control loop will limit the steady state voltage dropped across the LED current sense resistor to 250mV (typical) and the switch current sense resistor to 100mV (typical). Large footprint resistors such as 2010 may be needed for high power applications. Be sure to Kelvin all sense resistors connections to the LT8356-1.

### LED FAULT EVENTS

LT8356-1 provides a variety of fault detection to mitigate damage to external components. While LT8356-1 has many self-protection features, three LED types of faults (LED Short, Overvoltage and LED Overcurrent) will cause the part to immediately stop switching and, if an external PMOS is used according to instructions in the Pulse Width Modulation (PWM) Dimming section, disconnect the load from the output capacitor.

The LED overcurrent fault detection uses the LED current sense resistor $R_{ILED}$. If the voltage drop across the sense resistor is greater than 670mV (typical), an internal fault signal gets asserted. The LED Short fault senses load voltage. This can allow the detection of limited failures, such as one or two of the LEDs in a string becoming shorted. LT8356-1 senses the voltage at the FB pin and detects a LED Short fault if that voltage falls below 300mV (typical, excluding during start-up). It is important to note that the FB resistor divider must be in place to use the LED Short fault detection. The Overvoltage fault occurs when the voltage at the FB pin exceeds 1.26V (typical). The FB resistor divider must be in place to take advantage of the over voltage fault protection. LT8356-1 clears faults and resumes switching depending on the type of fault. Switching resumes as soon as an overvoltage fault has cleared.

Recovery from Short LED and LED Overcurrent faults will enter soft-start as if it had just been turned on via the EN/UVLO pin. Upon successful completion of the soft-start process with no faults, the internal fault clears and normal operation resumes. The PWM dimming logic falling edge is ignored for both internal and external PWM until soft-start is complete or the control loop approaches steady state. Table 4 summarizes operating conditions that can trigger a fault, and/or turn off switching at the PWMTG and GATE pins.

**Table 4. Conditions and Effects on $\overline{FAULT}$, PWMTG and GATE**

| TYPE | CONDITION | $\overline{FAULT}$ | PWMTG OFF | GATE OFF |
|---|---|---|---|---|
| Overvoltage | $V_{FB}$ > 1.26V | Yes | Yes | Yes |
| Open LED | 1.14V < $V_{FB}$ < 1.26V and $V_{ISP–ISN}$ < 25mV | Yes | No | No |
| Short LED | $V_{FB}$ < 300mV | Yes | Yes | Yes |
| Overcurrent | $V_{ISP–ISN}$ > 670mV | Yes | Yes | Yes |
| PWM OFF | PWM < 500mV, or CTRL < 300mV, or IADJ < 500mV | No | Yes | Yes |
| $INTV_{CC}$ UVLO | $INTV_{CC}$ < 4.3V | No | Yes | Yes |
| Thermal Shutdown | $T_J$ > 170°C | No | Yes | Yes |
| Above Voltage Regulation | 1.26V > $V_{FB}$ > 1.20V | No | No | Yes |
| Above Current Regulation | 0.67V > $V_{ISP–ISN}$ > 0.25V (or Set by Equation 2) | No | No | Yes |

### SOFT-START

To prevent a surge of current at start-up, LT8356-1 uses an internal soft-start. This feature affects both current limit and switching frequency. At start-up, the system will switch at around 20% of the switching frequency $f_{SW}$ with near zero current limit. As the clock runs, both constraints relax, leading to normal operation after around 256 switching periods. When a LED overcurrent occurs, or, in steady state, when short LED conditions occur, the part immediately stops switching and enters a cooldown period. The cooldown period lasts for at least 2048 switching periods. At the end of the cooldown period, the system attempts to start again, and enters soft-start as if

## APPLICATIONS INFORMATION

it had just been powered on for the first time. Regardless of whether it is the first soft-start after power-on or a soft-start resulting from a fault condition, LT8356-1 will wait until the first PWM dimming pulse arrives before beginning to power on the system. This PWM pulse can be from an external source or from the internal dimming PWM generator. At the arrival of the first PWM pulse, soft-start begins, and operation continues until the system has reached steady state. Until the system either finishes soft-start or observes the internal control loop state nearing steady state, the PWM low logic state is ignored, and the part runs continuously.

### USING THE EN/UVLO PIN

The EN/UVLO pin offers two modes of operation. First, it can be driven high (above 1.4V) or low (below 0.3V) to act as an enable pin, turning the part on and off. In addition to this, the pin can also be used to create an accurate external under voltage lockout (UVLO). To use this feature, connect the EN/UVLO pin to a resistive voltage divider from the $V_{IN}$ pin to ground. Select resistors to program the desired minimum $V_{IN}$ value for operation (see Equation 11 and Figure 7).

$$V_{IN(FALLING)} = 1.25V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right)$$
$$V_{IN(RISING)} = 1.31V \bullet \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) + 2.3\mu A \bullet R_{UV1} \quad (11)$$

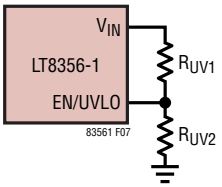



**Figure 7. LT8356-1 Resistor Network for Accurate UVLO**

The EN/UVLO threshold has a hysteresis window to prevent oscillating between the on and off states. When the EN/UVLO pin falls below its falling threshold (1.25V typical), switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the Pulse Width Modulation (PWM) Dimming section, the load is disconnected from the output capacitor. While the part is not enabled a current of 2.3µA flows into the EN/UVLO pin to allow for programmable hysteresis. Choose the value of the upper resistor $R_{UV1}$ in the EN/UVLO voltage divider such that around 2.3µA ($R_{UV1}$) provides the desired hysteresis.

### LOW VOLTAGE (SEPIC) START-UP

Certain power stage topologies, such as the SEPIC, may require the part to start-up in the condition where ISP and ISN are both near (or at) 0V. The LED current sense amplifier will continue to command the LED current programmed by CTRL and IADJ all the way down to 0V on ISP. However, recall that ISP provides the positive rail for the driver of the external disconnect PMOS. Therefore, the use of low side sensing of LED current is not recommended for applications that use PWM dimming or for any boost configuration applications requiring output short circuit protection.

### PLANNING FOR THERMAL SHUTDOWN

The LT8356-1 automatically shuts down when the internal temperature is above 170°C (typical). This shutdown is guaranteed to always be outside of the operating region of the device. The effects of thermal shutdown are like that of the load faults: switching stops, soft-start is reset, and if an external PMOS is used according to instructions in the Pulse Width Modulation (PWM) Dimming section, the load is disconnected from the output capacitor. The exposed pad is ground, and must be soldered to a good, large ground plane with many vias to aid thermal management. Since LT8356-1 controls power components and does not itself conduct any meaningful portion of the load current, power dissipation in the LT8356-1 may be lower than a monolithic converter. Power dissipation will increase with $V_{IN}$ and switching frequency. Die temperature will increase with power dissipation. Higher ambient temperature applications will not be able to dissipate as much power, and high power dissipation in any condition may over stress die temperature.

# APPLICATIONS INFORMATION

## PCB LAYOUT GUIDELINES AND INFORMATION

Printed Circuit Board (PCB) layout profoundly affects performance of all power applications. Proper electrical and thermal connection of the IC and power components with the outside world will mean the difference between success or failure of any system. Do not neglect spending adequate design time on the layout of any application PCB. The exposed ground pad on the bottom of the package must be soldered to a ground plane.

The switch current sense resistor $R_{SENSE}$ should connect to a large, unbroken ground plane. The ground terminal of the switch current sense resistor should be Kelvin connected to the SENSE pin of LT8356-1. Connect the $INTV_{CC}$ bypass capacitor from the $INTV_{CC}$ pin directly to the exposed pad by the shortest route possible. Analog and control functions such as $V_C$, PWM, CTRL, IADJ, and $V_{REF}$ should have a separate ground plane, which includes the exposed pad of the IC. The power and analog ground planes should meet only in a Kelvin connection to the exposed pad and at the power input to the PCB.

Be sure to design proper ground planes for power and analog functions within the application PCB. Ground planes should not be interrupted by other traces, and should be continuous, very wide sheets of copper. Connect the exposed pad of the IC to such a ground plane. Use as many vias as will fit in the exposed pad area to make the connection. Filled or capped vias may ease soldering for the exposed pad area. Do not copy any layout for the exposed pad connection, but instead use as many vias as will fit given the capabilities of the PCB fab house.

In addition to soldering down the exposed pad, it is critical to provide a good, robust layout for the power path. Use wide traces for $V_{IN}$ and to connect to the load. Keep the LED and switch current sense resistors close to the IC and ensure that the ISP and ISN traces run as close to one another as possible. It is strongly recommended not to allow ISP and ISN to take different paths to the LED current sense resistor, but instead to keep them beside one another as much as possible. Minimize the total area of any switching node (SW) traces, keep the output capacitor and external catch diode as close as possible to the external NMOS switch and switch current sense resistor to help this. Finally, use wide traces to connect to the external PMOS switch, if used. Note, however, that the gates of both external switches can be connected by narrower trace. Except for the external switch gates, avoid vias where possible in the power path. If vias are truly unavoidable, use many in parallel. Proper PCB layout is critical for suppressing radiated and conducted Electromagnetic interference (EMI). Minimizing the area of the SW node will decrease the amount of capacitance that the switch sees, and thus reduce the current spike seen during switching events. Failing to minimize the area of the so-called hot loop will dramatically degrade EMI performance. Keep the output capacitor and catch diode as close as possible to the external NMOS switch and switch current sense resistor to help this. For more information about hot loops see Analog Devices Application Notes AN136 and AN139.

An example 2-layer layout which takes the above considerations into account is provided in Figure 8. It is imperative that the layout of any PCB carefully consider the capabilities of the PCB manufacturer and other application constraints. The example provided here should guide the layout of an application PCB. If the application or manufacturing capabilities mandate a different layout, be sure to keep the above guidance in mind for all changes. Note that the 4-layer layout is recommended for best performance. Please contact the factory for the reference layout design.

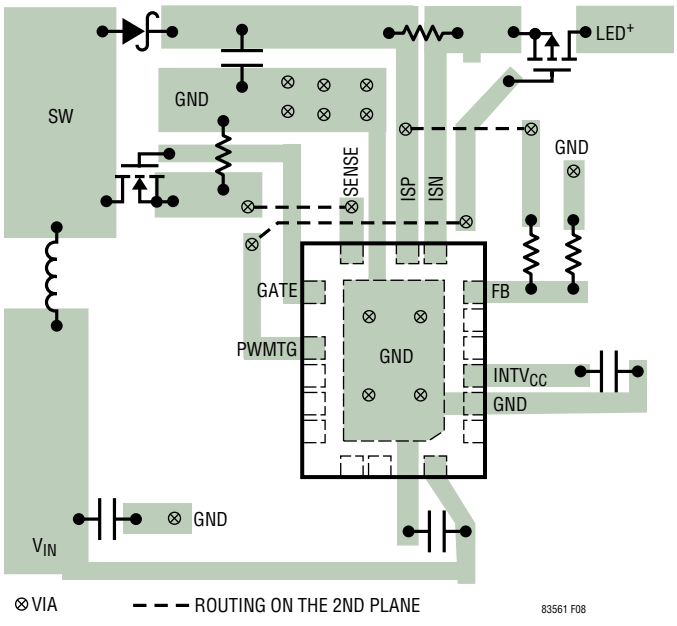
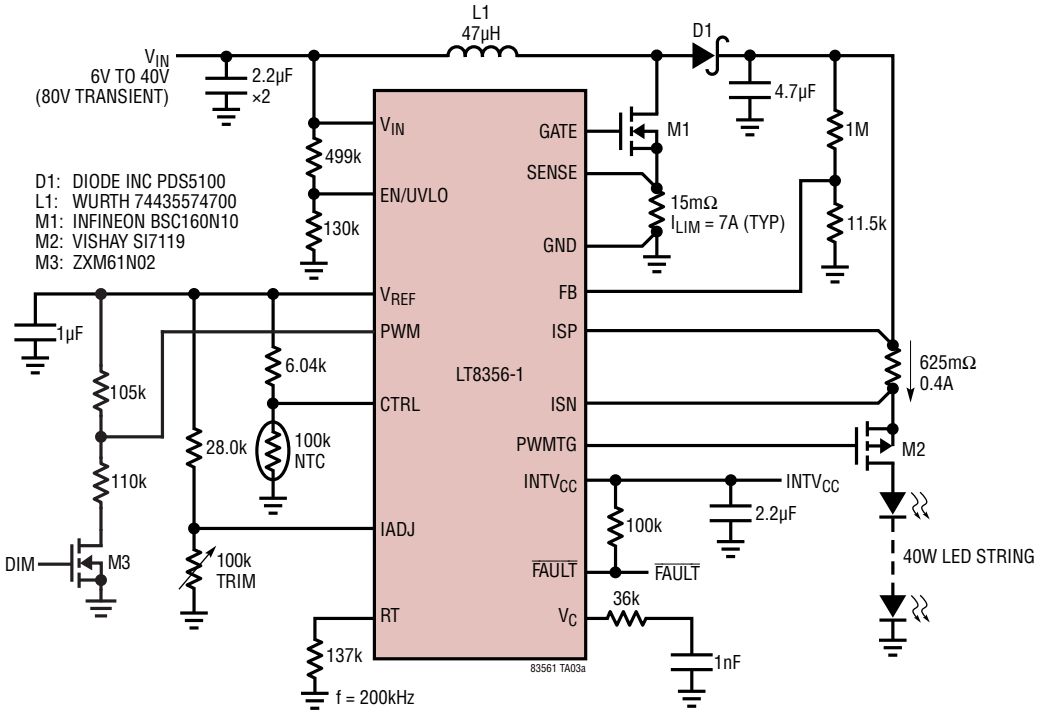


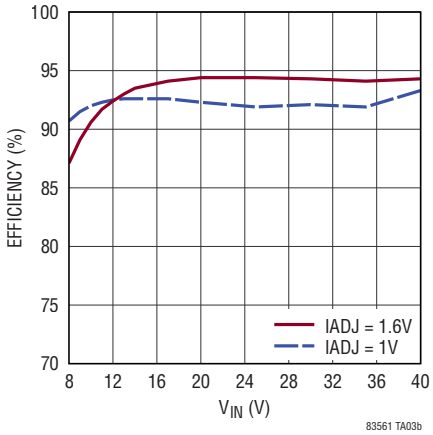

**Figure 8. Reference Layout for LT8356-1**

# TYPICAL APPLICATIONS

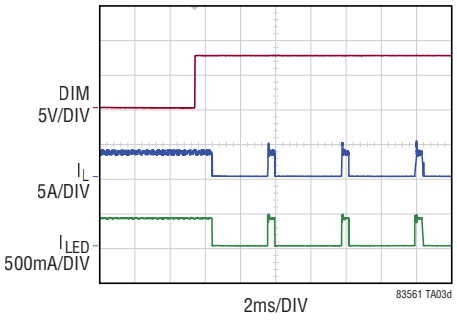
### 40W Boost LED Driver with Thermal Derating and Trim with Selectable 10% Internal PWM Dimming



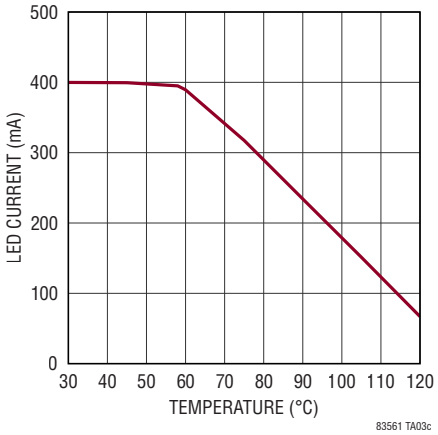

### Efficiency vs $V_{IN}$




### Enabling 10% Internal PWM Dimming

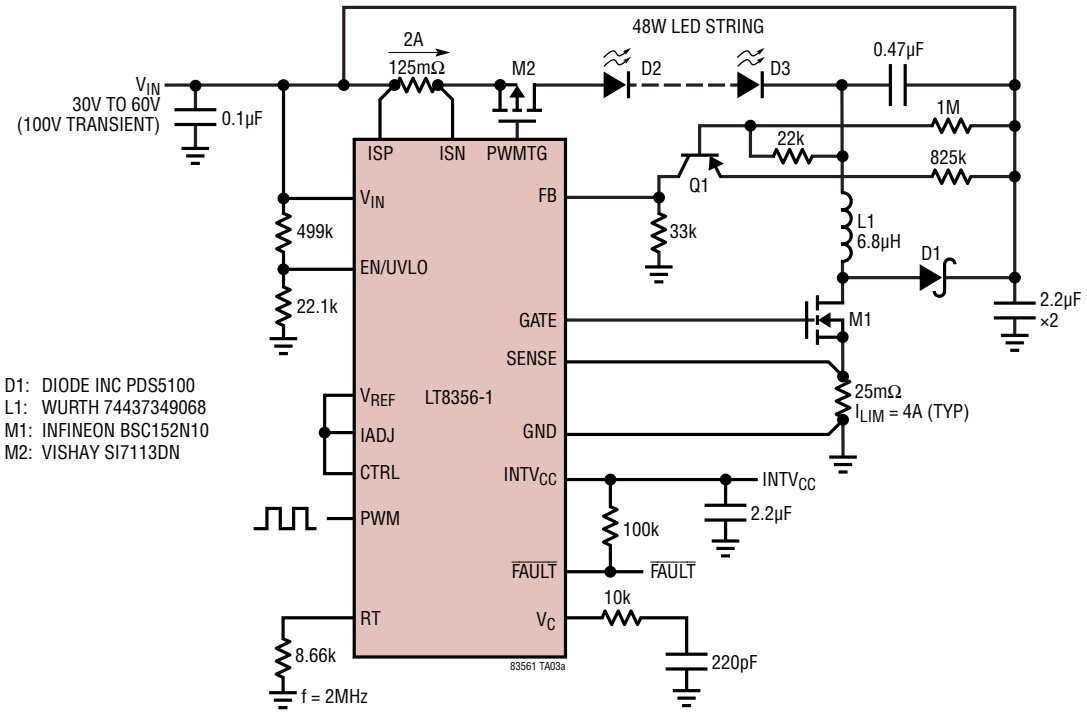



### LED Current Thermal Derating

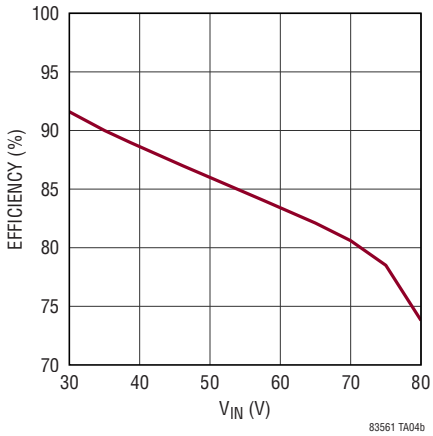


# TYPICAL APPLICATIONS

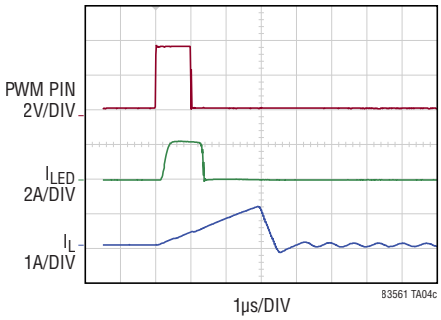
### 48W, 2MHz Buck-Mode LED Driver with High Dynamic Range PWM Dimming




### Efficiency vs $V_{IN}$

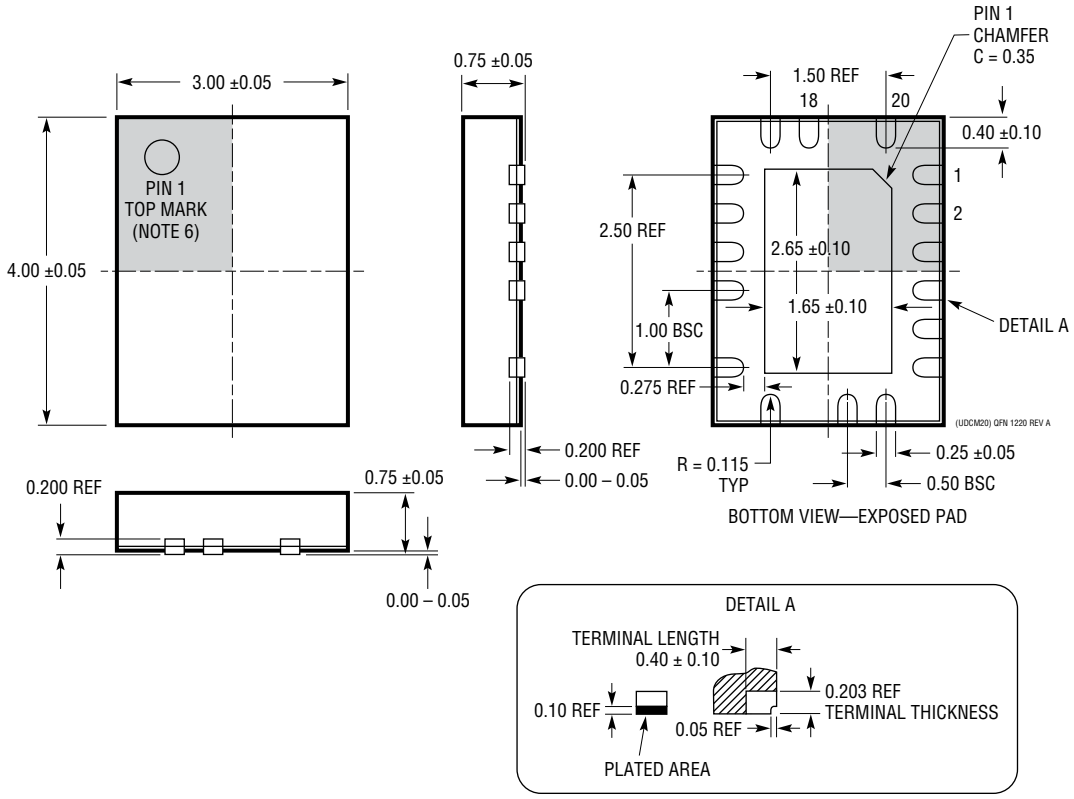



### 10,000:1 PWM Dimming at $f_{PWM}$ = 100Hz

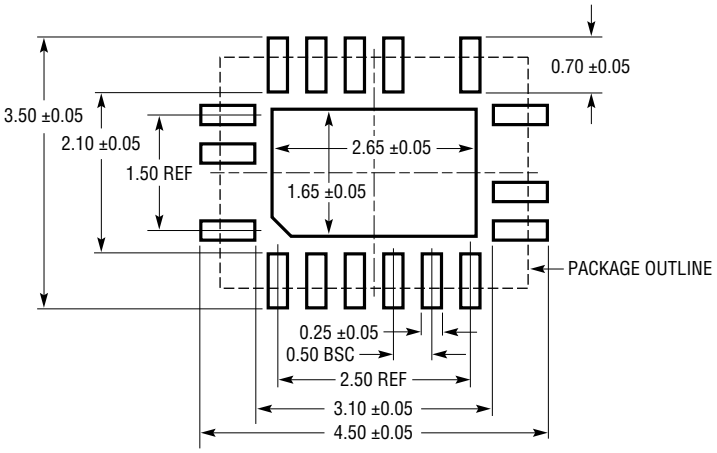


# PACKAGE DESCRIPTION

**UDCM Package**
**20-Lead Plastic Side Solderable QFN (3mm × 4mm)**
(Reference LTC DWG # 05-08-1793 Rev A)




NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED