

# Four-Channel Transimpedance Amplifier with Output Multiplexing

## FEATURES

- 600MHz –3dB Bandwidth with 0.5pF Input Capacitance
- Differential Output with Up to 2V<sub>P-P</sub> Swing into 100Ω Differential Load
- Built-In High-Speed ADC Driver with Output MUX
- Selectable 22.2/16.7/11.1/5.55kΩ Transimpedance Gain
- 1.8pA/3.7pA/√Hz Input Current Noise Density 100MHz/600MHz (0.5pF)
- 65nA<sub>RMS</sub> Integrated Input-Referred Current Noise Over 600MHz (0.5pF)
- Large Linear Input Current Range 0μA to 90μA
- Large Transient Overload Current >1A Peak
- Fast Overload Recovery: 2.5ns
- Fast Channel Switching: 10ns
- Power Dissipation: 194mW to 325mW on 3.3V, Varies with Output Mode (13mW in Shutdown)
- Output MUX allows multiple LTC6563s to Create 8, 12, 16 ... 32 Channel Solutions
- 3mm × 5mm, 24-Lead QFN Package, Wettable Flanks
- AECQ-100 Grade 1 Qualified (Pending)

## APPLICATIONS

- Automotive LIDAR Receiver
- Industrial LIDAR Receiver

## DESCRIPTION

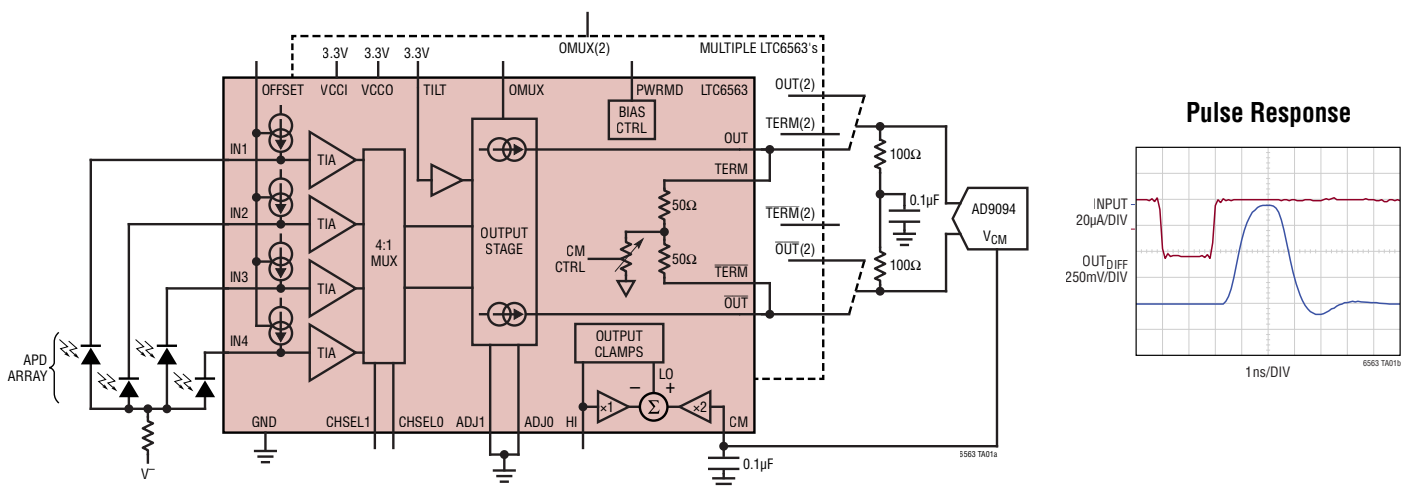
The LTC<sup>®</sup>6563 is a low-noise four-channel transimpedance amplifier (TIA) with 600MHz bandwidth. The LTC6563 TIA's low noise, wide linear range, and low power dissipation are ideal for LIDAR receivers using Avalanche photodiodes (APDs) and photodiodes (PDs). The amplifier features selectable 22.2/16.7/11.1/5.55kΩ Transimpedance gain (RT) and 90μA linear input current range. Using an APD with a total input capacitance of 0.5pF, the input current noise density is 1.8pA/√Hz at 100MHz and 3.7pA/√Hz at 600MHz. The LTC6563 consumes between 194mW and 325mW on a 3.3V supply depending on output mode. An internal 4-to-1 MUX simplifies the system design. In addition, external multiplexing capability allows channel expansion up to 64 channels, saving space and power. Fast overload recovery and fast channel switchover make the LTC6563 well suited for LIDAR receivers with multiple APDs. The built-in high-speed differential ADC driver can swing as much as 2V<sub>P-P</sub> while driving into 100Ω external differential load.

The LTC6563 is packaged in a 3mm × 5mm 24-pin exposed pad QFN package with wettable flanks.

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## TYPICAL APPLICATION

Typical Application with DC-Coupled Inputs Driving an ADC



# LTC6563

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage:

$V_{CCI}$  to GND ..... 3.6V

$V_{CCO}$  to GND ..... 3.6V

Input Current (CHSELO, CHSEL1, ADJ0, ADJ1, PWRMD, OMUX, CM, HI, OFFSET, TILT) .....  $\pm 10\text{mA}$

Amplifier Inputs (IN1, IN2, IN3, IN4):

Voltage .....  $-0.3\text{V}$  to  $3.6\text{V}$

Current .....  $10\mu\text{A}$  /  $-400\text{mA}_{\text{RMS}}$

Current (Note 5) .....  $-1\text{A}$  Transient

Amplifier Outputs (OUT,  $\overline{\text{OUT}}$ ):

Voltage .....  $-0.3\text{V}$  to  $3.6\text{V}$

Current .....  $\pm 100\text{mA}$

Amplifier Output Termination (TERM,  $\overline{\text{TERM}}$ ):

Voltage .....  $-0.3\text{V}$  to  $3.6\text{V}$

Current .....  $-72\text{mA}/6\text{mA}$

Operating Temperature Range:

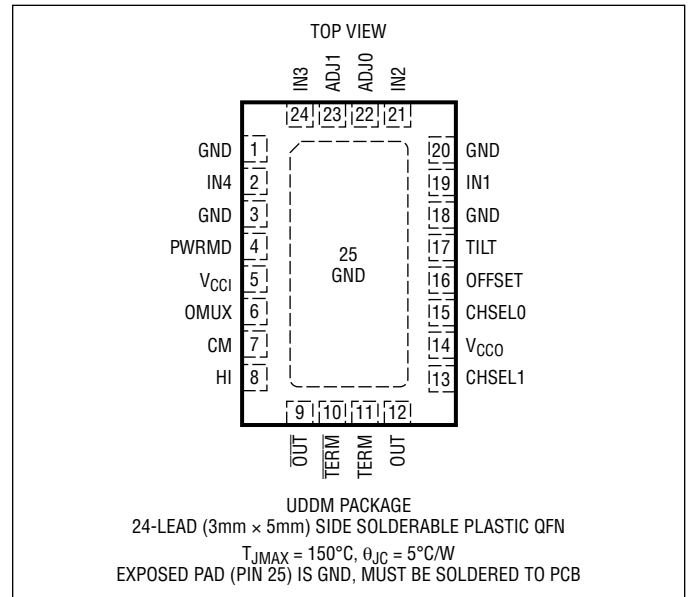
LTC6563I (Note 2) .....  $-40^\circ\text{C}$  to  $85^\circ\text{C}$

LTC6563H (Note 3) .....  $-40^\circ\text{C}$  to  $125^\circ\text{C}$

Storage Temperature Range .....  $-65^\circ\text{C}$  to  $150^\circ\text{C}$

Junction Temperature .....  $150^\circ\text{C}$

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6563IUDDM#PBF	LTC6563IUDDM#TRPBF	LHMH	24-Lead (3mm × 5mm) Side Solderable Plastic QFN	$-40^\circ\text{C}$ to $85^\circ\text{C}$
LTC6563HUDDM#PBF	LTC6563HUDDM#TRPBF	LHMH	24-Lead (3mm × 5mm) Side Solderable Plastic QFN	$-40^\circ\text{C}$ to $125^\circ\text{C}$

Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

[Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**AC ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $\text{ADJ0} = \text{ADJ1} = \text{PWRMD} = \text{OMUX} = \text{V}_{\text{CCI}} = \text{HI} = \text{V}_{\text{CCO}} = 3.3\text{V}$ ,  $\text{TILT} = \text{OFFSET} = 0$ ,  $\text{V}_{\text{CM}} = 1.5\text{V}$ . All other input pins are floating unless stated otherwise.  $\text{V}_{\text{OUTCM}}$  is defined as  $(\text{OUT} + \overline{\text{OUT}})/2$  and  $\text{V}_{\text{OUTDIFF}}$  is defined as  $(\text{OUT} - \overline{\text{OUT}})$ ,  $\text{R}_{\text{L\_EXT}} = 100\Omega$  differential,  $\text{OUT}$  connected to  $\text{TERM}$  and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
BW	-3dB Bandwidth	$200\text{mV}_{\text{P-P,OUT}}$ and $\text{C}_{\text{IN,TOT}} = 0.5\text{pF}$		600		MHz
SR	Slew Rate	$\text{C}_{\text{IN,TOT}} = 0.5\text{pF}$		3000		V/us
$t_{\text{R}}/t_{\text{F}}$	Rise/Fall Time	$\text{C}_{\text{IN,TOT}} = 0.5\text{pF}$		0.6		ns
$\text{R}_{\text{T}}$ Differential	Small Signal Transimpedance	$I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ00}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ01}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ10}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ11}$	4.9 9.6 14.1 18.1	5.55 11.1 16.7 22.2	6.5 12.5 18.2 23.4	$\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$
$\text{TCR}_{\text{T}}$	Transimpedance Temperature Coefficient	$I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ00}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ01}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ10}$ $I_{\text{IN}} < 2\mu\text{A}_{\text{P-P}}$ , $\text{ADJ11}$		-0.00125 -0.00246 -0.00403 -0.00609		$\text{k}\Omega/^\circ\text{C}$ $\text{k}\Omega/^\circ\text{C}$ $\text{k}\Omega/^\circ\text{C}$ $\text{k}\Omega/^\circ\text{C}$
$\text{R}_{\text{IN}}$	Input Impedance	$f = 100\text{kHz}$ Active Channel $f = 100\text{kHz}$ Inactive Channel		225 409		$\Omega$ $\Omega$
$\text{R}_{\text{TERM\_DIFF}}$	Internal Diff Termination Impedance	Measured from $\text{TERM}$ to $\text{TERMBAR}$		100		$\Omega$
$I_{\text{n}}$	Input Current Noise Density	$f = 100\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 200\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 300\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 400\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 500\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 600\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$		1.8 2.3 2.5 3 3.4 3.7		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
	Integrated Input Current Noise	$f = 0.1\text{MHz}$ to $100\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 0.1\text{MHz}$ to $200\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 0.1\text{MHz}$ to $300\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 0.1\text{MHz}$ to $400\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 0.1\text{MHz}$ to $500\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$ $f = 0.1\text{MHz}$ to $600\text{MHz}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$		19 27 36 45 55 65		$\text{nA}_{\text{RMS}}$ $\text{nA}_{\text{RMS}}$ $\text{nA}_{\text{RMS}}$ $\text{nA}_{\text{RMS}}$ $\text{nA}_{\text{RMS}}$ $\text{nA}_{\text{RMS}}$
$t_{\text{RECOVER}}$	Overload Recovery and Pulse Extension	$I_{\text{IN}} = -4\text{mA}$ , $\text{C}_{\text{IN\_TOT}} = 0.5\text{pF}$		2.5		ns
$t_{\text{CH\_SWITCH}}$	Channel Switching Time	Any Channel to Any Channel		10		ns
$t_{\text{OMUX\_SWITCH}}$	Output MUX Switching Time	OMUX		20		ns
Isolation	Channel to Channel Isolation	$400\text{MHz}$ , $\text{PWRMD} = \text{Logic Low}$ , Selected Channel to Any Unselected Channel		48		dB

**DC ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $\text{ADJ0} = \text{ADJ1} = \text{PWRMD} = \text{OMUX} = \text{V}_{\text{CCI}} = \text{HI} = \text{V}_{\text{CCO}} = 3.3\text{V}$ ,  $\text{TILT} = \text{OFFSET} = 0$ ,  $\text{V}_{\text{CM}} = 1.5\text{V}$ . All other input pins are floating unless stated otherwise.  $\text{V}_{\text{OUTCM}}$  is defined as  $(\text{OUT} + \overline{\text{OUT}})/2$  and  $\text{V}_{\text{OUTDIFF}}$  is defined as  $(\text{OUT} - \overline{\text{OUT}})$ ,  $\text{R}_{\text{L\_EXT}} = 100\Omega$  differential,  $\text{OUT}$  connected to  $\text{TERM}$  and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>IN1, IN2, IN3, IN4 Pins</b>						
$\text{V}_{\text{IN}}$	Input Bias Voltage	Active Channel Inactive Channel		0.8 0.7		V V
$I_{\text{IN}}$	DC Input Current Range	Tilt = $0\text{V}$ Tilt = $3.3\text{V}$		40 90		$\mu\text{A}$ $\mu\text{A}$
<b>OUT and <math>\overline{\text{OUT}}</math> Pins</b>						
$\text{V}_{\text{OCM\_DEFAULT}}$	Default Output Common-Mode Voltage	$\text{ADJ} = 00$		0.9		V
$\text{V}_{\text{OOD}}$	Differential Output Offset Voltage	$I_{\text{IN}} = 0\mu\text{A}$	-75	$\pm 10$	75	mV
$\text{TCV}_{\text{OOD}}$	Differential Output Offset Voltage Temperature Coefficient	$I_{\text{IN}} = 0\mu\text{A}$		-0.044		$\text{mV}/^\circ\text{C}$

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{SWINGDIFF}}$	Differential Output Voltage Swing	$I_{\text{IN}} = 0$ to $-200\mu\text{A}$ , Tilt = 3.3V	● 1.13	1.50		$V_{\text{P-P}}$ $V_{\text{P-P}}$
		$I_{\text{IN}} = 0$ to $-90\mu\text{A}$ , Tilt = 3.3V, $R_{\text{L\_EXT}} = 75\Omega$ SE on Each Output with Center Grounded (see Figure 3)		2.4		$V_{\text{P-P}}$
$V_{\text{OUTLOW}}$	Output Voltage Swing Low	Single-Ended Measurement, $I_{\text{IN}} = 0$ to $-200\mu\text{A}$ , Tilt = 3.3V		1.02		V
$V_{\text{OUTHIGH}}$	Output Voltage Swing High	Single-Ended Measurement, $I_{\text{IN}} = 0$ to $-200\mu\text{A}$ , Tilt = 3.3V		2.2		V
$V_{\text{COMPLIANCE}}$	Output Voltage Compliance	Single-Ended Measurement, $I_{\text{IN}} = 0$ to $-200\mu\text{A}$ , Tilt = 3.3V	2.0	$V_{\text{CC0}} - 1$		V

#### Output Common Mode Voltage Control (CM Pin)

$A_{\text{CM}}$	CM Pin Voltage Gain, CM Pin to Differential OUT	$V_{\text{CM}} = 1.5\text{V}$ to $1.7\text{V}$	0.95	1	1.05	V/V
$\text{TCA}_{\text{CM}}$	$A_{\text{CM}}$ Temperature Coefficient			9.3		$(\mu\text{V/V})/^\circ\text{C}$
$V_{\text{CM\_DEFAULT}}$	Default CM Pin Voltage			0.9		V
$V_{\text{CM\_OS}}$	Common Mode Offset Voltage	$V_{\text{OUTCM}} - V_{\text{CM}}$	-50	10	20	mV
$\text{TC}_{\text{VCM\_OS}}$	Common Mode Offset Voltage Temperature Coefficient	$V_{\text{OUTCM}} - V_{\text{CM}}$		-0.021		$\text{mV}/^\circ\text{C}$
$V_{\text{OUTCM\_MIN}}$	$V_{\text{OUTCM}}$ Minimum Voltage	$V_{\text{CM}} = 0\text{V}$ , $\text{ADJ00}$		0.38	0.43	V
$V_{\text{OUTCM\_MAX}}$	$V_{\text{OUTCM}}$ Maximum Voltage	$V_{\text{CM}} = 2.6\text{V}$ , $\text{ADJ11}$	2.2	2.3		V
$R_{\text{CM}}$	CM Pin Input Resistance			16.3		$\text{k}\Omega$
$C_{\text{CM}}$	CM Pin Input Capacitance			1.5		pF

#### Output Clamping (HI Pin) See Note 4

$V_{\text{HI\_DEFAULT}}$	Default HI Pin Voltage			1.8		V
$V_{\text{HI\_VOS}}$	High Side Clamp Offset Voltage	$V_{\text{OUT(MAX)}} - V_{\text{HI}}$ , $\text{HI} = 1.7\text{V}$ , $I_{\text{IN}} = -200\mu\text{A}$	-160	-65	25	mV
$V_{\text{LO\_VOS}}$	Low Side Clamp Offset Voltage	$V_{\text{OUTBAR(MIN)}} - (2 \cdot V_{\text{CM}} - V_{\text{HI}})$ , $\text{HI} = 1.7\text{V}$ , $I_{\text{IN}} = -200\mu\text{A}$	-50	50	150	mV
$R_{\text{HI}}$	HI Pin Input Impedance			13.6		$\text{k}\Omega$
$C_{\text{HI}}$	HI Pin Input Capacitance			1.5		pF

#### Input Current Cancellation (OFFSET Pin)

$V_{\text{OFFSET\_DEFAULT}}$	Default OFFSET Pin Voltage			0		V
$I_{\text{CANCEL\_MIN}}$	Minimum Input Cancellation Current	$V_{\text{OFFSET}} = 0\text{V}$		0		$\mu\text{A}$
$I_{\text{CANCEL\_MAX}}$	Maximum Input Cancellation Current	$V_{\text{OFFSET}} = 3.3\text{V}$ , Tilt = 3.3V	200	240		$\mu\text{A}$
$G_{\text{OFFSET}}$	OFFSET Pin Transconductance (OFFSET Pin Voltage to Input Offset Current)	$V_{\text{OFFSET}} = 0.2\text{V}$ to $0.4\text{V}$ , $I_{\text{IN}} = -40\mu\text{A}$	-145	-110	-75	$\mu\text{A}/\text{V}$
$R_{\text{OFFSET}}$	OFFSET Pin Impedance			6.6		$\text{k}\Omega$
$t_{\text{S\_OFFSET}}$	Offset Voltage to Output Settling	1% of Final Value, $I_{\text{IN}} = -40\mu\text{A}$		100		ns

#### Output Offset (TILT Pin)

$V_{\text{TILT\_DEFAULT}}$	Default Tilt Pin Voltage			2		mV
$A_{\text{TILT}}$	TILT Pin Slope, TILT to Differential Out	$V_{\text{TILT}} = 0.2\text{V}$ to $0.4\text{V}$	-1.25	-1	-0.7	V/V
$\text{TCA}_{\text{TILT}}$	$A_{\text{TILT}}$ Temperature Coefficient	$V_{\text{TILT}} = 0.2\text{V}$ to $0.4\text{V}$		-680		$(\mu\text{V/V})/^\circ\text{C}$
$R_{\text{TILT}}$	TILT Pin Input Impedance			22.7		$\text{k}\Omega$

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>ADJ0, ADJ1, CHSELO, CHSEL1 Pins with Internal Pull-Down Resistors</b>							
$\text{V}_{\text{IL}}$	Input Low Voltage					0.8	V
$\text{V}_{\text{IH}}$	Input High Voltage			2.4			V
$\text{I}_{\text{IL}}$	Input Low Current	Pin Voltage = 0.8V			3.8		$\mu\text{A}$
$\text{I}_{\text{IH}}$	Input High Current	Pin Voltage = 2.4V			7.2		$\mu\text{A}$
$\text{C}_{\text{IN}}$	Pin Input Capacitance				1.5		pF
$\text{R}_{\text{IN}}$	Pin Input Impedance	To GND			218		k $\Omega$
<b>OMUX, PWRMD, Pins with Internal Pull-Up Resistors</b>							
$\text{V}_{\text{IL}}$	Input Low Voltage					0.8	V
$\text{V}_{\text{IH}}$	Input High Voltage			2.4			V
$\text{I}_{\text{IL}}$	Input Low Current	Pin Voltage = 0.8V			-12		$\mu\text{A}$
$\text{I}_{\text{IH}}$	Input High Current	Pin Voltage = 2.4V			-8.6		$\mu\text{A}$
$\text{C}_{\text{IN}}$	Pin Input Capacitance				1.5		pF
$\text{R}_{\text{IN}}$	Pin Input Impedance	To $\text{V}_{\text{CCI}}$			208		k $\Omega$
<b>Power Supply</b>							
$\text{V}_{\text{S}}$	Operating Supply Range			3.15	3.3	3.45	V
$\text{I}_{\text{VCCI}}$	Input Supply Current	Any Adjust Setting	●	27.8	34	39.4 40.4	$\text{mA}$ $\text{mA}$
$\text{I}_{\text{VCCI\_SHUTDOWN}}$	Input Supply Current	$\text{PWRMD} = \text{OMUX} = \text{Logic Low}$	●		4.5	5.5 6	$\text{mA}$ $\text{mA}$
$\text{I}_{\text{VCC0}}$	Output Supply Current	$\text{ADJ1} = \text{Logic High}, \text{ADJ0} = \text{Logic High}$ $\text{V}_{\text{CM}} = 1.50\text{V}$	●	49.4	64.5	81 82	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic High}, \text{ADJ0} = \text{Logic Low}$ $\text{V}_{\text{CM}} = 1.25\text{V}$	●		51.5	64.9 65.9	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic Low}, \text{ADJ0} = \text{Logic High}$ $\text{V}_{\text{CM}} = 1.0\text{V}$	●		38	48 49	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic Low}, \text{ADJ0} = \text{Logic Low}$ $\text{V}_{\text{CM}} = 0.75\text{V}$	●		24.5	30.8 31.8	$\text{mA}$ $\text{mA}$
$\text{I}_{\text{VCC0\_SHUTDOWN}}$	Output Supply Current	$\text{PWRMD} = \text{OMUX} = \text{Logic Low}$	●		0.1	0.2 0.22	$\text{mA}$ $\text{mA}$
$\text{I}_{\text{S}}$	Total Supply Current ( $\text{I}_{\text{S}(\text{VCCI})} + \text{I}_{\text{S}(\text{VCC0})}$ )	$\text{ADJ1} = \text{Logic High}, \text{ADJ0} = \text{Logic High}$ $\text{V}_{\text{CM}} = 1.50\text{V}$	●		98.5	120.4 122.4	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic High}, \text{ADJ0} = \text{Logic High}$ $\text{V}_{\text{CM}} = 1.25\text{V}$	●		85.5	104.3 106.3	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic Low}, \text{ADJ0} = \text{Logic High}$ $\text{V}_{\text{CM}} = 1.0\text{V}$	●		72	87.4 89.4	$\text{mA}$ $\text{mA}$
		$\text{ADJ1} = \text{Logic Low}, \text{ADJ0} = \text{Logic Low}$ $\text{V}_{\text{CM}} = 0.75\text{V}$	●		58.5	70.2 72.2	$\text{mA}$ $\text{mA}$
$\text{I}_{\text{S\_SHUTDOWN}}$	Total Supply Current ( $\text{I}_{\text{S}(\text{VCCI})} + \text{I}_{\text{S}(\text{VCC0})}$ )	$\text{PWRMD} = \text{OMUX} = \text{Logic Low}$	●		4.6	5.8 6.3	$\text{mA}$ $\text{mA}$
$\text{PSRR}(\text{V}_{\text{CCI}})$	Input Power Supply Rejection Ratio ( $\Delta\text{V}_{\text{OUT}}/\Delta\text{V}_{\text{CCI}}$ )	$\text{V}_{\text{CCI}} = 3.15\text{V to } 3.45\text{V}, \text{V}_{\text{CC0}} = 3.3\text{V}$		33	36		dB
$\text{PSRR}(\text{V}_{\text{CC0}})$	Output Power Supply Rejection Ratio ( $\Delta\text{V}_{\text{OUT}}/\Delta\text{V}_{\text{CC0}}$ )	$\text{V}_{\text{CC0}} = 3.15\text{V to } 3.45\text{V}, \text{V}_{\text{CCI}} = 3.3\text{V}$		35	38		dB

## DC ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6563I is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

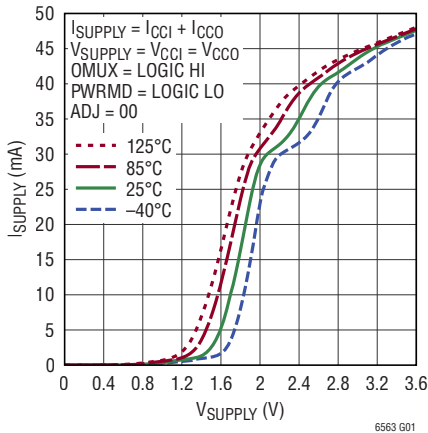
**Note 3:** The LTC6563H is guaranteed to meet specified performance from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**Note 4:** HI pin voltage should be at least  $0.2\text{V}$  higher than  $V_{\text{CM}}$ .

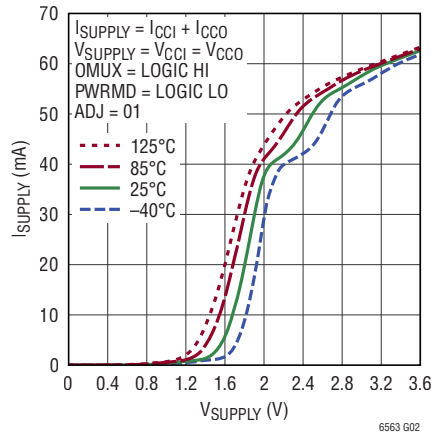
**Note 5:** This parameter is specified by design and/or characterization and is not tested in production.

**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at  $\text{CHSEL0} = \text{TILT} = \text{OFFSET} = 0\text{V}$ ,  $\text{HI} = \text{CHSEL1} = \text{PWRMD} = \text{ADJ0} = \text{ADJ1} = V_{\text{CCI}} = V_{\text{CCO}} = 3.3\text{V}$ , and  $\text{CM} = 1.5\text{V}$ .  $V_{\text{OUTCM}}$  is defined as  $(\text{OUT} + \overline{\text{OUT}})/2$  and  $V_{\text{OUTDIFF}}$  is defined as  $(\text{OUT} - \overline{\text{OUT}})$ ,  $R_{\text{L\_EXT}} = 100\Omega$  differential,  $\text{OUT}$  connected to  $\text{TERM}$  and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

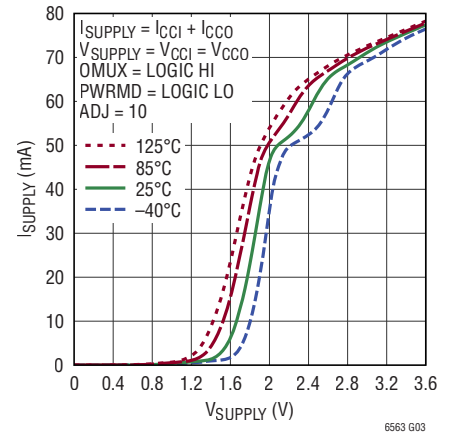
**$I_{\text{SUPPLY}}$  vs  $V_{\text{SUPPLY}}$  Over Temperature**



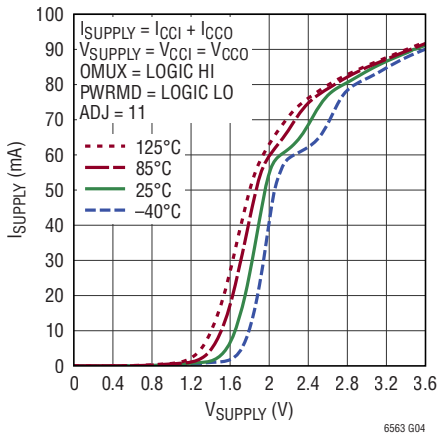
**$I_{\text{SUPPLY}}$  vs  $V_{\text{SUPPLY}}$  Over Temperature**



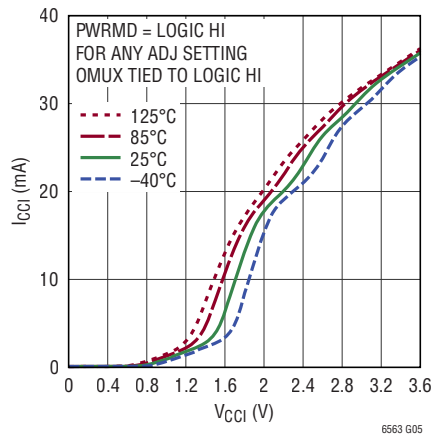
**$I_{\text{SUPPLY}}$  vs  $V_{\text{SUPPLY}}$  Over Temperature**



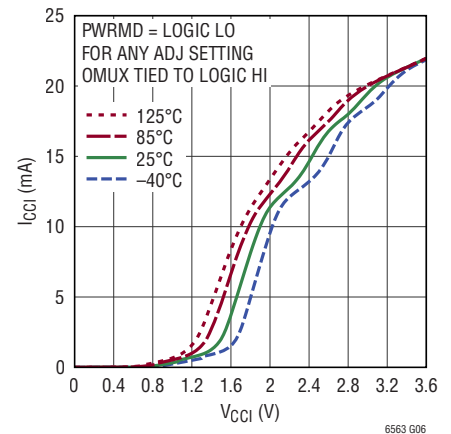
**$I_{\text{SUPPLY}}$  vs  $V_{\text{SUPPLY}}$  Over Temperature**



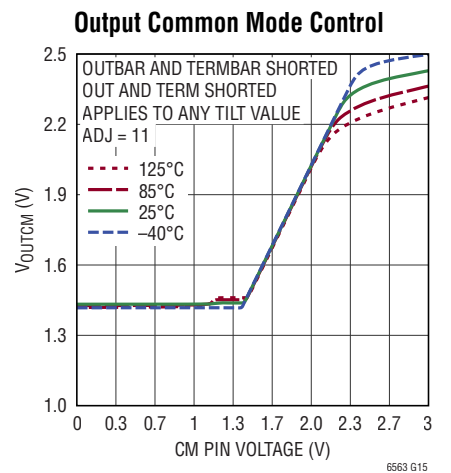
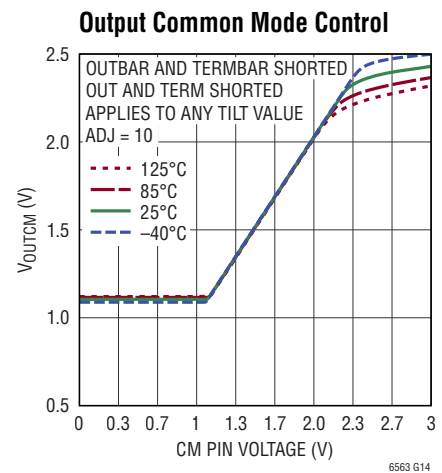
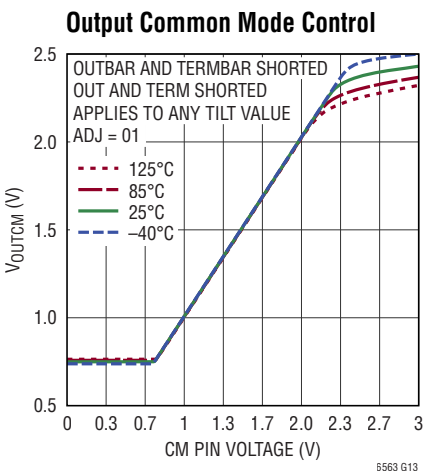
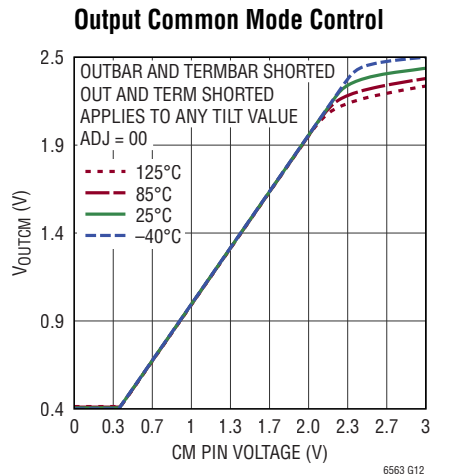
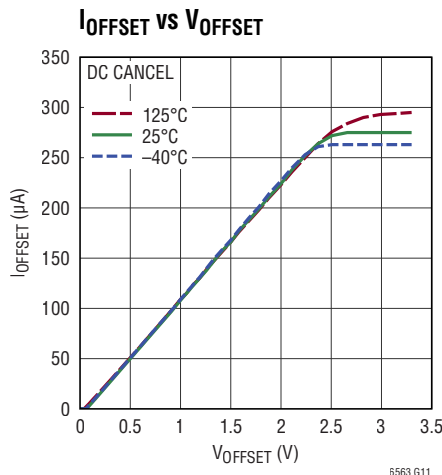
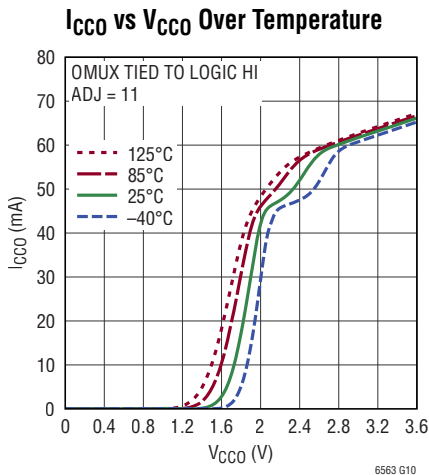
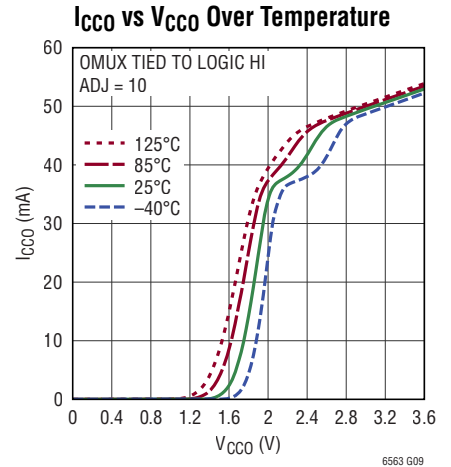
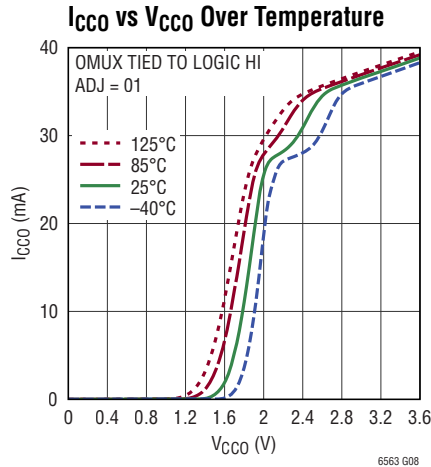
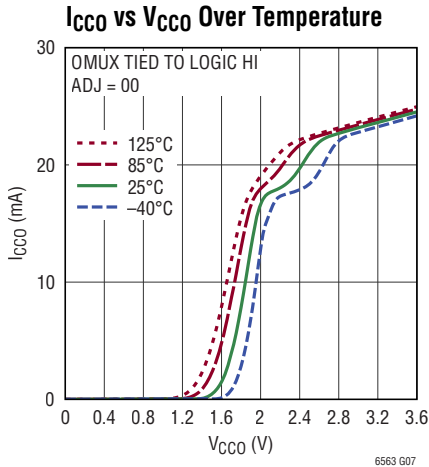
**$I_{\text{CCI}}$  vs  $V_{\text{CCI}}$  Over Temperature**



**$I_{\text{CCO}}$  vs  $V_{\text{CCO}}$  Over Temperature**

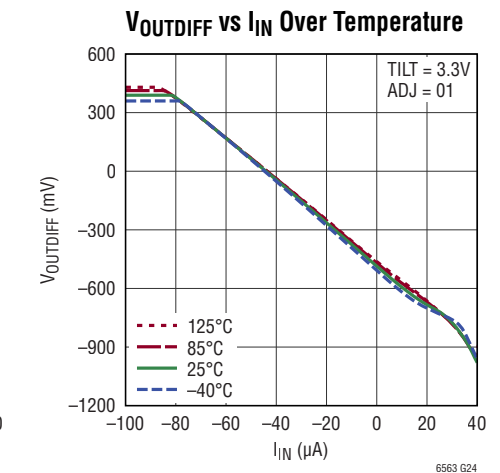
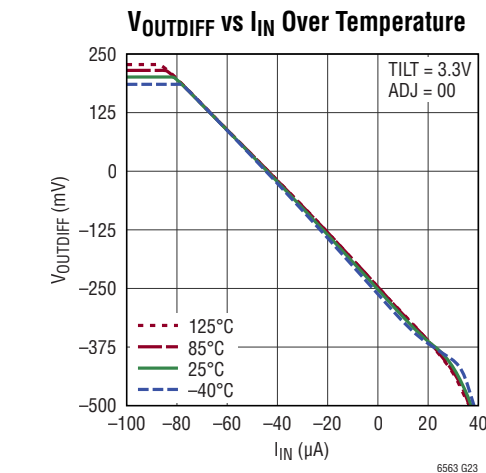
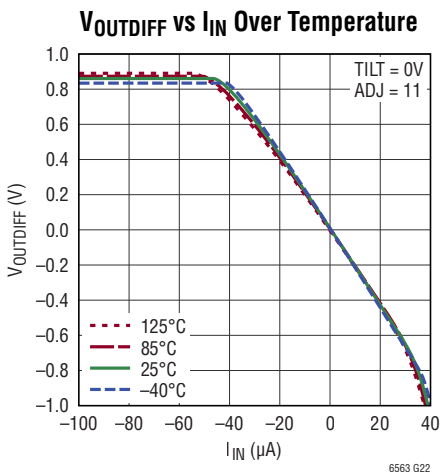
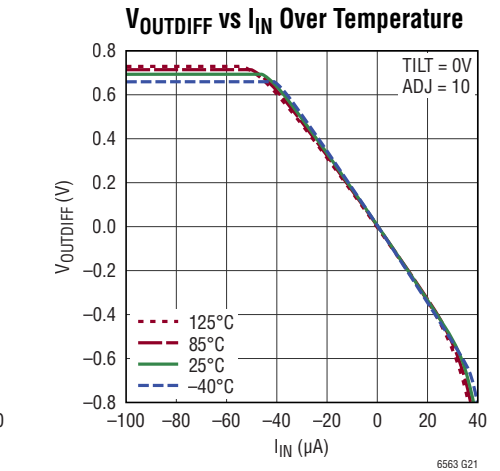
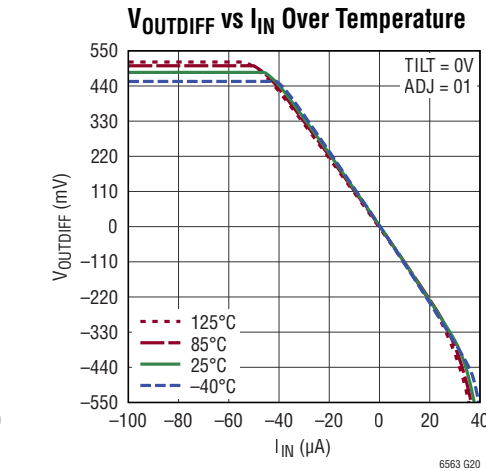
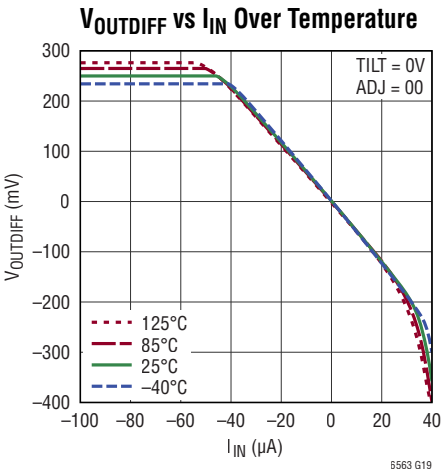
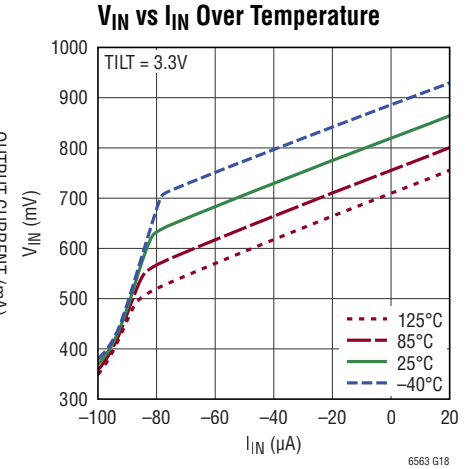
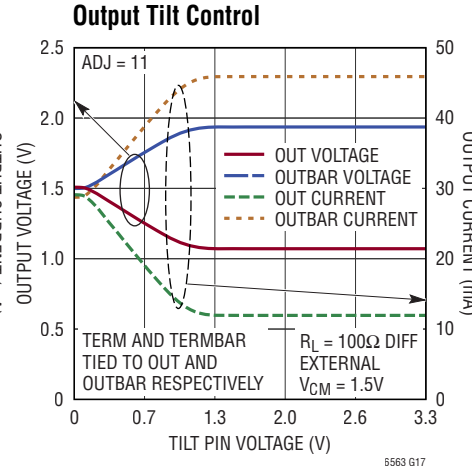
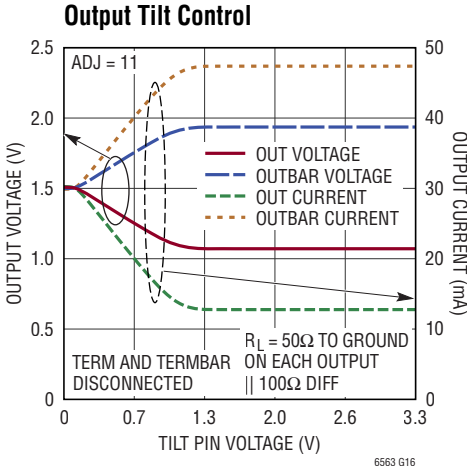


**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSELO = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJO = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .



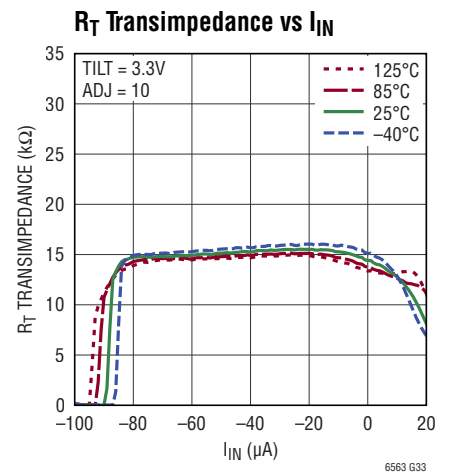
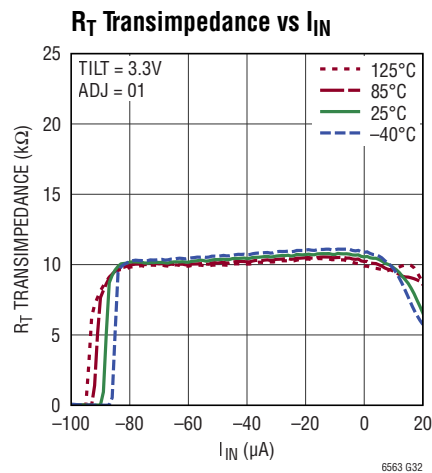
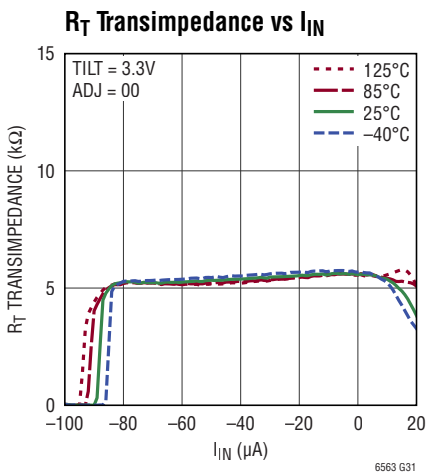
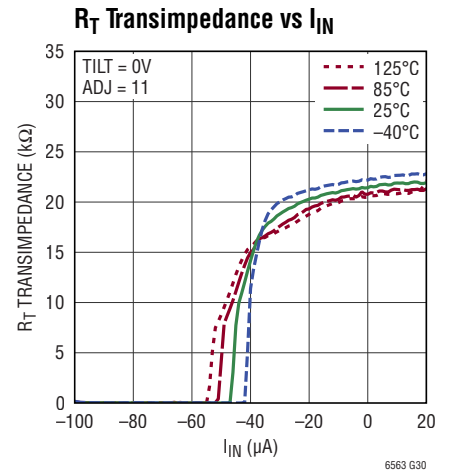
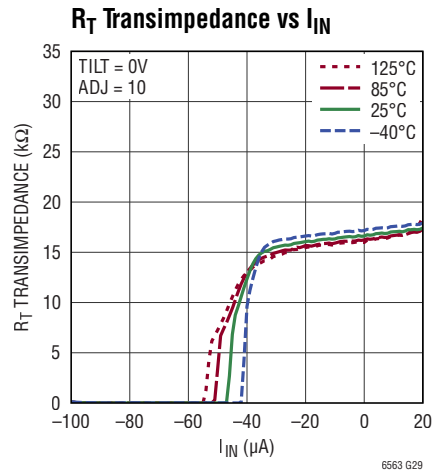
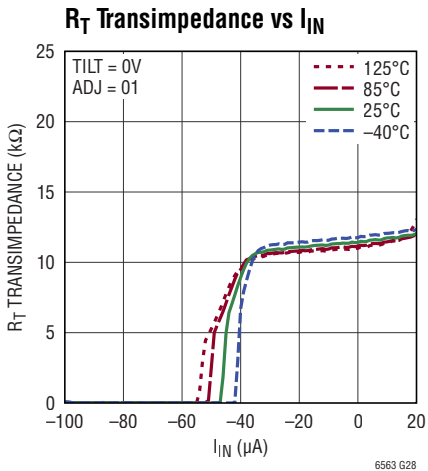
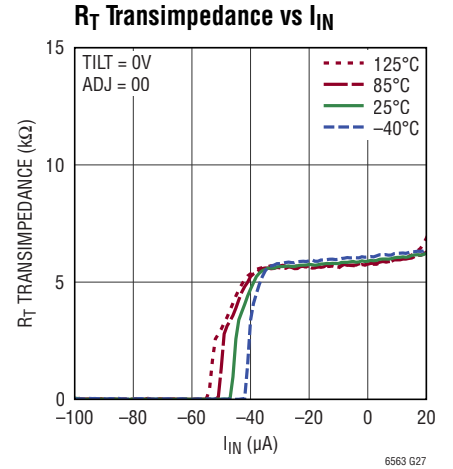
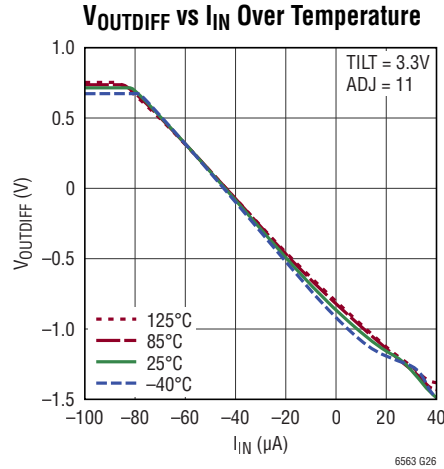
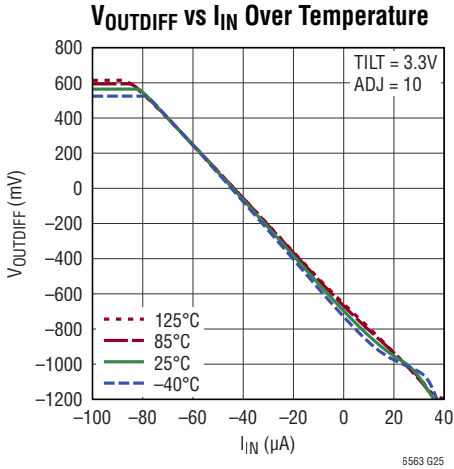
## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L\_EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

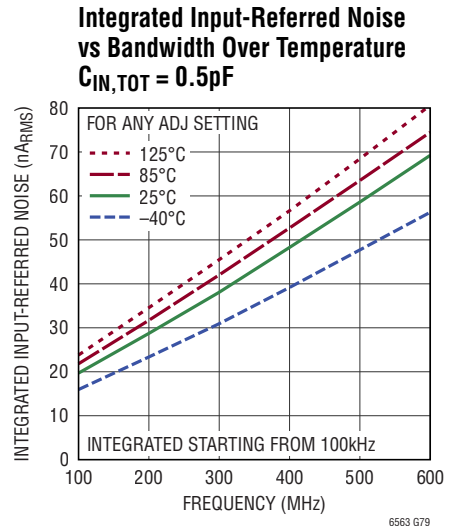
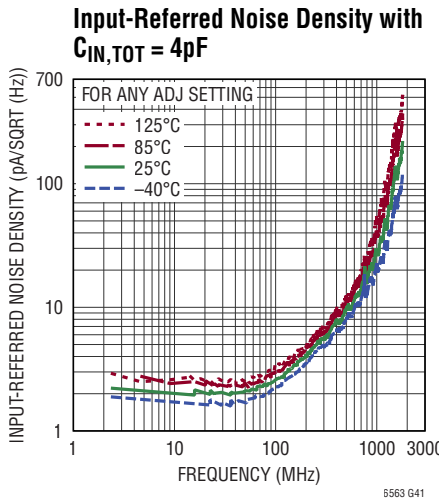
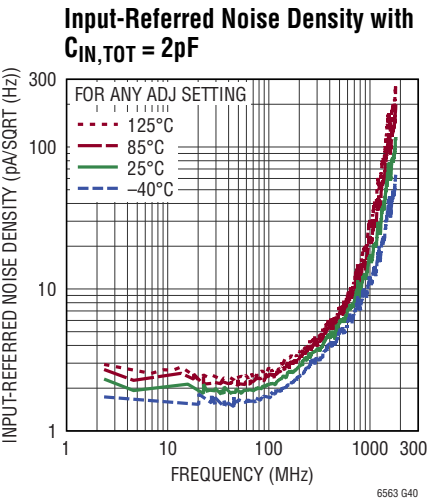
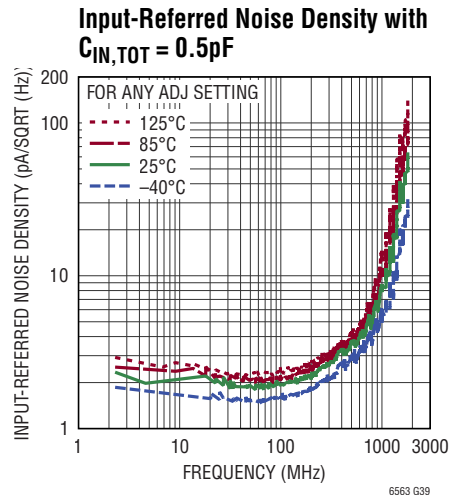
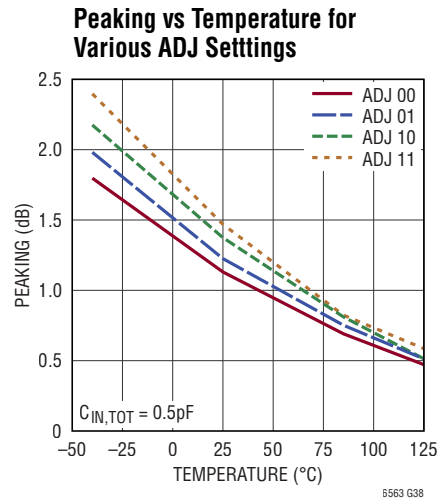
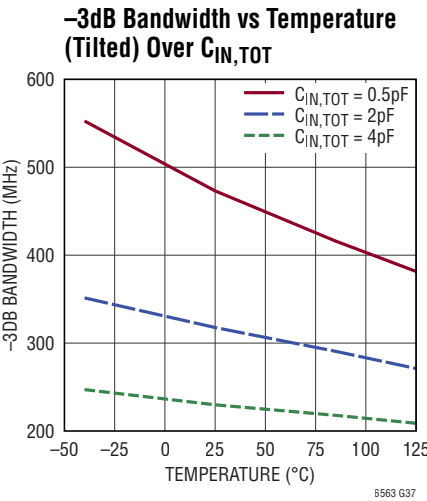
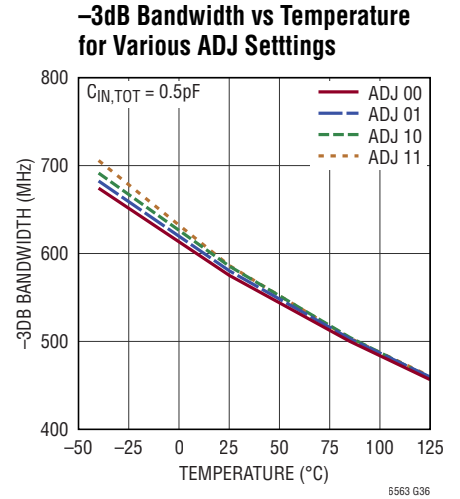
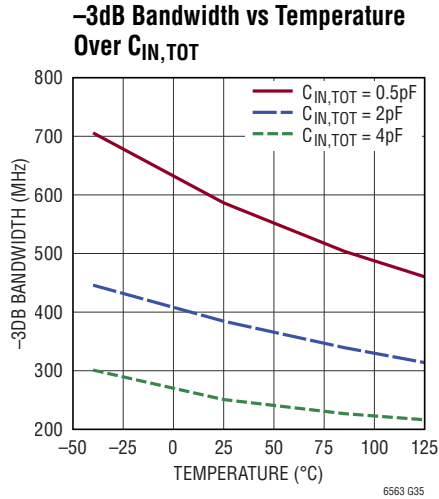
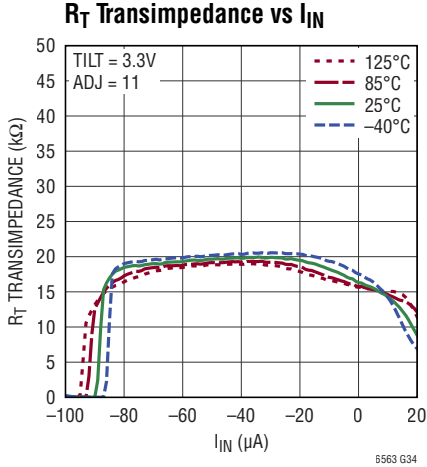




**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSELO = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

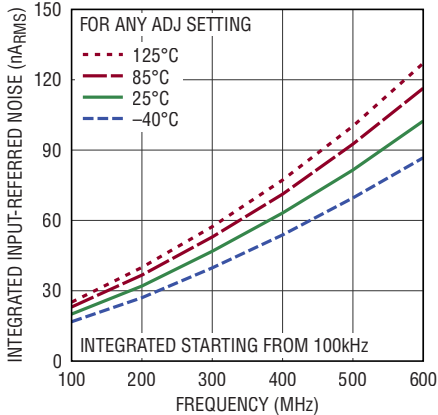


**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .



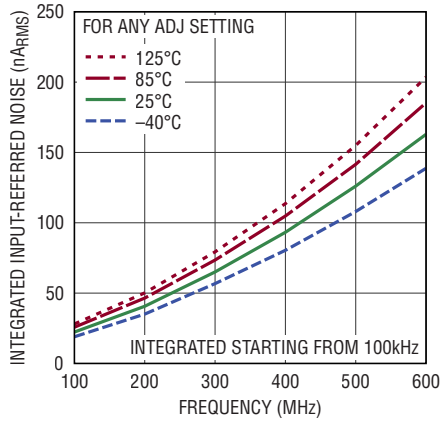
**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

**Integrated Input-Referred Noise vs Bandwidth Over Temperature**  
C<sub>IN,TOT</sub> = 2pF



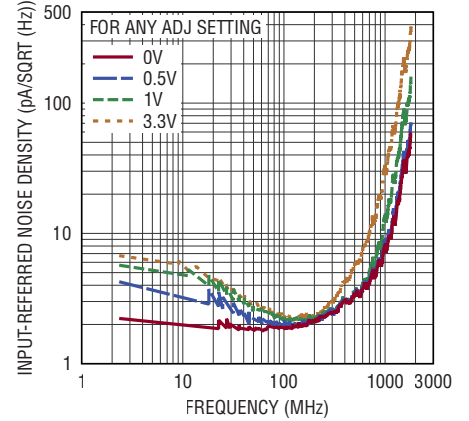
6563 G42

**Integrated Input-Referred Noise vs Bandwidth Over Temperature**  
C<sub>IN,TOT</sub> = 4pF



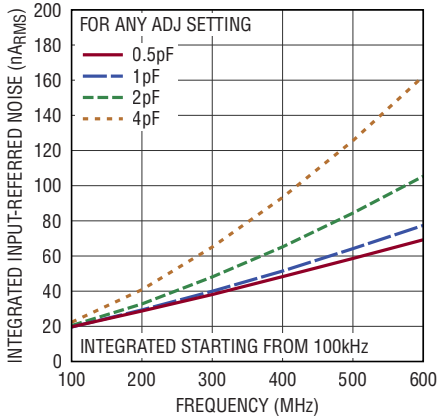
6563 G43

**Input-Referred Noise Density for various Tilt Voltages with**  
C<sub>IN,TOT</sub> = 0.5pF



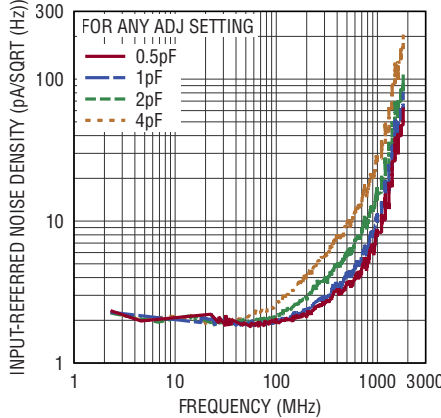
6563 G44

**Integrated Input-Referred Noise vs Bandwidth for various C<sub>IN,TOT</sub>**



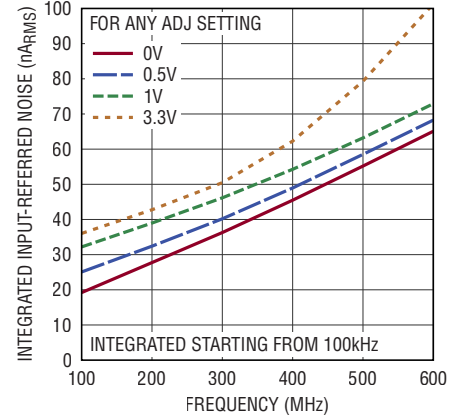
6563 G45

**Input-Referred Noise Density for various C<sub>IN,TOT</sub>**



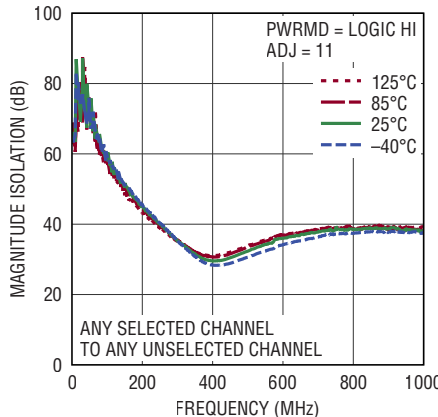
6563 G46

**Integrated Input-Referred Noise for various Tilt Voltages with**  
C<sub>IN,TOT</sub> = 0.5pF



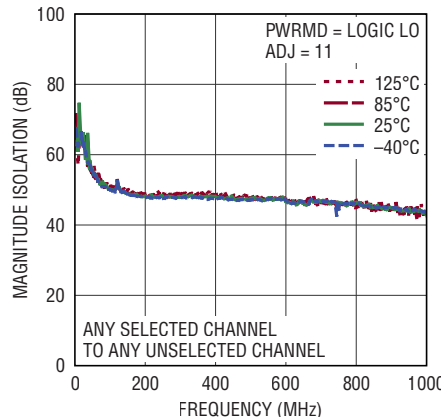
6563 G47

**Channel to Channel Isolation vs Frequency Over Temperature**



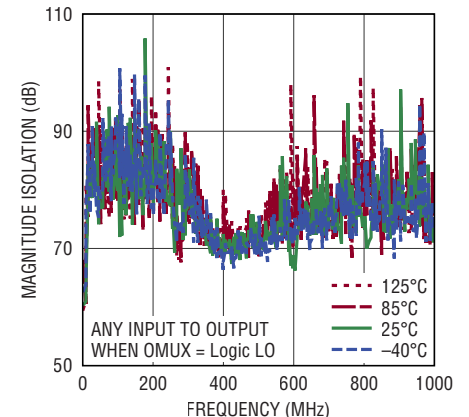
6563 G48

**Channel to Channel Isolation vs Frequency Over Temperature**



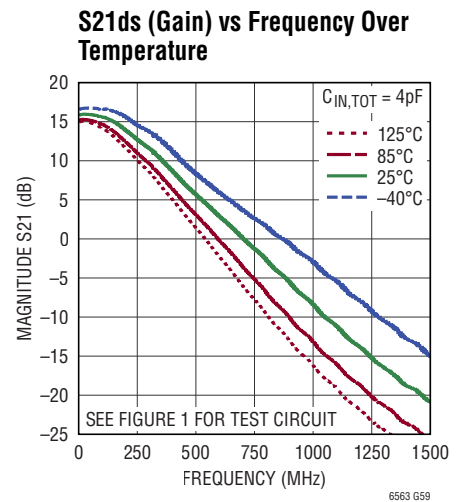
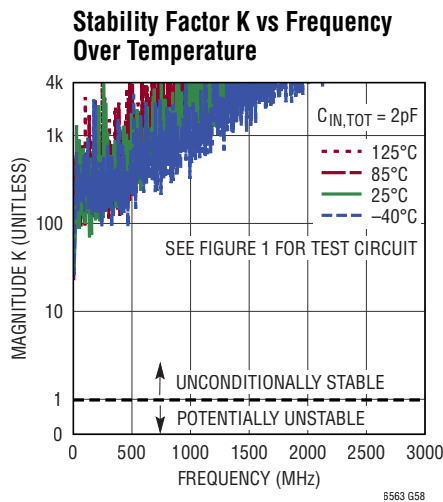
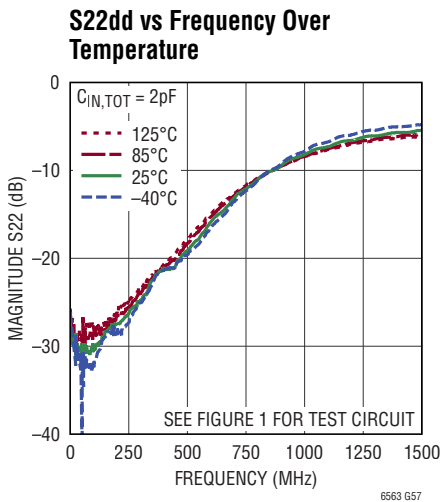
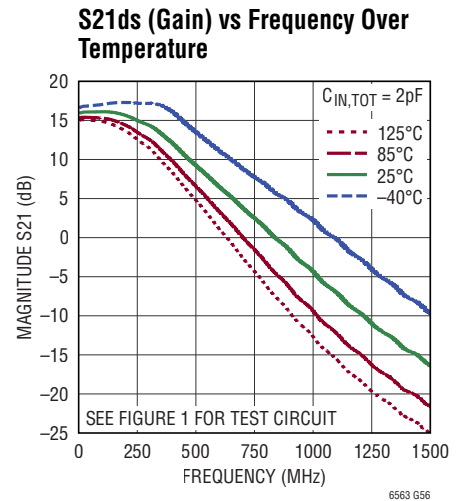
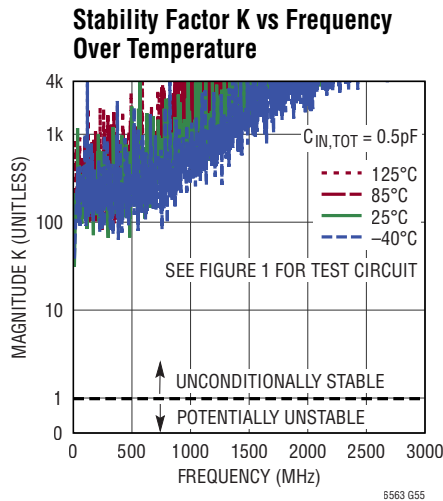
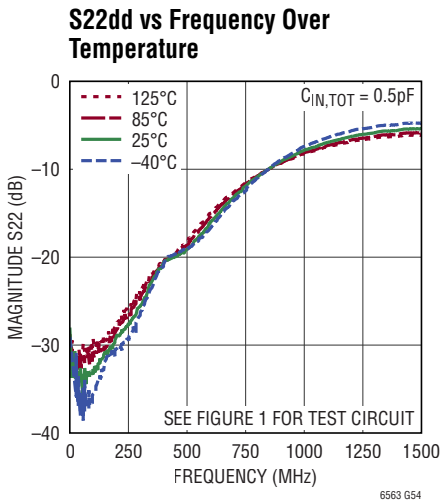
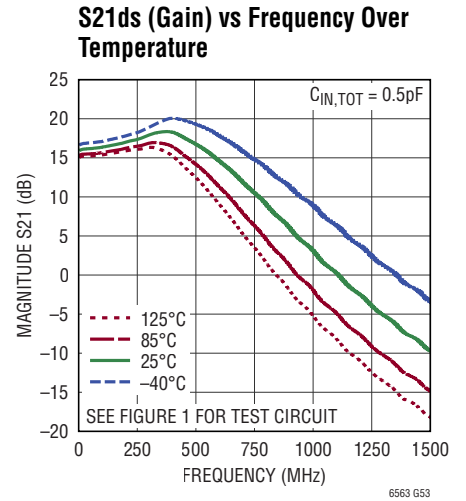
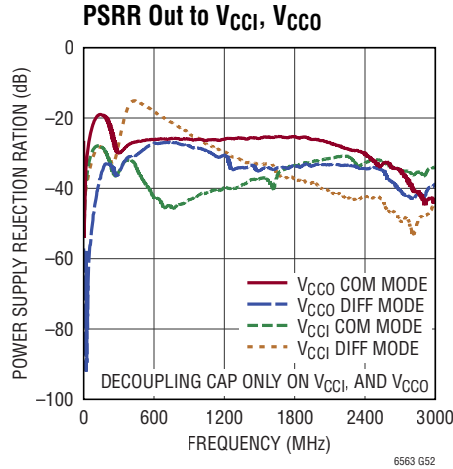
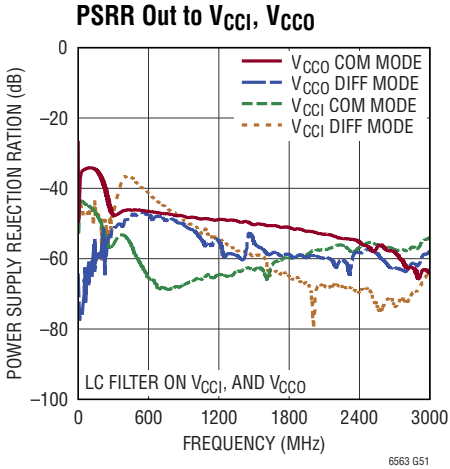
6563 G49

**OMUX Isolation vs Frequency Over Temperature**



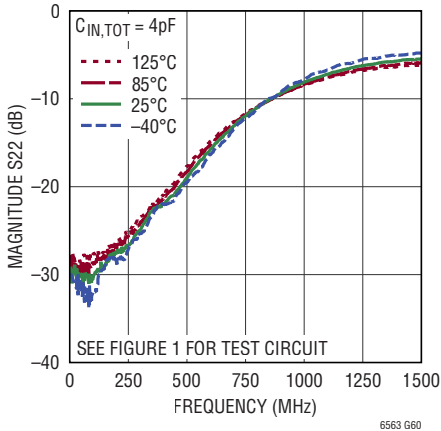
6563 G50

**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

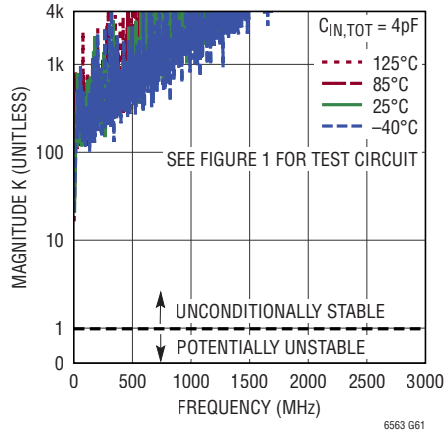


**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSEL0 = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJO = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

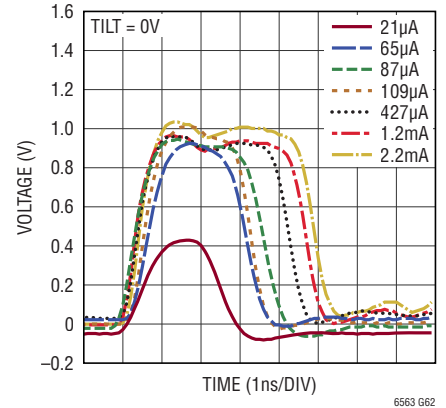
**S22dd vs Frequency Over Temperature**



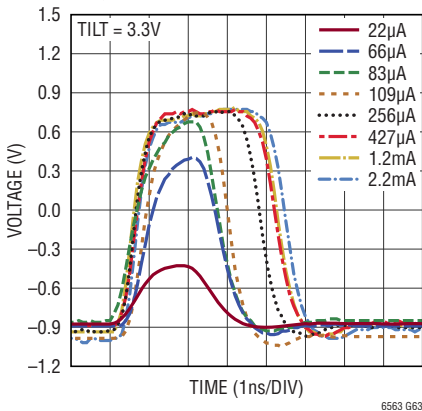
**Stability Factor K vs Frequency Over Temperature**



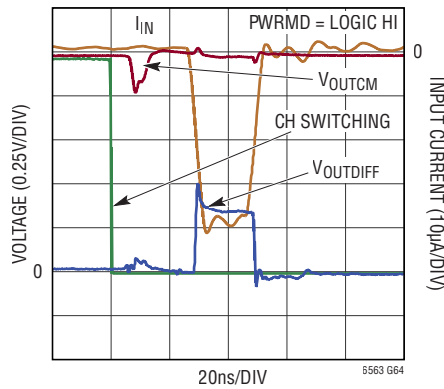
**Pulse Response for Various I<sub>IN</sub> C<sub>IN,TOT</sub> = 1pF, 2ns Pulse Width**



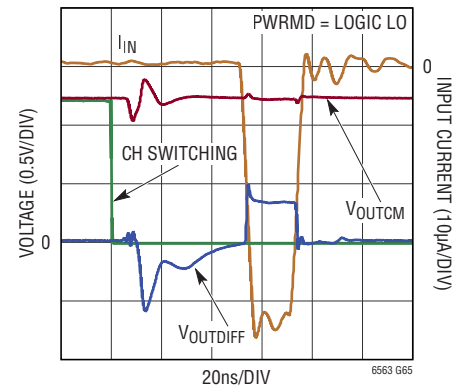
**Pulse Response for Various I<sub>IN</sub> C<sub>IN,TOT</sub> = 1pF, 2ns Pulse Width**



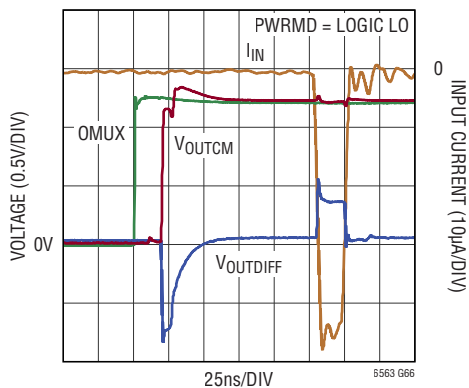
**Channel Switching Time**



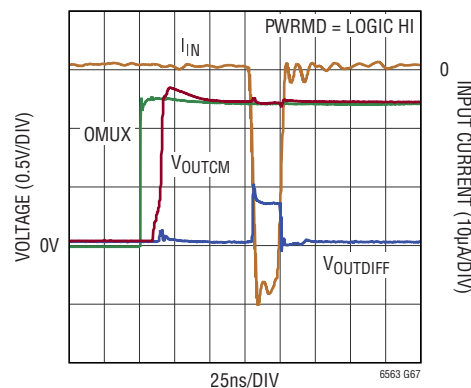
**Channel Switching Time**



**OMUX Switching Time**

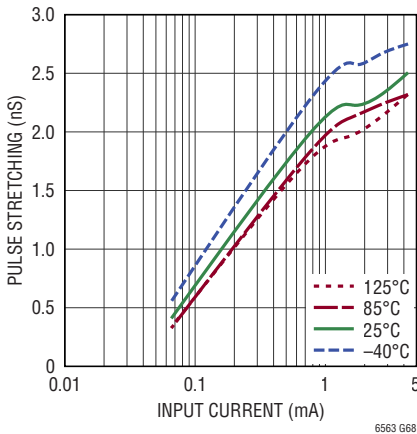


**OMUX Switching Time**

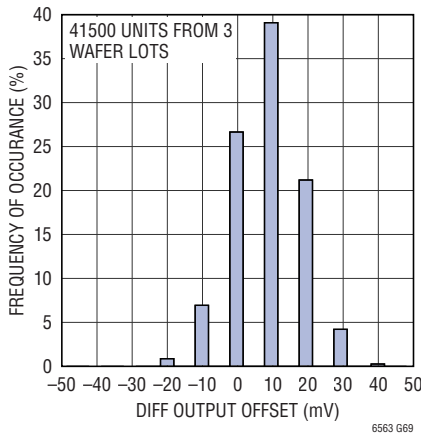


**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSELO = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJO = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L,EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

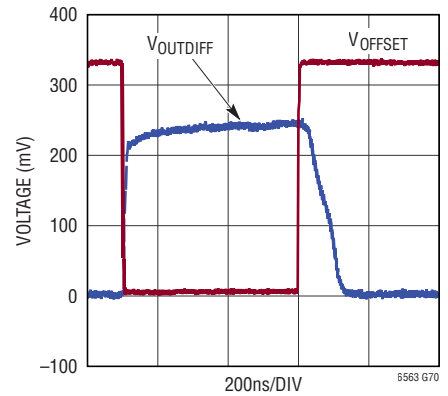
**Pulse Stretching vs Input Current**



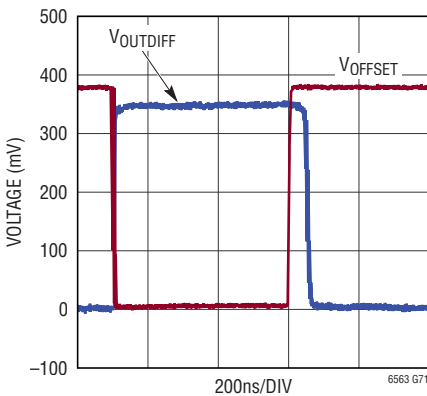
**Output Offset Histogram**



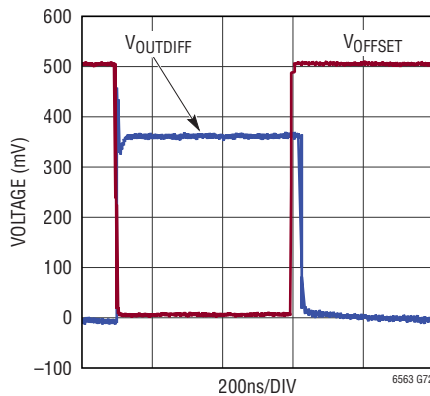
**Output Response to V<sub>OFFSET</sub> Pin Step**



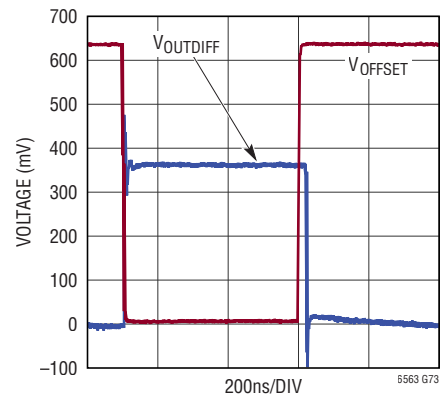
**Output Response to V<sub>OFFSET</sub> Pin Step**



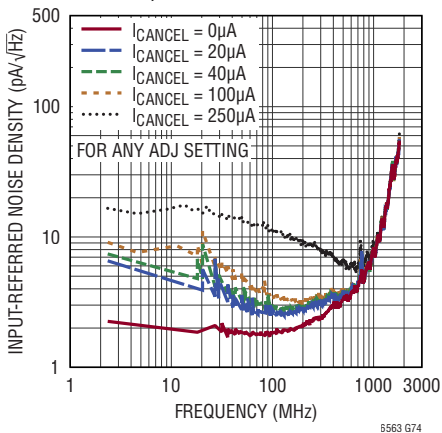
**Output Response to V<sub>OFFSET</sub> Pin Step**



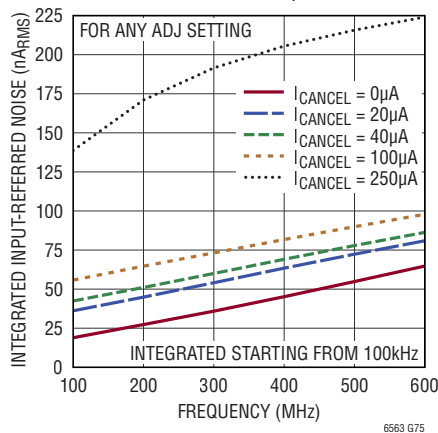
**Output Response to V<sub>OFFSET</sub> Pin Step**



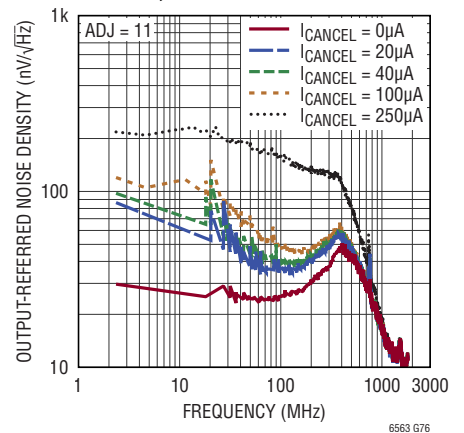
**Input-Referred Noise Density for Various Input Current Cancellation with C<sub>IN,TOT</sub> = 0.5pF**



**Integrated Input-Referred Noise for Various Input Current Cancellation with C<sub>IN,TOT</sub> = 0.5pF**



**Output-Referred Noise Density for Various Input Current Cancellation with C<sub>IN,TOT</sub> = 0.5pF**



**TYPICAL PERFORMANCE CHARACTERISTICS** Unless otherwise noted specifications are at CHSELO = TILT = OFFSET = 0V, HI = CHSEL1 = PWRMD = ADJ0 = ADJ1 = V<sub>CCI</sub> = V<sub>CCO</sub> = 3.3V, and CM = 1.5V. V<sub>OUTCM</sub> is defined as (OUT +  $\overline{\text{OUT}}$ )/2 and V<sub>OUTDIFF</sub> is defined as (OUT -  $\overline{\text{OUT}}$ ), R<sub>L\_EXT</sub> = 100Ω differential, OUT connected to TERM and  $\overline{\text{OUT}}$  connected to  $\overline{\text{TERM}}$ .

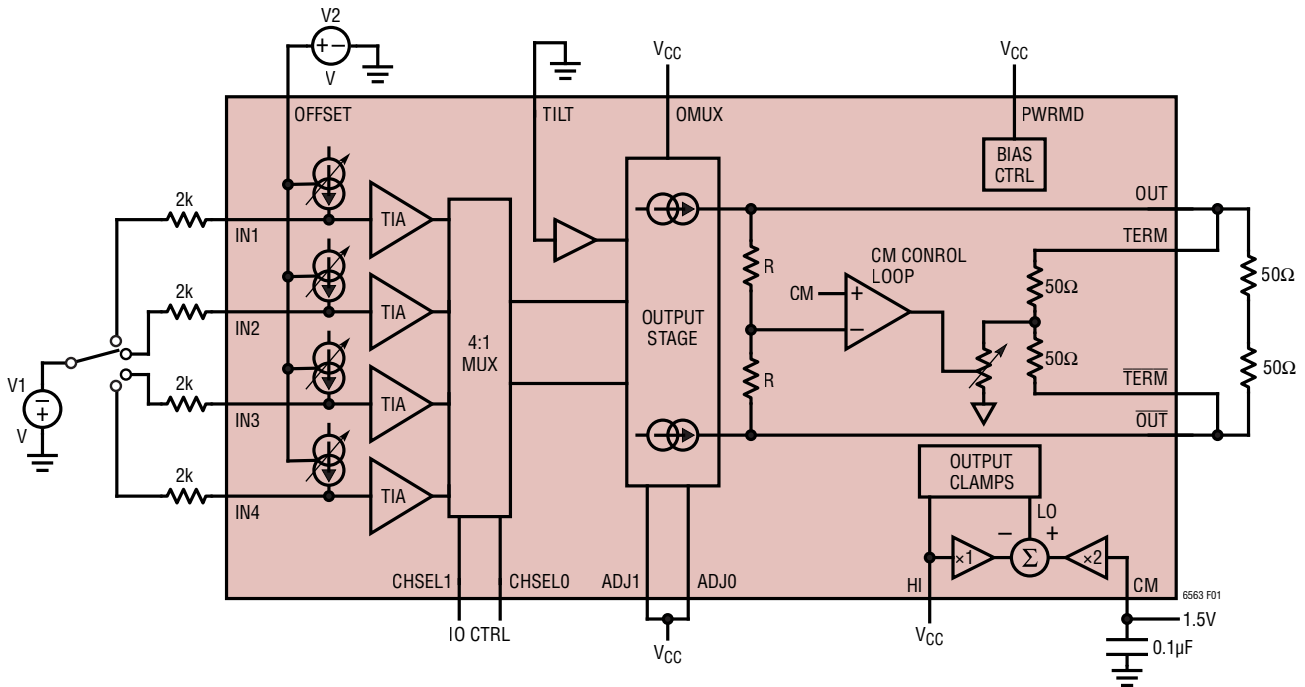
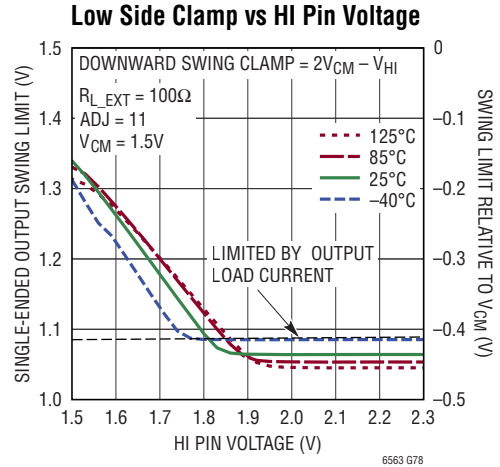
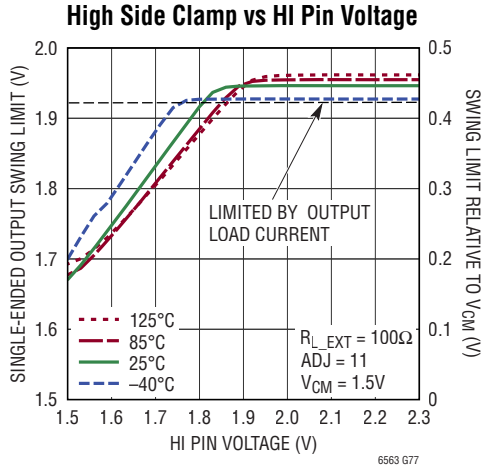
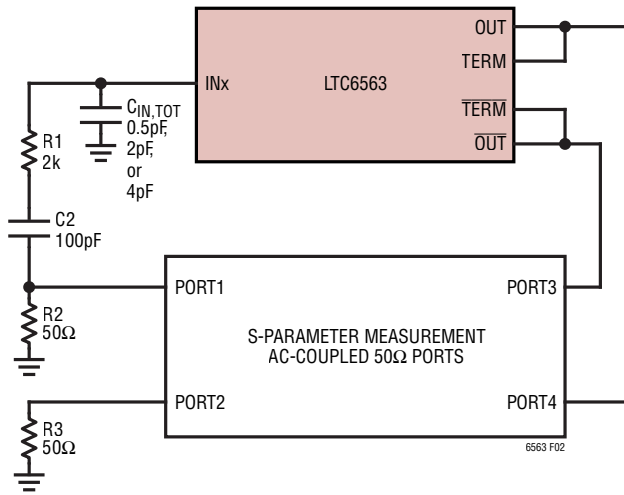
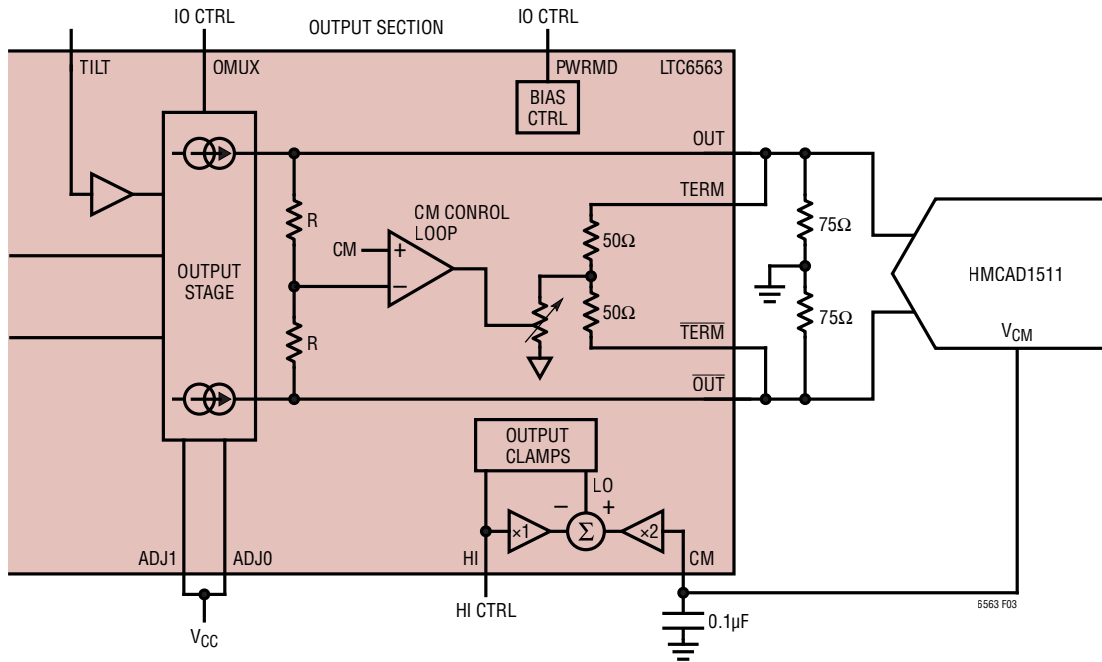


Figure 1. Electrical Characterization Test Circuit

**TYPICAL PERFORMANCE CHARACTERISTICS**



**Figure 2. S-Parameters Test Circuit**



**Figure 3. Driving HMCAD1511 (ADJ11, Tilt = 3.3V, CM = 0.9V, FS = 2.4V<sub>p-p</sub>)**



## PIN FUNCTIONS

**GND (Pins 1, 3, 18, 20, Exposed Pad Pin 25):** Negative Power Supply. Normally tied to ground. All GND pins and the exposed pad must be tied to the same voltage. The exposed pad (pin 25) should have multiple via holes to the underlying ground plane for low inductance and good heat transfer.

**IN4, IN1, IN2, IN3 (Pin 2, Pin 19, Pin 21, Pin 24,):** Input pins for the transimpedance amplifier for channels 4, 1, 2, and 3 respectively. The active channel is internally biased to 0.8V. See the Applications Information section for specific recommendation.

**PWRMD (Pin 4):** Power mode is a CMOS input for controlling the power consumption. The PWRMD pin has a 208k internal pull-up resistor to  $V_{CC1}$ . Default value is 3.3V.

**$V_{CC1}$  (Pin 5):** Positive power supply for the input stages. Typically, 3.3V. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitor of 680pF and 0.1 $\mu$ F should be placed as close to the part as possible between  $V_{CC1}$  and ground.

**OMUX (Pin 6):** Output MUX is a CMOS input for controlling the output multiplexing function. The OMUX pin has internal 208k pull-up resistor to  $V_{CC1}$ . Default value is 3.3V.

**CM (Pin 7):** Output Common Mode Reference Voltage. The voltage on this pin sets the output common mode voltage level. On a 3.3V supply, the CM pin floats to a default 0.9V. The CM pin has an input impedance of 16.3k $\Omega$ . The CM pin should be bypassed with a high-quality ceramic capacitor of at least 0.01 $\mu$ F.

**HI (Pin 8):** High Side Clamp Voltage. The voltage applied to the HI pin sets the upper voltage limit to  $\overline{\text{OUT}}$  and OUT pins. The HI voltage also limits the lower voltage swing on both output pins to  $2V_{CM} - HI$ , for symmetrical clamping around the CM voltage. On a 3.3V supply, the HI pin will

float to a default 1.8V. The HI pin has an input impedance of 13.6k $\Omega$ . The HI pin should be bypassed with a high-quality ceramic capacitor of at least 0.01 $\mu$ F.

**$\overline{\text{OUT}}$ , OUT (Pin 9, Pin 12):** Differential Output Pins. For voltage mode output, connect  $\overline{\text{OUT}}$  to  $\overline{\text{TERM}}$  and OUT to TERM. For current mode output or when using external load resistors, float  $\overline{\text{TERM}}$  and TERM.

**$\overline{\text{TERM}}$ , TERM (Pin 10, Pin 11):** Internal Termination. These pins have 50 $\Omega$  load resistors coupled to GND and are intended to connect to the differential output pins.

**CHSEL1, CHSEL0 (Pin 13, Pin 15):** MSB and LSB for Channel Selection. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

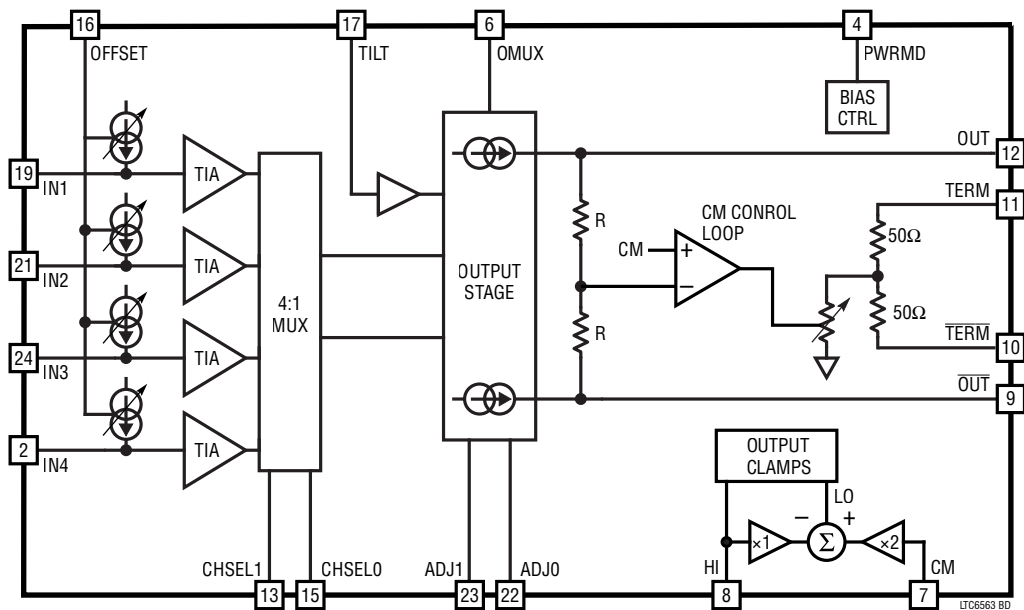
**$V_{CC0}$  (Pin 14):** Positive power supply for the output stage. Typically, 3.3V.  $V_{CC0}$  can be tied to  $V_{CC1}$  for single supply operation. A series ferrite bead such as the MPZ1005A331ETD25 should be used and bypass capacitors of 680pF and 0.1 $\mu$ F should be placed as close as possible between  $V_{CC0}$  and ground.

**OFFSET (Pin 16):** Input Offset Adjust. This pin accepts a voltage input that controls current sources on each input pin. These current sources can be used to cancel DC currents flowing into the detector. The OFFSET pin has an internal pull-down resistor to GND.

**TILT (Pin 17):** Output Differential Offset. The voltage on this pin controls the outputs' differential offset. The TILT pin has an internal 22.7k pull-down resistor to GND.

**ADJ0, ADJ1 (Pin 22, Pin 23):** LSB and MSB for output gain and current adjusts. The adjust pins set the output stage quiescent current and current gain. See Applications Information section to optimize the ADC interface. These pins are CMOS inputs with internal 218k pull-down resistors to GND.

## BLOCK DIAGRAM



## OPERATION

The LTC6563 is a four channel transimpedance amplifier with an integrated 4-to-1 multiplexer and ADC driver stage. Each of the transimpedance amplifiers converts an input current to an output voltage. The integrated 4:1 multiplexer simplifies the system design while saving space and power. In addition, output multiplexing is possible by using the OMUX pin. This allows multiple 4-channel LTC6563 devices to be combined. 8, 12, 16 ... 32 input channels are easily multiplexed into a single differential output.

The LTC6563 is optimized to drive high speed differential input analog-to-digital converters (ADCs).  $\overline{\text{OUT}}$  and  $\text{OUT}$  have single-ended swings from as low as about 180mV to about  $V_{\text{CC0}} - 1\text{V}$ . The LTC6563 provides four modes of output drive for matching input swing of high-speed ADCs.

The tilt feature allows the output stage to offset to take advantage of the full differential input range of the ADCs. The outputs have programmable clamps that limit the

output swing in saturation events. These clamps provide protection to the front end of the ADC. The HI pin sets the maximum swing, while a symmetric minimum swing limit is set up internally.

In typical LIDAR applications, the LTC6563 amplifies the output current of an APD. APD are biased near breakdown to achieve high current gain. Under intense optical illumination, they can conduct large currents, often in excess of 1A. The LTC6563 survives and quickly recovers from large overload currents of this magnitude. During recover, any TIA is blinded from subsequent pulses. The LTC6563 recovers from 1mA saturation events in less than 2.5ns without phase reversal, minimizing this form of data loss.

Ambient light is problematic for LIDAR receiver chains. The DC current can easily saturate the linear range of any TIA. The LTC6563 provides a control for DC cancelation to the inputs and can cancel up to 200 $\mu\text{A}$  of DC current. The DC cancelation is designed to minimizing additive noise.

## APPLICATIONS INFORMATION

### Output Offset and Current Control

The output stage of the LTC6563 has many options. The ADJ1 and ADJ0 pins provide four options for the output current drive. The output voltage swing is dependent on the adjust setting, the external differential termination resistor, and the Tilt input. The purpose of the Tilt input is to offset the DC output voltages, thereby increasing the full output swing of the TIA for unipolar inputs. Output TILT is essential for the ADC as the input from the photodetector is unipolar. To maximize the input swing of the ADC, the DC value of OUT is offset low while the DC value of OUT is offset high. This allows the LTC6563 to maximize the full dynamic range of the ADC. These pins should be connected to low noise inputs.

LTC6563 transimpedance gain ( $R_T$ ) consists of the overall gain from the multi-stages involved in producing the

output for a given input current. The output is differential and  $\frac{1}{2} R_T$  is achieved if only one of the outputs is utilized.

It is possible to change the transimpedance gain ( $R_T$ ) by changing  $R_{L\_EXT}$  as shown in Table 1, and Table 2. Also, since the ADJ pins respond in less than 100ns, these pins can be used for on the fly gain switching if the application needs that. An example would be to reduce the TIA gain if an overly strong signal is received by the LTC6563. It's important to note the following regarding gain adjustment:

- The linear input current range (40 $\mu$ A with no Tilt, 90 $\mu$ A with full Tilt) is not affected by these changes.
- $R_{L\_DIFF}$  refers to the total load seen by the differential output(s) whereas  $R_{L\_EXT}$  is the external differential load. Refer to Figure 17 to Figure 19 to see examples of various external single-ended load (50 $\Omega$ , 75 $\Omega$ , and 100 $\Omega$ ) illustrated.

**Table 1. Output Stage when Tilt Pin = 0V, OUT Connected to TERM and  $\overline{OUT}$  Connected to  $\overline{TERM}$ <sup>1</sup>**

IIN ( $\mu$ A)	ADJ1	ADJ0	OUT (mA)	OUTBAR (mA)	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = 100\Omega$ DIFF	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = 200\Omega$ DIFF	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = OPEN$
0	0	0	7	7	5.55k	7.4k	11.1k
	0	1	14	14	11.1k	14.8k	22.2k
	1	0	21	21	16.65k	22.2k	33.3k
	1	1	28	28	22.2k	29.6k	44.4k
45	0	0	12	2	5.55k	7.4k	11.1k
	0	1	24	4	11.1k	14.8k	22.2k
	1	0	36	6	16.65k	22.2k	33.3k
	1	1	48	8	22.2k	29.6k	44.4k

<sup>1</sup> Output voltage compliance to be observed at higher  $R_{L\_EXT}$  and higher ADJ settings.

**Table 2. Output Stage when Tilt Pin =  $V_{CC}$ , OUT Connected to TERM and  $\overline{OUT}$  Connected to  $\overline{TERM}$ <sup>1</sup>**

IIN ( $\mu$ A)	ADJ1	ADJ0	OUT (mA)	OUTBAR (mA)	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = 100\Omega$ DIFF	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = 200\Omega$ DIFF	$R_T$ ( $\Omega$ ) $R_{L\_EXT} = OPEN$
0	0	0	2	12	5.55k	7.4k	11.1k
	0	1	4	24	11.1k	14.8k	22.2k
	1	0	6	36	16.65k	22.2k	33.3k
	1	1	8	48	22.2k	29.6k	44.4k
90	0	0	12	2	5.55k	7.4k	11.1k
	0	1	24	4	11.1k	14.8k	22.2k
	1	0	36	6	16.65k	22.2k	33.3k
	1	1	48	8	22.2k	29.6k	44.4k

<sup>1</sup> Output voltage compliance to be observed at higher  $R_{L\_EXT}$  and higher ADJ settings.

## APPLICATIONS INFORMATION

- Increasing  $R_{LDIFF}$  slightly reduces the signal bandwidth.
- Output voltage compliance ( $V_{COMPLIANCE}$ ) to be observed relative to  $R_{LDIFF}$ , ADJ settings, and CM voltage. Here is an example where output voltage compliance is violated:

$$R_{LDIFF} = 100\Omega, \text{ Tilt} = V_{CC}, \text{ ADJ1} = 1, \text{ ADJ0} = 0, \\ \text{CM} = 1.7V, I_{IN} = 90\mu A$$

Output Voltage (max) =

$$V_{CM} + \frac{|I_{OUT} - I_{OUTBAR}|}{2} \cdot \frac{R_{LDIFF}}{2}$$

Referring to Table 2 to read output current values:

Output Voltage (max) =

$$1.7V + \frac{|36mA - 6mA|}{2} \cdot \frac{100\Omega}{2} = 2.45V!$$

The maximum output voltage must remain below  $V_{CCO} - 1V$  (~2.3V) to comply with the  $V_{COMPLIANCE}$  rating. Possible remedies are reducing output current(s) by using lower power ADJ settings, reducing the input APD current, reducing the differential load, or reducing the CM voltage.

### Power Considerations

The LTC6563 has many power modes of operation. The state of the PWRMD, OMUX and ADJ pins will dictate the amount of current the LTC6563 will draw. Multiple power modes are offered to allow the user to select the

appropriate one based upon the application while minimizing power dissipation.

### Coupling the TIA Input – AC vs DC

Although the LTC6563 can AC-couple to the detector, best performance is achieved when DC-coupled to a negatively biased APD. DC-coupling reduces component count while allowing a DC current path from the APD. The LTC6563 OFFSET feature is designed to cancel DC currents. The maximum performance for switching speeds and saturation recovery occurs in this DC-coupled configuration.

When AC-coupling to the TIA input,  $R_B$  is needed to establish a bias point for the detector. It is worth noting that  $R_B$  is a parallel path with the TIA for the APD current to flow through and it will impact the effective signal chain output gain.

This value of the biasing resistor and AC-coupling capacitor,  $C_{AC}$ , can potentially create a long time-constant.  $C_{AC}$  is chosen based on the reactance at the frequency of interest. However,  $R_B$  ideally should be large to avoid stealing

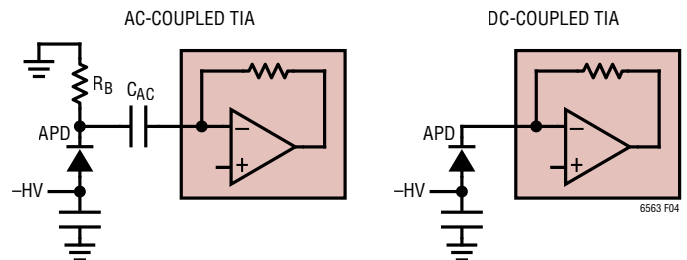


Figure 4. AC-Coupled Detector Circuit

Table 3. LTC6563 Power Dissipation Modes. X = Don't Care

PWRMD	OMUX	ADJ1	ADJ0	$I_{VCC1}$ (mA)	$I_{VCC0}$ (mA)	$I_{TOTAL}$ (mA)	DESCRIPTION
0	0	X	X	4.5	0.1	4.6	LTC6563 shutdown.
0	1	0	0	21	24.5	45.5	LTC6563 enabled, non-selected inputs powered down, CM pin control disabled. This setting appropriate for a Responder device in a multi-chip/multi-channel application.
0	1	0	1	21	38	59	
0	1	1	0	21	51.5	72.5	
0	1	1	1	21	64.5	85.5	
1	0	X	X	35	0.1	35.1	LTC6563 deselected (outputs stage off), non-selected inputs powered up.
1	1	0	0	34	24.5	58.5	LTC6563 enabled, non-selected inputs powered up, CM pin control active in setting output CM voltage. This setting appropriate for a Controller device in a multi-chip/multi-channel application.
1	1	0	1	34	38	72	
1	1	1	0	34	51.5	85.5	
1	1	1	1	34	64.5	98.5	

## APPLICATIONS INFORMATION

current from the TIA path from APD signal. On one hand large  $R_B$  causes large RC time constants, while low  $R_B$  reduces the effective gain of the APD.

Another negative impact of this RC network is in the case for saturation events. When a large signal is received from the APD, this event will charge  $C_{AC}$ . This will negatively move the input bias of the TIAs and change the TIAs input impedance to transimpedance  $14k\Omega$ . This  $14k\Omega$  coupled with  $R_B$  and  $C_{AC}$  time constant will add the saturation recover time. Practical values of  $100pF$   $C_{AC}$  and  $R_B$  of  $2.2k\Omega$  will have large saturation recovery times  $>1\mu s$  with  $>50mA$  input signals. This effectively blinds the signal chain for the next input signal.

### Channel Selection

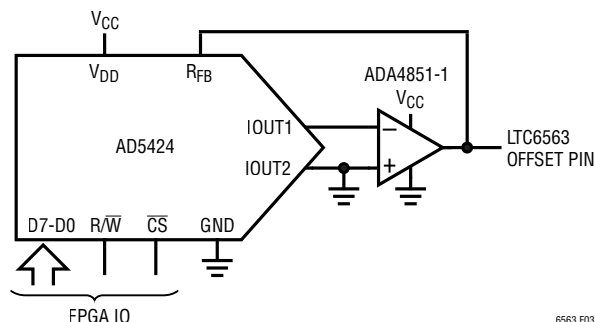
There are four TIA inputs to the LTC6563. The active channel is selected using two channel selection bits CHSEL0 and CHSEL1. When a channel is changed and PWRMD is high, an output glitch takes  $<10ns$  to settle. When PWRMD is low and a channel is changed, an output glitch takes  $<500ns$  to settle. Inactive channels have 30dB of channel to channel isolation at 400MHz when PWRMD pin is high. When PWRMD is low the channel isolation is increased to more than 48dB.

**Table 4. Channel Selection**

CHSEL1	CHSEL0	OMUX	ACTIVE CHANNEL
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4
X	X	0	Hi-Z

### DC Input Cancellation

The LTC6563 features a voltage controlled current source for DC input current cancellation with minimal noise impact. Identical currents are applied to each TIA input. The maximum current cancellation is  $200\mu A$ . The OFFSET pin was designed to accommodate external closed loop design for fast settling and fast switching times. See  $I_{OFFSET}$  vs  $V_{OFFSET}$  curve for the transfer function. It is recommended to use a high-speed DAC to control the OFFSET pin.



**Figure 5. Recommended DC Cancel Circuit**

### Output MUXing

Refer to Figure 6 schematic. The output multiplexing (OMUX) requires at least one additional LTC6563 devices to operate in a Controller/Responder relationship. To multiplex multiple LTC6563's they need to share a DC connection at their outputs. The controller LTC6563 (U1) output stage needs to be connected to the internal termination resistors. For the CM control to function, the controller PWRMD pin must remain HIGH during the time any of the inputs of all the parallel network are enabled. That is because the CM servo loop is disabled if PWRMD is deasserted (low). The controller LTC6563 output circuit (U1) will control the common mode for all the multiplexing. All CM pins (U1-U4) are to be connected to the common mode of the ADC. If the output clamping feature (HI pin) is implemented, all CM pins (U1-U4) need to be connected to the same voltage for proper operation. Also, tie all HI pins (U1-U4) together and apply the required clamping voltage to them. The HI pin is used to set the high side clamp voltage at outputs. Internal circuitry generates a symmetric low side clamp voltage with respect to the common mode voltage  $V_{CM}$ .

Maximum output high side voltage = HI pin voltage

Minimum output low side voltage =  $V_{CM} - (HI - V_{CM}) = 2V_{CM} - HI$

### Setting the Output CM Voltage

The LTC6563 can set the output Common Mode (CM) voltage using the CM input pin provided on the device.

# APPLICATIONS INFORMATION

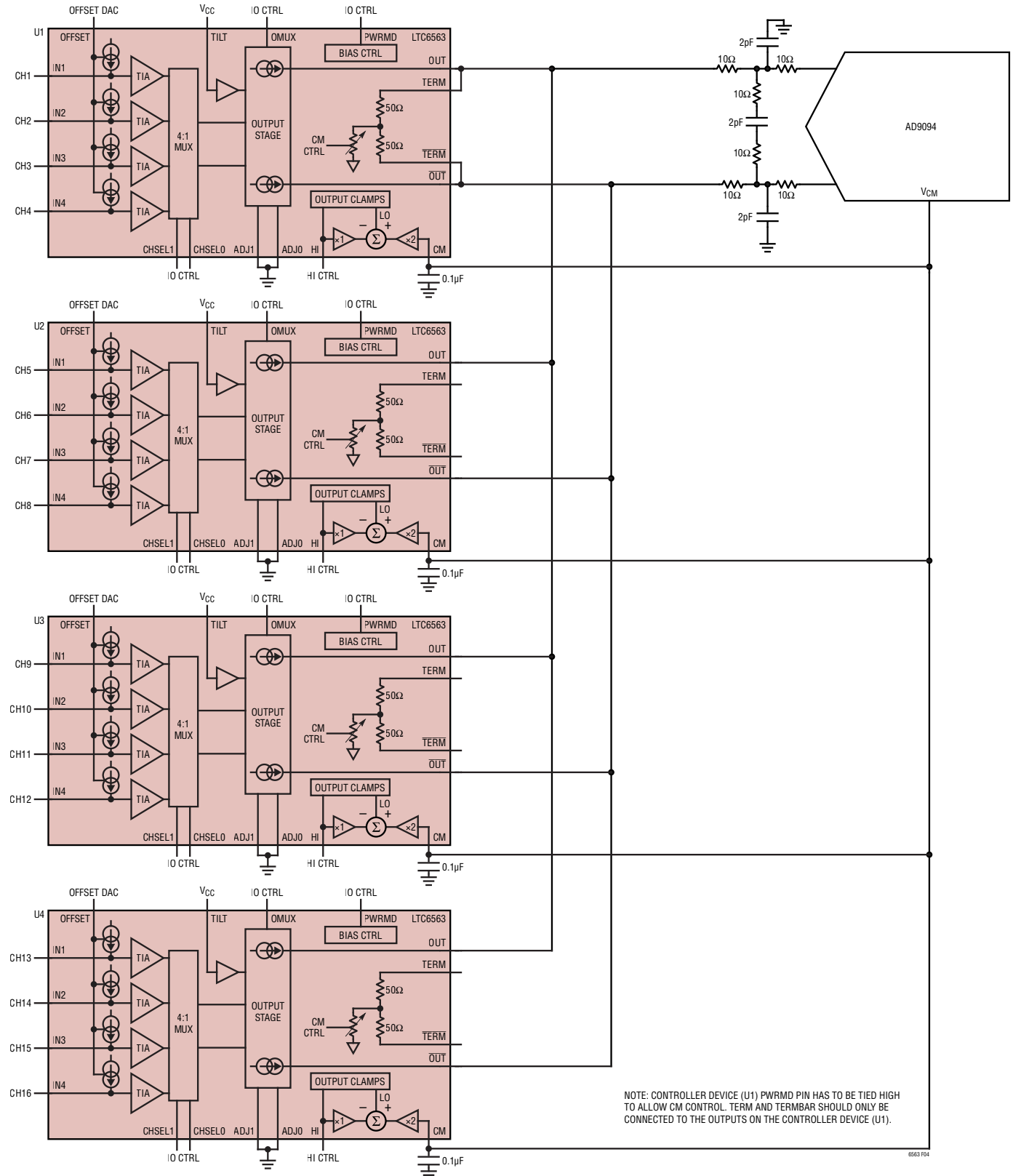


Figure 6. Typical Application with Multiplexed Outputs

## APPLICATIONS INFORMATION

In applications where the LTC6563 is to drive an ADC, this is useful in matching the TIA output(s) to the ADC analog input CM. This effectively eliminates the need for a separate ADC-driver which saves cost, power, as well as board complexity and real estate.

The CM servo loop operates by varying the CM CTRL variable resistor internal to the LTC6563 such that  $V_{CM0}$ , average of  $V_{OUT}$  and  $V_{OUTBAR}$  voltages or  $(V_{OUT} + V_{OUTBAR})/2$ , matches the voltage applied to the CM. The loop will NOT function unless two conditions are met:

1. PWRMD must be set HI to activate the CM circuit.
2.  $\overline{OUT}$  and  $\overline{OUT}$  must have a DC connection to TERM and  $\overline{TERM}$  respectively.

The internal  $50\Omega$  resistor(s) on the TERM and  $\overline{TERM}$  pins provide a current path for CM servo functionality and serve as the load for the LTC6563's current mode output. Driving  $50\Omega$  terminated transmission lines or other impedance-matched loads is easily done using these internal resistors.

When using the output MUXing capability with multiple LTC6563's, such as the schematic shown in Figure 6, only one pair of TERM and  $\overline{TERM}$  pins should be connected

to the OUT and  $\overline{OUT}$ . The device with the connected TERM and  $\overline{TERM}$  will then set the CM for the MUX'ed devices.

### Determining the CM Range

CM servo loop's voltage range is easily calculated using Ohm's law, as the output circuit can be described as a pair of current sources and a resistor network (see Figure 8). The amount of current supplied by the OUT and  $\overline{OUT}$  current sources is determined by the ADJ setting, and the impedance at the output pins is determined by the internal and external resistor networks. These factors will determine the range of possible DC voltages at the outputs.

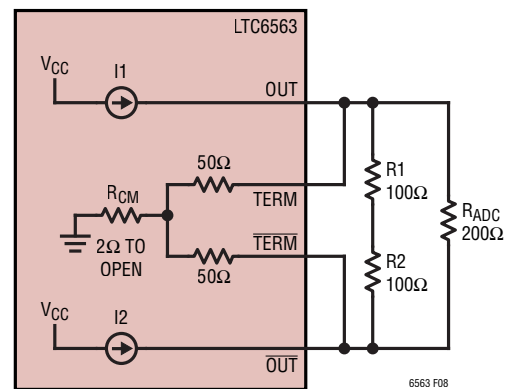


Figure 8. Equivalent Circuit for Driving an ADC with no GND (CM Referenced) External Load

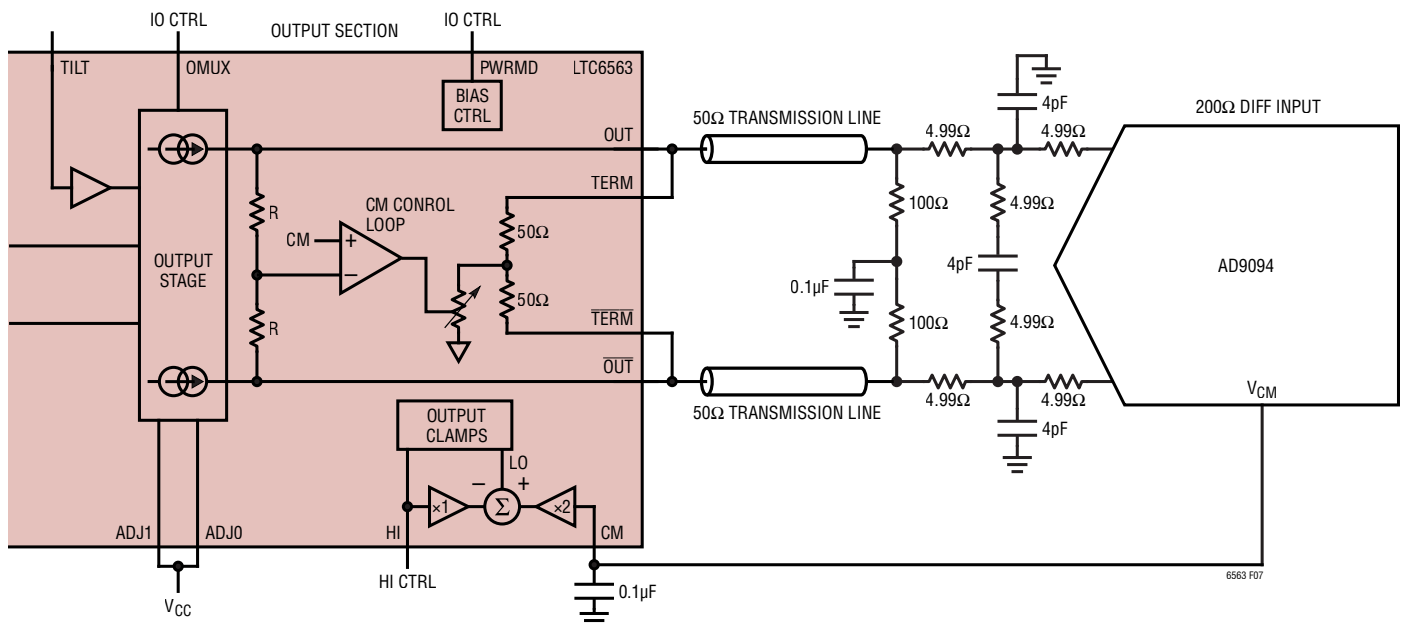
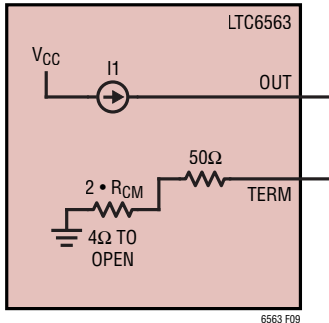


Figure 7. Typical Connection for CM Control/ADC Driving

## APPLICATIONS INFORMATION

In order to simplify the analysis, an intuitive way to look at the output loading is to examine its equivalent half-circuit as shown in Figure 9. With the half-circuit method, any impedance that is shared between the two halves appears as double its original value (e.g.  $R_{CM}$  appears as  $2 \cdot R_{CM}$  below).



**Figure 9. CM Half-Circuit Equivalent for a Non-Grounded External Load**

The internal CM CTRL resistance varies from about  $2\Omega$  to essentially an open circuit. At the lower end of the CM CTRL resistance,  $R_{CM}$ , the output CM voltage will be at the minimum it can reach. And at the higher end of  $R_{CM}$ , it will be at the maximum it can reach.

The external CM resistance can also vary greatly, depending on whether any external loads are terminated differentially or to GND.

### Detailed Example 1: Differential Termination ONLY

With an external load connected, the output CM current splits between the internal TERM pin and the external load. However, with the configuration shown in Figure 7 and simplified in Figure 8, with no external CM DC current path to ground, the entire output CM current must flow through the internal TERM resistor(s).

In Figure 8, the external loading by the ADC and the cable termination network of R1, and R2 has no effect on the CM loading of the LTC6563. The range of output CM voltage will be as follows:

$$V_{CMO} = I_O \cdot (50\Omega + 2R_{CM}) \quad (1)$$

For the ADJ setting of 00 where  $I_O$  is 7mA (see Table 1 and Table 5) here is the computation of min  $V_{CMO}$  possible (corresponding to  $R_{CM} = 2\Omega$ ):

$$V_{CMO} \text{ (minimum)} = 7\text{mA} \cdot (50\Omega + 2 \cdot 2\Omega) = 380\text{mV} \quad (2)$$

At the other extreme of  $V_{CMO}$  when  $R_{CM}$  opens, the output CM voltage will only be limited to the LTC6563 output compliance voltage which is about 1V below  $V_{CC}$  (or about 2.3V with  $V_{CC} = 3.3\text{V}$ ).

Naturally, if the ADJ setting is changed, the  $V_{CMO}$  range will vary accordingly. Table 5 shows the minimum computed output CM voltage, output full scale swing, and TIA gain (RT) for various ADJ settings applied to the circuit in Figure 7.

For a higher Transimpedance gain (RT) or higher ADC FS swing, higher ADJ output current settings can be chosen. Summary of how ADJ affects the TIA gain and differential output voltage swing is tabulated in Table 5.

Here is a sample calculation of the values in Table 5 (50Ω Net diff load, full tilt) for ADJ 00 as an illustration:

- Output current values (ADJ 00) with max input current of  $90\mu\text{A}$  (from Table 2): 12mA, 2mA
- Net diff output load:  $50\Omega$  ( $25\Omega$  on each output)  
RT Calculation:  $RT(\text{k}\Omega) =$   
c.  $\frac{25\Omega[(12\text{mA} - 2\text{mA}) - (2\text{mA} - 12\text{mA})]}{90\mu\text{A}} = 5.56\text{k}\Omega$

**Table 5. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 7**

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT $I_O$ (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV <sub>P-P</sub> )	MIN CM VOLTAGE (mV)
0	0	7	5.6	500	380
0	1	14	11.1	1000	756
1	0	21	16.7	1500	1134
1	1	28	22.2	2000	1512



## APPLICATIONS INFORMATION

- d. ADC FS diff voltage calculation =  $90\mu\text{A} \cdot 5.56\text{k}\Omega = 500\text{mV}_{\text{P-P}}$
- e.  $I_0$  CM/Average Output Current (from Table 1): 7mA
- f.  $V_{\text{CMO}}$  (minimum) =  $I_0 \cdot (50\Omega + 2 \cdot 2\Omega) = 380\text{mV}$  where  $I_0 = 7\text{mA}$ ,  $50\Omega$  is the TERM internal resistance, and the  $2\Omega$  is the internal  $R_{\text{CM}}$  minimum value

The data in Table 5 can be used to examine the real-world problem of driving the AD9094 ADC, the input requirements of which are shown below:

Differential Input Voltage Range:  $1.44\text{V}_{\text{P-P}}$  to  $2.16\text{V}_{\text{P-P}}$  (programmable)

Common Mode Voltage: 1.43V

As can be seen from Table 5, operating the LTC6563 with ADJ 10 falls in the range of the required AD9094 FS swing voltage ( $1.44\text{V}_{\text{P-P}}$  to  $2.16\text{V}_{\text{P-P}}$ ), and also complies with the required AD9094 CM voltage (1.43V) by allowing an output CM voltage as low as 1.13V. Therefore, ADJ 10 is an appropriate setting for driving the AD9094.

### Detailed Example 2: Lowering the CM Voltage with a Tee Resistor or External DC Termination to Ground

Adding a path to ground from the center of the load resistors ( $R_1$ , and  $R_2$ ) can lower the CM voltage. This can be in the form of grounding the middle of  $R_1$ , and  $R_2$ , or alternatively adding a TEE resistor to avoid

dropping the CM voltage too low. This technique (shown in Figure 10) allows for more flexibility in aligning the TIA to an ADC or a given differential load and ADJ setting.

The TEE resistor will appear as double its value in the half-circuit. The equivalent CM load and CM voltage can be written as:

$$V_{\text{CMO}} = I_0 \cdot [(50\Omega + 2R_{\text{CM}}) \parallel (R_1 + 2R_{\text{TEE}})] \quad (3)$$

Note that adding  $R_{\text{TEE}}$  to the schematic only affects the CM parameters of the circuit and has no bearing on the differential voltage swing and the resulting transimpedance gain of the circuit. A shunt capacitor to ground across  $R_{\text{TEE}}$  can be added to ensure no spurious AC signal appears at this node.

For the particular case of Figure 7 schematic modified to include  $R_{\text{TEE}} = 20\Omega$  with ADJ = 11 ( $I_0 = 28\text{mA}$  from Table 1), the AD9094 CM voltage requirement (1.43V) would be easily satisfied since the CM servo loop would be able to adjust the output CM from 1.1V minimum (with  $R_{\text{CM}} = 2\Omega$ , previously 1.51V minimum from Table 5 without  $R_{\text{TEE}}$ ) to  $>2.3\text{V}$  (device output compliance voltage) maximum using Equation 3.

### Operation without Internal CM Servo Loop

There may be applications where the CM servo loop function built into the LTC6563 is not needed, as would be the case if the TIA output is not used to drive an ADC.

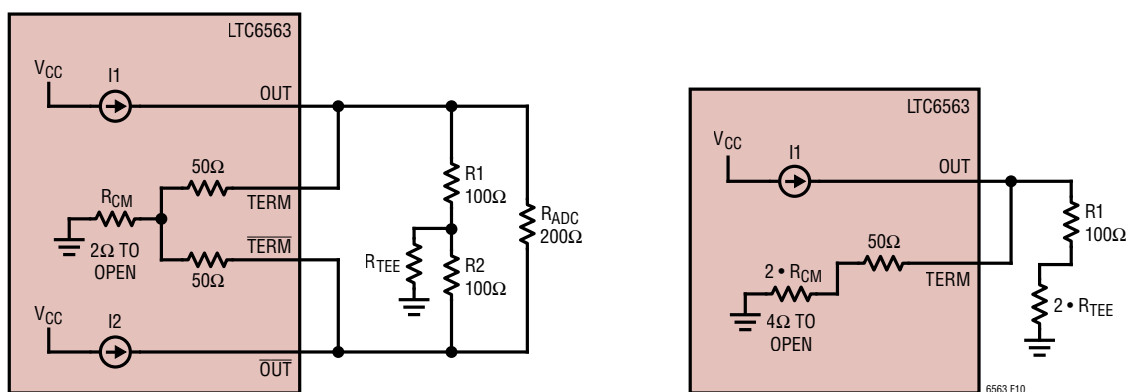


Figure 10. TEE Resistor Loading (Left) and Its Equivalent CM Half-Circuit (Right)

## APPLICATIONS INFORMATION

Under these conditions, the following pin settings should be used:

1. TERM and  $\overline{\text{TERM}}$  should be left floating.
2. An external circuit capable of sinking the output current must be used. This task is most easily accomplished by providing external termination to ground.
3. The CM pin *must* be tied to the expected output CM voltage. The output clamp levels are calculated from CM and HI pins, so failure to set the CM pin properly may result in undesired signal clamping.

When the TERM and  $\overline{\text{TERM}}$  pins are left floating, the output CM voltage will be solely a function of the LTC6563 ADJ setting and the external CM load. For example, with ADJ11 setting ( $I_O = 28\text{mA}$ ) and  $50\Omega$  to ground on each output, the output CM voltage will be:

$$V_{\text{CMO}} = I_O \cdot R_{\text{LOAD\_CM}} = 28\text{mA} \cdot 50\Omega = 1.4\text{V} \quad (4)$$

With the CM servo loop function disabled, the LTC6563's CM pin should be tied to a voltage that is close to the expected CM value (1.4V in the example stated just above). The output clamp circuit assumes that CM is equal to the actual output CM voltage. If this is not the case, the clamping voltage set by the HI pin will be miscalculated, and undesired signal clipping may result. For this

purpose, a replica  $V_{\text{CMO}}$  voltage can simply be generated off the device  $V_{\text{CC}}$  pin using  $k\Omega$  range voltage division resistors.

### Increasing Output Impedance

It may be desirable to change the output termination impedance in order to adjust the output signal amplitude. In addition, the flexibility of LTC6563's output structure allows for impedance matching to a variety of different loads or transmission line impedances, which is critical for high speed signal integrity. In the following example, the output circuit will be modified to present a  $75\Omega$  source impedance for driving a  $75\Omega$  transmission line and ADC load.

Consider the configuration shown in Figure 11 schematic. The output impedance of the LTC6563 is raised to  $75\Omega$  by adding  $24.9\Omega$  resistors in series with the internal  $50\Omega$  TERM resistors. The TIA now presents an output impedance that matches the  $75\Omega$  transmission line as well as the net ADC-side SE impedance. The transmission line ADC-side impedance can be calculated by:

$$((200\Omega/2) + (2 \cdot 4.99) \parallel 300\Omega) = 80\Omega.$$

Let's now take a look at the output CM voltage that pertains to the schematic of Figure 11, simplified in Figure 12:

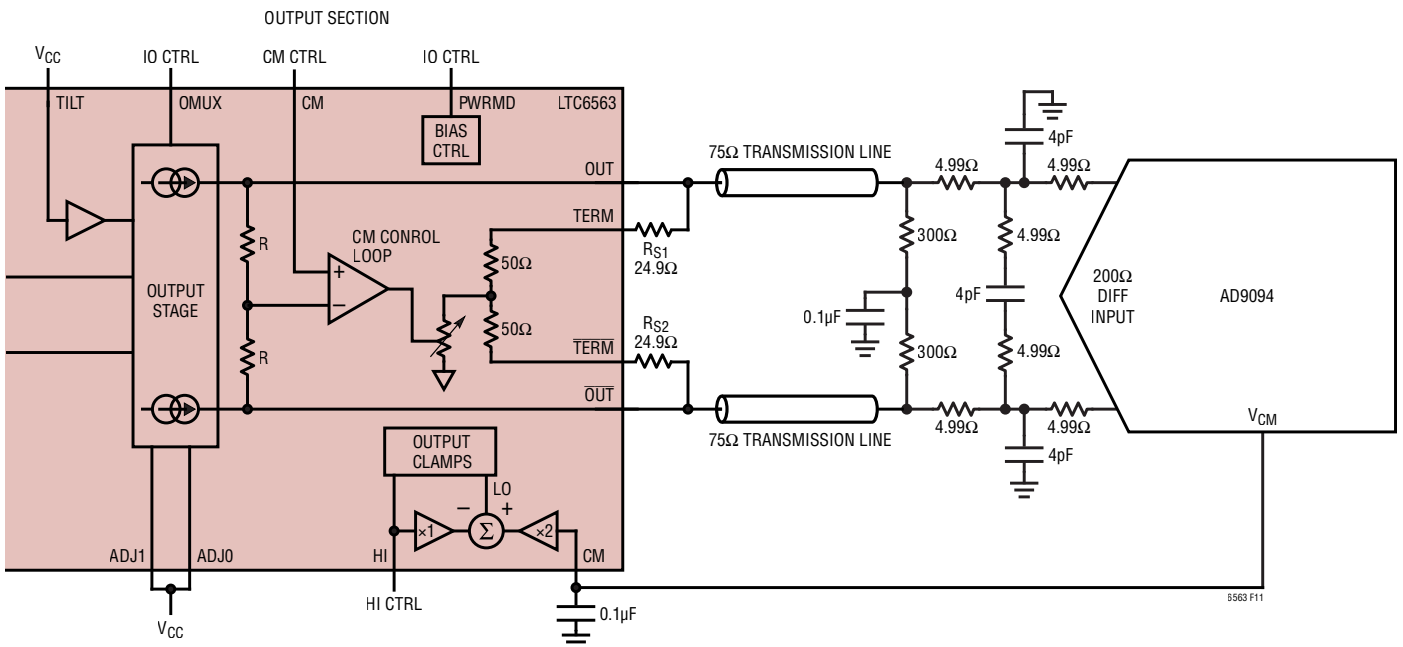


Figure 11. Increasing Diff Load Resistance and Matching to  $75\Omega$

## APPLICATIONS INFORMATION

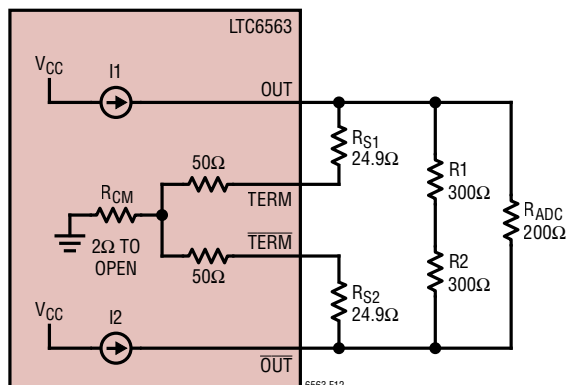


Figure 12. TIA 75Ω Matched Load Equivalent Circuit

As in the previous cases, for analysis purposes, it is useful to break the output load circuit into its equivalent half-circuit to compute how the CM voltage is affected, as shown in Figure 13.

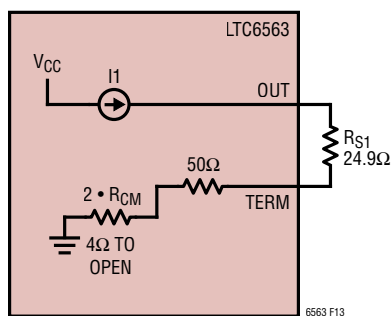


Figure 13. CM Half-Circuit Equivalent Circuit for 75Ω Load

As before, the CM circuit is not affected by the R1, R2 or the ADC differential input impedance of 200Ω. The output CM will be given by:

$$V_{CM0} = I_0 \cdot (24.9\Omega + 50\Omega + 2R_{CM}) \quad (5)$$

Table 6. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 11

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT $I_0$ (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV <sub>P-P</sub> )	MIN CM VOLTAGE (mV)
0	0	7	8.3	750	553
0	1	14	16.7	1500	1106
1	0	21	25.0	2250*	1659
1	1	28	33.3	3000*	2212*

\*Limited by output voltage compliance

So, in addition to raising the TIA output impedance,  $R_{S1}$  and  $R_{S2}$  also contribute to an increase in the minimum output CM voltage.

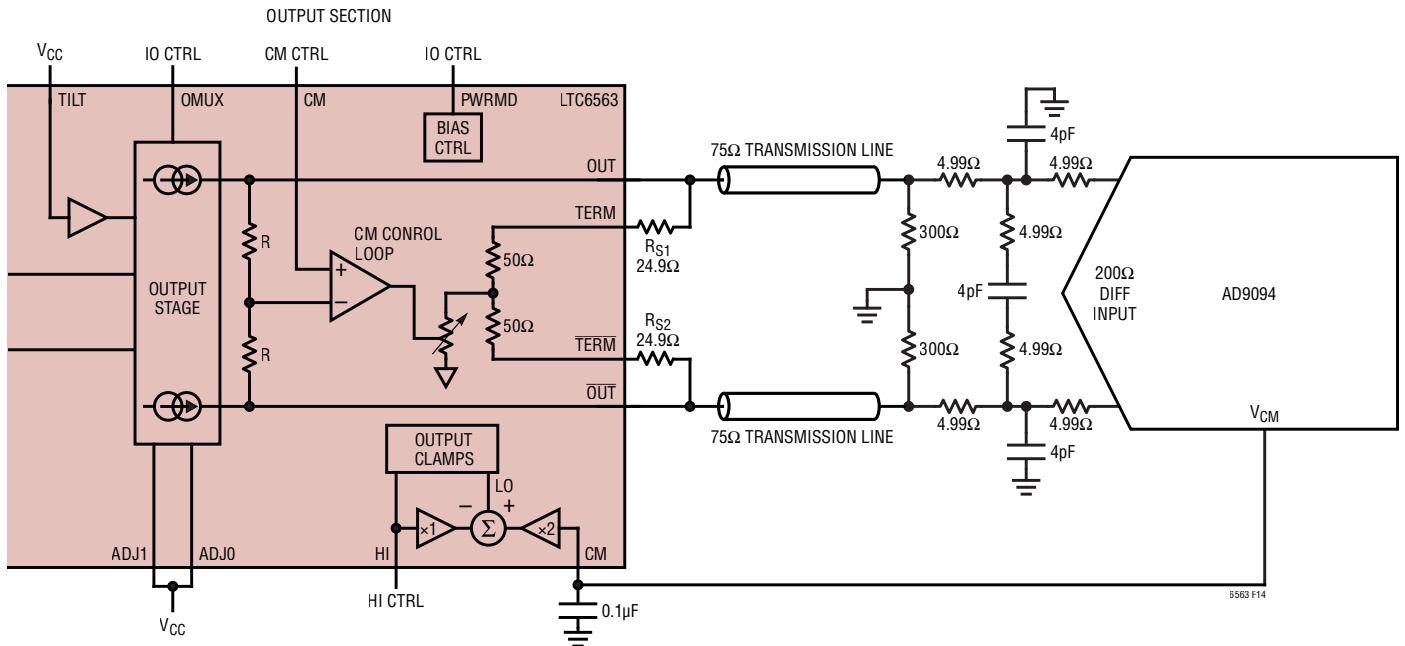
Table 6 shows the computed minimum CM voltage, TIA gain (RT), and ADC FS diff voltage swing for various ADJ settings applied to the Figure 11 configuration.

Here is a sample calculation of the values in Table 6, related to the Figure 11 schematic, for ADJ 00 as an illustration:

- Output current values (ADJ 00) with max input current of 90μA (from Table 2): 12mA, 2mA
- Net diff output load: 75Ω (37.5Ω on each output)  
RT Calculation:  $RT(k\Omega) =$
- $$\frac{37.5\Omega[(12mA - 2mA) - (2mA - 12mA)]}{90\mu A} = 8.3k\Omega$$
- ADC FS diff voltage calculation =  $90\mu A \cdot 8.3k\Omega = 750mV_{P-P}$
- $I_0$  CM / Average Output Current (from Table 1): 7mA
- $V_{CM0}$  (minimum) =  $I_0 \cdot (24.9\Omega + 50\Omega + 2 \cdot 2\Omega) = 553mV$ , where  $I_0 = 7mA$ , 24.9Ω is the resistors in series with the TERM pin, 50Ω is the TERM internal resistance, and the 2Ω is the internal  $R_{CM}$  minimum value

In the Figure 11 schematic and tabulated results in Table 6, the ADJ 11 setting's Min CM voltage is too high to be usable. Thus, the technique of lowering CM voltage (Detailed Example 2) discussed earlier can be employed

# APPLICATIONS INFORMATION



**Figure 14. Reducing the Min CM Voltage with Grounding the External Load Midpoint**

if ADJ 11 is to be used as shown in Figure 14 where the external loads (300Ω) mid-point is grounded.

With the modified schematic of Figure 14 the CM voltage is:

$$V_{CMO} = I_O \cdot [(24.9\Omega + 50\Omega + 2R_{CM}) || 300\Omega] \quad (6)$$

Resulting in the min VCMO for ADJ 11:

$$V_{CMO} \text{ (minimum)} = I_O \cdot [(24.9\Omega + 50\Omega + 2 \cdot 2\Omega) || 300\Omega] = 28\text{mA} \cdot 62.5\Omega = 1.75\text{V} \quad (7)$$

Table 7 shows the computed minimum CM voltage, TIA gain (RT), and ADC FS diff voltage swing for various ADJ settings applied to the Figure 14 configuration:

Here is a sample calculation of the values in Table 7, related to the Figure 14 schematic, for ADJ 00 as an illustration:

- Output current values (ADJ 00) with max input current of 90μA (from Table 2): 12mA, 2mA
- Net diff output load: 75Ω (37.5Ω on each output)  
RT Calculation:  $RT(k\Omega) = \frac{37.5\Omega[(12\text{mA} - 2\text{mA}) - (2\text{mA} - 12\text{mA})]}{90\mu\text{A}} = 8.3\text{k}\Omega$
- ADC FS diff voltage calculation =  $90\mu\text{A} \cdot 8.3\text{k}\Omega = 750\text{mV}_{P-P}$

**Table 7. CM Minimum Voltage and Other Operating Performance Values for Various ADJ Settings of Figure 14**

ADJ1	ADJ0	CM/AVERAGE OUTPUT CURRENT I <sub>O</sub> (mA)	RT (kΩ)	ADC FS DIFF VOLTAGE SWING WITH FULL TILT (mV <sub>P-P</sub> )	MIN CM VOLTAGE (mV)
0	0	7	8.3	750	437
0	1	14	16.7	1500	875
1	0	21	25.0	2250*	1312
1	1	28	33.3	3000*	1750

\*Limited by output voltage compliance

## APPLICATIONS INFORMATION

- e.  $I_O$  CM/Average Output Current (from Table 1): 7mA
- f.  $V_{CMO}$  (minimum) =  $I_O \cdot [(24.9\Omega + 50\Omega + 2 \cdot 2\Omega) || 300\Omega]$   
 $= I_O \cdot [78.9\Omega || 300\Omega] = I_O \cdot 62.5\Omega = 437\text{mV}$ , where  $I_O$   
 $= 7\text{mA}$ ,  $24.9\Omega$  is the resistors in series with the TERM  
 pin,  $50\Omega$  is the TERM internal resistance, and the  $2\Omega$   
 is the internal  $R_{CM}$  minimum value.

As can be seen, the only difference between Table 6 and Table 7 is in the last column, Min CM voltage, where this column's values are lowered in Table 7 by grounding the mid-point of the external load resistors.

### Summary of TIA Operating Conditions and Their Effects

The current output nature of the LTC6563 provides a great deal of flexibility in tailoring the circuit to drive a variety of ADCs, transmission lines, or other loads that are found in various applications. The TIA gain (RT), full scale swing (FS), and output CM voltage design can be optimized using internal termination networks, external termination networks (ground referenced and differential), and ADJ settings.

Designing the TIA load and operational settings involves juggling these interdependent parameters. See Table 8 for a summary of how different TIA output operating conditions influence various important aspects of the TIA design:

### Clamp Function

LTC6563 has internal output voltage clamps that restrain its differential output swing. These clamps maintain

control of the OUT and  $\overline{\text{OUT}}$  voltages to prevent overloading the ADCs inputs. The clamping speed is on the order of the TIA bandwidth so the ADCs functionality and signal integrity will be minimally affected by output signals that would otherwise exceed the ADCs input range.

OUT and  $\overline{\text{OUT}}$  will be confined to the range of voltages shown below:

Maximum output high side voltage = HI pin voltage

Minimum output low side voltage =  $V_{CM} - (HI - V_{CM})$   
 $= 2V_{CM} - HI$

*Please remember that  $V_{CM}$  is the pin voltage of the CM input. If the actual output CM voltage differs from the CM pin voltage, unexpected clamping may occur.*

Consider the example where, with  $CM = 1.4\text{V}$  and  $HI = 2.2\text{V}$ . The difference between CM and HI is  $0.8\text{V}$ , so the outputs will be clamped between  $1.4\text{V} \pm 0.8\text{V}$ . The OUT pin will not exceed  $2.2\text{V}$  due to an input signal. At the same time,  $\overline{\text{OUT}}$  will be limited to the same swing below the CM voltage or  $1.4\text{V} - 0.8\text{V} = 0.6\text{V}$ . Done this way, a symmetrical swing is guaranteed whilst a single input voltage dictates the voltage limit in both swing directions.

It is critical that the voltage applied to the CM device pin represents the actual output CM voltage, otherwise the clamp(s) will not function correctly. With the TERM pins utilized, this requires a valid servo operation where LTC6563 maintains the output CM voltage. When the CM servo loop is not utilized (i.e. TERM and  $\overline{\text{TERM}}$  are open), the clamps can still function as long as the CM pin is tied to a voltage that is close to the actual output CM voltage.

**Table 8. Summary of LTC6563 Output Operating Conditions and Their Performance Effect**

OPERATING CONDITION	EFFECT ON OUTPUT CM	EFFECT ON OUTPUT FS SWING	EFFECT ON TOTAL POWER DISSIPATION	EFFECT ON OVERALL GAIN	EFFECT ON SOURCE IMPEDANCE WHEN DRIVING TRANSMISSION LINE
$R_{L\text{DIFF}}$ Value Increase	No Effect	Increase	No Effect	Increase	Increase
Add/Increase R in Series with TERM	Increase	Increase	No Effect	Increase	Increase
$R_{TEE}$ Value Decrease	Reduce	No Effect	No Effect	No Effect	No Effect
ADJ (Logic Input) Increase	Increase	Increase	Increase	Increase	No Effect

## APPLICATIONS INFORMATION

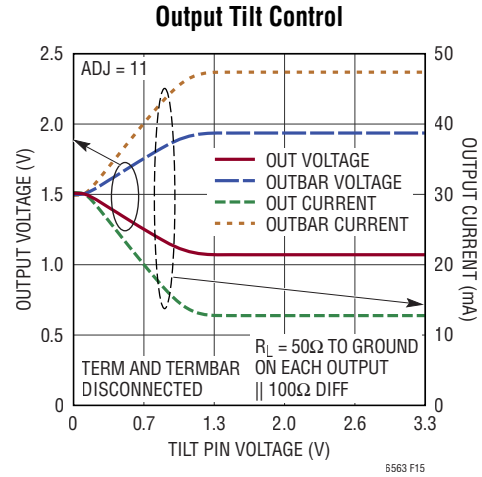
### Avoiding Zero-Input Signal Clipping when Using TILT along with Clamp

Clamp operation is meant to mainly safeguard against transient overload conditions. Under normal operation, ensure that the clamps are not engaged with nominal signal levels and/or zero input current signal! To do this, set the HI input above the expected output voltage, or alternatively, tie HI input to  $V_{CC1}$  to disable clamp operation. When the TILT input is used to maximize the output swing, the voltage applied to the TILT input should be just enough to provide the required differential full-scale voltage without running the output(s) to the clamp region.

Referring to Figure 15 for this particular operating point example:

- $ADJ = 11$ ,  $R_L = 50\Omega$  to ground on each output pin,  $V_{CM}$  pin tied to 1.5V to match actual output CM voltage since CM servo loop is not used here

If clamps are used, set TILT to 1.3V, which is just above the Tilt voltage needed to ensure the maximum output swing can be achieved without running into the clamp(s). In this example, the HI pin should be tied to approximately 2V or higher. If clamps are disabled (HI pin tied to  $V_{CC1}$ ),



**Figure 15. Tilt Input Transfer Function Example (ADJ11) with no TIA Input Current**

TILT input can simply be tied to  $V_{CC1}$  since running into the clamps is not an issue.

### Limitations of Output Clamp Architecture

The out clamps will only prevent overload scenarios that originate from the LTC6563’s signal chain itself. Overloads caused by external stimuli at the LTC6563’s may not be clamped, e.g. injecting current into the LTC6563’s output(s).

# TYPICAL APPLICATIONS

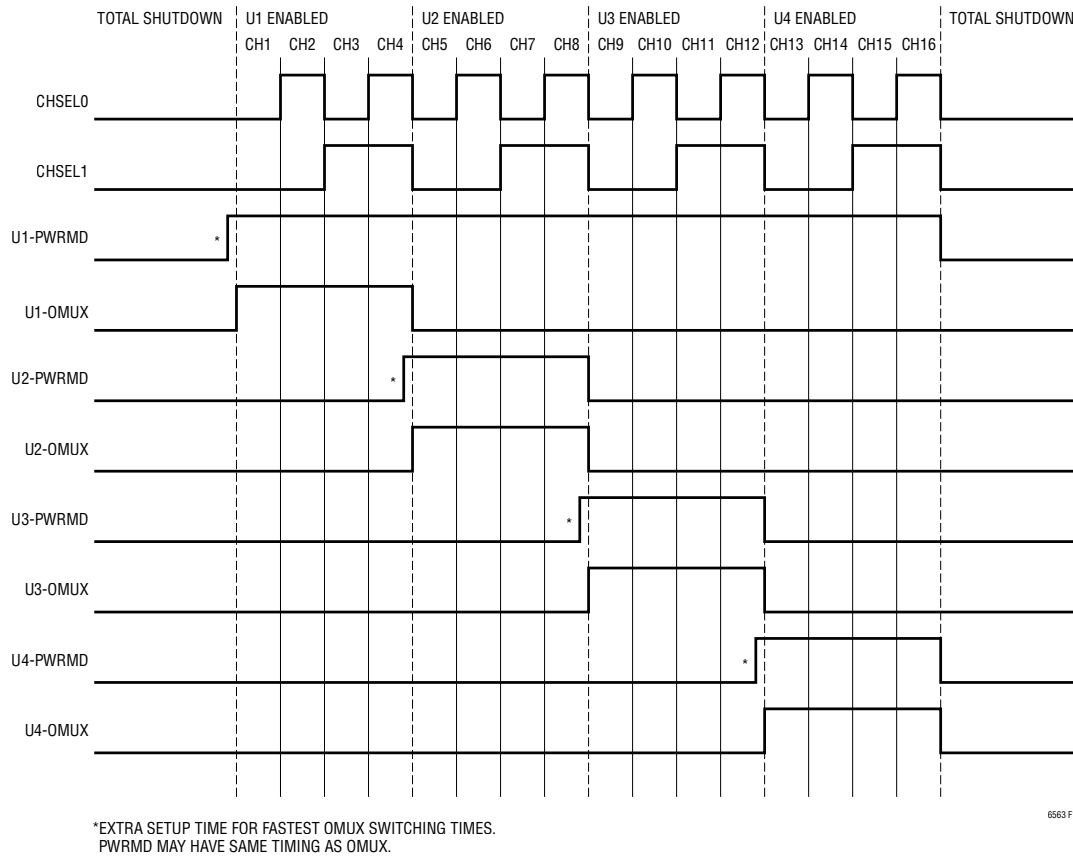


Figure 16. Timing Diagram for OMUX and Channel Control

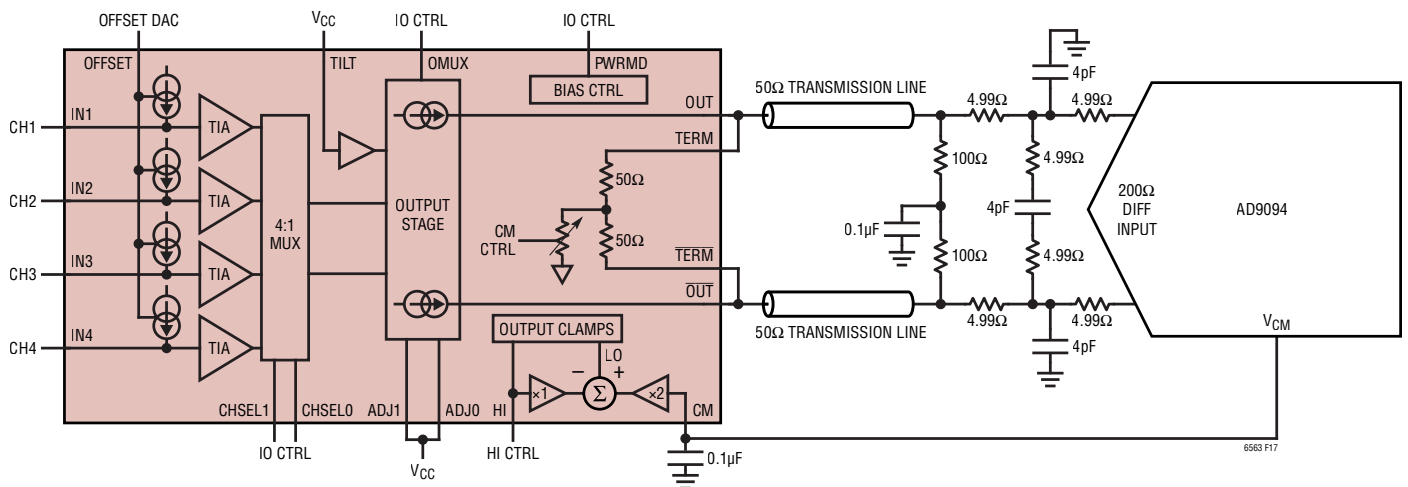


Figure 17. LTC6563 50Ω Transmission Line Circuit

## TYPICAL APPLICATIONS

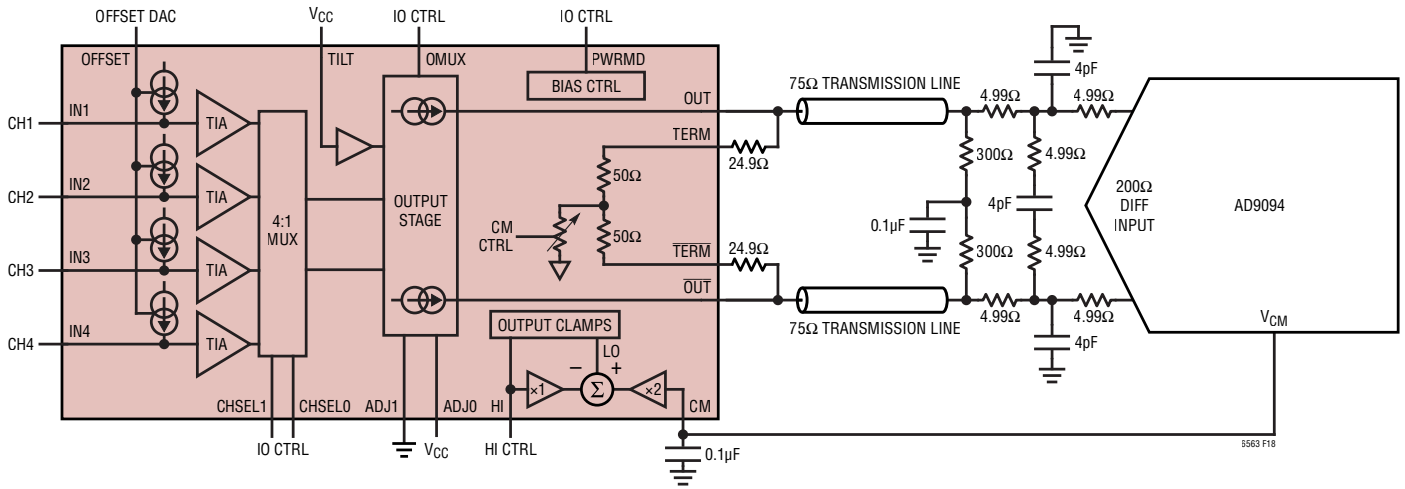


Figure 18. LTC6563 75Ω Transmission Line Circuit

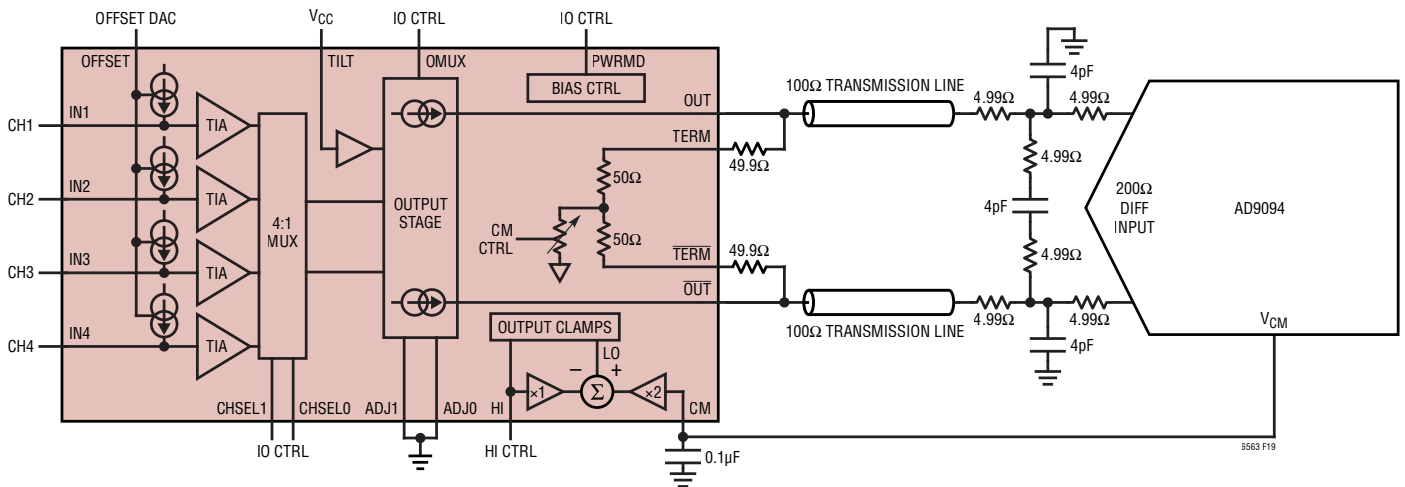
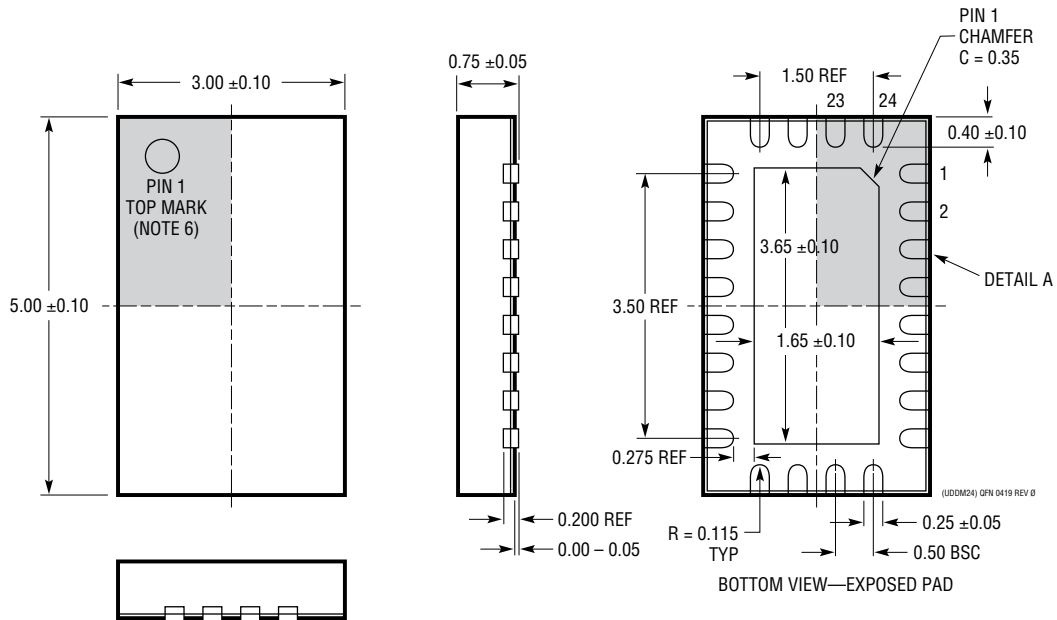


Figure 19. LTC6563 100Ω Transmission Line Circuit



# PACKAGE DESCRIPTION

## UDDM Package 24-Lead Plastic Side Solderable QFN (3mm × 5mm) (Reference LTC DWG # 05-08-1795 Rev 0)



**NOTE:**

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

