

User manual for MA evaluation boards

EVAL_AUDIO_MA2304DNS_B and EVAL_AUDIO_MA2304PNS_B

About this document

Scope and purpose

This document describes the use and operation of the EVAL_AUDIO_MA2304xNS_B evaluation kit (EVK). The MA2304xNS EVK is an evaluation and demonstration kit for MA2304DNS and MA2304PNS proprietary multilevel amplifiers.

Intended audience

Audio amplifier design engineers.

Attention: *Please read this user manual before operating the board. When powering up the board, make sure to follow the instructions in the “MA2304xNS start-up sequence” section.*

Stuck or in need of help?

Support for Infineon’s class D audio portfolio can be found quickly and easily by visiting the [Class D Audio Amplifier IC Forum](#) or community.infineon.com. The community forum features members of the audio applications team who are ready to provide timely support, helping you get your designs done quickly, reliably and right the first time.

Safety precautions

Note: *Please note the following warning regarding hazards associated with development systems.*

Table 1 Safety precautions


	<p>Caution: <i>The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with ESD control procedures, refer to the applicable ESD protection handbooks and guidelines.</i></p>
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Table of contents

About this document	1
Stuck or in need of help?	1
Safety precautions	1
Table of contents	2
1 Overview	3
1.1 Board features and audio performance	3
1.2 EVK device type	3
2 Setup guide	4
2.1 EVK connections and interfaces	5
2.1.1 EVAL_AUDIO_MA2304xNS_B board.....	5
2.1.2 Interface boards	6
2.1.3 Optional heatsink.....	7
2.1.4 EVK headers and connectors	7
2.2 Notes on the digital I/O breakout header.....	9
3 Operating the demonstration board	10
3.1 Recommended operating conditions.....	10
3.2 Toggle switches	10
3.3 Speaker load.....	10
3.4 MERUS™ audio amplifier configurator	11
3.5 MA2304xNS start-up sequence	11
4 Measurement methods	12
5 Schematic	14
5.1 Main page.....	14
5.2 Amp page.....	15
5.3 Power page.....	16
5.4 MCU page.....	17
6 PCB layout	18
7 Bill of materials	21
Revision history	25
Disclaimer	26

Overview

1 Overview

The demonstration board EVAL_AUDIO_MA2304xNS_B is an evaluation and demonstration board for MERUS™ audio's MA2304DNS and MA2304PNS amplifiers.

It contains digital input/output (I/O) and a variety of output and setup/selection features. It also contains one onboard buck power supply generator (1.8 V/3.3 V selectable) so only one external power supply (PVDD) is necessary.

The board can be used to evaluate or demonstrate key features/advantages of the MERUS™ technology:

- Energy efficiency
 - Power losses at typical audio listening levels
 - Idle power loss
- Adaptive power management system
- No output filter components
 - Solution cost and size reduction
- Audio performance
 - THD performance and audio quality

1.1 Board features and audio performance

- | | |
|-----------------------------------|---|
| • Number of audio channels | 2 (BTL) or 1 (PBTL) |
| • Audio input format | Digital (I ² S, LJF, RJF or TDM) |
| • Typical supply voltage | 18 V (PVDD) |
| • Output noise level | 52 μ V _{RMS} (high audio performance mode) |
| • Dynamic range | 106 dB (high audio performance mode) |
| • Idle consumption at PVDD = 18 V | 52 mW (low power consumption mode) |
| • Efficiency | |
| – 1 W, 8 Ω | More than 79 percent |
| – Full-scale, 8 Ω | More than 90 percent |

Note: Idle consumption is the sum of output stage (PVDD) current, VDD and VDD_IO supply current. As all the supplies are tied to PVDD, the efficiency of the buck converter should be considered when measuring idle current consumption directly from PVDD. Features on the EVK make it possible to break the input and output of the buck converters for these purposes (see [Table 3](#)). Please refer to the MA2304xNS device datasheet for exact current figures.

1.2 EVK device type

The type of device – MA2304DNS/MA2304PNS – is printed on the top of the EVK, and is also stated on the serial number label on the bottom side of the EVK PCB.

Setup guide

2 Setup guide

The following is included in the MA2304xNS evaluation kit:

- EVAL_AUDIO_MA2304xNS_B board
- I²S interface boards: analog in, S/PDIF coax and S/PDIF optical
- Micro-USB cable
- 22 μ H power inductor

Additional equipment required for operation and evaluation:

- 10 to 20 V DC power supply capable of driving 6 A (BTL) or 12 A (PBTL)
- Loudspeaker and speaker wires, as shown in **Figure 1**

In addition, for datasheet spec testing, as shown in **Figure 1**:

- 2 to 8 Ω resistor load
- Audio analyzer with class D measurement filter

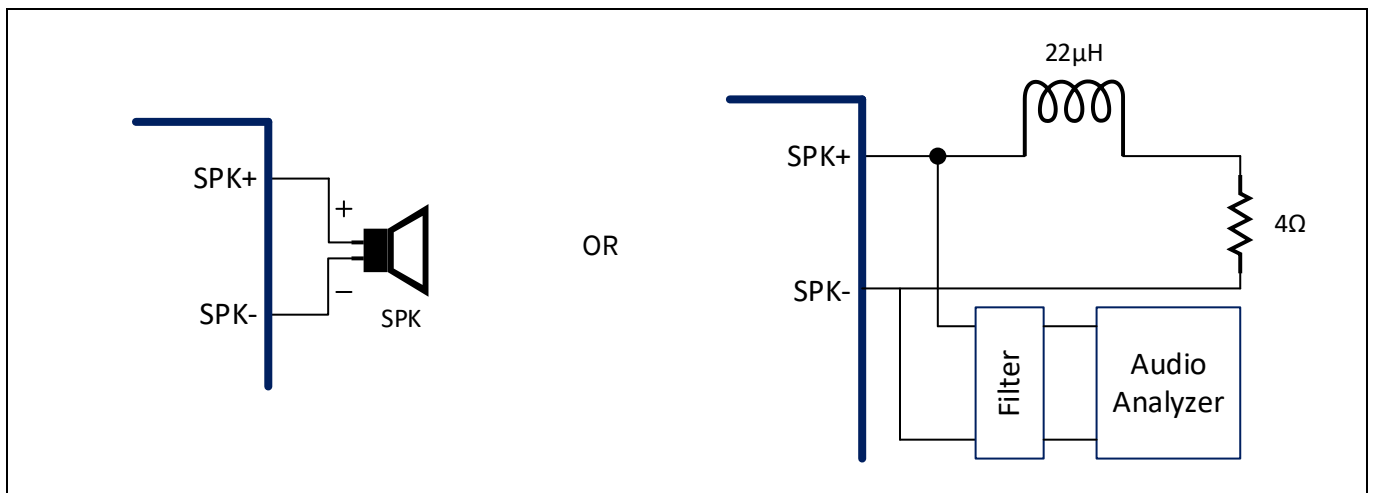


Figure 1 Setup for “speaker test” or “datasheet spec test”

User manual for MA evaluation boards

EVAL_AUDIO_MA2304DNS_B and EVAL_AUDIO_MA2304PNS_B

Setup guide

2.1 EVK connections and interfaces

The MA2304xNS EVK includes the main EVAL_AUDIO_MA2304xNS_B board and three interface boards.

2.1.1 EVAL_AUDIO_MA2304xNS_B board

The board features MA2304xNS silicon, digital I/O headers, enable and mute switches, speaker terminals, power supply terminal blocks, and a USB port.

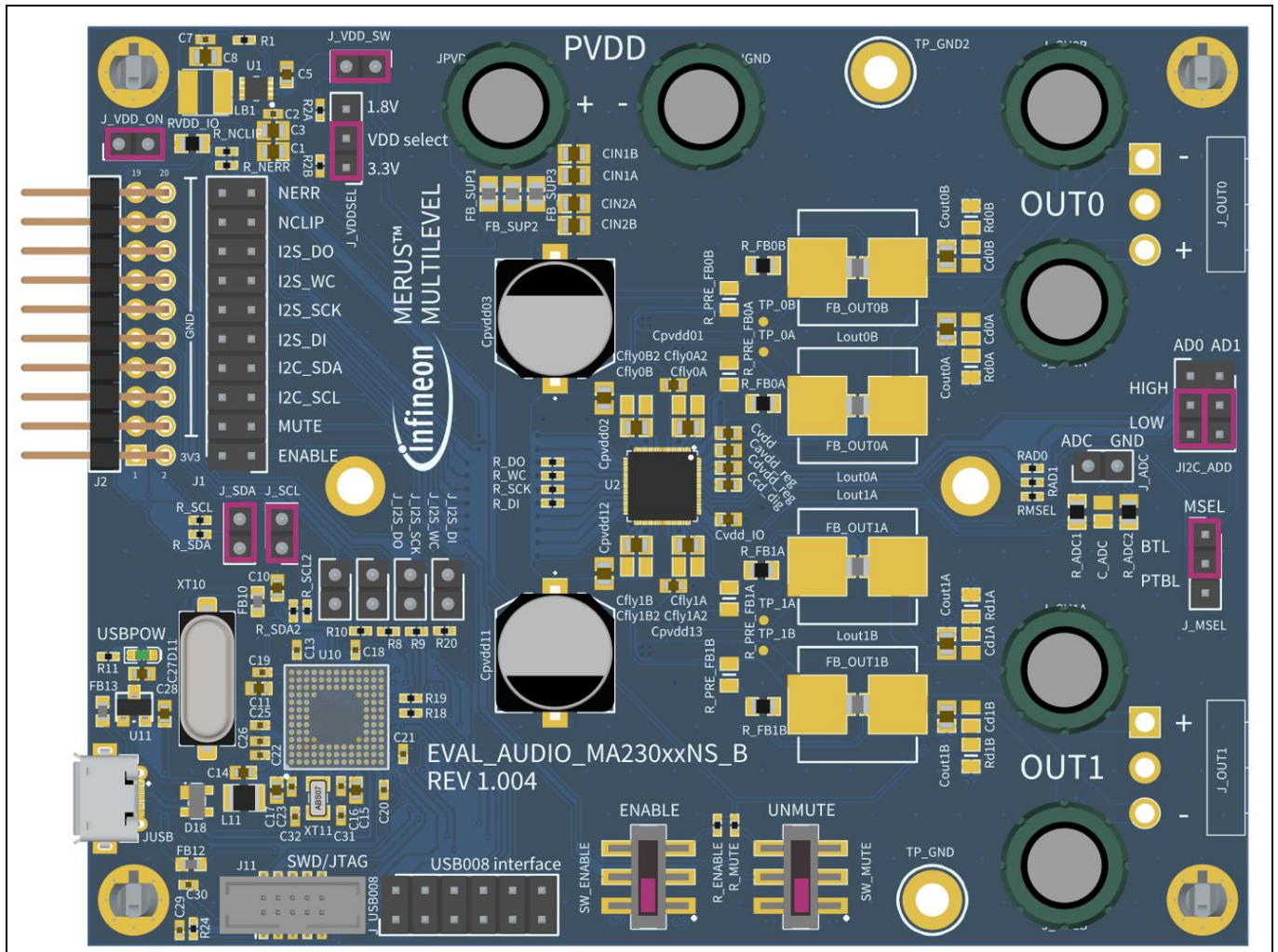


Figure 2 EVAL_AUDIO_MA230xxNS_B board (top view)

2.1.2 Interface boards

Three interface boards are included: analog in, S/PDIF coax and S/PDIF optical. These are plugged in to the J1 digital I/O breakout header for simple evaluation.

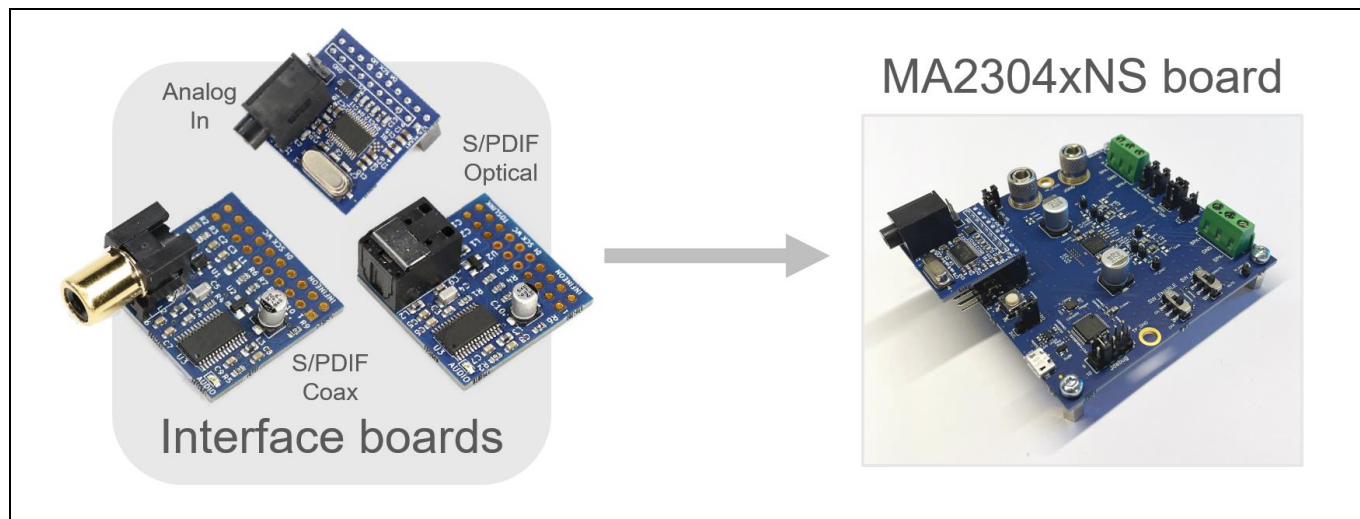


Figure 3 Interface boards

There is no need to configure the MA2304xNS when using these interface boards, as its digital audio output format matches the MA2304xNS defaults.

Note that the interface boards are not compatible with a 1.8 V supply. When using the onboard buck converter, ensure that the MA2304xNS board’s VDD_SEL jumper is configured for 3.3 V (pins 1 and 2).

Interface board input/output specifications are provided in [Table 2](#).

Table 2 Interface board I/O specifications

Interface board	Input	Output
Analog in ¹	3.5 mm (1/8 in.) stereo TRS jack 2.1 V _{RMS} full-scale	I ² S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 48 kHz
S/PDIF coax	RCA jack 0.2 V minimum, 5 V tolerant 32 to 96 kHz support	I ² S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 32 to 96 kHz
S/PDIF optical	Optical input jack 32 to 96 kHz support	I ² S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 32 to 96 kHz

¹Noise measurements and other specs will show degraded performance when using the analog in interface board.

2.1.3 Optional heatsink

EVAL_AUDIO_MA2304xNS_B boards include holes for an optional heatsink. When high continuous output power is required, it is recommended to use a heatsink. Recommended parts are Wakefield-Vette 960-31-28-D-AB-0. Thermal conductivity material may be 3M Electronic Specialty 5519-155x210.

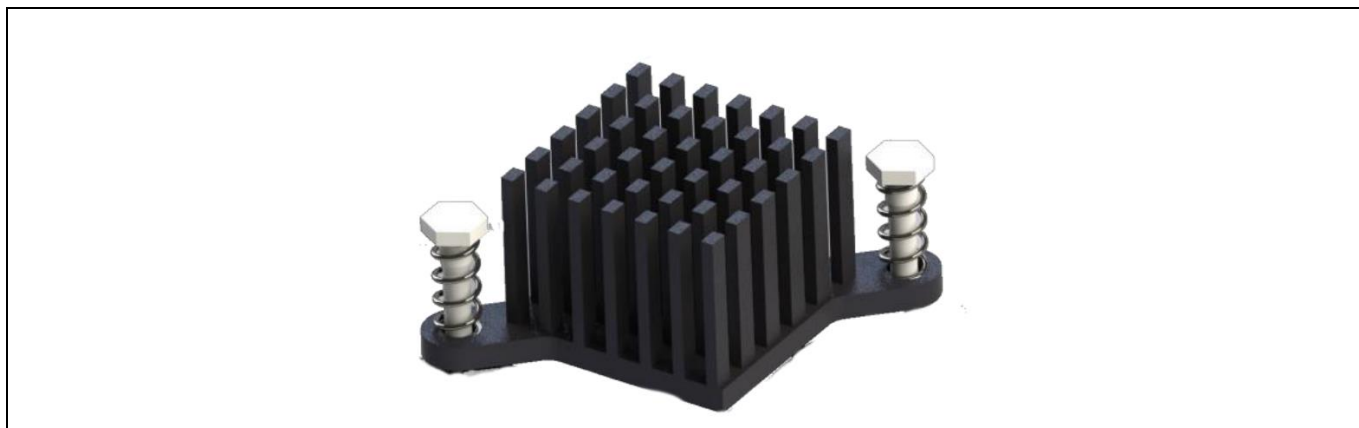


Figure 4 Recommended optional heatsink for continuous output power evaluation

2.1.4 EVK headers and connectors

The following table provides a description of each jumper, header, switch and test point. Defaults are shown in the “Comment” column.

Table 3 EVK headers and connectors

Name	Description	Comment
J1	Digital I/O breakout header. Refer to Section 2.2 for details.	I/O pins. Do not jumper.
J2	Interface board connector	I/O pins. Do not jumper.
J_MSEL	Selects amplifier output mode between PBTL (L) and BTL (H)	Default: BTL (pins 1 and 2)
JI2C_ADD	These headers select the I ² C slave address (see Table 4)	Default: I ² C address 0b0100000 AD1: Low (pins 4 and 6) AD0: Low (pins 3 and 5)
SW_ENABLE	Controls the amplifier’s ENABLE pin. Sets the amplifier into enabled state when set to on.	Default: Off
SW_MUTE	Controls the amplifier’s NMUTE pin. Mutes the amplifier when set to mute.	Default: Mute
J_CH0A	OUT0A speaker connection	CH0 positive speaker output terminal
J_CH0B	OUT0B speaker connection	CH0 negative speaker output terminal
J_CH1A	OUT1A speaker connection	CH1 positive speaker output terminal
J_CH1B	OUT1B speaker connection	CH1 negative speaker output terminal

Setup guide

Name	Description	Comment
J_OUT0	OUT0 speaker connector	Pin 1: OUT0B Pin 2: GND Pin 3: OUT0A
J_OUT1	OUT1 speaker connector	Pin 1: OUT1A Pin 2: GND Pin 3: OUT1B
J_ADC	AUX_ADC input header	Pin 1: ADC input Pin 2: GND
J_VDDSEL	Sets the onboard buck converter output as: 3.3 V (pins 1 and 2) 1.8 V (pins 2 and 3)	Default: 3.3 V (pins 1 and 2)
J_VDD_SW	Provides the option to measure PVDD current into the buck converter	Default: Jumpered
J_VDD_ON	Provides the option to measure the buck converter output current	Default: Jumpered
J_SCL	Provides the option to isolate I2C_SCL from the MCU	Default: Jumpered
J_SDA	Provides the option to isolate I2C_SDA from the MCU	Default: Jumpered
J_I2S_SCK	Provides the option to isolate I2S_SCK from the MCU	Default: Removed
J_I2S_WC	Provides the option to isolate I2S_WC from the MCU	Default: Removed
J_I2S_DO	Provides the option to isolate I2S_DO from the MCU	Default: Removed
J_I2S_DI	Provides the option to isolate I2S_DI from the MCU	Default: Removed
J11	SWD/JTAG header for the onboard MCU	
J_USB008	For future use	
TP_OUT0A	Direct connection to device output node OUT0A	Output measurement pin
TP_OUT0B	Direct connection to device output node OUT0B	Output measurement pin
TP_OUT1A	Direct connection to device output node OUT1A	Output measurement pin
TP_OUT1B	Direct connection to device output node OUT1B	Output measurement pin
TP_GND TP_GND2	Ground test points	
MH1 MH2	Ground-connected mounting holes	

Setup guide

Name	Description	Comment
MH3		
MH4		

Table 4 I²C address decoding (JI2C_ADD)

I ² C device address	AD1	AD0	7-bit I ² C address
0x20	L	L	0b0100000
0x21	L	H	0b0100001
0x22	H	L	0b0100010
0x23	H	H	0b0100011

2.2 Notes on the digital I/O breakout header

The digital I/O breakout header (J1) provides access to audio and control signals (I²S and I²C, respectively) as well as several MA2304xNS GPIO pins and the onboard VDD supply (3.3 or 1.8 V). The J1 header is meant for use with the interface boards, and/or external connections (external I²S, MCU, etc.) for measurements and debugging. The J2 header contains exactly the same signals as J1 but can be used for monitoring the I/O digital signals.

The MA2304xNS acts as an I²S slave, accepting SCK (bit clock) and WC (word clock) as inputs, with SCK = 64 x WC as default.

Table 5 Digital I/O breakout header

Pin	Signal	Signal	Pin
20	GND	/AMP_ERR	19
18	GND	/AMP_CLIP	17
16	GND	I2S_DO	15
14	GND	I2S_WC	13
12	GND	I2S_SCK	11
10	GND	I2S_DI	9
8	GND	I2C_SDA	7
6	GND	I2C_SCL	5
4	GND	/AMP_MUTE	3
2	3.3V	AMP_ENABLE	1

3 Operating the demonstration board

3.1 Recommended operating conditions

Table 6 Recommended operating conditions

Parameter	Minimum	Nominal	Maximum	Unit
PVDD	10	18	20	V
Output peak current (BTL)			6.0	A
Output peak current (PBTL)			12.0	A

3.2 Toggle switches

The board has two MA2304xNS-related toggle switches, as shown in [Table 7](#). The toggle switches have the following functions:

Table 7 Switch function

Switch	Function
SW_ENABLE	Off/enable (default set to “off”)
SW_MUTE	Mute/unmute (default set to “mute”)

3.3 Speaker load

The demonstration board is configured as a filterless amplifier. This means that no LC filter is placed between the amplifier outputs and the load. In normal use the amplifier relies on the inherent inductance of the loudspeaker, so no extra inductance is needed.

Inductors for use in series with power resistors are included with the demonstration board. These can be used when making any measurements without a real loudspeaker as the load, and having no external low-pass filter (LPF) in front of the audio analyzer input section.

Please note that many audio measurement analyzers do not perform correctly when connected directly to a filterless amplifier output. Please refer to [Section 4](#) for more information on measurement methods.

3.4 MERUS™ audio amplifier configurator

The demonstration board is used with PC graphical user interface (GUI) software to control the MA2304xNS device.

The MA2304xNS can play audio by default without configuration, but to take advantage of the many features the chip offers it is necessary to configure the device.

Refer to the MERUS™ audio amplifier configurator user manual for details on how to install and use this software.



Figure 5 MA2304DNS GUI main window

3.5 MA2304xNS start-up sequence

Follow this (recommended) sequence to start the board:

1. Make sure toggle buttons are in “off” and “mute” positions.
2. Connect all cables (speakers/load, USB and power) to the EVK.
3. Connect an external I²S digital audio source to the EVK digital I/O header (J1). The EVK default I/O voltage is 3.3 V.
4. Turn on the PVDD power supply.
5. Make sure the I²S clocks are present before enabling the amplifier.
6. Start board by setting the SW_ENABLE toggle switch to the “on” position.
7. Start playing sound by setting the SW_MUTE toggle switch to the “unmute” position.

Mute and turn off the PVDD power supply when finished.

4 Measurement methods

Setting up a reliable measurement configuration for the MA2304DNS or the MA2304PNS takes a little more effort than for linear amplifiers, and even “regular” switching amplifiers. This is mainly because the MA2304xNS is a filterless amplifier, which means it does not require an external (usually expensive and bulky) LC filter to remove switching residuals. The filterless application is enabled by the MERUS™ audio multilevel technique, which ensures the switching residual is orders lower compared to “regular” switching amplifiers. For more information on the multilevel switching technique, please refer to the datasheet.

To obtain reliable measurement results, the MA2304xNS devices require a separate external LPF in front of the input stage of the audio analyzer. Most audio analyzers are bandwidth-limited at their input stage, which means they cannot follow the rapid changes of the amplifier’s output stage. This can result in inaccurate and high THD+N measurements.

Figure 6 shows the recommended measurement setup. The setup shows a LPF stage (AUX-0025) in front of the audio analyzer (APx525 with the serial interface I/O option installed). In this case the measurement setup has been built around Audio Precision hardware, but this can also be some other audio analyzer hardware. Please note that it is recommended to use a balanced input measurement configuration.

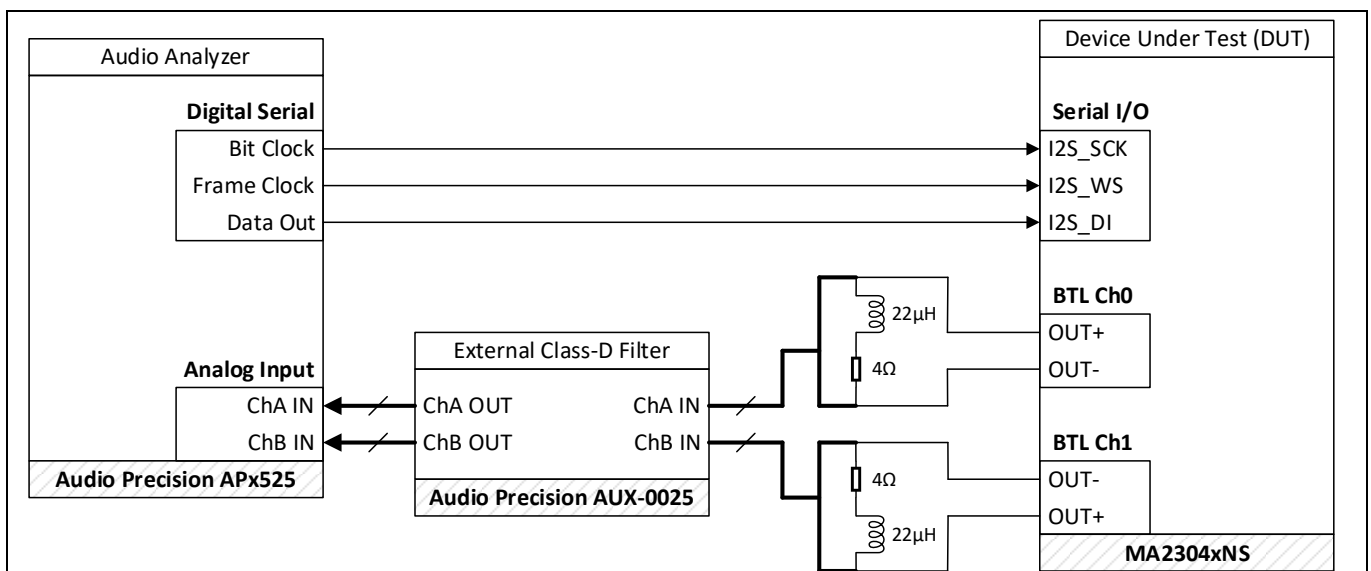


Figure 6 Recommended audio measurement setup

User manual for MA evaluation boards

EVAL_AUDIO_MA2304DNS_B and EVAL_AUDIO_MA2304PNS_B

Measurement methods

Figure 7 shows an example measurement setup using an 8 Ω/22 μH load, similar to the setup shown in Figure 6.

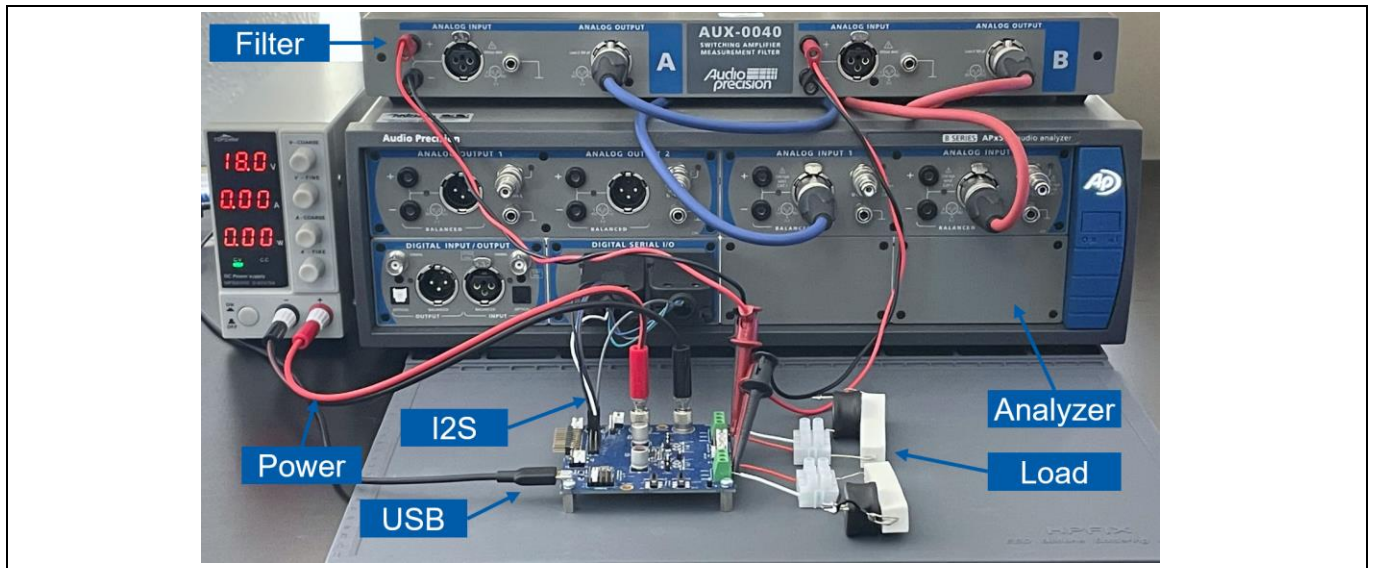


Figure 7 Audio measurement setup example

Figure 8 shows an example dynamic range measurement performed with the previous measurement setup.

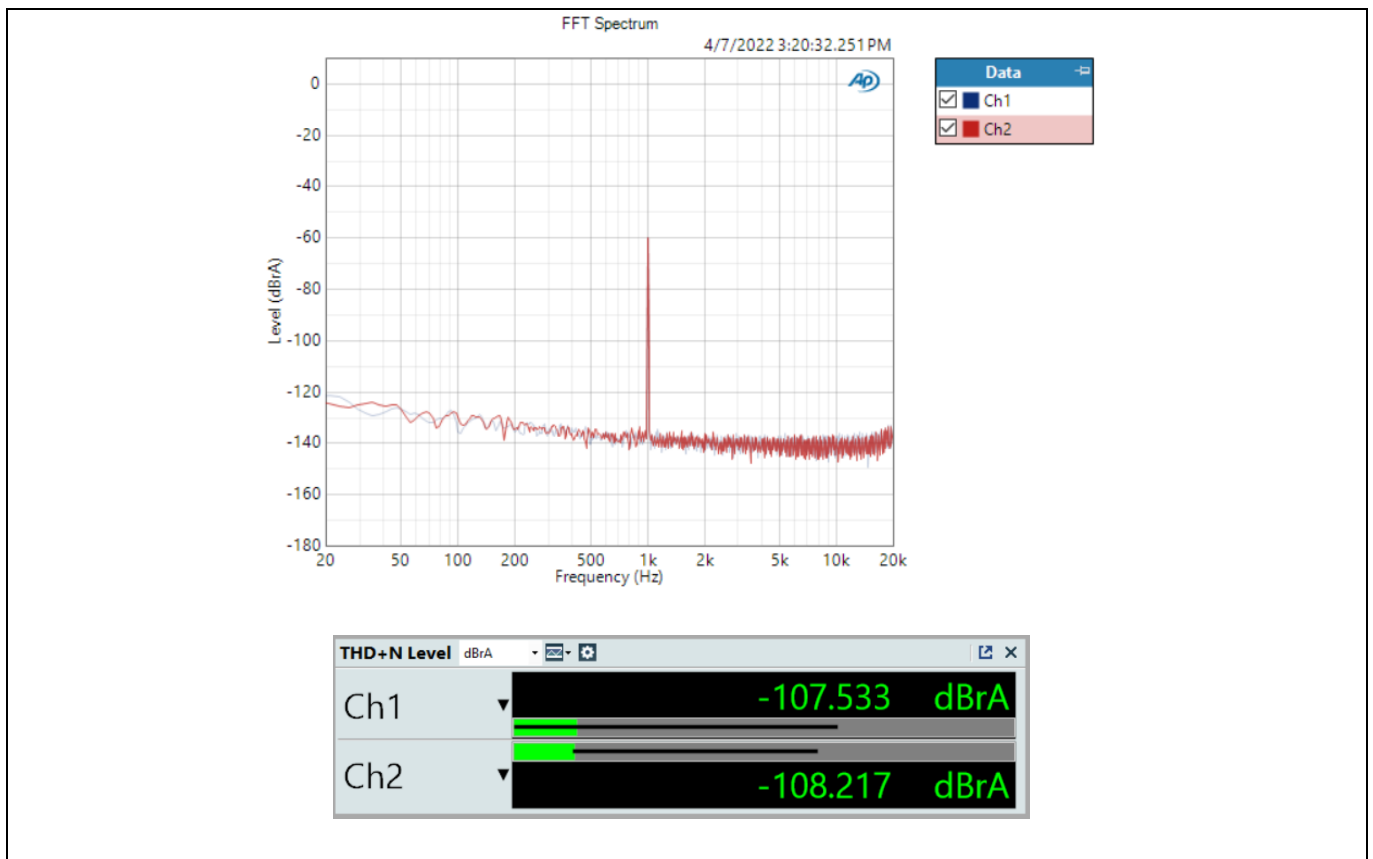


Figure 8 Dynamic range measurement example

User manual for MA evaluation boards

EVAL_AUDIO_MA2304DNS_B and EVAL_AUDIO_MA2304PNS_B

Schematic

5.4 MCU page

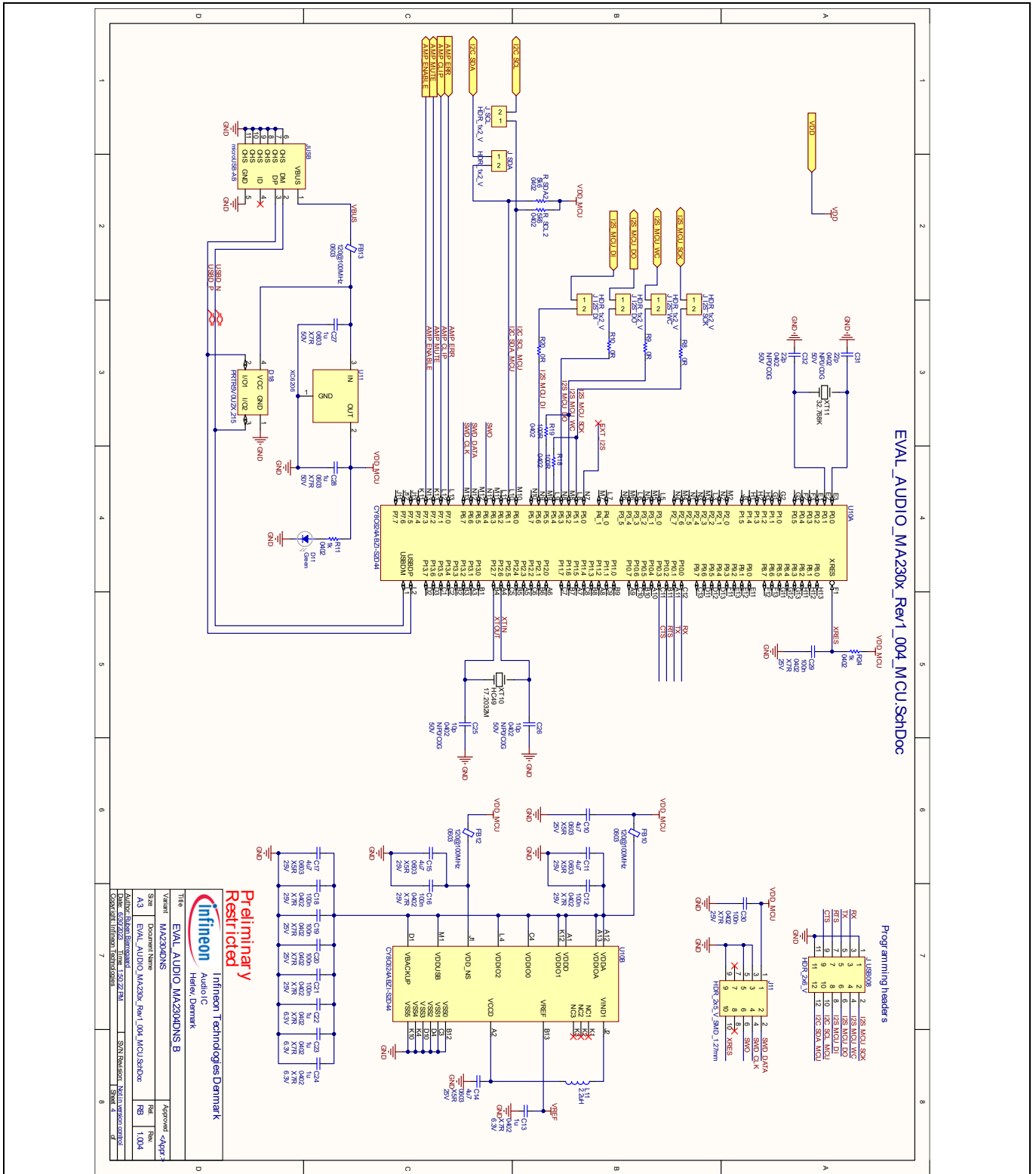


Figure 12 MCU page

6 PCB layout

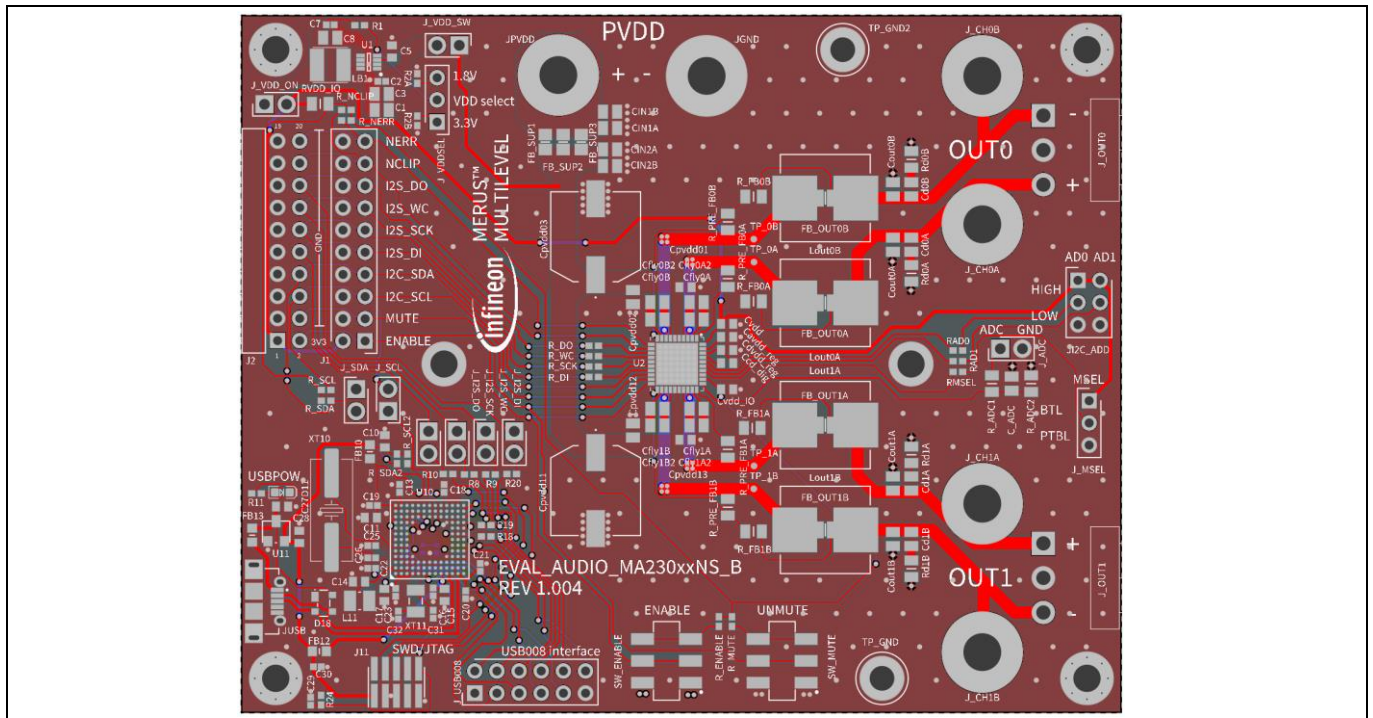


Figure 13 PCB layout (top x-ray view)

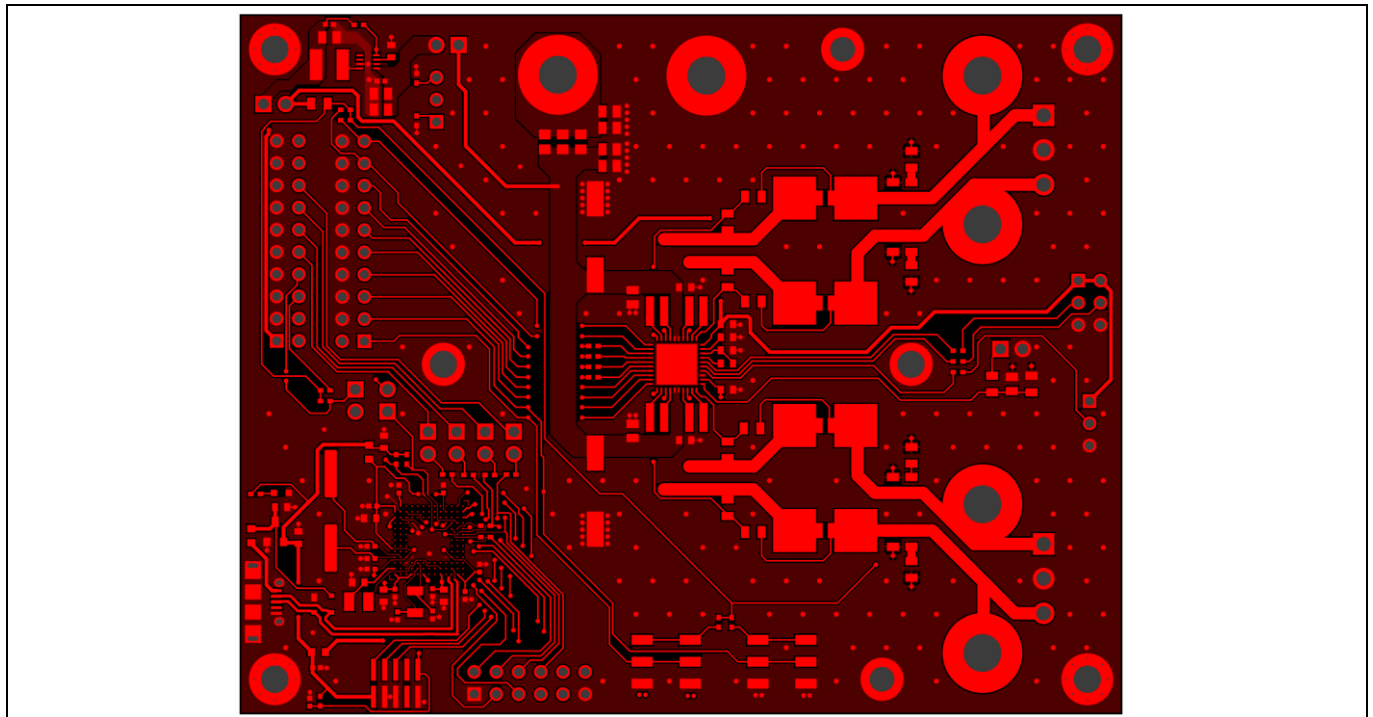


Figure 14 PCB layout (top layer)

PCB layout

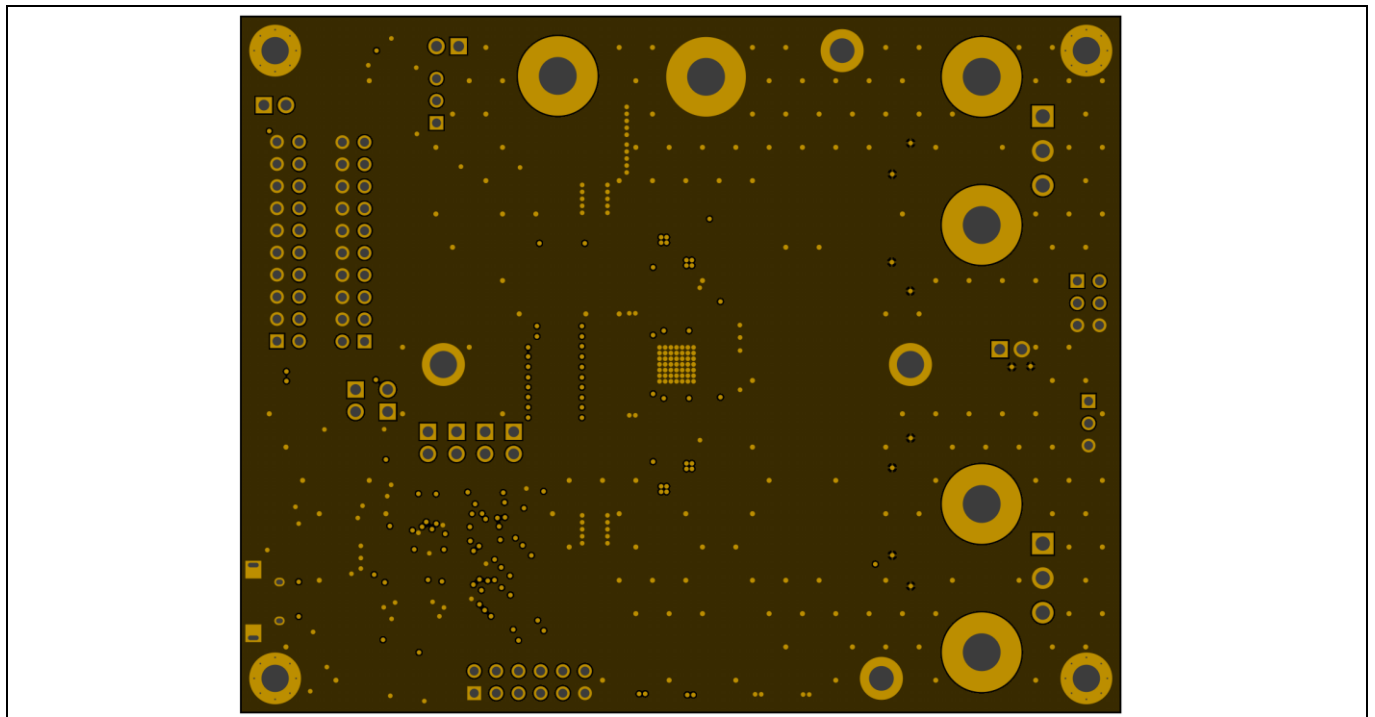


Figure 15 PCB layout (layer 1)

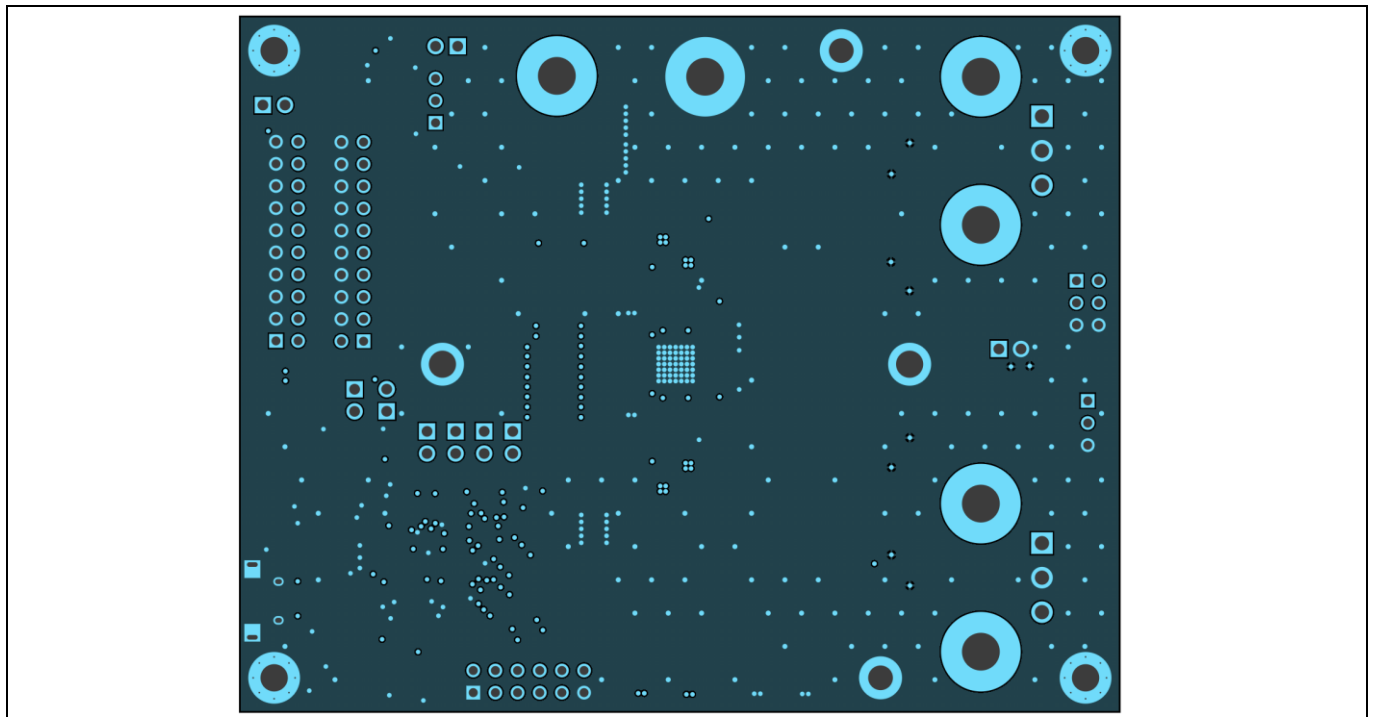


Figure 16 PCB layout (layer 2)

PCB layout

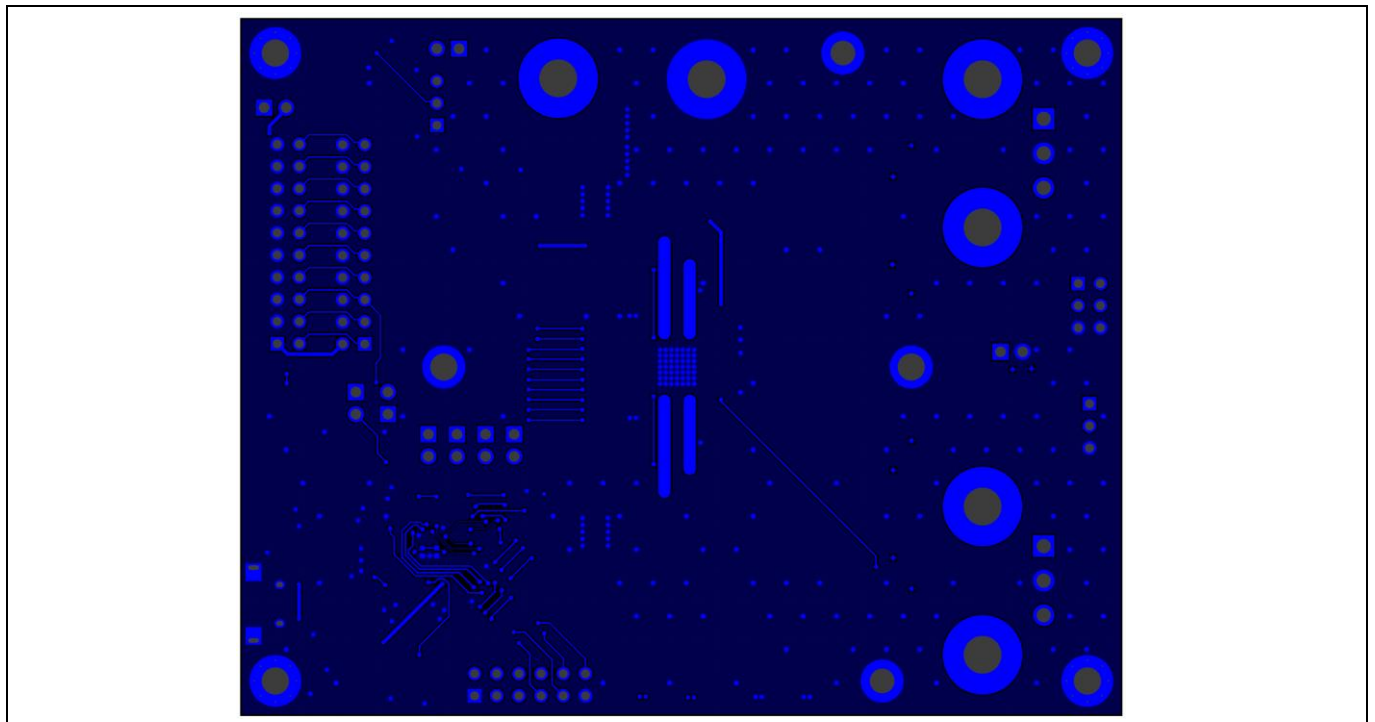


Figure 17 PCB layout (bottom layer)

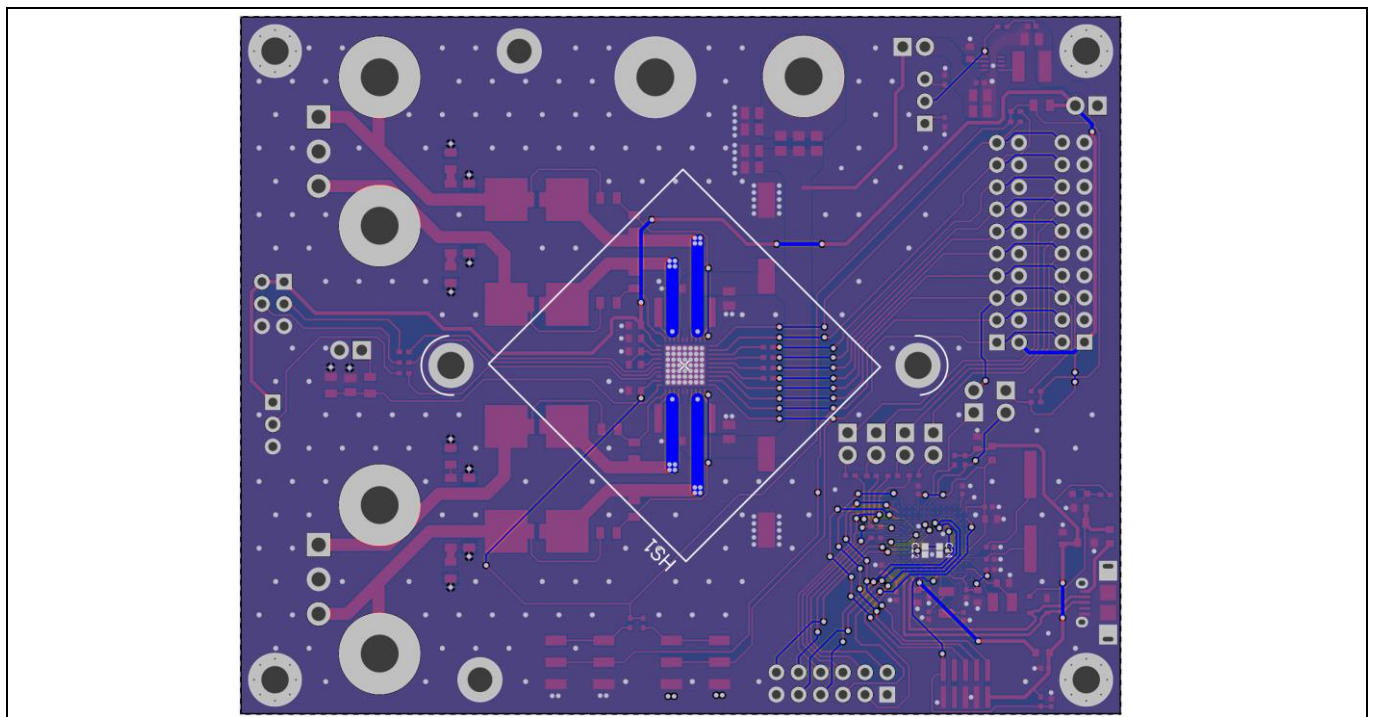


Figure 18 PCB layout (bottom x-ray view, mirrored)

Bill of materials

7 Bill of materials

Table 8 Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
1	XT11	1	Crystal 32.7680 kHz 9 pF SMD	Abrakon	ABS07-32.768KHZ-9-1-T
2	XT10	1	2.2 μ F 50 V X5R 0805	Würth Elektronik	WE-XTAL QUARTZ CRYSTAL 17.20320
3	U11	1	40 dB at (1 kHz) 100 mA 240 mV at (50 mA) F	Torex	XC6206P332MR
4	U10	1	IC dual-core MCU 32 B 1 M 124 BGA	Cypress Semiconductor	CY8C624ABZI-S2D44
5	U2	1	DUT	Infineon Technologies	MA2304xxx
6	U1	1	IC buck regulator ADJ 300 mA 8TDFN	Maxim Integrated	MAX15462CATA+T
7	TP_0A, TP_0B, TP_1A, TP_1B	4			
8	SW_ENABLE, SW_MUTE	2	Slide switch DPDT 300 mA 6 V	C&K Components	JS202011SCQN
9	SPA1, SPA2, SPA3, SPA4	4	Hex standoff M3 Nylon 30 mm	Essentra Components	MTS-30
10	SCRW1, SCRW2, SCRW3, SCRW4	4	Slotted mach. screw pan M3X0.5	Keystone	29341
11	RAD0, RAD1, RMSEL	3	Resistor 0 Ω jumper 1/16 W 0402	Vishay/Dale	CRCW04020000Z0EDC
12	R_SCL, R_SCL2, R_SDA, R_SDA2	4	Resistor SMD 5.6K Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF5601X
13	R_FB0A, R_FB0B, R_FB1A, R_FB1B	4	Resistor SMD 0 Ω jumper 1/8W 0805	Bourns	CR0805-J/-000ELF
14	R_ENABLE, R_MUTE, R_NCLIP, R_NERR	4	Resistor 10K Ω 1% 1/16W 0402	Vishay/Dale	CRCW040210K0FKEDC
15	R_DI, R_DO, R_SCK, R_WC	4	Resistor 33 Ω 1% 1/16W 0402	Vishay/Dale	CRCW040233R0FKEDC
16	R_ADC2	1	Resistor SMD 10K Ω 1% 1/8W 0805	Bourns	CR0805-FX-1002ELF
17	R_ADC1, RVDD_IO	2	Resistor 0 Ω jumper 1/8 W 0805	Yageo	AC0805FR-070RL
18	R18, R19	2	Resistor SMD 100 Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF1000X
19	R11, R24	2	Resistor SMD 1K Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF1001X

Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
20	R8, R9, R10, R20	4	Resistor 0 Ω jumper 1/16 W 0402	Yageo	RC0402FR-070RL
21	R2B	1	Resistor SMD 68K Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF6802X
22	R1, R2A	2	Resistor SMD 180K Ω 1% 1/10 W 0402	Panasonic	ERJ-2RKF1803X
23	MH1, MH2, MH3, MH4	4			
24	LB1	1	Fixed inductor 33 μH 500 mA 366 mΩ SMD	Bourns	SRN4026-330M
25	L11	1	Fixed inductor 2.2 μH 1.15 A 216 mΩ SM	Sunlord	SWPA252012S2R2MT
26	JUSB	1	Connector receptor micro-USB AB 5P SMD RA	Molex	47589-0001
27	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16	8	Jumper with test point 1 x 2 pins 2.54 mm	Würth Elektronik	60900213421
28	J12C_ADD	1	Vertical header connector 6 position 2.54 mm	Würth Elektronik	61300621121
29	J_USB008	1	Vertical header connector 12 position 2.54 mm	Würth Elektronik	61301221121
30	J_MSEL, J_VDDSEL	2	Vertical header connector 3 position 2.54 mm	Würth Elektronik	61300311121
31	J_CH0B, J_CH1B, J_GND	3	Connector bind post knurled black	Pomona	3760-0
32	J_CH0A, J_CH1A, J_VDD	3	Connector bind post knurled red	Pomona	3760-2
33	J_ADC, J_I2S_DI, J_I2S_DO, J_I2S_SCK, J_I2S_WC, J_SCL, J_SDA, J_VDD_ON, J_VDD_SW	9	Vertical header connector 2 position 2.54 mm	Würth Elektronik	61300211121
34	J11	1	Header connector SMD 10 position 1.27 mm	CNC Tech	3221-10-0300-00

Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
35	J2	1	Header connector R/A 20 position 2.54 mm	Würth Elektronik	61302021021
36	J1	1	Vertical header connector 20 position 2.54 mm	Würth Elektronik	61302021121
37	HS1	1	Heatsink 31 x 23 mm diameter push pin	Wakefield	960-31-23-D-AB-0
38	FB_SUP1, FB_SUP2, FB_SUP3	3	Ferrite bead 330 Ω 0805 1LN	Murata	BLM21SP331SZ1#
39	FB_OUT0A, FB_OUT0B, FB_OUT1A, FB_OUT1B	4	Ferrite bead 15 Ω 0806 1LN	Murata Electronics	NFZ2MSD150SN10L
40	FB10, FB12, FB13	3	Ferrite bead 120 Ω 0603 1LN	Murata	BLM18KG121TN1D
41	D18	1	TVS diode 5.5 V WM SOT-143B	NXP Semiconductors	PRTR5V0U2X,215
42	D11	1	LED green clear chip SMD	Lite-On	LTST-C190KGKT
43	Cpvdd03, Cpvdd11	2	Aluminum capacitor 330 μF 20% 35 V SMD	Vishay/BC Components	MAL215099003E3
44	Cpvdd02, Cpvdd12	2	Ceramic capacitor 10 μF 50 V X5R 0805	Murata	GRM21BR61H106KE43L
45	Cpvdd01, Cpvdd13	2	Ceramic capacitor 1 μF 50 V X5R 0603	TDK	C1608X5R1H105K080AB
46	Cout0A, Cout0B, Cout1A, Cout1B	4	Ceramic capacitor 220 pF 50 V X7R 0805	Kemet	C0805C221K5RAC
47	CIN1B, CIN2B	2	Ceramic capacitor 2200 pF 50 V X7R 0805	Murata	GCJ216R71H222KA01D
48	CIN1A, CIN2A	2	Ceramic capacitor 2.2 μF 50 V X7R 0805	Taiyo Yuden	UMK212BB7225KG-T
49	Cfly0A, Cfly0B, Cfly1A, Cfly1B	4	Ceramic capacitor 10 μF 25 V X7R 0805	Samsung Electro- Mechanics	CL21B106KAYQNE
50	Cavdd_reg, Ccd_dig, Cdvdd_reg, Cvdd, Cvdd_IO	5	Ceramic capacitor 1 μF 25 V X5R 0603	Samsung	CL10A105KA8NFNC
51	C31, C32	2	Ceramic capacitor 22 pF 50 V C0G/NP0 0402	Kemet	CBR04C220J5GACAUTO

Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
52	C27, C28	2	Ceramic capacitor 1 μ F 50 V X5R 0603	Murata	GRT188R61H105ME13D
53	C25, C26	2	Ceramic capacitor 10 pF 50 V C0G/NP0 0402	Kemet	C0402C100F5GACTU
54	C13, C22, C23	3	Ceramic capacitor 1 μ F 6.3 V X6S 0402	TDK	CGB2A1X6S0J105M033BC
55	C8	1	Ceramic capacitor 22 μ F 10 V X5R 0805	Samsung	CL21A226MPCLRNC
56	C7, C16, C18, C19, C20, C21, C29, C30	8	Ceramic capacitor 0.1 μ F 25 V X5R 0402	Samsung	CL05A104KA5NNND
57	C5, C10, C11, C14, C15, C17	6	Ceramic capacitor 4.7 μ F 25 V X5R 0603	Samsung	CL10A475KA8NQNC
58	C2	1	Ceramic capacitor 0.1 μ F 50 V X7R 0402	Murata	GRM155R71H104KE14D
59	C1, C3	2	Ceramic capacitor 2.2 μ F 50 V X5R 0805	Samsung	CL21A225KBQNNNE



Revision history

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Document version	Date of release	Description of changes
V 1.0	2023-07-14	Initial release