2ED28073J06F
600 V half-bridge gate driver with integrated bootstrap diode

Features

- Negative VS transient immunity of 70 V, dV/dt immune
- Lower di/dt gate driver for better noise immunity
- Floating channel designed for bootstrap operation
- Operating voltages (VS node) upto + 600 V
- Maximum bootstrap voltage (VB node) of + 625 V
- Integrated bootstrap diode
- Integrated shoot-through protection with built-in dead time
- Integrated short pulse / noise rejection filter on input
- Independent under voltage lockout for both high and low side
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V and 15 V input logic compatible
- Maximum supply voltage of 25 V
- Outputs in phase with inputs
- Suitable for both trapezoidal and sinusoidal motor control
- Available in small footprint DSO-8
- RoHS compliant

Product summary

V_{S_OFFSET} = 600 V max
$I_{O+\ pk}$ / $I_{O-\ pk}$(typ) = + 20 mA/ - 80 mA
V_{CC} = 10 V to 20 V
Delay matching = 50 ns max.
Deadtime (typ.) = 300 ns
t_{ON} / t_{OFF} (typ.) = 530 ns/ 530 ns

Package

8-Lead DSO-8

Potential applications

Driving IGBTs, enhancement mode N-Channel MOSFETs in various motor control applications.
Infineon recommendation for driving fast body diode CoolMOS™ PFD7 super junction MOSFETs and IGBTs in

- Refrigeration Compressors
- Air Conditioner fans
- Washing Machines and dishwasher pumps
- General Purpose Inverters
- Micro/Mini Inverter Drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC78/20/22

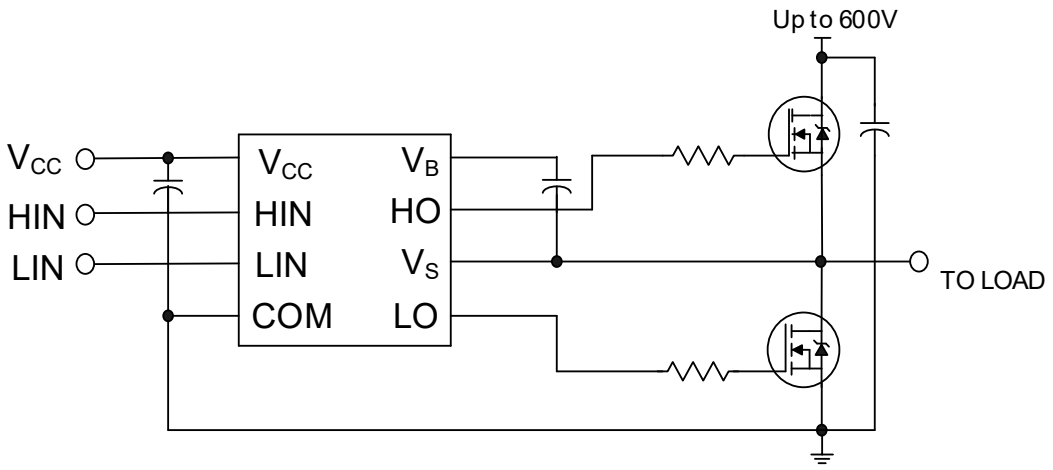
Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED28073J06F	DSO-8	Tape and Reel	2500	2ED28073J06FXUMA1

Description

The 2ED28073J06F is a high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The

floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600V.



Refer to lead assignments for correct pin configuration. This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application block diagram

1 Table of contents

2 Block diagram

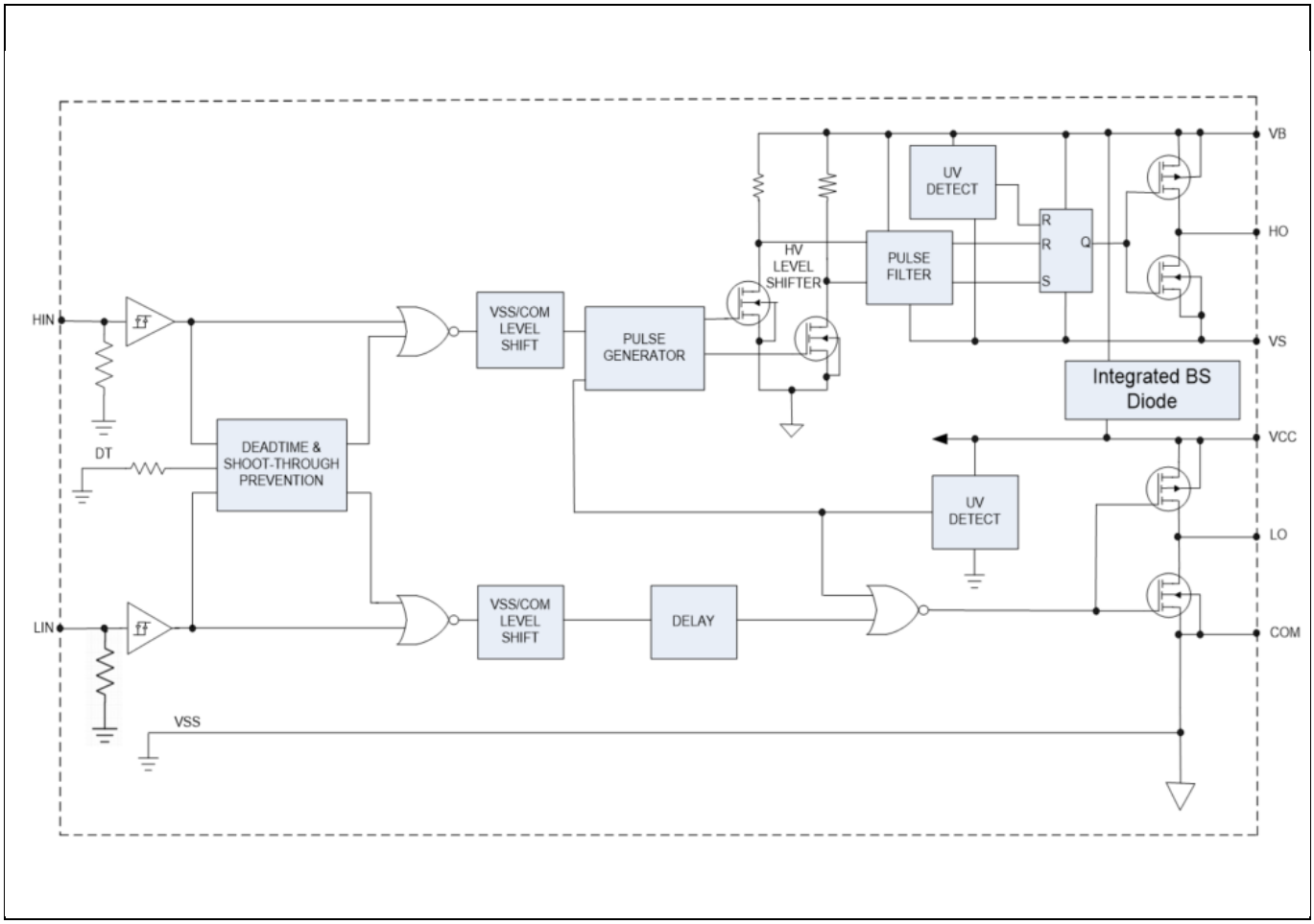
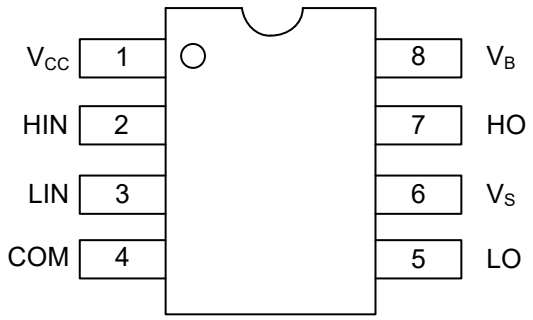


Figure 2 Block diagram

3 Pin configuration and functionality

3.1 Pin configuration



8-Lead DSO-8 (150 mil)
2ED28073J06F

Figure 3 2ED28073JS06F pin assignments (top view)

3.2 Pin functionality

Table 1

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 2 Absolute maximum ratings

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating well supply voltage (Note 1)		-0.3	625	V
V_S	High-side floating well supply return voltage		V_B – 25	V_B + 0.3	
V_{HO}	Floating gate drive output voltage		V_S – 0.3	V_B + 0.3	
V_{CC}	Low side supply voltage		-0.3	25	
V_{LO}	Low-side output voltage		–0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)		COM -0.3	V_{CC} + 0.3	
dV_S/dt	Allowable V_S offset supply transient relative to COM		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8-Lead DSO-8	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead DSO-8	—	200	°C/W
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B. Zener clamps are included between V_{CC} & COM, V_B & V_S (20V).

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – COM) = (V_B – V_S) = 15 V.

Table 3 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	Bootstrap voltage	V_S + 10	V_S + 20	V
V_{BS}	High-side floating well supply voltage	10	20	
V_S	High-side floating well supply offset voltage	COM- 8[2]	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	COM	V_{CC}	
T_A	Ambient temperature	-40	+125	°C

Note 2: Logic operational for V_S of -8V to +600V. Logic state held for V_S of -8V to -V_{BS}.

4.3 Static electrical characteristics

(V_{CC}– COM) = (V_B – V_S) = 15 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 4 Static electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.9	7.7	8.5		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	—	1.2	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.0	8.9	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	6.9	7.7	8.5		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	—	1.2	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	uA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		V_{IN} = 0V or 4V
I_{QCC}	Quiescent V_{CC} supply current	1000	1800	3000		
V_{OH}	High level output voltage drop, V_{cc}- V_{LO} , V_B- V_{HO}	—	1.3	—	V	I_O = 4 mA
V_{OL}	Low level output voltage drop, V_O	—	0.16	—		
I_{o+}	Peak output current turn-on[1]	—	20	—	mA	V_O = 0 V PW ≤ 10 µs
I_{o-}	Peak output current turn-off[1]	—	80	—		V_O = 15 V PW ≤ 10 µs
V_{IH}	Logic “1” input voltage	2.2	—	—	V	Vcc=10 V to 20 V
V_{IL}	Logic “0” input voltage	—	—	0.8		
I_{IN+}	Input bias current (Output = High)	—	5	20	µA	V_{IN} = 4 V
I_{IN-}	Input bias current (Output = Low)	—	—	2		V_{IN} = 0 V
R_{BSD}	Bootstrap diode resistance	—	200	—	Ω	

[1] Not subjected to production test, verified by characterization.

4.4 Dynamic electrical characteristics

V_{CC} = V_{BS}= 15 V, V_{SS} = COM, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Table 5 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	530	790	ns	V_S = 0 V or 600 V
t_{OFF}	Turn-off propagation delay	—	530	790		
t_R	Turn-on rise time	—	1500	—		V_S = 0 V
t_F	Turn-off fall time	—	225	—		
MT	Delay matching time (HS & LS turn-on/off)	—	—	50		
DT	Deadtime: LO Turn-off to HO Turn-on & HO Turn-off to LO turn-on	—	300	—		V_S = 0 V, 5 V
t_{fil}	Minimum pulse input filter time	—	300	—		

5 Application information and additional details

5.1 IGBT / MOSFET gate drive

The 2ED28073J06F HVIC is designed to drive MOSFET or IGBT power devices. Figures 4 and 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

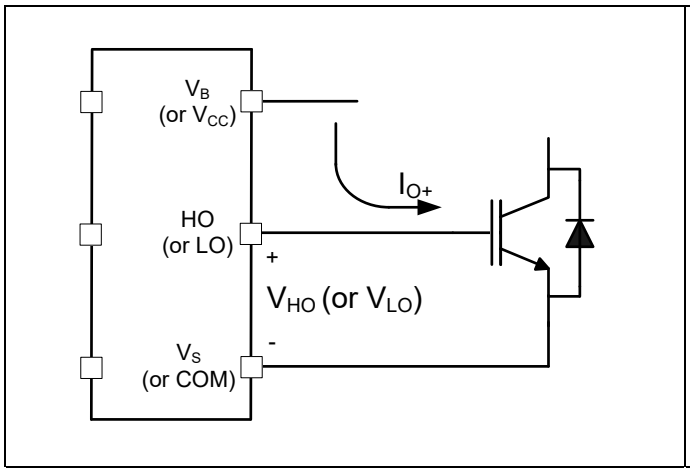


Figure 4 HVIC Sourcing current

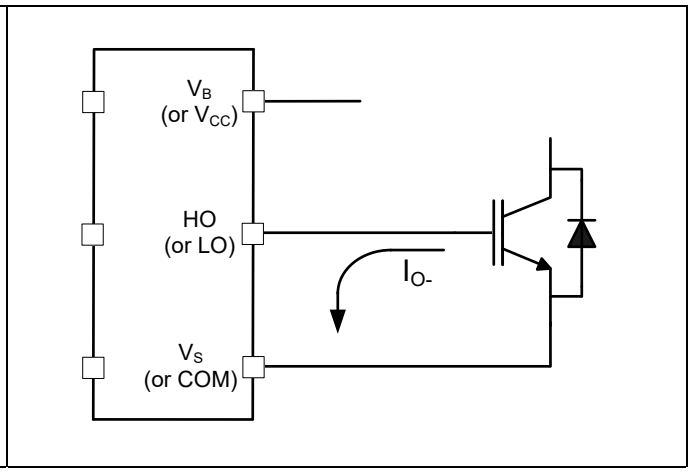


Figure 5 HVIC Sinking current

5.2 Switching and timing relationships

The relationships between the input and output signals of the 2ED28073J06F are illustrated below in Figure 6 and Figure 7. From these figures, we can see the definitions of several timing parameters (i.e. PW_{IN}, PW_{OUT} , t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

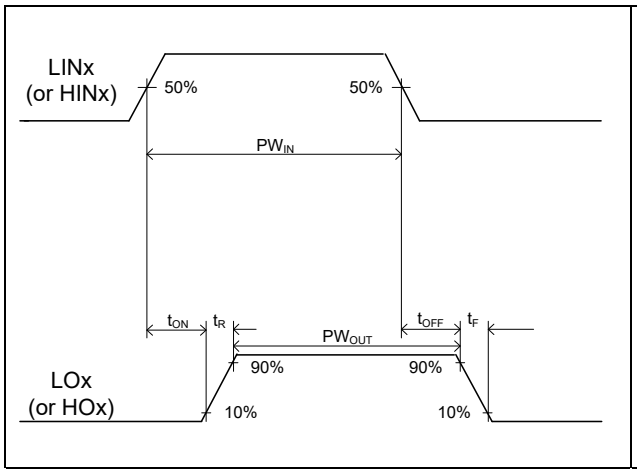


Figure 6 Switching timing diagram

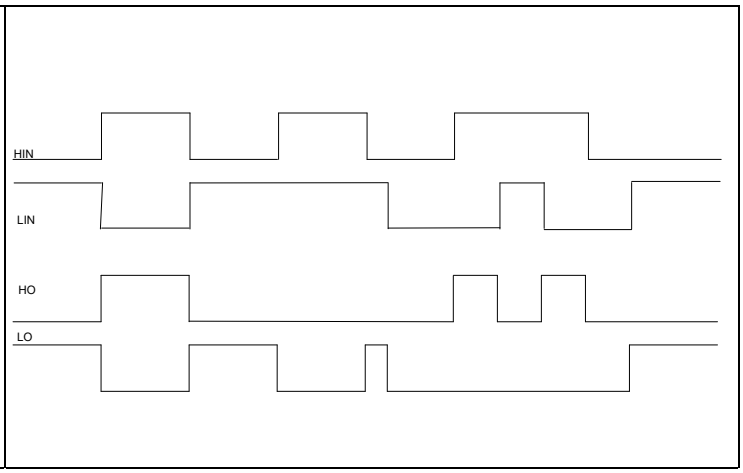


Figure 7 Input/output logic diagram

5.3 Deadtime and matched propagation delays

This family of HVICs features integrated deadtime protection circuitry. The deadtime for these ICs is fixed. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver.

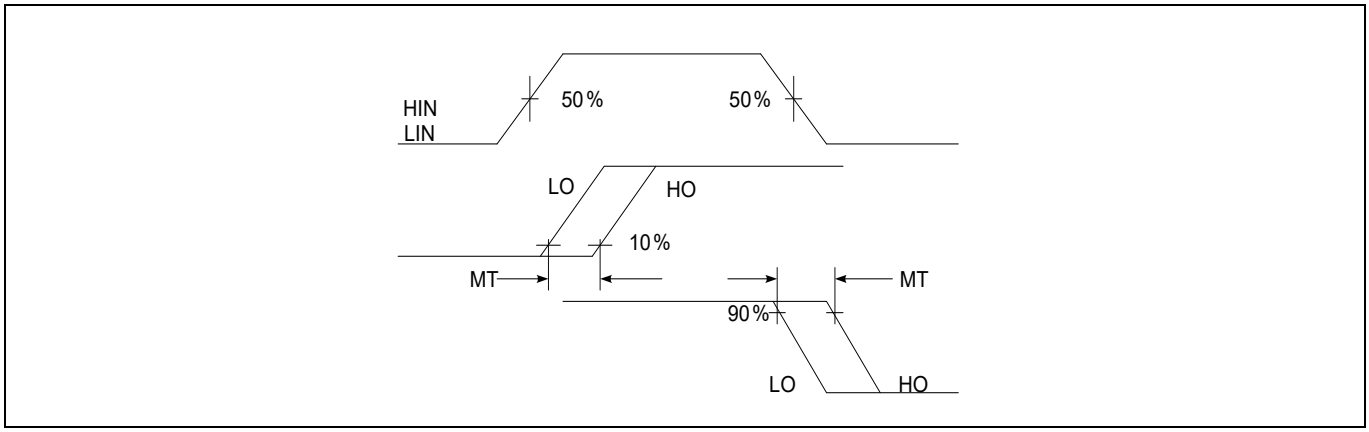


Figure 8 Delay matching waveform definition

The 2ED28073J06F family of HVICs is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 2ED28073J06F is matched to the propagation turn-on delay (t_{OFF}).

5.4 Input logic compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The 2ED28073J06F has been designed to be compatible with 3.3V and 5V logic-level signals. Figure 9 illustrates an input signal to the 2ED28073J06F, its input threshold values, and the logic state of the IC as a result of the input signal. With typical high threshold (V_{IH}) of 2.2 V and typical low threshold (V_{IL}) of 0.8 V, along with very little temperature variation as summarized, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 1.2 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED28073J06F also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED28073J06F features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 2ED28073J06F family has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

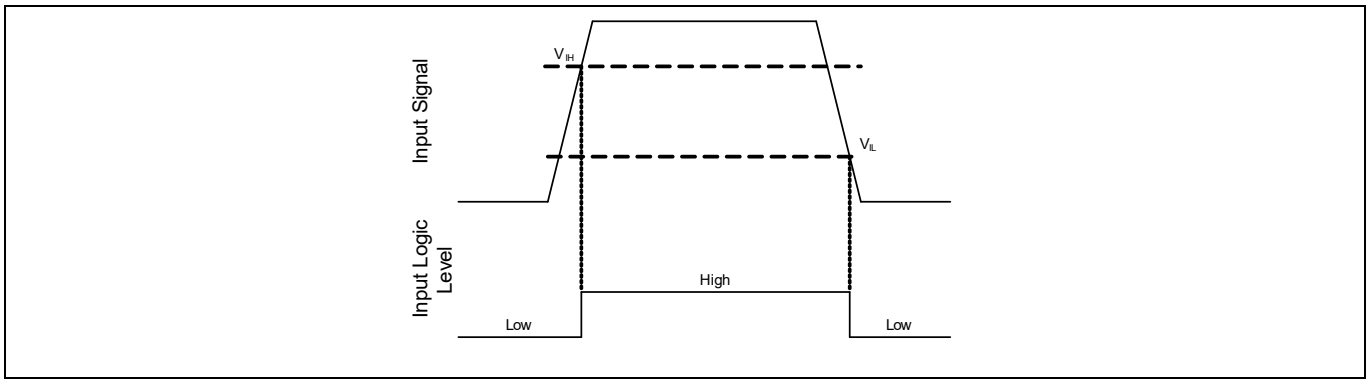


Figure 9 HIN & LIN input thresholds

5.5 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 10 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC won't turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

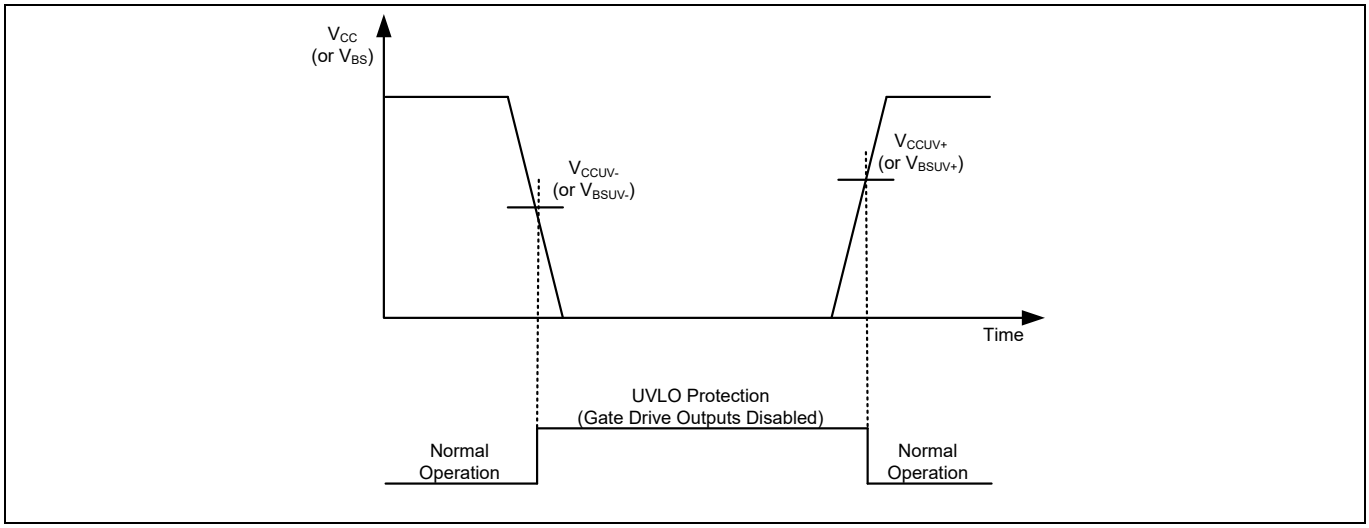


Figure 10 UVLO protection

5.6 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs. The working principle of the new filter is shown in Figures 11 and 12.

Figure 11 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 12 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

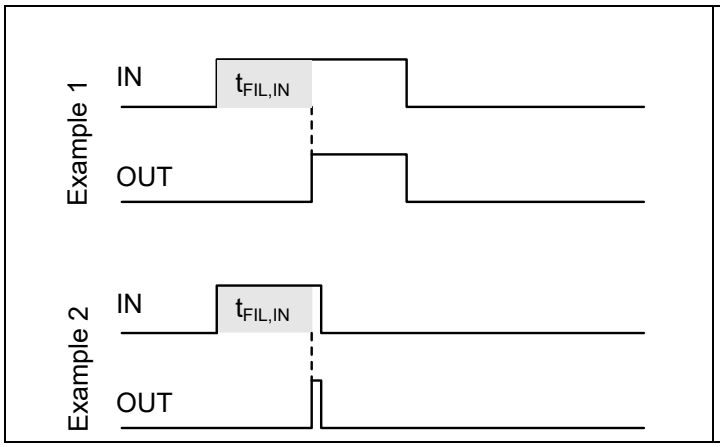


Figure 11 Typical input filter

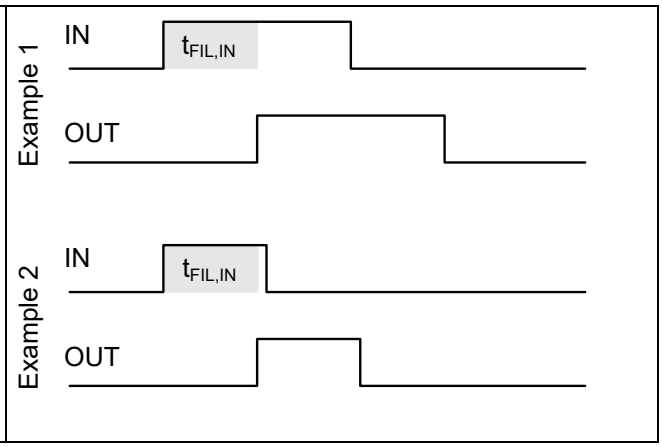


Figure 12 Advanced input filter

5.7 Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 13 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 13 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

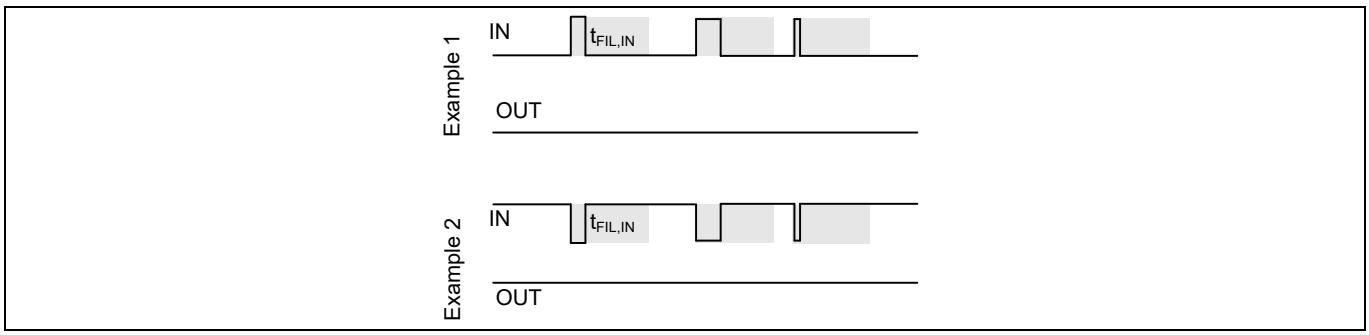


Figure 13 Noise rejecting input filters

Figures 14 and 15 present lab data that illustrates the characteristics of the input filters while receiving ON and OFF pulses.

The input filter characteristic is shown in Figure 14; the left side illustrates the narrow pulse ON (short positive pulse) characteristic while the left shows the narrow pulse OFF (short negative pulse) characteristic. The x-axis of Figure 14 shows the duration of PWIN, while the y-axis shows the resulting PW_{OUT} duration. It can be seen that for a PWIN duration less than $t_{FIL,IN}$, that the resulting PW_{OUT} duration is zero (e.g., the filter rejects the input signal/noise). We also see that once the PWIN duration exceed $t_{FIL,IN}$, that the PW_{OUT} durations mimic the PW_{IN} durations very well over this interval with the symmetry improving as the duration increases. To ensure proper operation of the HVIC, it is suggested that the input pulse width for the high-side inputs be ≥ 500 ns.

The difference between the PWOUT and PWIN signals of both the narrow ON and narrow OFF cases is shown in Figure 15; the careful reader will note the scale of the y-axis. The x-axis of Figure 15 shows the duration of PW_{IN}, while the y-axis shows the resulting PW_{OUT}–PW_{IN} duration. This data illustrates the performance and near symmetry of this input filter.

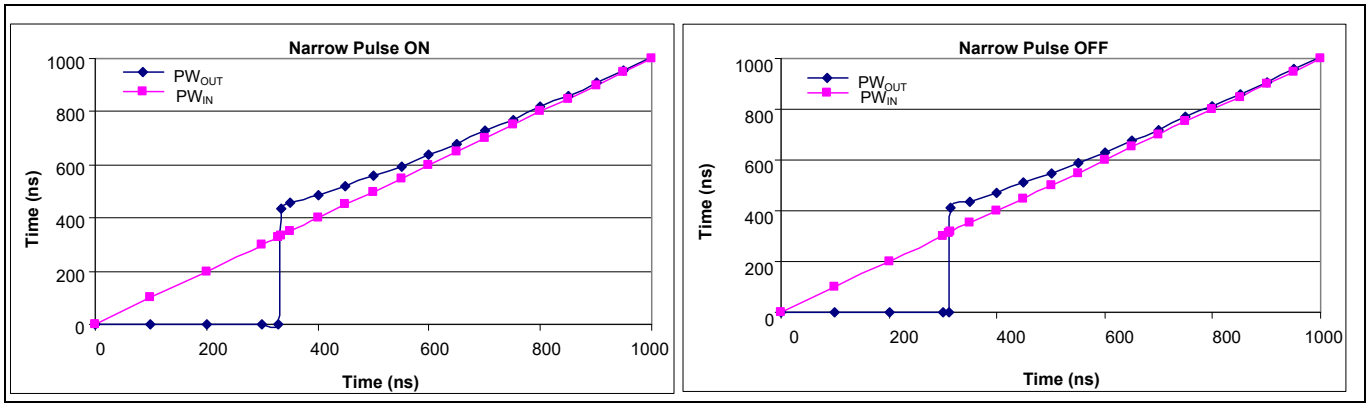


Figure 14 Input filter characteristic

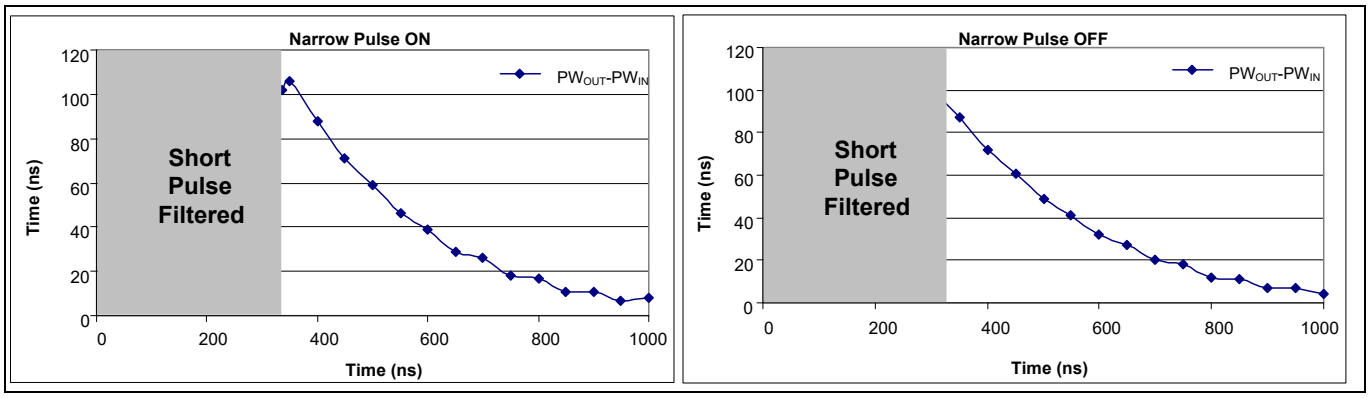


Figure 15 Difference between the input pulse and the output pulse

5.8 Integrated bootstrap functionality

The 2ED28073J06F embeds an integrated bootstrap FET that allows an alternative drive of the bootstrap supply for a wide range of applications. A bootstrap FET is connected between the floating supply V_B and V_{CC} (see Fig. 16).

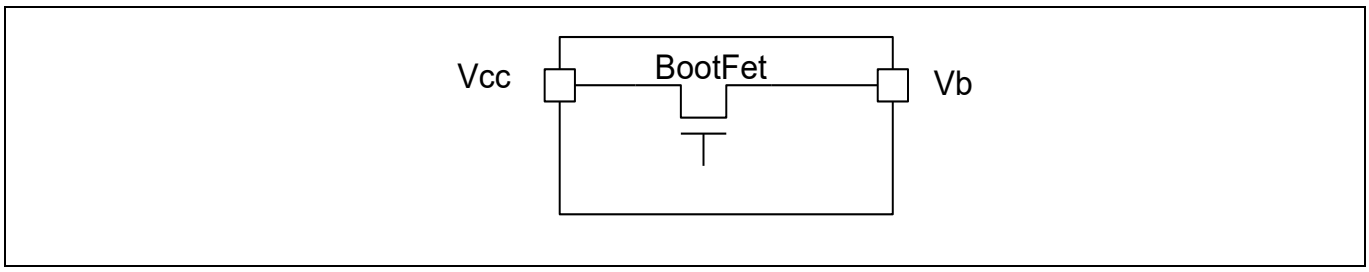


Figure 16 Simplified BootFET connection

The bootstrap FET is suitable for most PWM modulation schemes, including trapezoidal control, and can be used either in parallel with the external bootstrap network (diode+ resistor) or as a replacement of it. The use of the integrated bootstrap as a replacement of the external bootstrap network may have some limitations at a very high PWM duty cycle due to the bootstrap FET equivalent resistance (R_{BS}, see page 7).

The integrated bootstrap FET is turned on during the time when LO is 'high', and it has a limited source current due to R_{BS}. The V_{BS} voltage will be charged each cycle depending on the on-time of LO and the value of the C_{BS} capacitor, the drain-source (collector-emitter) drop of the external IGBT (or MOSFET), and the low-side free-wheeling diode drop.

The bootstrap FET follows the state of low-side output stage (i.e., the bootstrap FET is ON when LO is high, unless the V_B voltage is higher than approximately V_{CC}. In that case, the bootstrap FET is designed to remain off until V_B returns below that threshold; this concept is illustrated in Figure 17.

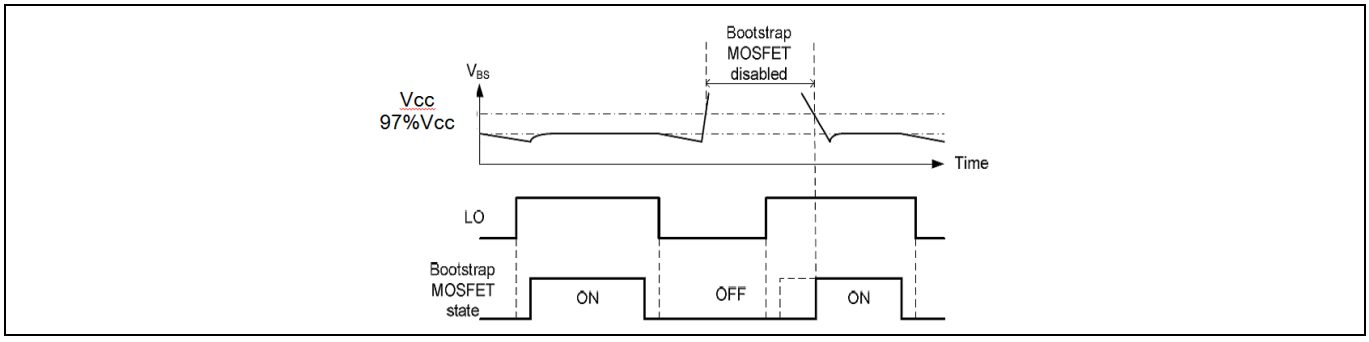


Figure 17 BootFET timing diagram

5.9 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 18. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor.Proper capacitor choice can reduce drastically these limitations.

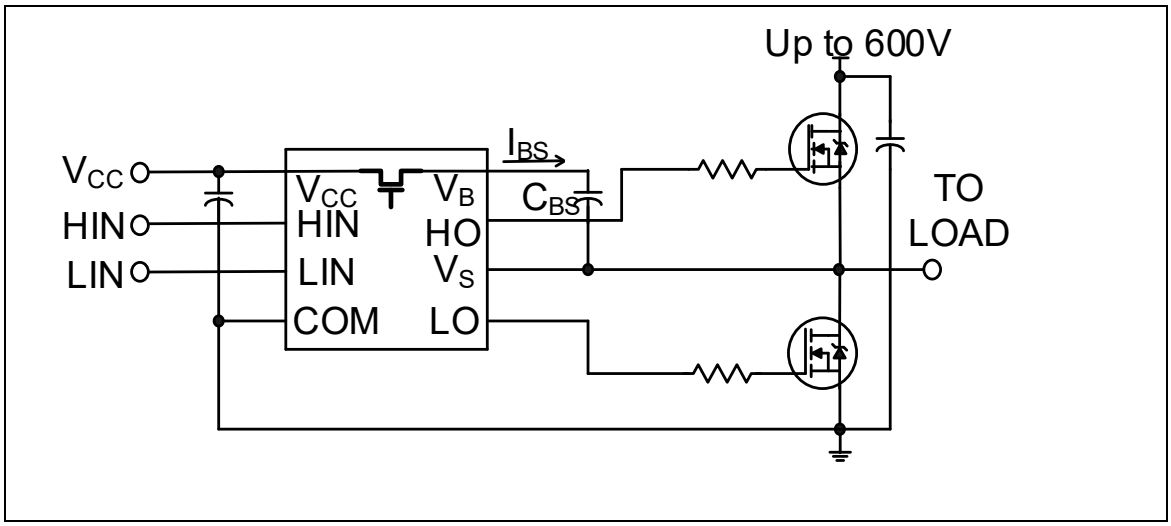


Figure 18 Half bridge bootstrap circuit in 2ED28073

When the low side MOSFET turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{CC} results in a charging current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and V_{CC}. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, the 2ED28073J06F has the UVLO at each supply section in order to actively avoid such undesired UVLO triggers.

The internal bootFET R_{DSon} reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GEmin} - V_{CEon})$$

$V_{GEmin} > V_{BSUV-}$, V_{GEmin} is the minimum gate emitter voltage we want to maintain and VBSUV- is the high-side supply undervoltage negative threshold.

VCC is the IC voltage supply, VF is bootstrapdiode forward voltage and VCEon is emitter-collector voltage of low side IGBT

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- IGBT turn on required Gate charge (Q_G)
- IGBT gate-source leakage current (I_{LK_GE})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS}); typical 1 nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GE}} + I_{LK} + I_{LK_{DIODE}} + I_{DS-} + I_{LK_{CAP}}\right) * T_{HON}$$

ILK_CAP is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramci may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.10 Negative voltage transient tolerance of VS pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 19, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in Figures 20 and 21) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

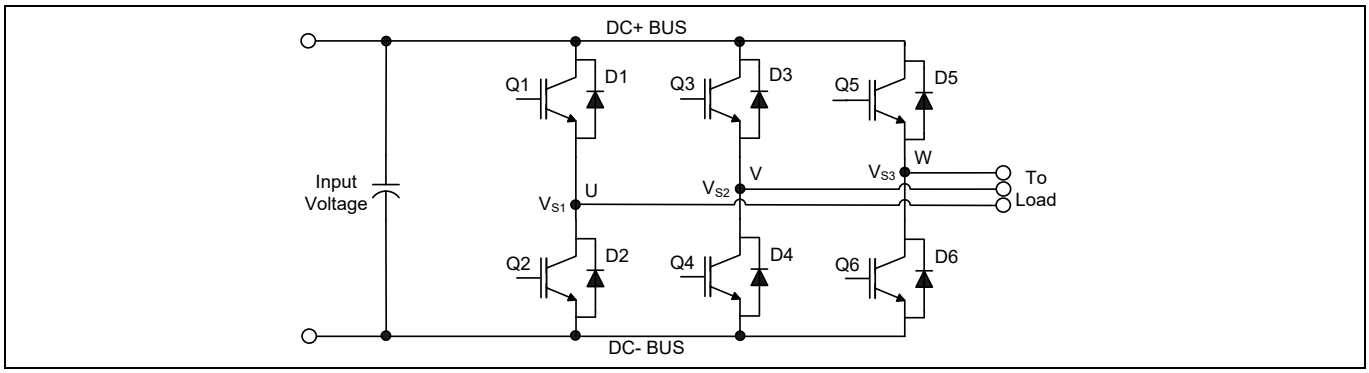


Figure 19 Three phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figures 20 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient"

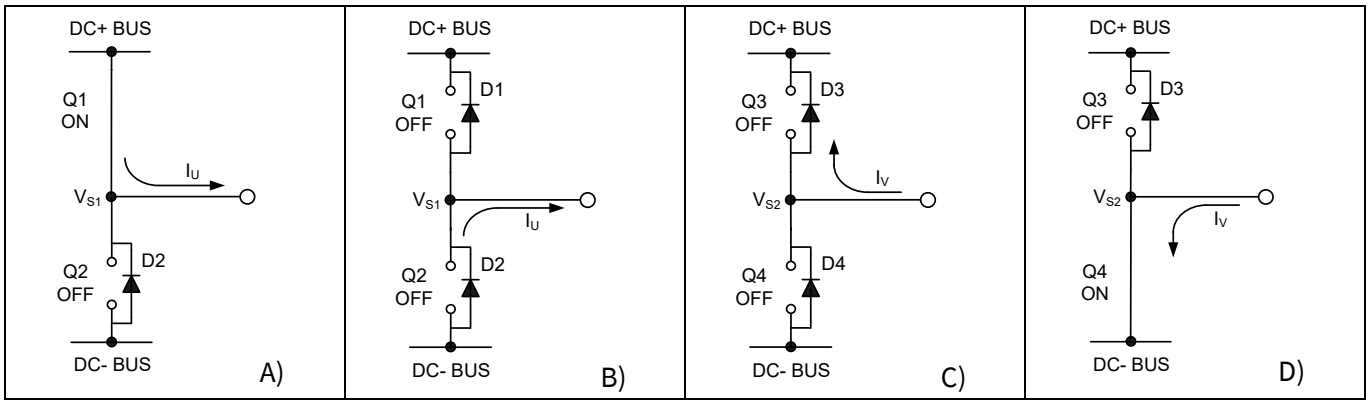


Figure 20 A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting

The circuit shown in Figure 21-A depicts one leg of the three phase inverter; Figures 21-B and 21-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

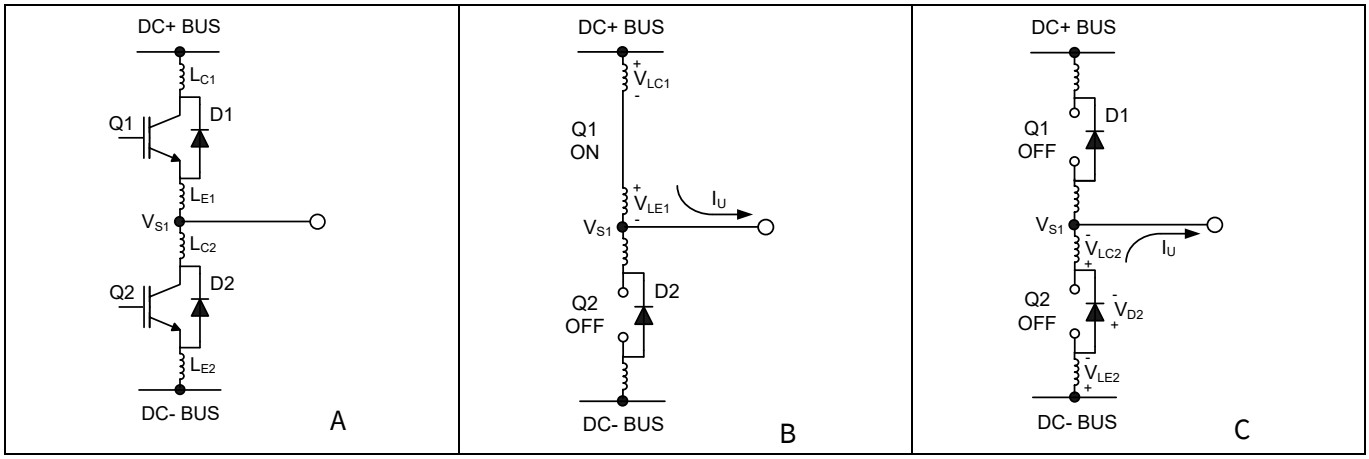


Figure 21 Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative

5.11 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2ED28073J06F's robustness can be seen in Figure 22, where the 2ED28073J06F's Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

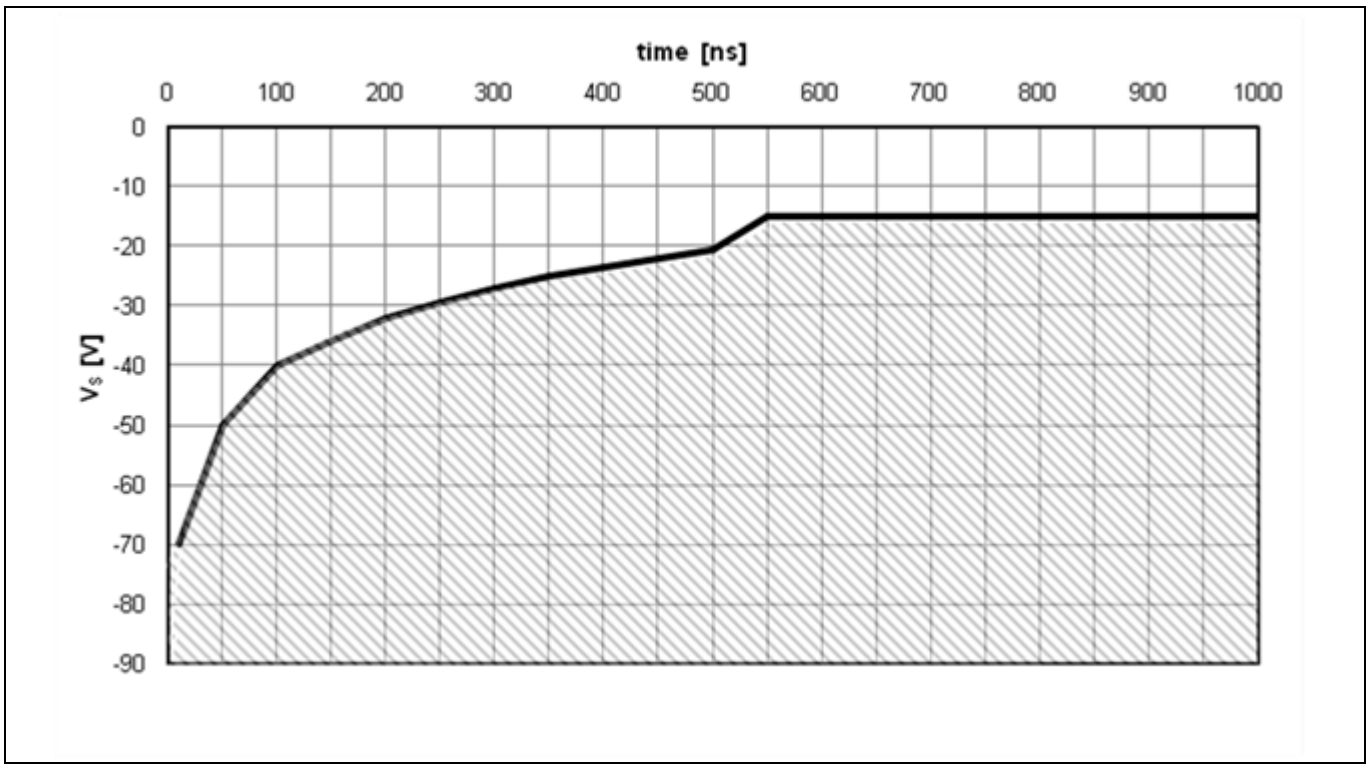


Figure 22 Negative VS transient SOA for 2ED28073J06F @ VBS=15 V

Even though the 2ED28073J06F has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5.12 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 23). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

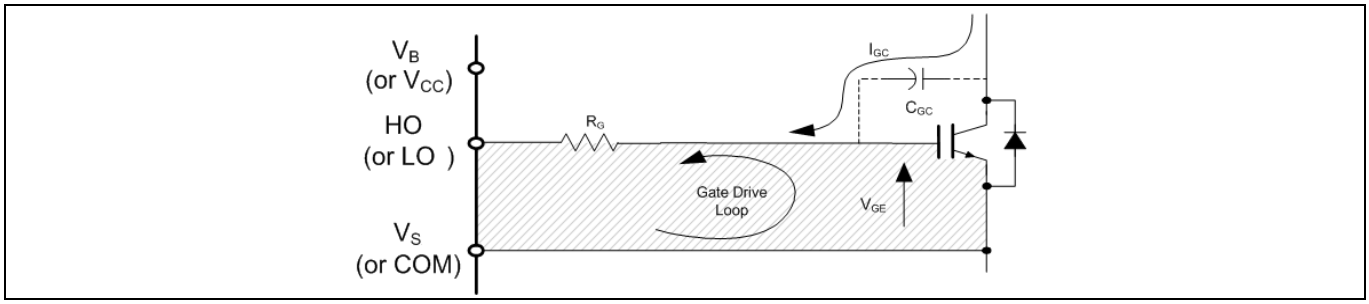


Figure 23 Avoid antenna loops

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 24), and in some cases using a clamping diode between COM and V_S (see Figure 25). See DT04-4 at www.infineon.com for more detailed explanations.

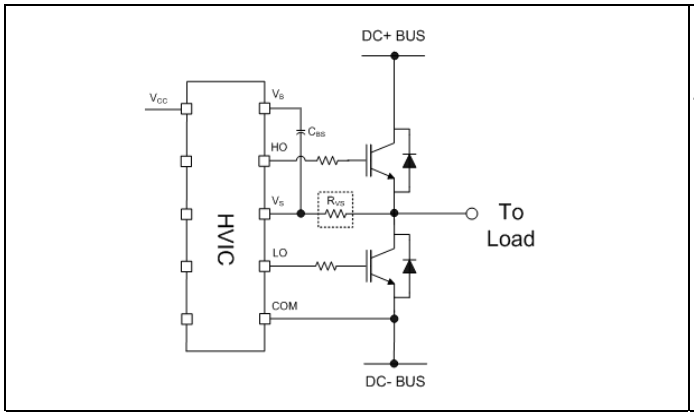


Figure 24 Resistor between the VS pin and the switch node

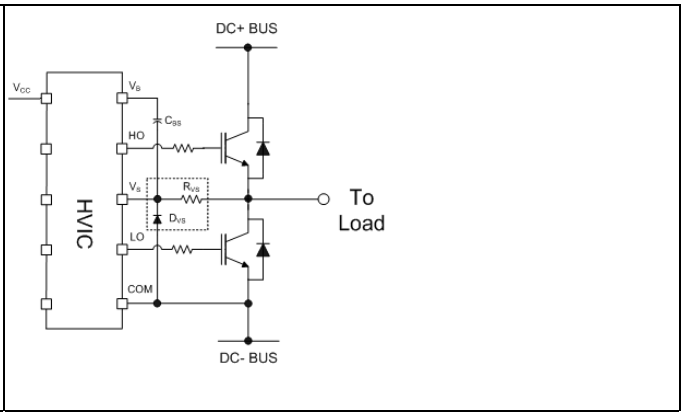


Figure 25 Clamping diode between COM and V_S

6 Qualification information[1]

Table 6 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-8	MSL2†††, 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class B (per EIA/JEDEC standard EIA/JESD22-A115)	
	Human body model	Class 2 (2 kV) (per JEDEC standard JESD22-A114)	
IC latch-up test		Class I Level A (per JESD78)	
RoHS compliant		Yes	

7 Related products

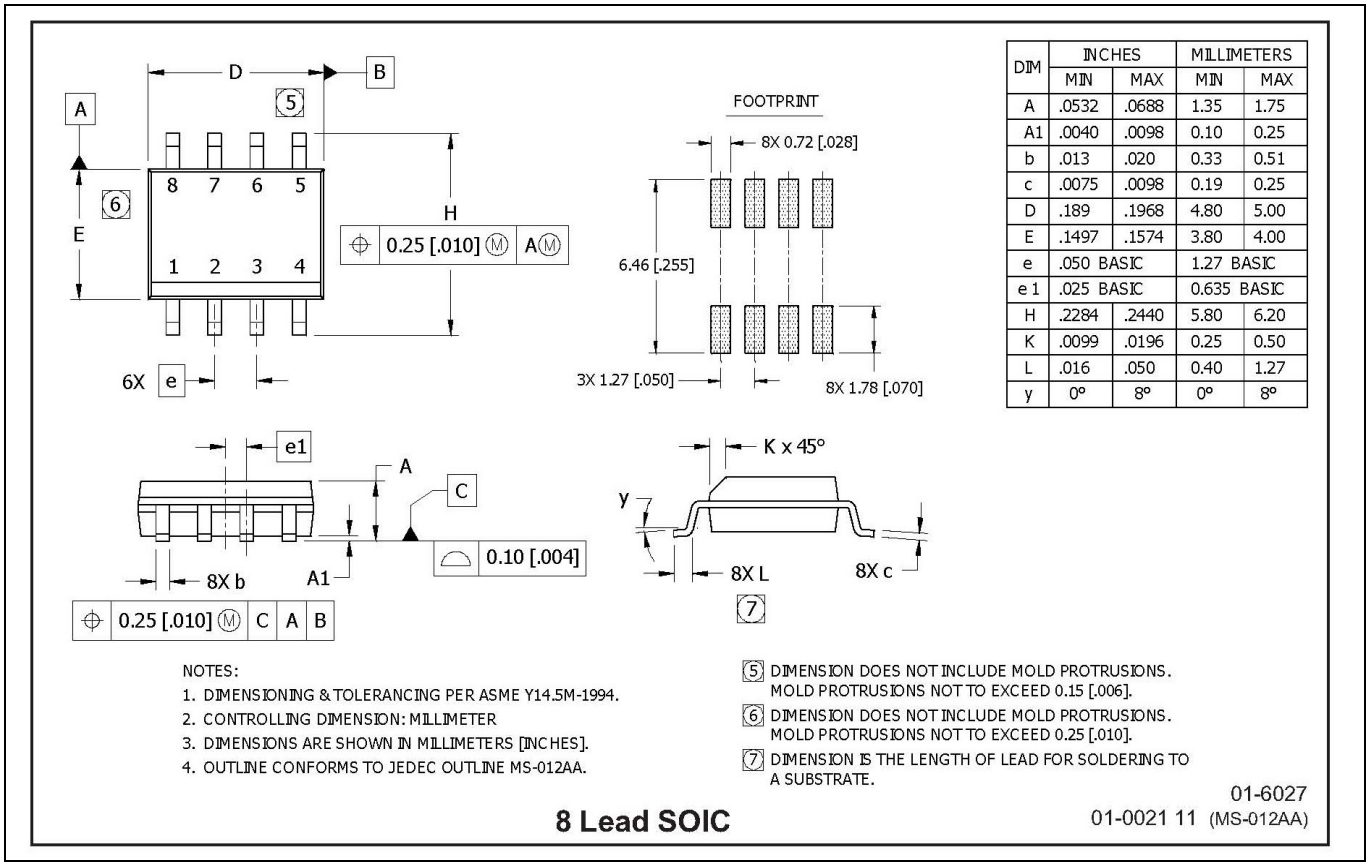
Table 7

Product	Description
Gate Driver ICs	
2ED2108	650V half bridge gate driver with integrated bootstrap diode. 290/700 mA source/sink current drive
2ED2182	650V half bridge gate driver with integrated bootstrap diode. 2.5/2.5 A source/sink current drive
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL23I06 / 2EDL23N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low *R*DSON bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current drive r, and one pin Enable/Fault function for MOSFET or IGBT switches.
Power Switches	
IPS60R1K0PFD7S	600 V PFD7 CoolMOS™ SJ MOSFET with integrated fast body diode in IPAK
IPD60R1K5PFD7S	600 V PFD7 CoolMOS™ SJ MOSFET with integrated fast body diode in DPAK
IPS60R2K0PFD7S	600 V PFD7 CoolMOS™ SJ MOSFET with integrated fast body diode in DPAK
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

[1] Qualification standards can be found at Infineon's web site www.infineon.com

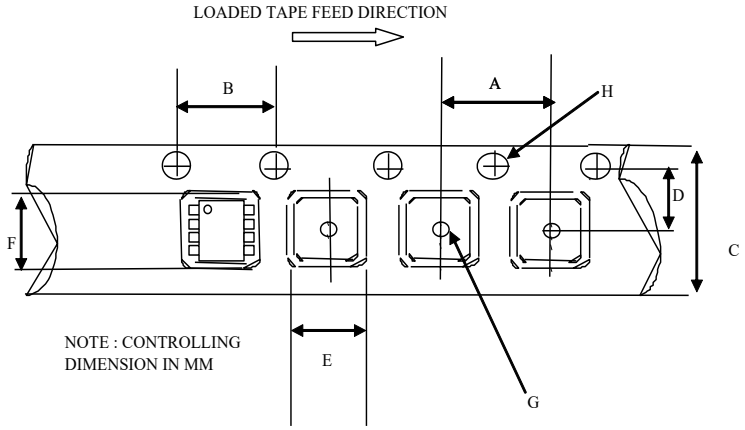
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

8 Package details



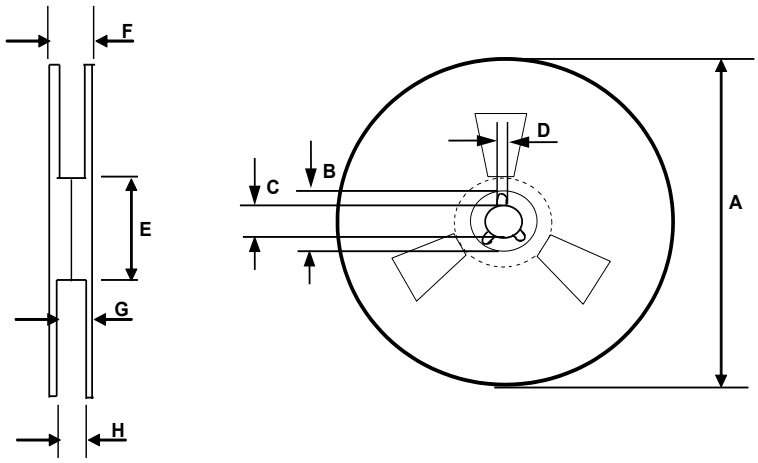
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

Figure 26 8 - Lead SOIC (2ED28073J06F)



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 27 Tape and reel details (2ED28073J06F)

9 Part marking information

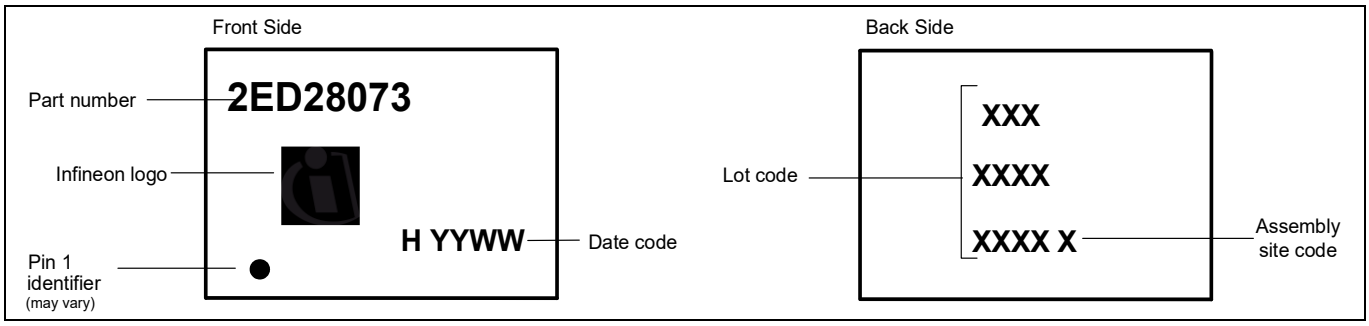


Figure 28 Marking information PG-DSO-8 (2ED28073J06F)

10 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

10.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

11 Revision history

Document version	Date of release	Description of changes
2	April 23, 2020	Final Datasheet