CoolGaN™ IPS half-bridge evaluation board with IGI60F1414A1L

EVAL_HB_GANIPS_G1

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About this document

Scope and purpose

This application note explains how to setup and use the CoolGaN™ Integrated Power Stage (IPS) half-bridge evaluation board featuring Infineon's 600 V IGI60F1414A1L chipset. The board features an isolated power supplies for the gate drivers along with input logic that provides adjustable dead time. Additionally, the board provides direct access to the logic inputs of the CoolGaN™ IPS chipset to drive the chipset with an external microcontroller or digital signal processor (DSP). Using an external inductor, the board can be setup for buck, boost, inverter operation, double-pulse testing or continuous pulse width modulation (PWM) operation and hard or soft-switching at power levels up to 100 W and frequencies up to 1 MHz range.

Intended audience

This application note is intended for power electronic design engineers, applications engineers and students who are familiar with MOSFET or IGBT-based converters.

Infineon components featured

- IGI60F1414A1L

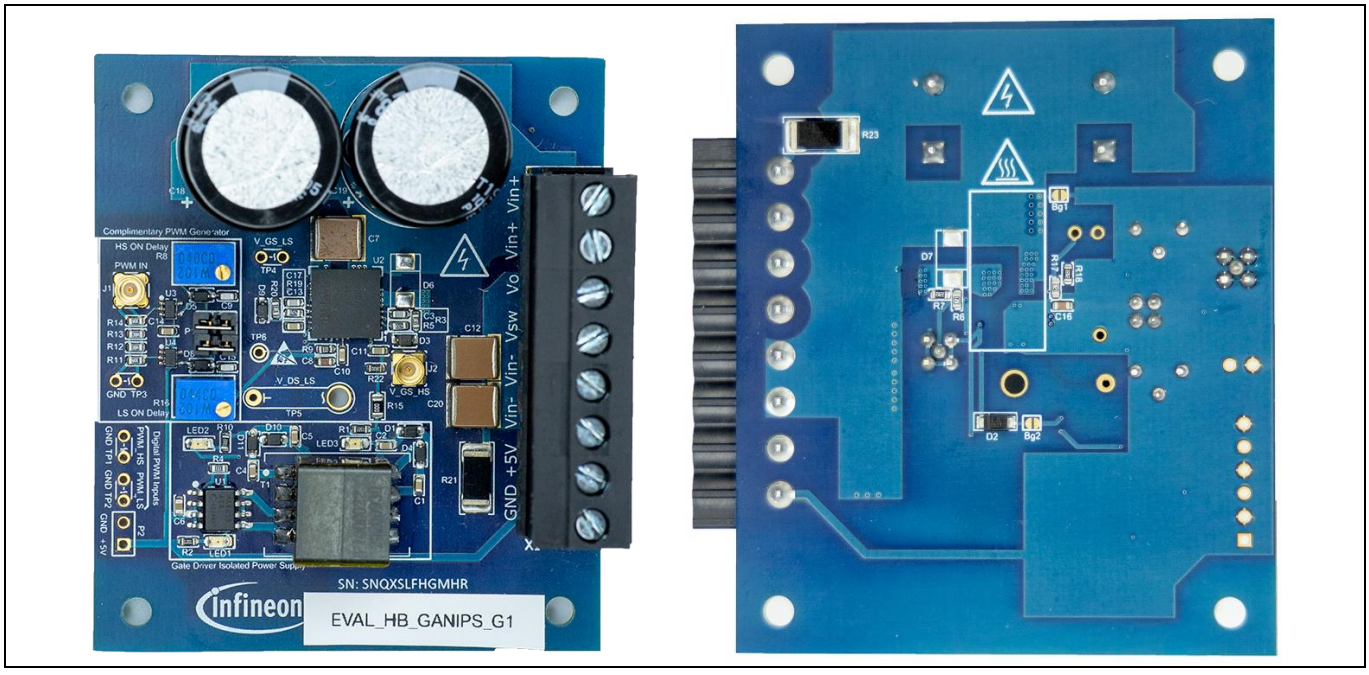

Figure 1 Front and back view of the CoolGaN™ IPS half-bridge evaluation board

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1 Introduction

This hardware provides an easy and quick way to setup and test Infineon's CoolGaN™ IPS half-bridge chipset. The hardware is configurable for boost, buck, inverter operation, pulse testing or continuous full-power operation. Multiple test points are provided to connect signals to an oscilloscope for observation and measuring the switching performance of CoolGaN™ transistors and gate driver embedded in the chipset. This board provides a quick way to evaluate the digital in-power-out feature of the installed CoolGaN™ IPS half-bridge chipset.

The circuit board has a single PWM input intended for connection to a 50 Ω pulse or signal generator. Moreover, direct access to the digital inputs of the IPS is provided for microcontroller interface. The power for the low voltage side will be provided from a single 5 V external power supply. Default deadtime between the high and low-side is pre-set to 100 ns, but is adjustable via trimpots by the user. An external (user-supplied) inductor is needed to configure the hardware in multiple possible test setups through the supplied pluggable terminal-block connector. The output and bus voltage can range up to 450 V which is limited by the capacitor rating. This half-bridge can switch continuous currents of 4 A, and peak currents of 10 A, hard or soft-switching. Depending on the IPS chipset power dissipation, the operating frequency can be up to 1 MHz (limited to about 3 W per device with appropriate heatsink and airflow).

1.1 Evaluation board specifications

Table 1 Evaluation board specifications and limits

Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
V_{cc} input voltage	4.8	5.0	5.2	V	
V_{cc} input current	25			mA	
PWM logic input levels (Applied to J1 terminal)	0		5	V	Standard 5 V TTL levels, 50 Ω terminated
PWM logic input levels (Applied to TP1 and TP2)	0		5	V	Standard 3.3/5 V CMOS/TTL levels
V_{in+} to V_{in-}	0	400	450	V	Limited by capacitor voltage ratings
V_O to V_{in-}	0		450	V	(There may be ±30 V spikes appearing on V_o)
Chipset transistor current, DC			4	A	Keep the case temperature below 125 °C
Chipset transistor current, pulse (non-repetitive)			23	A	Keep the case temperature below 125 °C
Chipset total power dissipation			3 6	W W	No heatsink (T_{case}<125 °C, T_a=25°C) With heatsink, airflow to keep T_{case}<125 °C
Operating frequency	(DC)		1	MHz	Within dissipation, temperature limits
PWM pulse width	100		∞	ns	With 100 ns deadtime setting
Deadtime adjustment range	0		180	ns	Default setting is 100 ns. If longer deadtime is necessary, C9, C15 can be increased, thereby extending the adjustment range.

*Note: The PCB dimensions are 60*70 mm (max.).*

2 Functional description

For a typical double-pulse testing **Figure 2** shows the proper configuration with this hardware. The 5 V power supply provides the circuit power which also powers the IPS logic section and the isolated gate driver power supply. A 0-400 V power supply provides the DC bus voltage and the input PWM signal is provided by a lab pulse generator. A test inductor is needed to connect from the DC bus to the switch-node output. An oscilloscope is used to observe and measure the inductor current (with a current probe), switch-node voltage or any other signal on the hardware board. **Table 2** includes all the available test points.

The inductor can be connected to either the positive DC bus (shown in **Figure 2**), and for inverting double-pulse test, as shown in **Figure 3**, it can be connected to negative bus (V_{in-}). In this case the high-side is the active switch, and the low-side is the freewheeling synchronous rectifier.

This evaluation board can also be configured as a buck, boost, or inverter topology. See section 4.2 for further details.

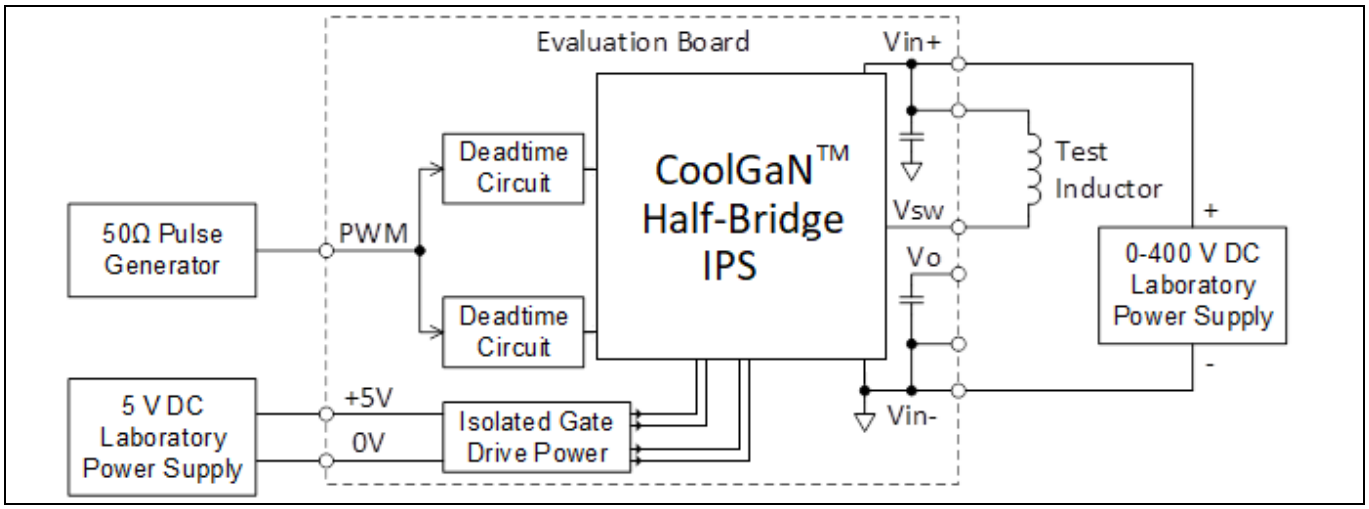

Figure 2 Evaluation board typical application example (double-pulse test)

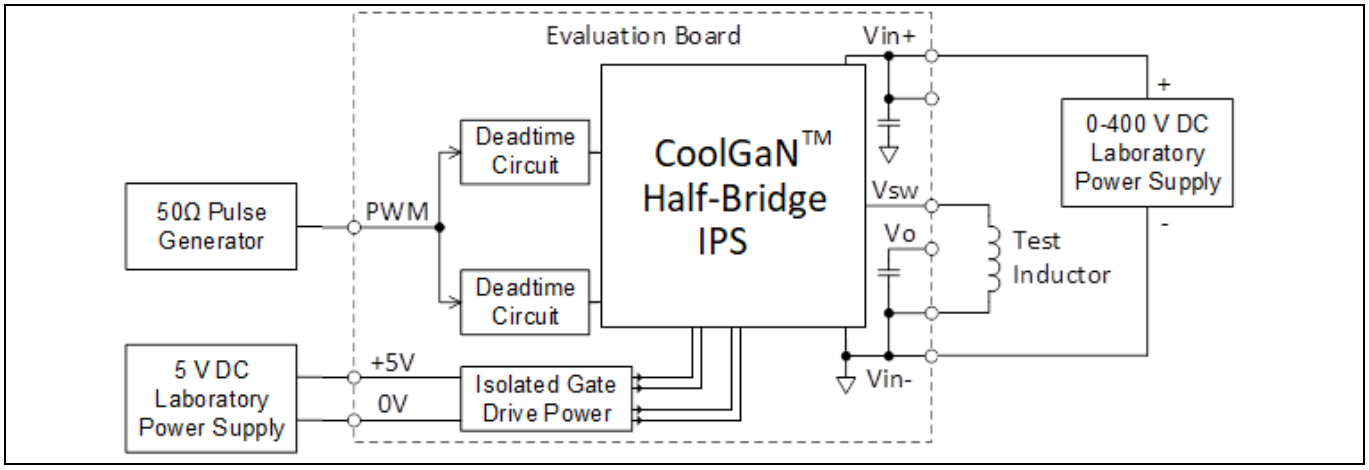

Figure 3 Evaluation board connected for inverted double-pulse test

3 Circuit description

The following sections explain each part of the hardware in detail.

3.1 Input logic and deadtime generator

Two logic inputs are provided on this board. First input is a logic level PWM input connected to J1 (MMCX connector) which is terminated by 50 Ω (the parallel combination of R11-14). The input is buffered by noninverting buffer U3 for the high-side, and inverting buffer U4 for the low-side (show in **Figure 4**). These buffers are compatible with the standard logic-level (low ≤0.8 V and high 2-5 V). When the PWM input is low, the switch node V_{SW} is low (the low-side GaN transistor turns on). Conversely, when the PWM input is high, the V_{SW} node is driven high as the high-side GaN transistor turns on and when the PWM input is low then the low-side GaN transistor is turned on and V_{sw} node is connected to V_{in-}. Make sure that the jumpers on P1 header is placed to apply the PWMs to the IPS chipset (shown in **Figure 5**). The outputs can be observed from TP1 and TP2.

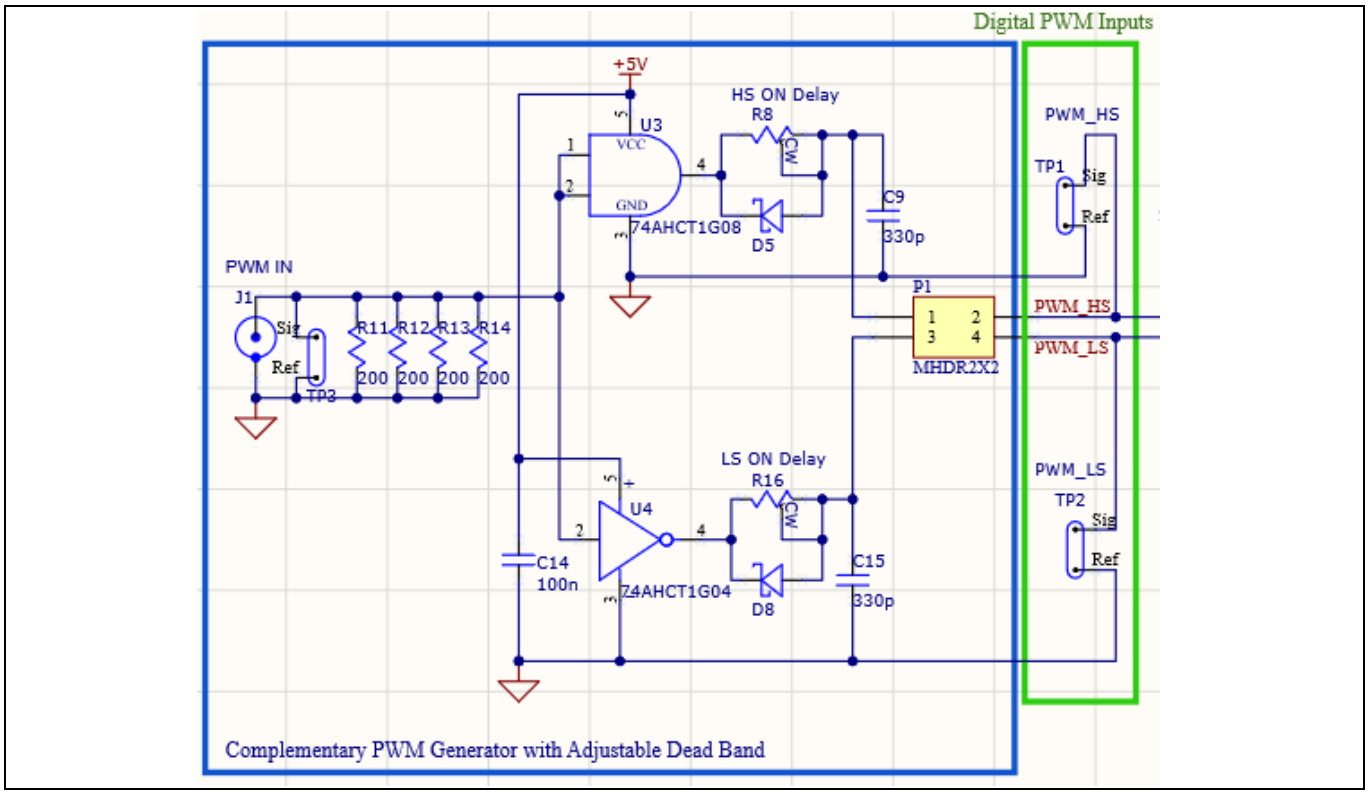

Figure 4 Input logic and deadtime generator

The logic unit in the IPS chipset does not have a shoot-through protection. Applying logic high and low to INL and INH simultaneously will turn-on both high and low-side GaN and this will short the DC bus and result in damaging the IPS chipset permanently. To avoid this situation, a deadtime circuit is provided to make sure that the high and low-side GaN transistors are never turned on simultaneously. For the function of this circuit refer to section 3.1 in reference [1].

The second logic source for the IPS is the external PWM source through the TP1 and TP2 testpoints for high and low-side logics. The jumpers on P1 header must be removed as shown in **Figure 6**. This feature is provided in case a microcontroller is used to drive the IPS for evaluation or independent control of the GaN transistors is desired. Also a 5 V header (P2) is provided to supply power to the external digital control card.

Attention: ***In this case it is user's responsibility to make sure that simultaneous turn-on for both high and low signal will not happen. In case of using microcontroller PWM a minimum deadtime of 50 nS is recommended.***

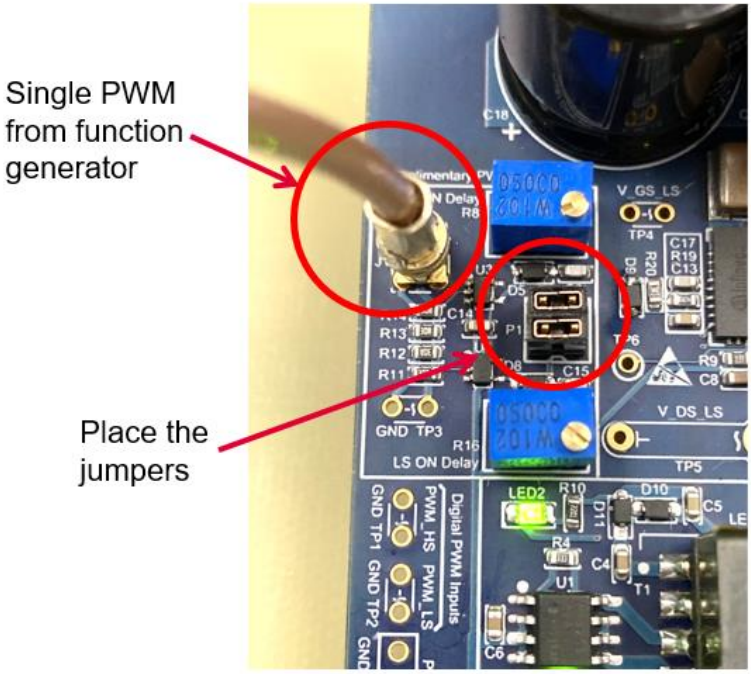

Figure 5 PWM source provided by the function generator and onboard complimentary PWM generator

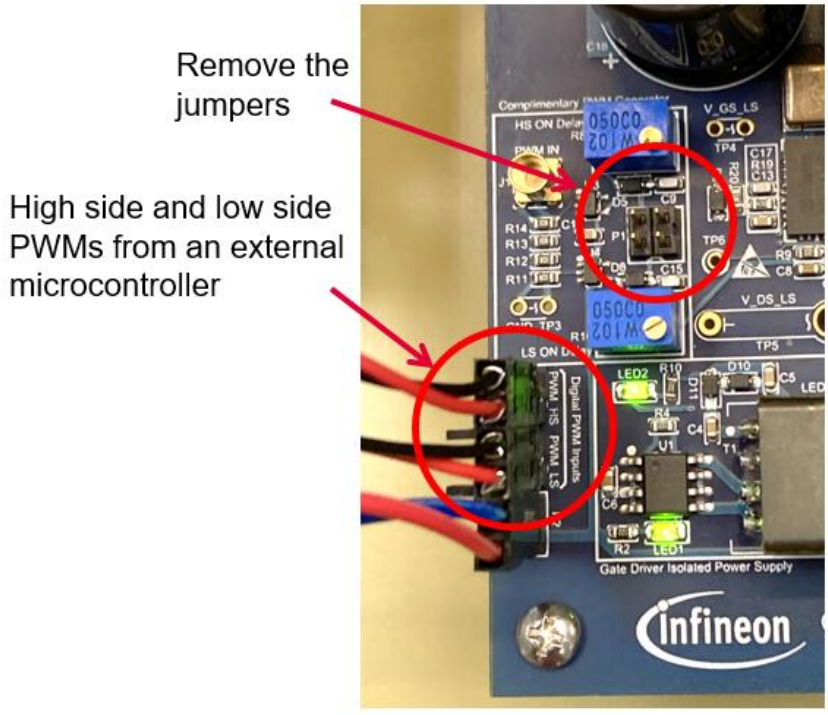

Figure 6 PWM source provided by and external microcontroller

3.2 Isolated gate driver power supply

Figure 7 shows the isolated power supply provided for high and low-side gate driver. For the operation detail and the transformer type, refer to section 3.2 in reference [1].

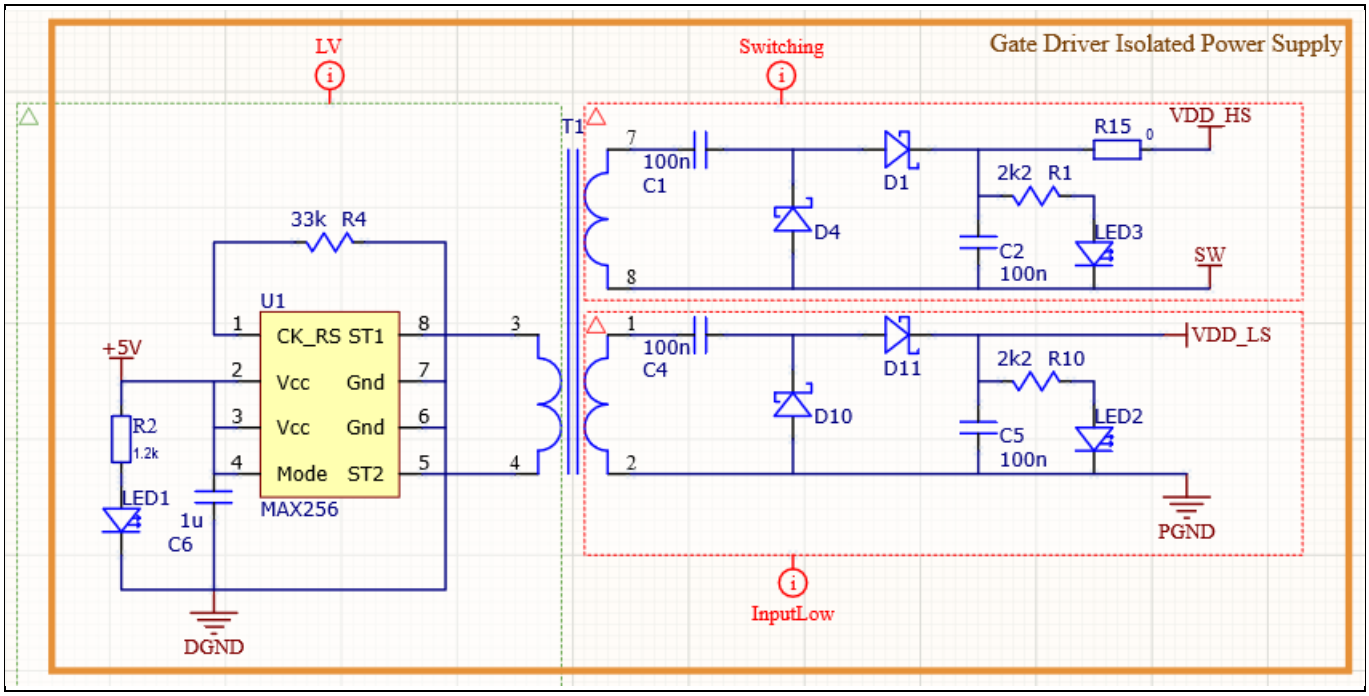

Figure 7 Isolated gate drive power supply

3.3 CoolGaN™ IPS half-bridge circuitry

Figure 8 shows the circuitry around CoolGaN™ IPS half-bridge IGI06F1414A1L. The details are as the following:

3.3.1 Logic power circuitry

R9, C10 is placed to use the internal 3.3 V supply in the chipset. Note that the internal 3.3 V is enabled but pulling down the SLDON pin (#23). R9 value will provide about 5 mA supply to VDDI pin which is sufficient to operate the chipset. For R9 calculation refer to the datasheet.

3.3.2 Low-side gate driver

The gate driver is supplied by the isolated gate driver power supply (VDD_LS) with about 8 V. The RRC network for this channel consist of R17, R19, and C17. Additionally, a fast turn-off circuit including D9 and R20 is provided to reduce R19 value during the turn-off on low-side GaN transistor. R18 is a standard 22k gate pull-down resistor that helps ensure the gate-source voltage remains at zero even when the gate driver is unpowered. For sizing the circuit values refer to the datasheet.

3.3.3 High-side gate driver

The gate driver is supplied by the isolated gate driver power supply (VDD_HS) with about 8 V. The RRC network for this channel consist of R5, R6, and C3. In here D3, R3, and R18 functions are same as D9, R20, and R18 in low-side gate driver. In addition, a bootstrap circuit consist of D2, and R22 is provided to evaluate using bootstrap circuit to power up the high-side gate driver of this IPS from the low-side gate driver power supply. To enable this, remove R15 to disconnect VDD_H and solder the bridge Bg2 (back side of the PCB). Note that to charge the

bootstrap capacitor C11, the low-side GaN transistor has to turn-on with enough pulse width to charge C11 first.

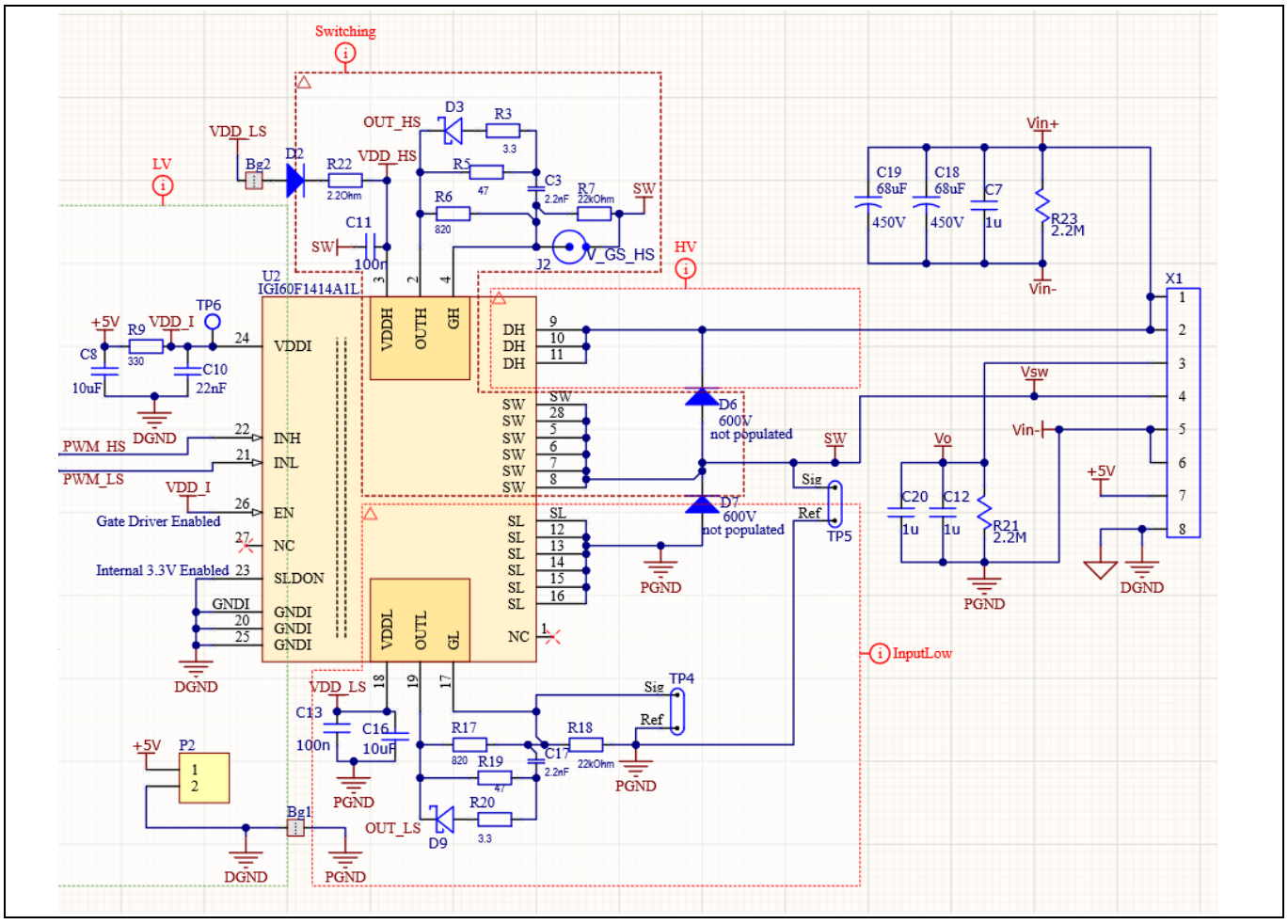

Figure 8 Chipset circuitry and the output connection

3.4 Half-bridge output circuit

This evaluation board makes it easy to access to the IPS power terminals. The drain of the high-side GaN transistor (DH) is connected to the DC bus (V_{in+}) and a combination of ceramic and electrolytic capacitors (C7, C18, and C19) is included to provide the DC bus bulk capacitance. This will provide a surge current source with minimum inductance loop through the power return path to IPS chipset. R23 is a bleeder resistor to discharge the DC bus capacitors after disconnecting from the source.

Attention: ***Do not rely on the lab power supply discarding capability when shutting it off. Always ensure that the capacitors are discharged before handling the board.***

The DC bus labeled as "V_o." is provided for buck converter or inverter mode (provided output filtering). It also provides an easy way to connect the inductor back to a low-impedance DC bus for filtering. The V_o bus also has a bleed-down resistor (R21) to drain the bus capacitors when it is disconnected. See **Figure 10** for the connections in this mode. It is possible to configure the board in boost-mode operation. In this case, V_o becomes the input voltage node, and V_{in+} becomes the output bus. See section 4.2.3 for complete details. D6 and D7 are place holder for external freewheeling Schottky diode if user wants to compare the performance insteaded of using the reverese channel of the GaN for freewheeling.

4 Setup and use

Attention: ***This evaluation hardware has high-voltage terminals and exposed areas. To avoid electric shock, use appropriate measures. The hardware does not have any overcurrent and overvoltage protection and shutdown system. Use appropriate protective epoxy shield or box to cover the hardware to prevent any possible injury.***

Attention: ***Always observe the input and output voltages and keep them below 450 V. Use lab test power supply with current limit and set it in a proper value to avoid catastrophic damage to the board in case of any failure. Eye and ear protection is recommended for safety as all power electronic labs employ it. For any safety concern and technical question reach out to your sales team.***

4.1 Test equipment needed

For test equipment needed refer to section 4.1 in reference [1].

4.2 Connections to the terminal block

For wiring an 8-position pluggable terminal is provided in the hardware kit. This terminal provides a convenient way to connect the hardware to the external inductor, power supply and output load.

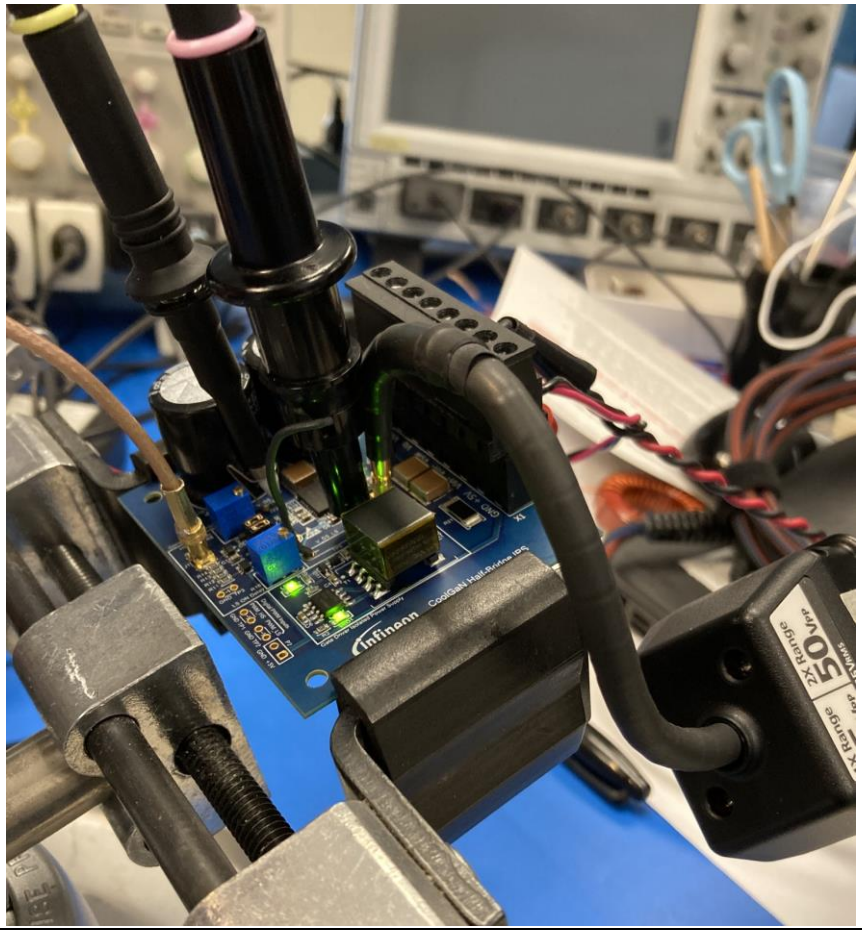

Figure 9 Typical test setup with secured hardware and probes

4.2.1 Connections for double-pulse testing

Figure 2 shows a proper setup and connections for double-pulse testing. Terminal X1 has all 6 output power connections. 5 V DC supply connection is provided in this terminal. The inductor also connects to the terminal block. The inductor energy is dissipated in the freewheeling transistor; therefore, there is no need for external load. For double pulse testing refer to section 4.8 in reference [1].

4.2.2 Connections for buck topology

Figure 10 shows the setup in buck topology configuration. Connect the external inductor between the DC load and the half-bridge output terminal (V_{sw}) and the V_o terminal. DC load connects to V_o. The output voltage is proportional to the duty cycle of the PWM applied to the J1. If a resistive load is applied and the inductor current is above the boundary condition (continuous current mode) then the high-side will turn-on in a hard switching condition. Therefore, select a proper switching frequency (<150 kHz), duty cycle (<75 percent), and load value (>100 ohm).

Attention: ***It is recommended to monitor the temperature of the IPS chipset to not exceed T_c=125°C.***

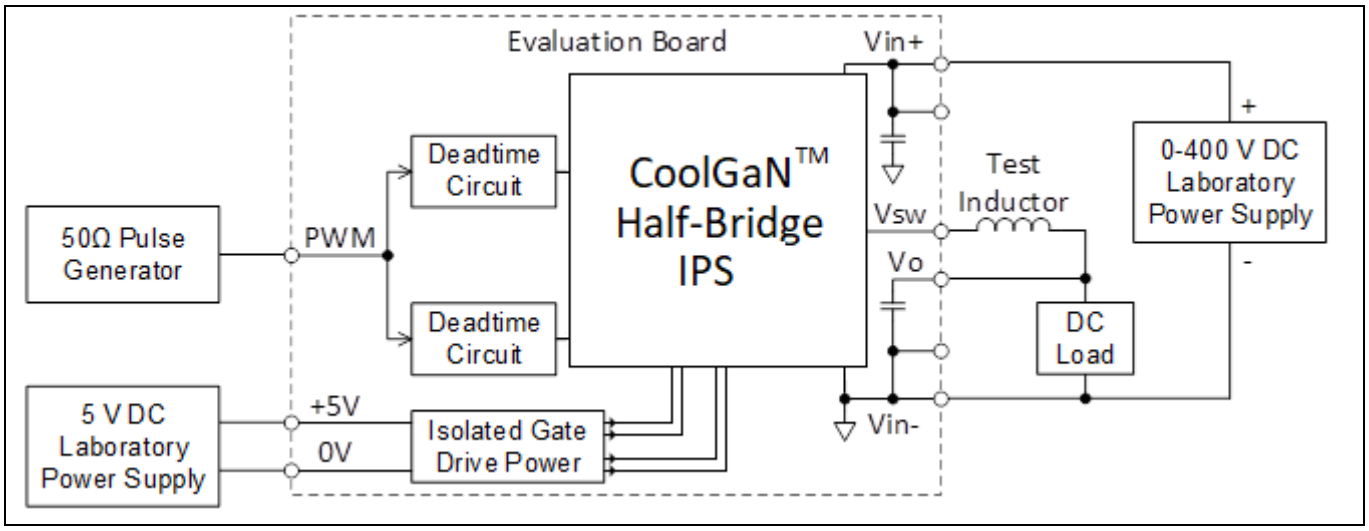

Figure 10 Connecting the evaluation board in the buck topology

4.2.3 Connections for boost topology

In the boost topology (shown in **Figure 11)** V_o is the input source and V_{in+} is the output terminal. This setup will provide a boost testing hardware and the DC bus value and the duty cycle has to be carefully selected to ensure the output voltage will not exceed 450 V rating of the capacitors.

Attention: ***There is no closed loop control in the boost condition and losing the DC load will result in charging the output capacitors rapidly and will result in a catastrophic failure. All safety measures must be considered setting up a boost topology.***

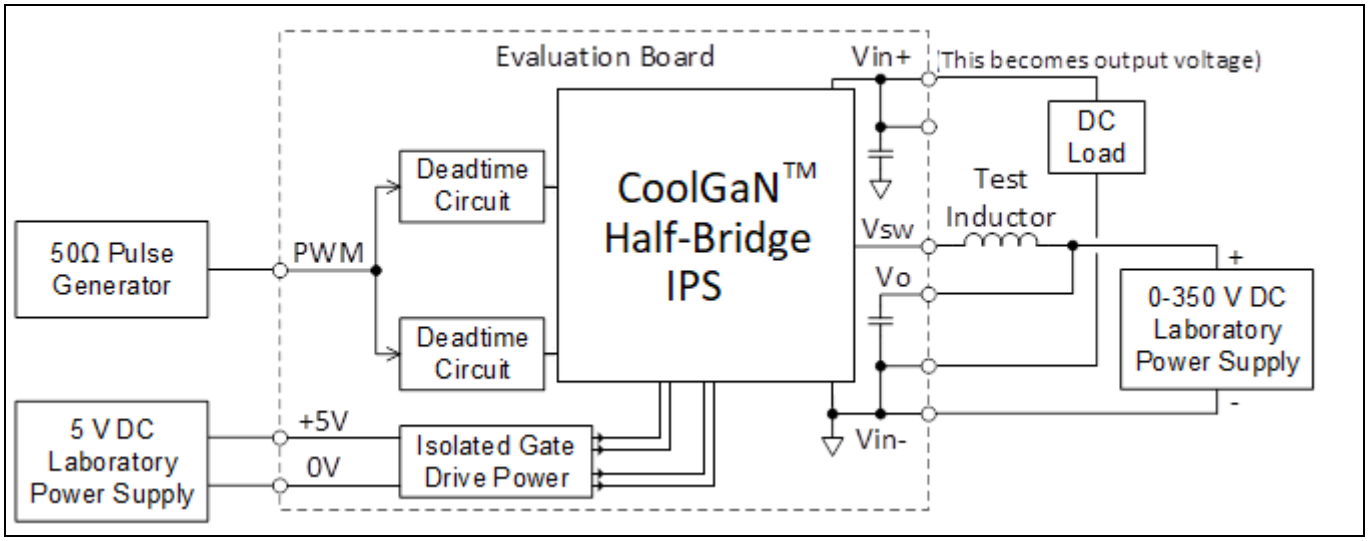

Figure 11 Connecting the evaluation board in the boost topology

4.3 Input PWM generator connections and settings

The PWM input to J1 is a single source PWM with zero to 5 V limit. Provided that the jumpers are placed in P1 header (according to **Figure 5**) applying logic high on this input will turn-on the high-side GaN transistor in the IPS and the switching node will be connected to the DC bus. Applying logic low will turn-on the low-side GaN transistor inside the IPS and the switching nod will be connected to the $-V_{in}$. Setting up the PWM sequence is up to the user (continues, but, double pulse).

4.4 Measurement points

There are 7 test points to connect to oscilloscope for observation (either through-hole pad-pair, or MMCX connector). The pad-pairs reference is designated by the ⊥ symbol. **Table 2** includes the test point description.

Table 2 Test point descriptions

Test point label	Description
TP1	Input to the high-side logic of the IPS (INH)
TP2	Input to the low-side logic of the IPS (INL)
TP3	PWM input – parallel to J1. Typical levels here should be 0 – 5 V
TP4	Low-side GaN transistor gate voltage: signal is the gate of low-side GaN transistor, reference is the Kelvin source of the low-side GaN transistor.
TP5	This is the test-point to observe the Drain-source of the low-side GaN transistor which is the half-bridge switch-node output. This point switches between zero to 450 V (maximum DC bus). Recommended probe is Tektronix TPP0850 50X high-voltage 800 MHz probe with its short ground pin.
TP6	This testpoint is to observe if the VDDI logic supply of the chipset is active with about 3.3 V voltage level respect to the digital ground.
J2	High-side GaN transistor gate voltage: signal is the gate of high-side GaN transistor, reference is the Kelvin source of this transistor. This test point is an MMCX connector and is designed to be directly connected to the input of a Tektronix IsoVue isolated probe. Do not use any non-isolated probe since the reference in this test point is the switching node (0-450 V switching)

4.5 Power-up and power-down sequencing

To power up the board, make sure to turn-on the 5 V power supply. Then ramp up the DC bus from zero to the desired voltage (maximum 450 V). Depending to the load, adjust the current limit. To power down the hardware, reduce the DC bus to zero and then turn-off the 5 V supply.

4.6 Verifying and adjusting deadtime

For adjusting and trimming the deadtime, refer to section 4.6 in reference [1]. **Figure 12** and **Figure 13** show the adjusted 100 ns deadtime in rising and falling edge of the PWM after trimming (default setting).

4.7 Test inductor recommendation

A good high-frequency capable inductor is used for testing for best results. We recommend a low-loss inductor with high saturation current (>25 A) and self-resonant frequency >20 MHz. Micrometals T-series toroidal core with wire winding in a single-layer is recommended for clean observation.

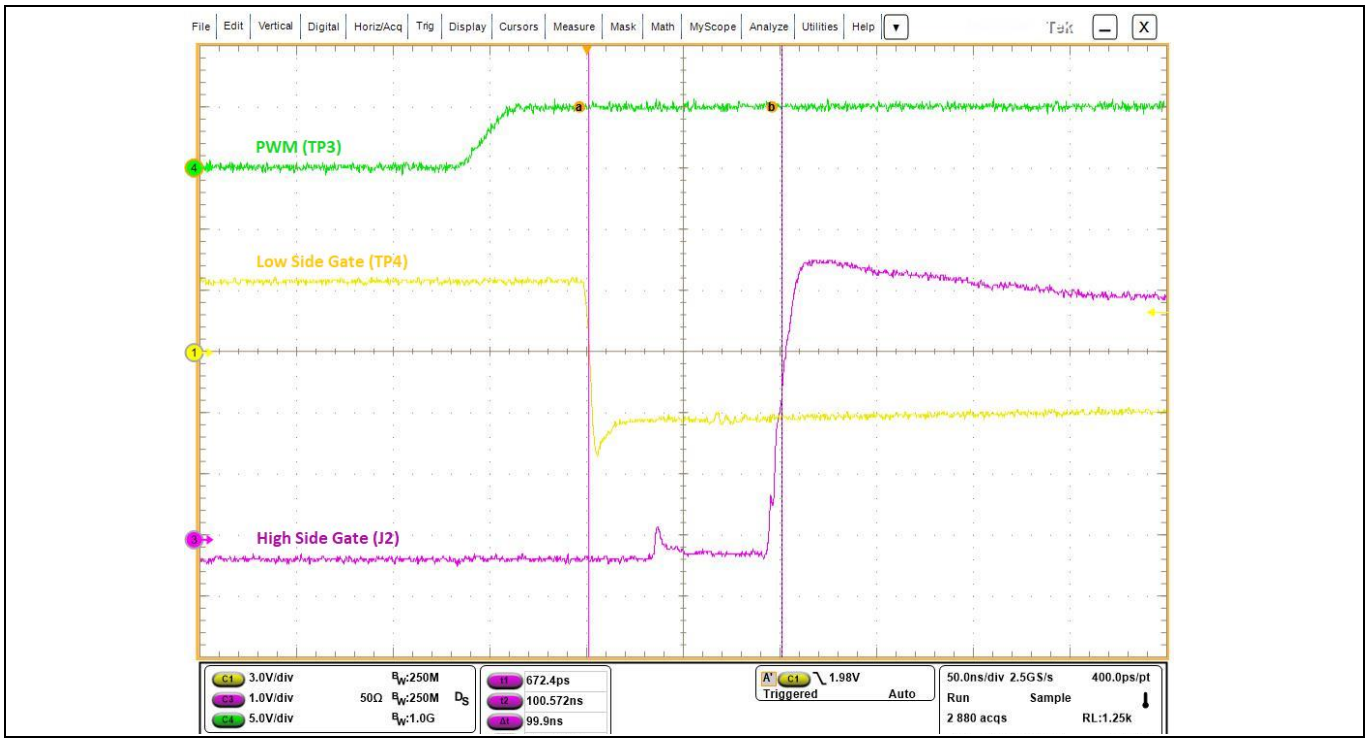

Figure 12 Measuring deadtime on the rising edge of PWM

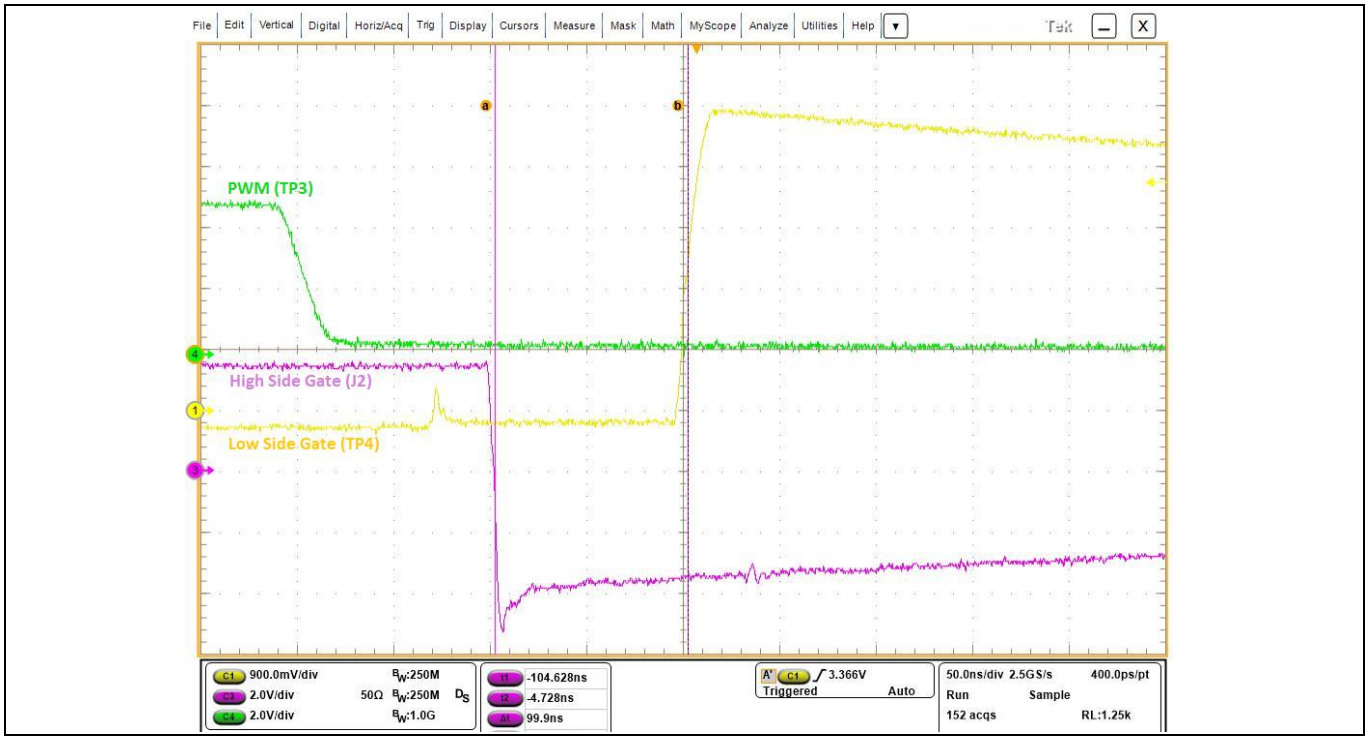

Figure 13 Measuring deadtime on the falling-edge of PWM

4.8 Initial checkout

After setting up the board per section 4.6, the next step adding the external inductor for desired test topology. This example shows how to setup the board for buck topology testing. Before powering up, you may want to observe the gate voltages. **Figure 14** shows an example of the gate voltage of low-side GaN transistor captured from TP4. In this condition the PWM applied to the J1 is 36 percent for buck mode testing.

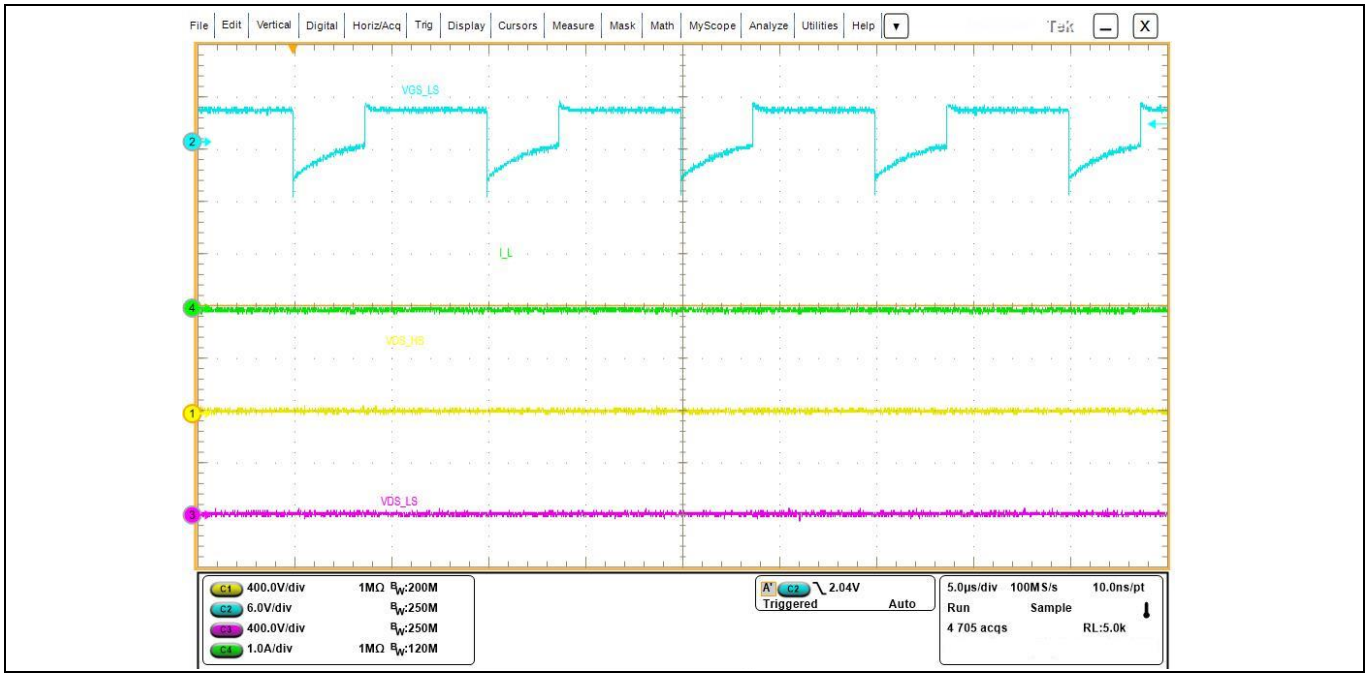

Figure 14 Low-side GaN transistor gate voltage waveform at 100 kHz

Setup and use

The circuit is connected per **Figure 10**, using a 1.1mH RF inductor. The input voltage is ramped up to 400 V, and the output voltage is about 145 V (36 percent duty-cycle). The load is set to 98 ohm, about 200 W output power. **Figure 15** shows V_{DS} of the high and low-side GaN transistors with the inductor current. Note that both the gate and drain voltages are clean with minimal ringing or overshoot even though the switching speed is fast.

Temperature of the chipset and heatsink can be monitored in real-time using a FLIR infrared camera. **Figure 17** shows the thermal image of the hardware in the buck testing condition without any thermal relief or heatsink. IPS chipset operates around 100°C (below the recommended operating temperature Tj< 125°C).

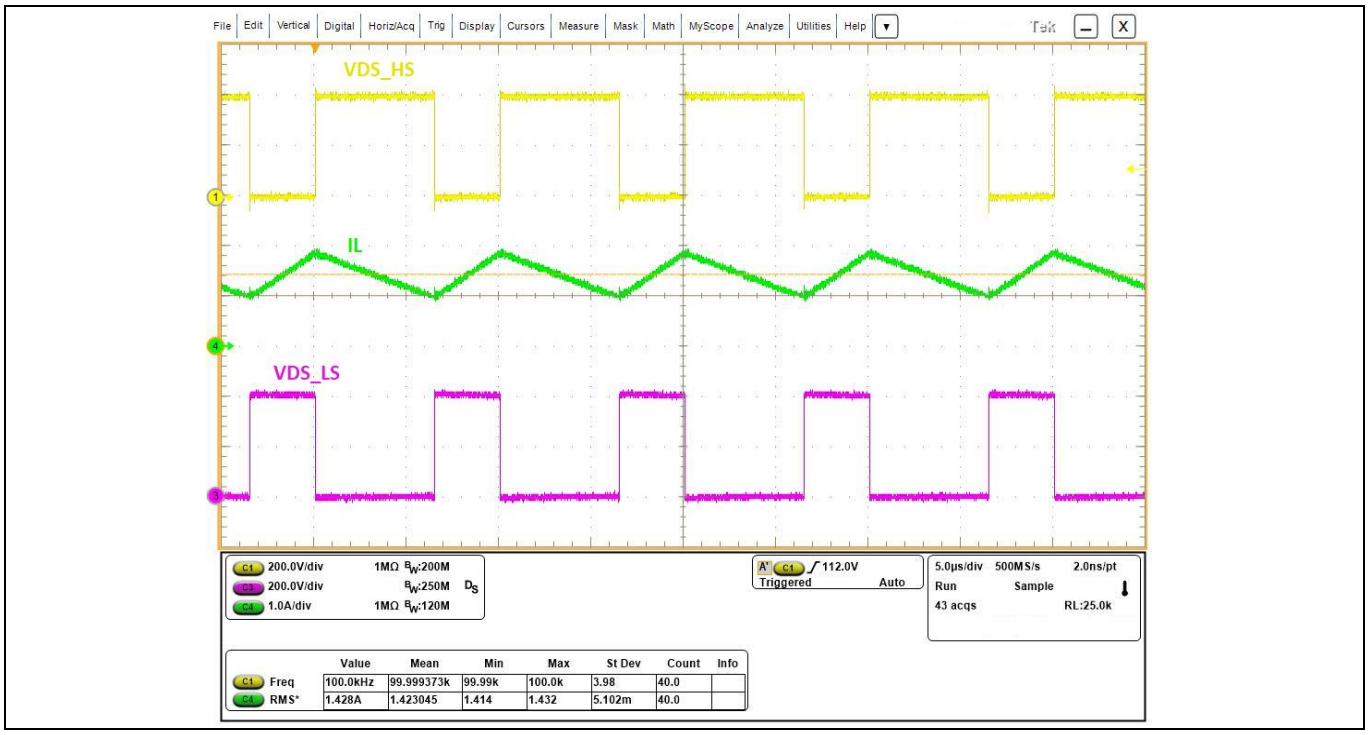

Figure 15 Operating waveforms buck-mode at 100 kHz, 200 W load

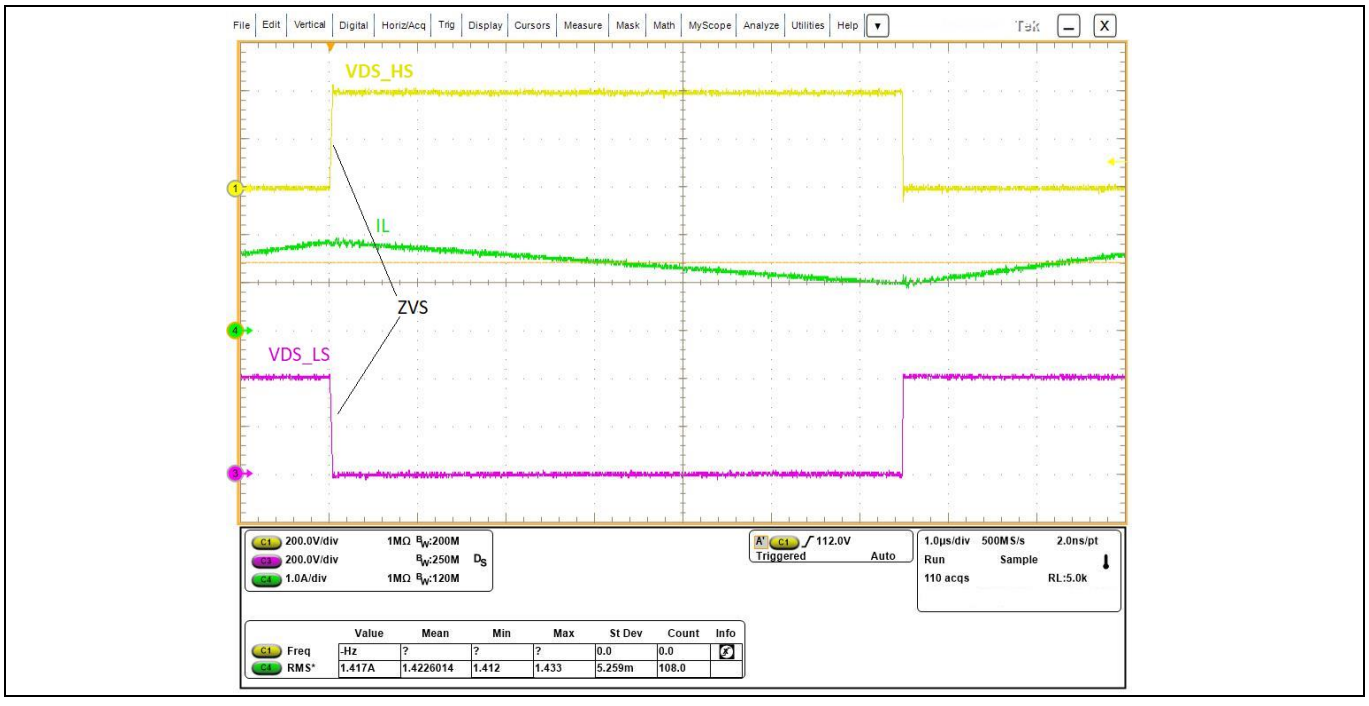

Figure 16 Expanded view of the operating waveforms in buck-mode at 100 kHz, 200 W load

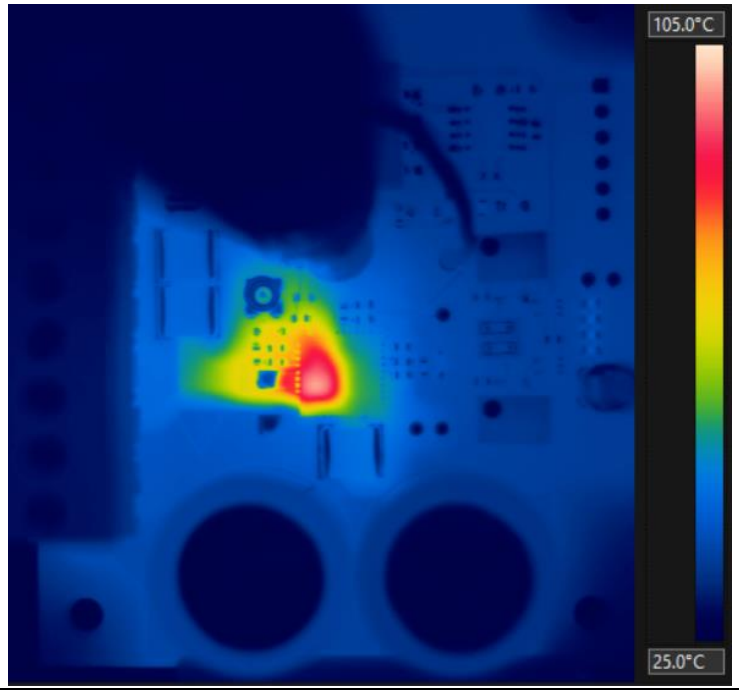

Figure 17 Thermal image of the chipset in buck-mode at 100 kHz, 200 W load

4.9 Operation at high power levels

The IPS chipset without any active thermal relief can dissipate about 3 W in total without exceeding 125°C on chipset case temperature. To increase the power dissipation capability of the chipset a heatsink can be attached to the bottom side of the PCB in the marked area beneath the chipset (shown in **Figure 18**). The heatsink must be attached with an isolated thermal pad (recommending 3M 8810 double side adhesive thermal pad). A cooling fan can be setup to cool down the heatsink. With airflow about 10 m/s this can increase the power dissipation limit of the chipset to 6.5 W.

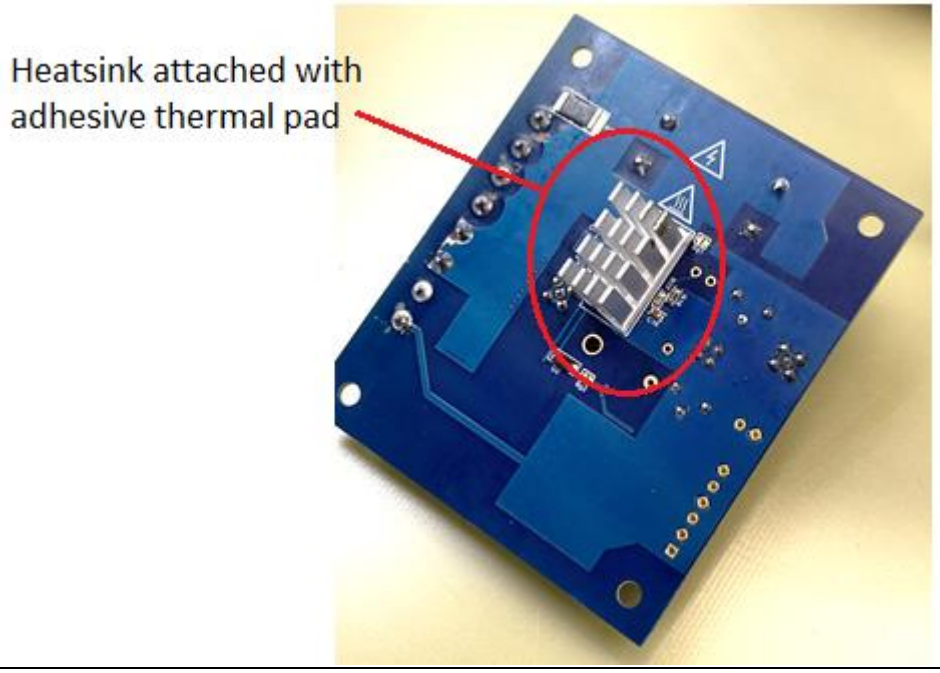

Figure 18 Heatsink added the back side of the PCB

4.10 Soft-switching performance test

With buck topology and no DC load connected to the evaluation board, a complete soft-switching performance of the chipset can be observed. **Figure 19** shows the test performed on the board using 100 uH inductor and function generator set at 200 kHz with duty cycle of 50 percent. With 400 V DC bus, the output settles at 200 V and the peak-peak current will be about 5 AMP. The expanded view is shown in **Figure 20**. Both high and low side GaN transistors are operating in ZVS mode with about 8 V/ns. The negative spikes on the high side gate voltage is due to the non-linear capacitance of C_{rss} (related to the GaN device) for more information refer to section 4.2.2 in reference [1]. **Figure 21** shows the thermal image of the IPS chipset operating at around 54°C.

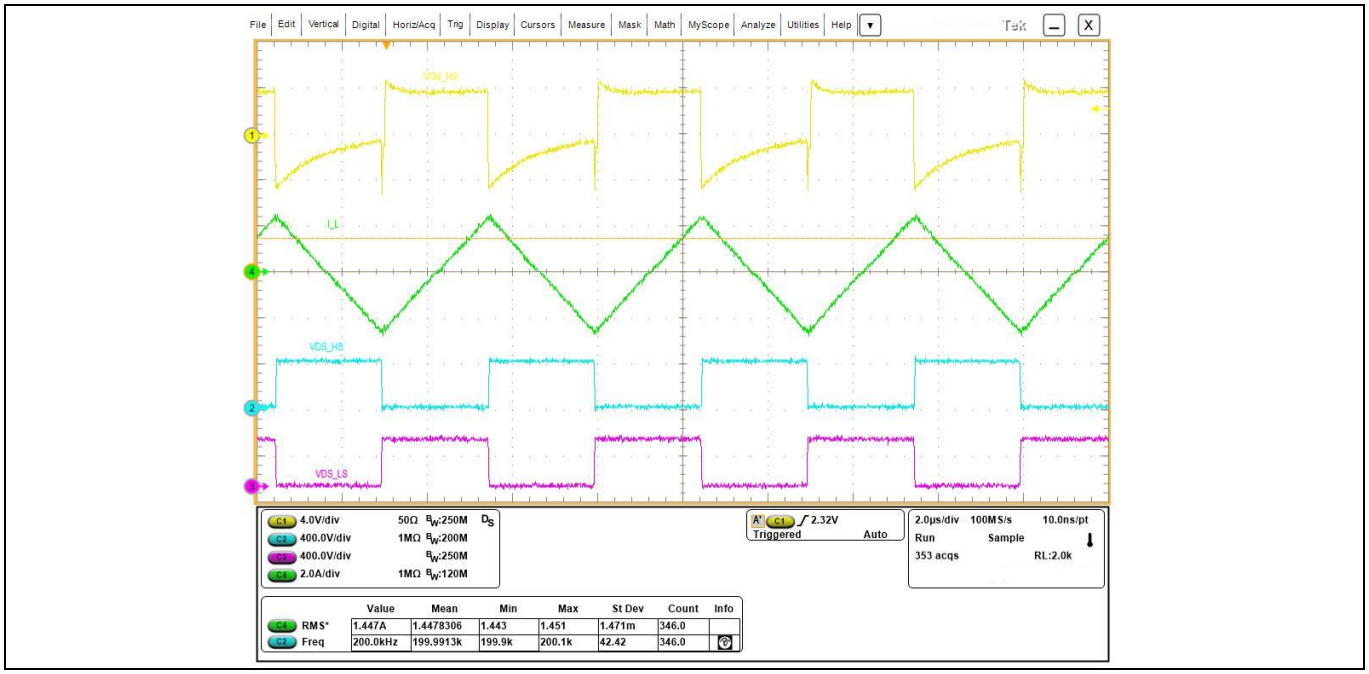

Figure 19 Operating waveforms in soft-switching mode at 200 kHz , 5 A pk-pk current

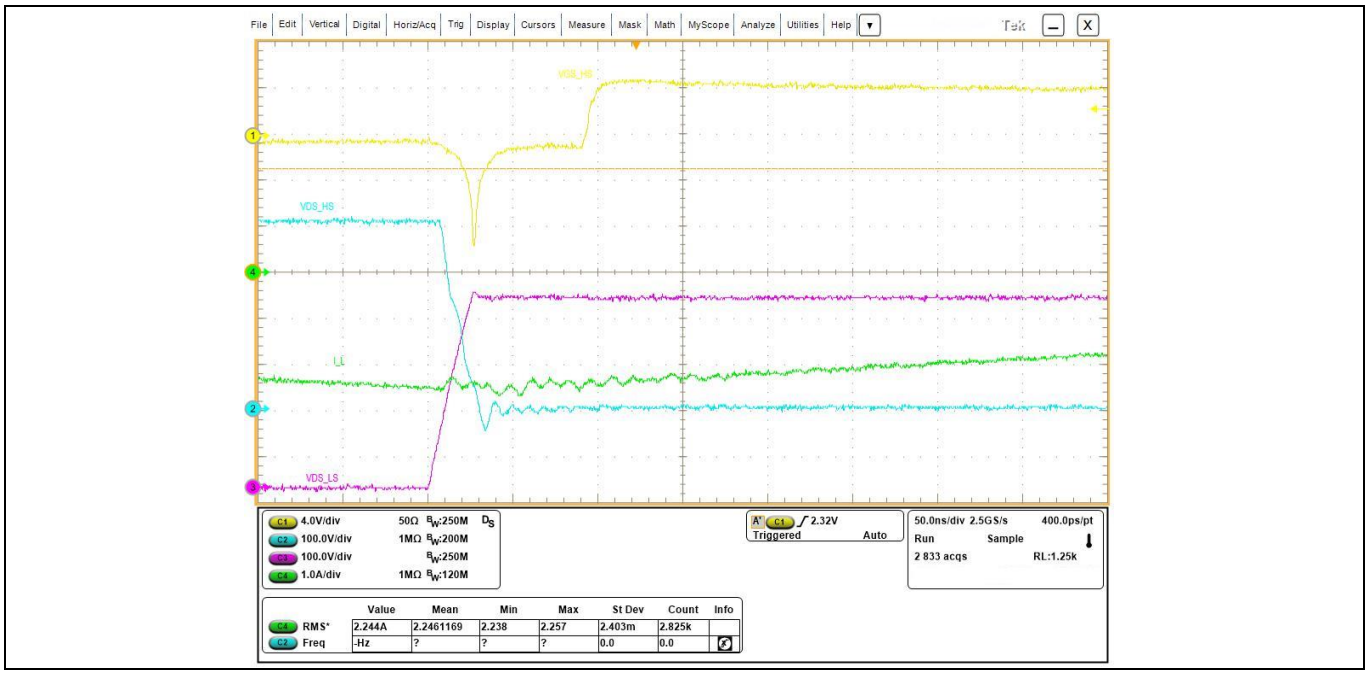

Figure 20 Expanded view of operating waveforms in soft-switching mode at 200 kHz , 5 A pk-pk current

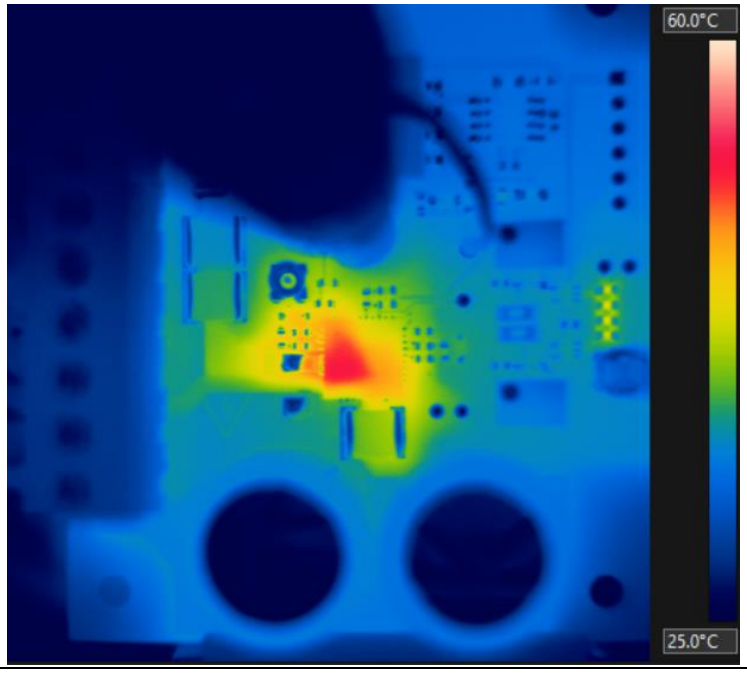

Figure 21 Thermal image of the chipset in soft switching condition at 200 kHz, 5 A pk-pk current

4.11 Inverter test

A full-bridge inverter can be setup using two evaluation boards configured in buck topology. The output capacitors C20 and C12 can be used as the half-bridge inverter output filter. **Figure 22** shows the topology configuration using the evaluation hardware. For each half-bridge, complimentary PWM signals are supplied by a microcontroller and is connected directly to the digital input terminals (shown in **Figure 6**). The deadtime can be as low as 50 ns. **Figure 23** shows the inverter hardware setup. The microcontroller used in this setup is Infineon XMC1404 programmed to drive the half-bridges with Sine-PWM unipolar pattern. The generated output line frequency is 60 Hz and the switching frequency is 65 kHz. For this test there is no closed loop control (only open loop inverter drive with constant modulation index). The modulation index is set to have about 240 V AC output when DC bus is 380 V. The output voltage in this case is 60 Hz.

Figure 24 shows the load voltage and current. Each half-bridge is delivering about 72 W power (total 144 W). The thermal image from the chipset is shown in **Figure 25**. Without any thermal relief the temperature of the chipset is below 40°C. This test setup shows the benefits of using CoolGaN™ IPS half-bridge device in inverter application in which the transistors operate in hard switching condition and a direct digital interface with a microcontroller can save the hardware size and the BOM cost if all devices are placed in one PCB. With a very low power dissipation, the thermal relief solution for this IPS chipset is not a challenge.

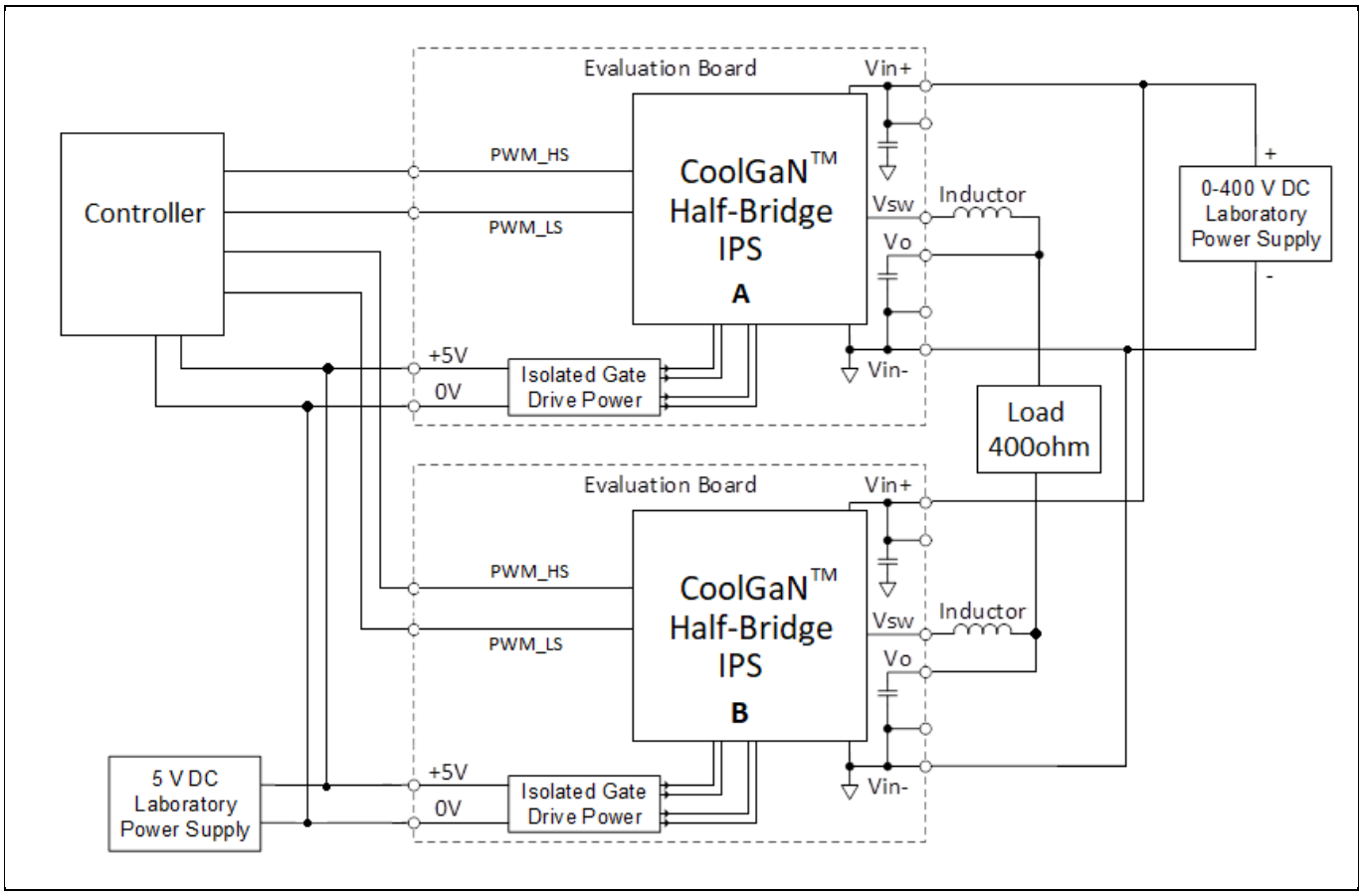

Figure 22 Inverter setup with two half-bridge evaluation boards

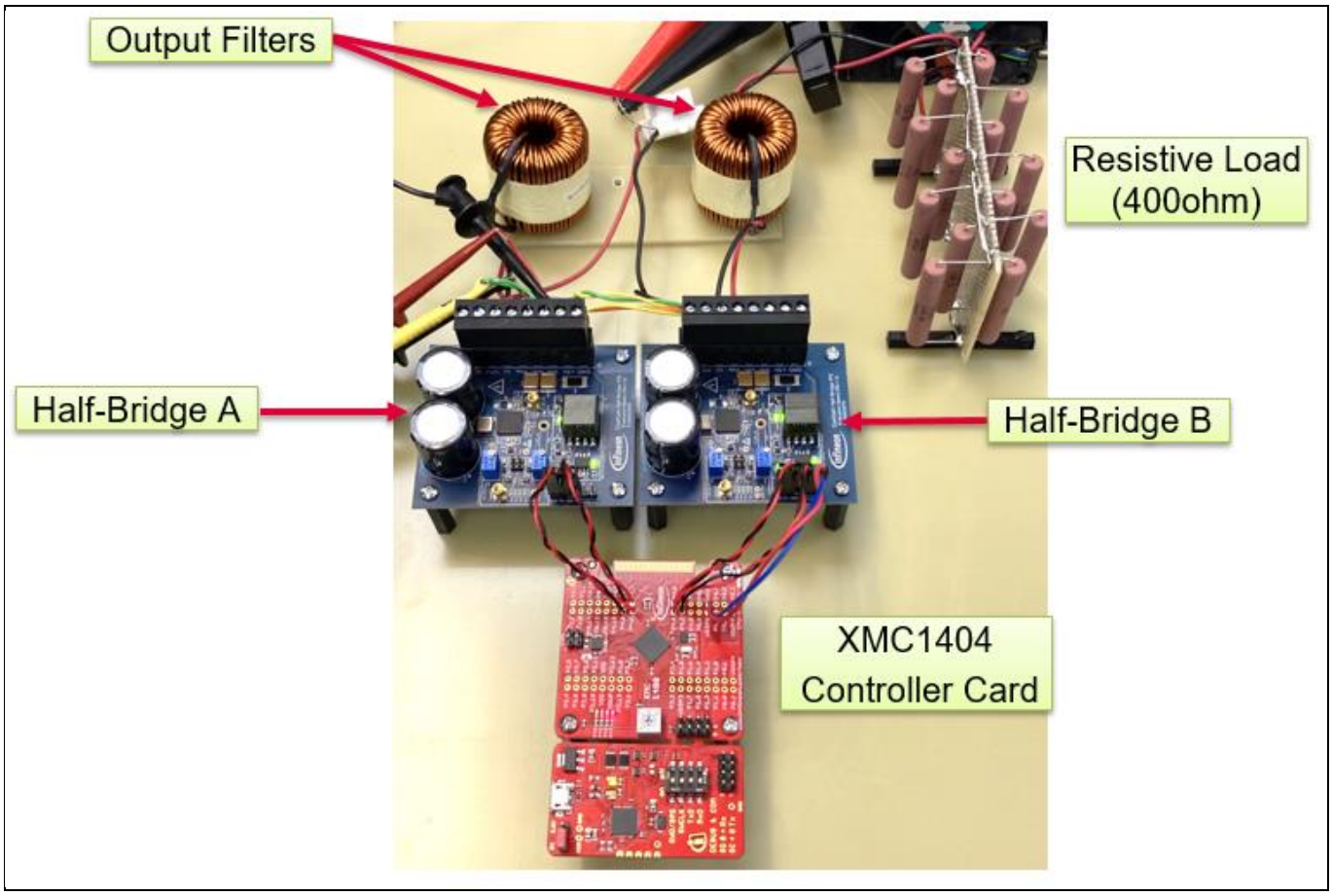

Figure 23 Inverter setup with two half-bridge evaluation boards

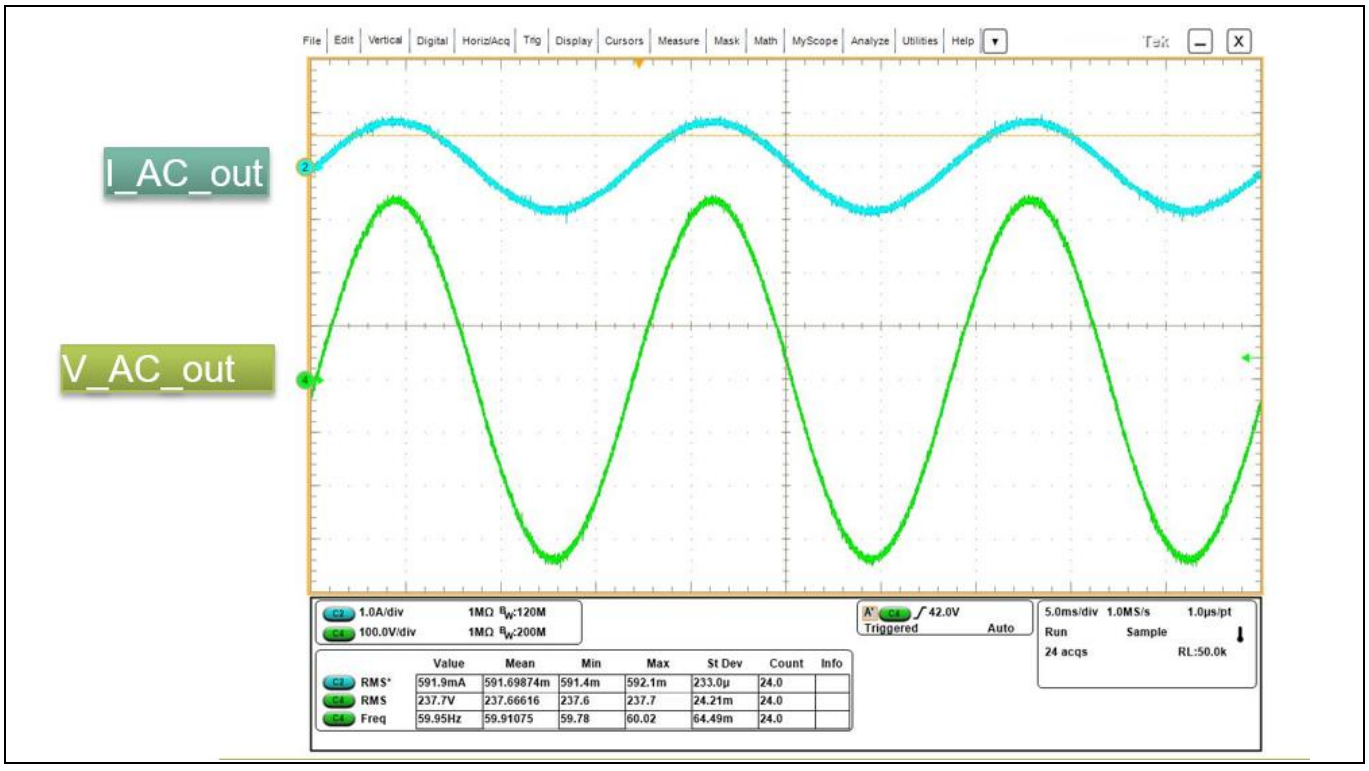

Figure 24 Inverter voltage and current output

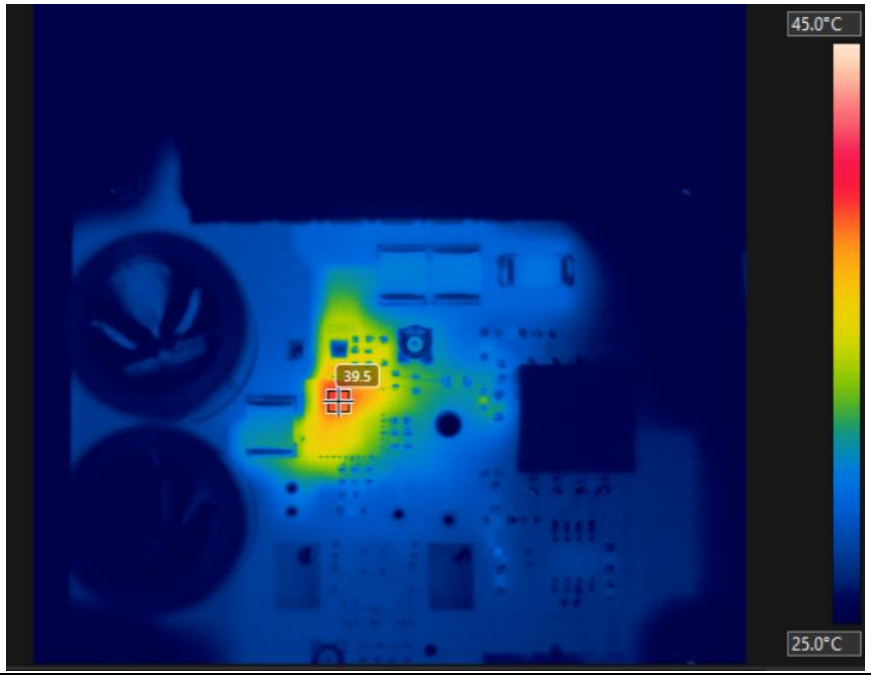

Figure 25 Thermal image of the half-bridge A

5 Complete schematic

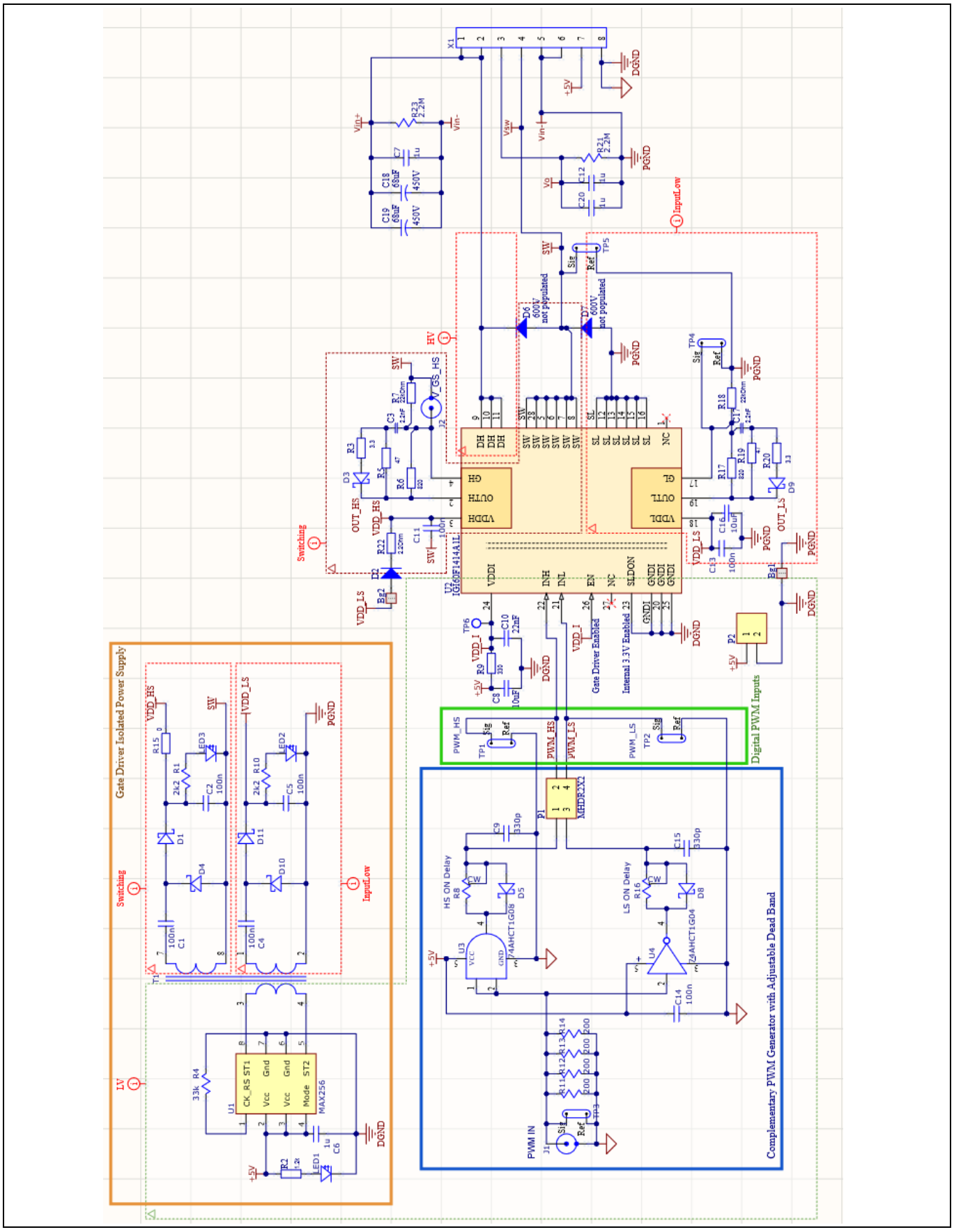

Figure 26 Schematic of CoolGaN™ IPS half-bridge evaluation board

6 PCB layout

The evaluation board is 1.3 mm thick, with 4-layers 70 µm thick copper. The layer stackup is depicted below.

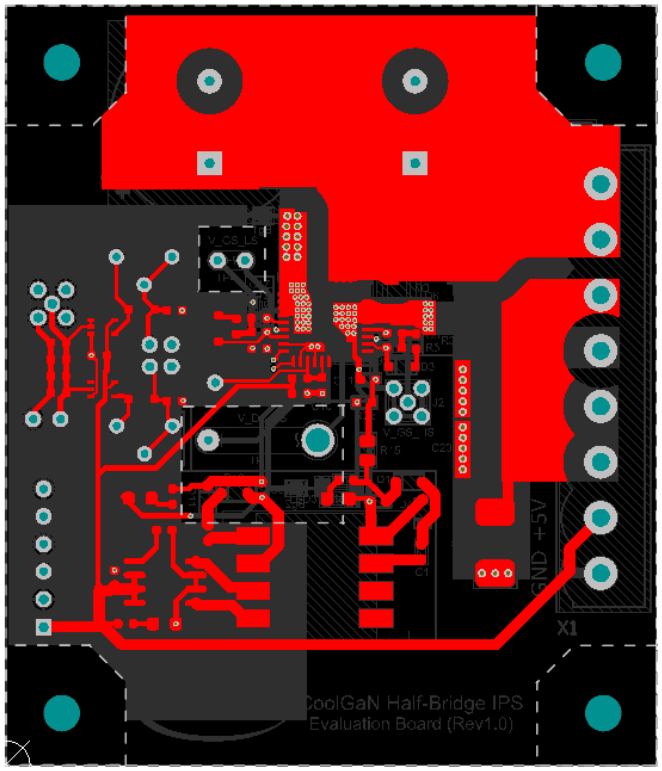

Figure 27 Top layer copper layer

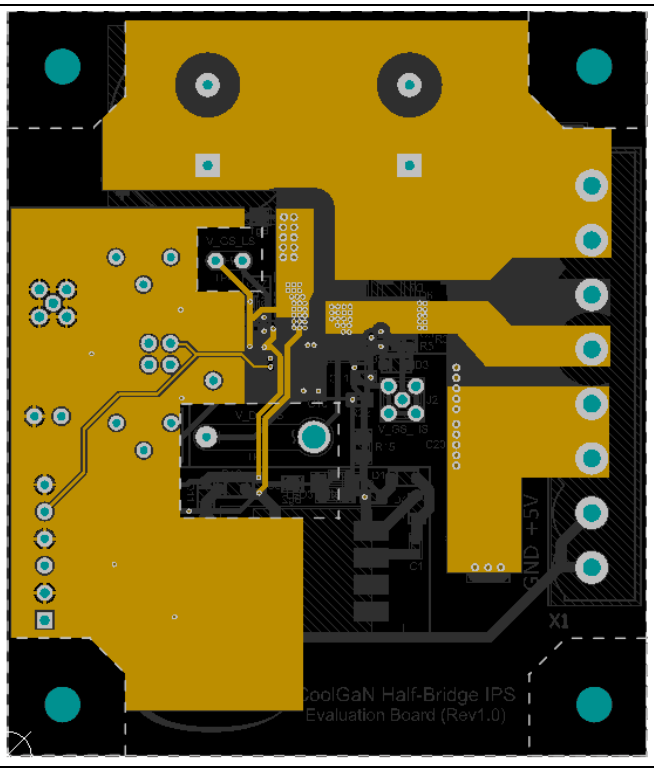

Figure 28 Upper middle copper layer

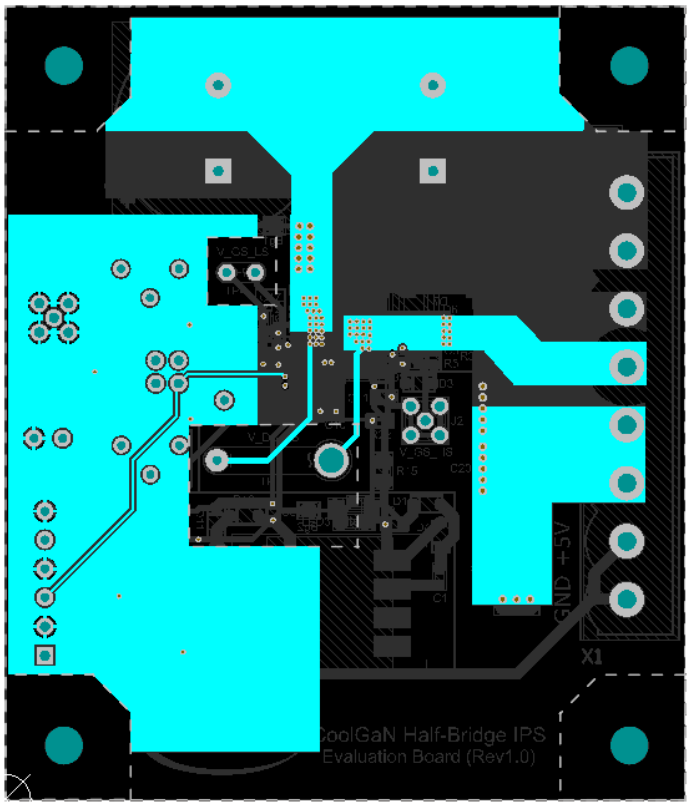

Figure 29 Lower middle copper layer

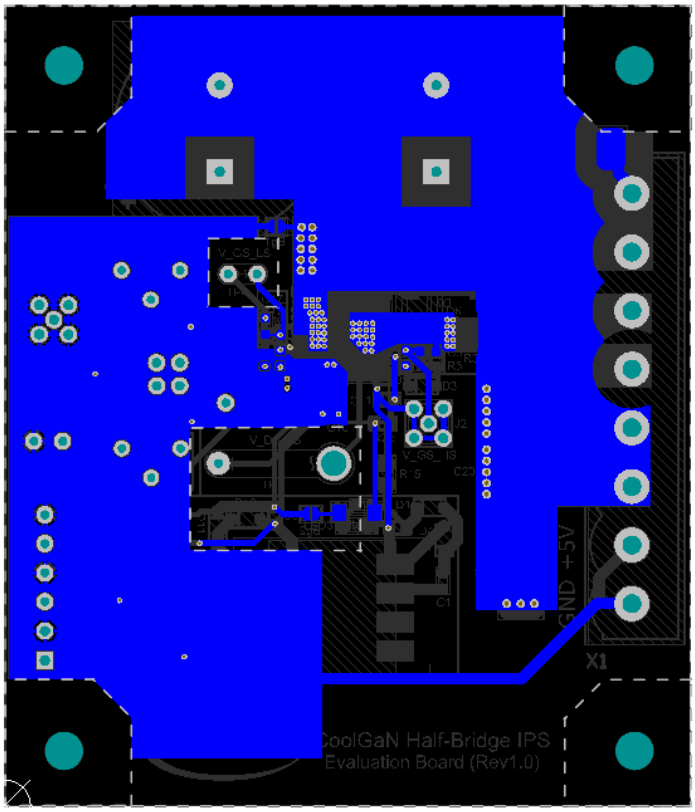

Figure 30 Bottom copper layer

7 Bill of materials

The following table describes all of the components on the PCB.

Table 3 PCB BOM

Designator	Description	Quantity	Vendor
C1, C2, C4, C5, C11, C13, C14	CAP CER 0.1UF 25V X7R 0603	7	490-16477-1-ND
C3, C17	CAP CER 2200PF 25V NP0 0603	2	399-15381-1-ND
C6	CAP CER 1UF 16V X7R 0603	1	311-1446-1-ND
C7, C12, C20	CAP CER 1UF 450V X7T 2220	3	445-6841-1-ND
C8, C16	CAP CER 10UF 16V X5R 0603	2	490-12736-1-ND
C9, C15	CAP CER 330PF 16V C0G/NP0 0603	2	399-10047-1-ND
C10	CAP CER 0.022UF 16V X7R 0603	1	399-1093-1-ND
C18, C19	CAP ALUM 68UF 20% 450V	2	1189-4260-ND
D1, D3, D4, D5, D8, D9, D10, D11	DIODE SCHOTTKY 30V 200MA SOD323	8	BAT54HT1GOSCT-ND
D2	DIODE ES1JL 600V 1A Sub SMA Fast Recovery	3	ES1JLR3GCT-ND
D6,D7	DIODE GEN PURP 600V 1A Sub_SMA Fast Recovery, Diode (Not Populated)	3	ES1JLR3GCT-ND
J1, J2	CONN MMCX JACK STR 50 OHM PCB	2	WM9481-ND
LED1, LED2, LED3	LED GREEN CLEAR 0805 SMD	3	732-4986-1-ND
P1	CONN HEADER VERT 4POS 2MM	1	0877580417-ND
R1, R10	SMD 2.2K OHM 1% 1/10W 0603	2	P2.20KHCT-ND
R2	SMD 1.2K OHM 1% 1/10W 0603	1	P1.20KHCT-ND
R3, R20	SMD 3.3 OHM 1% 1/10W 0603	2	P3.3GCT-ND
R4	SMD 33K OHM 1% 1/10W 0603	1	P33.0KHCT-ND
R5, R19	SMD 47 OHM 1% 1/10W 0603	2	P47.0HCT-ND
R6, R17	SMD 820 OHM 1% 1/10W 0603	2	P820HCT-ND
R7, R18	SMD 22K OHM 1% 1/10W 0603	2	P22.0KHCT-ND
R8, R16	TRIMMER 1K OHM 0.25W PC PIN TOP	2	3266W-1-102LF
R9	SMD 330 OHM 1% 1/10W 0603	1	P330HCT-ND
R11, R12, R13, R14	SMD 200 OHM 1% 1/10W 0603	4	P200HCT-ND
R15	SMD 0 OHM 1% 1/10W 0805	1	P0.0ACT-ND
R21, R23	SMD 2.2M OHM 5% 1W 2512	2	541-2.2MXCT-ND
R22	SMD 2.2 OHM 1% 1/10W 0603	1	P2.2AJCT-ND
T1	Transformer ICE1235	1	N/A
U1	IC DVR H-BRIDGE 3W 8-SOIC	1	MAX256ASA-ND
U2	**Infineon CoolGaN™ IGI60F1414A1L**	**1**	**Infineon IGI60F1414A1L**
U3	IC GATE AND 1CH 2-INP SOT-353	1	74AHCT1G08SE-7DICT-ND
U4	IC SINGLE INVERTER GATE SOT353	1	74AHCT1G04SE-7DICT-ND
X1	8 way connector	1	WM7842-ND

8 References

[1] Application note on “**CoolGaN™ 600 V half-bridge evaluation platform featuring EiceDRIVER™ GaN**”

Revision history

Document version	Date of release	Description of changes
V 1.0	30-04-2021	First release