



EVCS180X-S-Y-00A

Linear Hall-Effect Current Sensor Evaluation Board

DESCRIPTION

The EVCS180X-S-Y-00A is an evaluation board designed to demonstrate the capabilities of the MCS180X family, which are linear Hall-effect current sensors for AC and DC current sensing. The Hall array is differential, which cancels out stray magnetic field. This series of parts provides two power supply options (3.3V or 5V) and six full current ranges of 5A to 50A for the best accuracy in different applications.

The output voltage (V_{OUT}) is proportional to the primary applied current flowing through the primary conductor. The galvanic isolation between the primary conductive path pins and the sensor leads allow the MCS180X to take the place of optoisolators or other expensive isolation devices. The MCS180X is available in an SOIC-8 package.

FEATURES

- 3.3V or 5V Supply Voltage
- 5A to 50A Primary Applied Current
- Differential Hall Array for External Magnetic Field Cancellation
- 0.9mΩ Internal Conductor Resistance
- 100kHz Maximum Bandwidth
- 4μs Minimum Output Rise Time

APPLICATIONS

- Motor Controls
- Automotive Systems
- Load Detection and Load Management
- Switch-Mode Power Supplies
- Over-Current Fault Protections

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

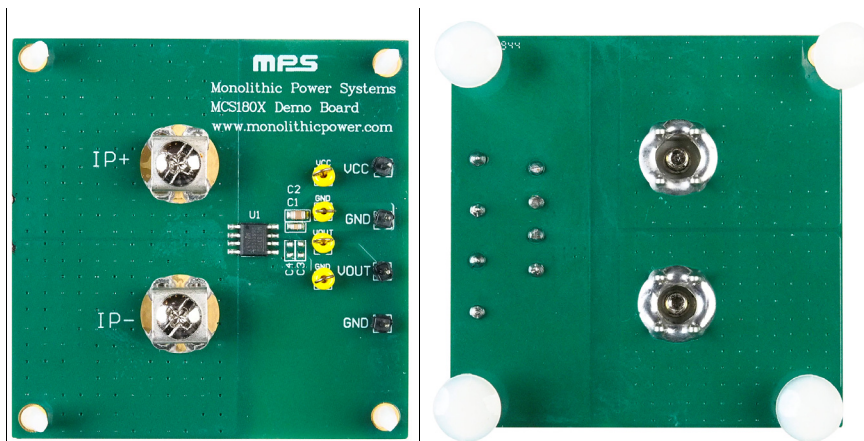
ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Supply voltage	V_{CC}	3.3 or 5	V
Maximum primary applied current	I_{P_MAX}	Six ranges from 5 to 50	A
Output voltage	V_{OUT}	$0.5 \times V_{CC} + Sens_{(TYP)} \times I_P^{(1)}$	V

Note:

1) $Sens_{(TYP)}$ is the symbol for "typical sensitivity."

EVCS180X-S-Y-00A EVALUATION BOARD



LxWxH (58mmx58.5mmx12mm)

Board Number	MPS IC Number
EVCS180X-S-Y-00A	MCS180XGS-Y

EVALUATION BOARD BASIC INFORMATION

Evaluation Board PN	Typical VCC Supply Voltage (V)	Optimized Primary Current (A)	Typical Sensitivity (mV/A)
EVCS1800-S-12-00A	3.3	±12.5	110
EVCS1800-S-25-00A		±25	55
EVCS1801-S-12-00A	5	±12.5	160
EVCS1801-S-25-00A		±25	80
EVCS1802-S-05-00A	3.3	±5	264
EVCS1802-S-10-00A		±10	132
EVCS1802-S-20-00A		±20	66
EVCS1802-S-30-00A		±30	44
EVCS1802-S-40-00A		±40	33
EVCS1802-S-50-00A		±50	26.4
EVCS1803-S-05-00A		5	±5
EVCS1803-S-10-00A	±10		200
EVCS1803-S-20-00A	±20		100
EVCS1803-S-30-00A	±30		66
EVCS1803-S-40-00A	±40		50
EVCS1803-S-50-00A	±50		40

QUICK START GUIDE

1. Preset the DC power supply to 3.3V or 5V.
2. Turn off the power supply.
3. Connect the DC power supply terminals to:
 - a. Positive (+): VCC
 - b. Negative (-): GND
4. Connect the current source load terminals to:
 - a. Positive (+): IP+
 - b. Negative (-): IP-
5. Turn on the DC power supply and current source. Measure the output result via the VOUT pin.
6. C4 determines the sensor's bandwidth. A larger C4 capacitance leads to a lower sensor bandwidth.

EVALUATION BOARD SCHEMATIC

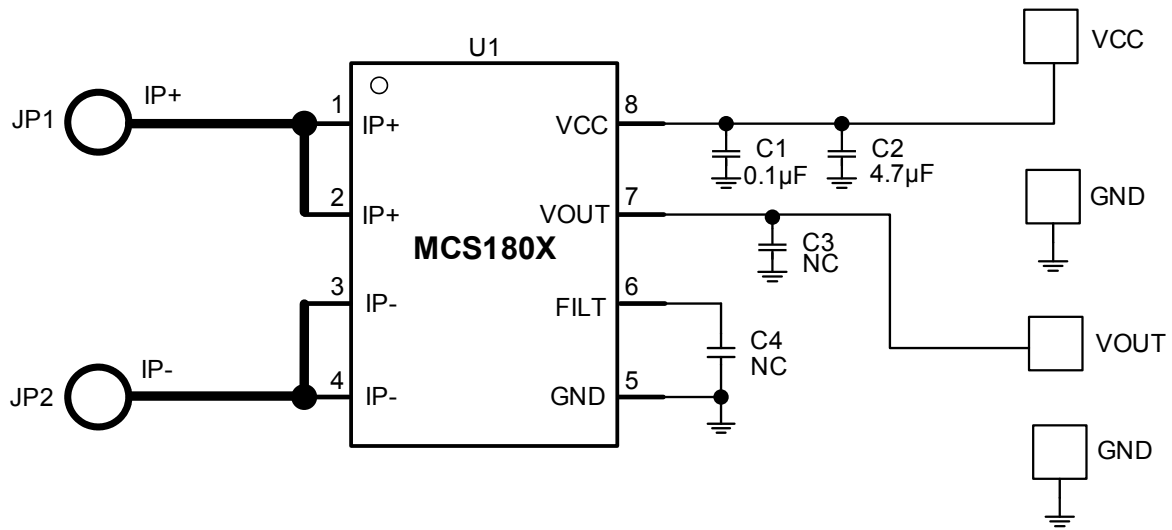


Figure 1: Evaluation Board Schematic

EVCS180X-S-Y-00A BILL OF MATERIALS

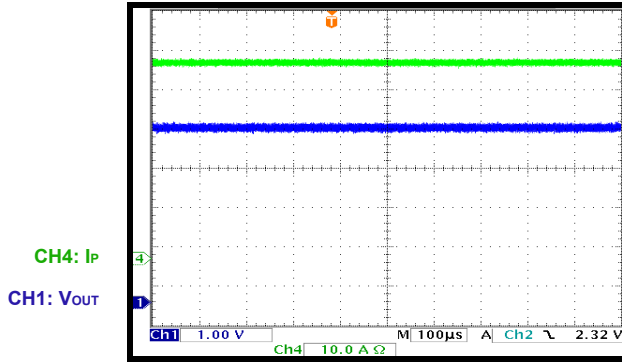
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	0.1µF	VCC ceramic decoupling capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C2	4.7µF	VCC ceramic decoupling capacitor, 16V, X7R	0805	Murata	GCM21BR71C475KA73L
1	C3	NS	Optional filter cap			
1	C4	NS	Optional filter cap			
4	Pin header	2.54mm	Male pin header	DIP	BKL Electronic	10120920
2	IP+, IP-	6.32 Philips	4-pin screw terminal	DIP	Keystone Electronics	8191K-ND
1	U1	MCS180X	Current sensor	SOIC-8	MPS	MCS180XGS-Y

EVB TEST RESULTS

Performance waveforms are tested on the EVCS1803-S-50-00A evaluation board. $V_{CC} = 5V$, C3 is open, C4 is open, $T_A = 25^\circ C$, unless otherwise noted.

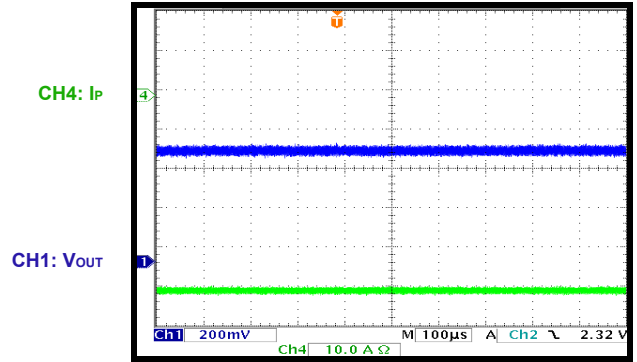
DC Current Status

$I_P = 50A$



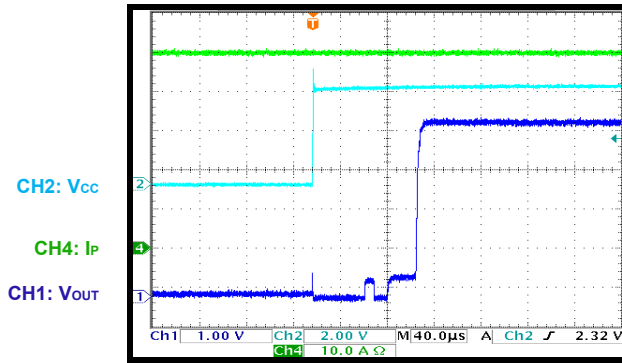
DC Current Status

$I_P = -50A$



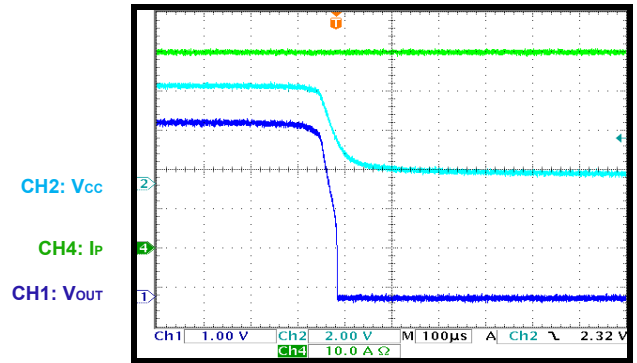
Start-Up through VCC

$I_P = 50A$

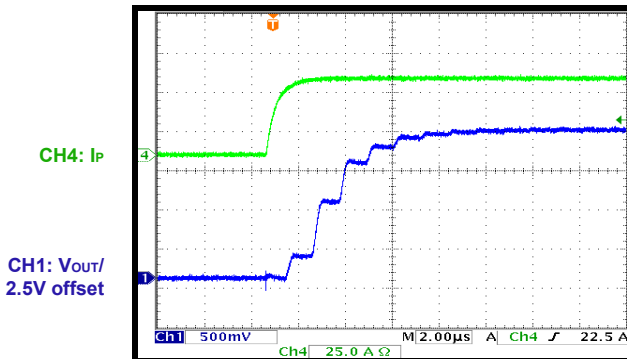


Shutdown through VCC

$I_P = 50A$

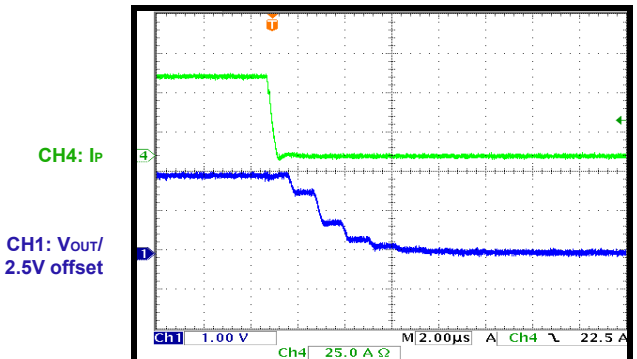


Step-Up Current



Step-Down Current

$I_P = 50A$



PCB LAYOUT

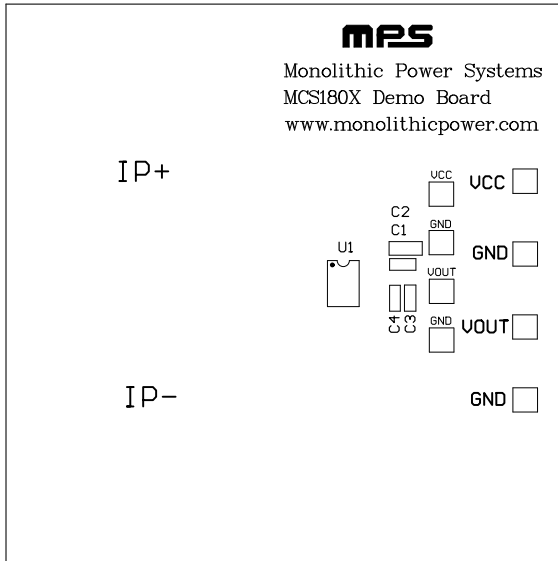


Figure 2: Top Silk

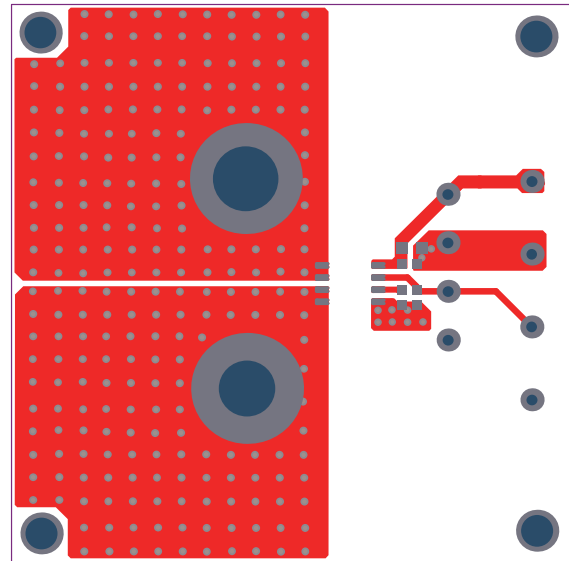


Figure 3: Top Layer

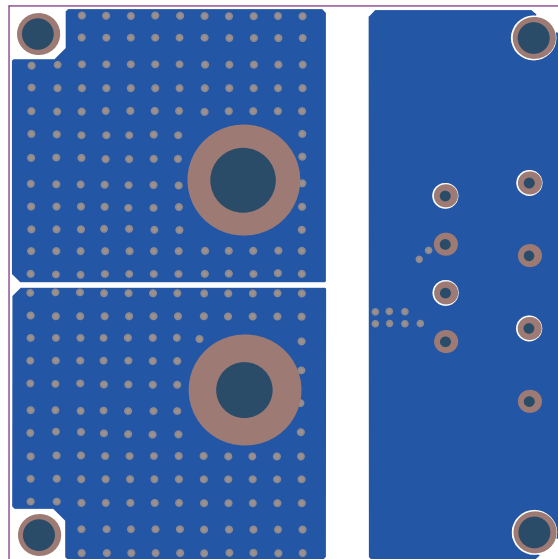


Figure 4: Bottom Layer