Evaluation board for AEM30940 - RF harvesting

Description

The AEM30940 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM30940 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM30940 (Document DS_AEM30940).

The AEM30940 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting. It includes two matching networks and rectifiers for a 50 Ω single-ended antenna. It allows easy connections to the RF energy harvester, the storage element and the low-voltage and high-voltage loads. It also provides all the configuration access to set the device in configuration modes described in the datasheet. The MPPT ratio is fixed at 50 % to optimize the rectifier efficiency. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performance.

The AEM30940 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes) for the design of a highly efficient radio frequency powered subsystem in your target application. There are two designs of the AEM30940 evaluation board for RF harvesting. One is for the 868 MHz band and another for the 915 MHz band.

- RF harvesting
- Industrial monitoring
- Indoor geolocation
- Home automation
- E-health monitoring
- Wireless sensor nodes

Features

Three two-way screw terminals
- Low-voltage load
- High-voltage load
- Primary energy storage element

One three-way screw terminal
- Energy storage element (battery or (super)capacitor)

Two male 50 Ω SMA connectors
- Connections to the RF source
- Associated matching networks and rectifiers

One 2-pin "Shrouded Header"
- Alternative connection for the storage element

Nine 3-pin headers
- Low drop-out regulators (LDOs) enabling
- Energy storage elements and LDOs configuration
- Dual-cell supercapacitor configuration
- Connection from rectifier to AEM30940

Two 2-pin headers
- Primary battery configuration

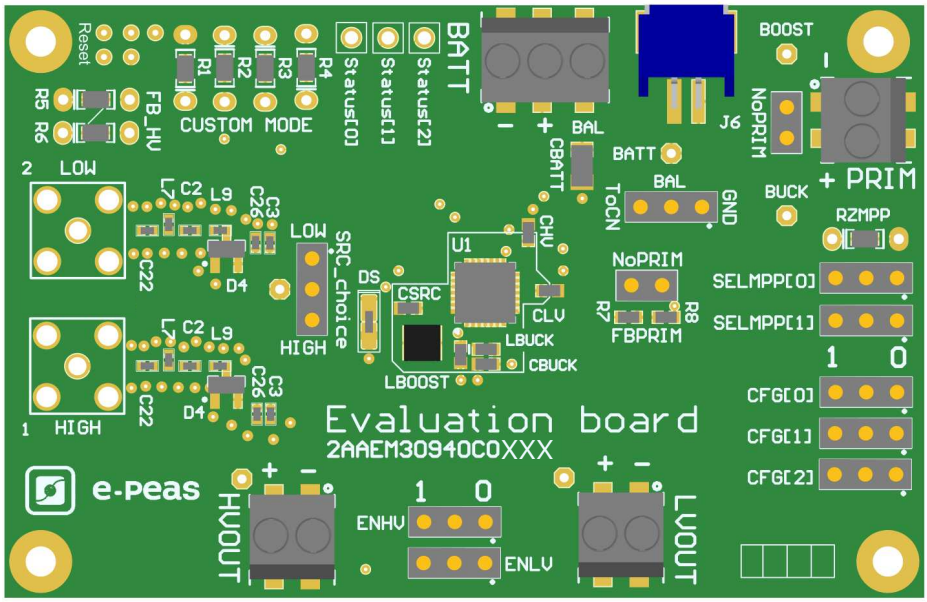
Provision for nine resistors
- Custom mode configuration
- Primary battery configuration
- ZMPP configuration

Three 1-pin headers
- Access to status pins

Device information

Part number	Dimensions
2AAEM30940C0XXX	76 mm x 50 mm
XXX: 211	868 MHz
XXX: 310	915 MHz

Appearance



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1 Connections Diagram

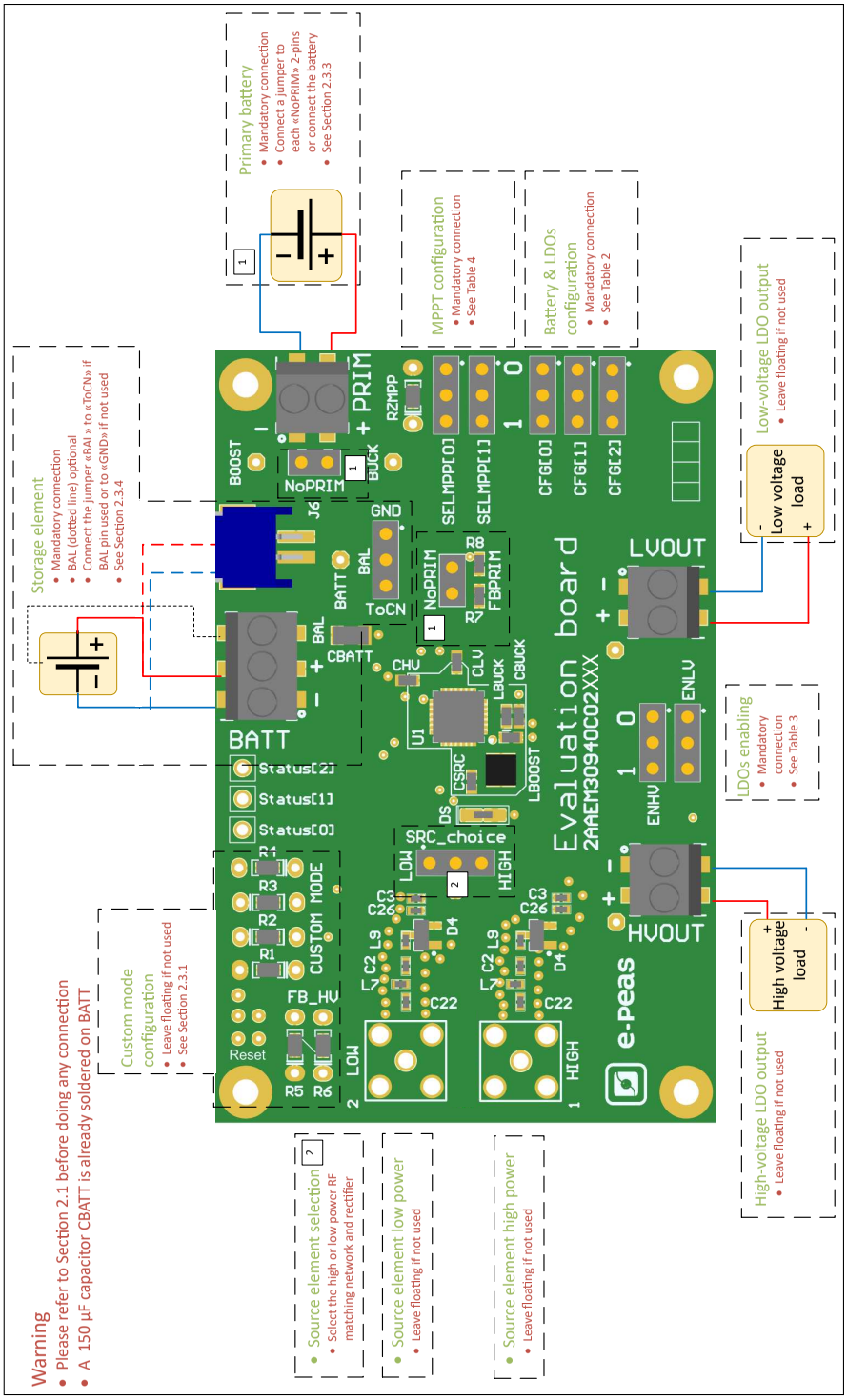


Figure 1: Connection diagram

1.1 Signals description

NAME	FUNCTION	CONNECTION	
Power signals		**If used**	**If not used**
LVOUT	Output of the low-voltage LDO regulator.	Connect a load.	
HVOUT	Output of the high-voltage LDO regulator.	Connect a load.	
BAL	Connection to mid-point of a dual-cell supercapacitor.	Connect mid-point and jumper BAL to "ToCN".	Connect jumper BAL to "GND".
BATT	Connection to the energy storage element.	Connect storage element in addition to CBATT (150 µF).	Do not remove CBATT.
PRIM	Connection to the primary battery.	Connect primary battery.	Connect a jumper to each NoPRIM 2-pins.
Debug signals			
VBOOST	Output of the boost converter.		
VBUCK	Output of the buck converter.		
SRC	Output of the rectifier		
Configuration signals			
CFG[2]	Configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.	Connect jumper (see Table 2).	Cannot be left floating (see Table 2).
CFG[1]			
CFG[0]			
SRC_CHOICE	Selection of the high or low power matching network and rectifier.	Connect jumper SRC_CHOICE to high or low.	Cannot be left floating
FBPRIM	Configuration of the primary battery.	Use resistors R7-R8 (see Section 2.3.3).	Connect a jumper to each NoPRIM 2-pins.
FB_HV	Configuration of the high-voltage LDO in the custom mode.	Use resistors R5-R6 (see Section 2.3.1).	Leave floating.
RZMPP	Conguration of the constant impedance MPP.	Use resistor RZMPP	Leave floating
Control signals			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
Status signals			
STATUS[2]	Logic output. Asserted when the AEM performs the MPP evaluation.		
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		

Table 1: Pin description

2 General Considerations

2.1 Safety information

Always connect the elements in the following order:

1. Reset the board - see "How to reset the AEM30940 evaluation board" on page 7.
2. Completely configure the PCB (jumpers/resistors);
   - Battery and LDOs configuration (CFG[0], CFG[1], CFG[2] and, if needed, R1-R2-R3-R4-R5-R6) - see Table 2,
   - Primary battery configuration (NoPRIM or R7-R8) - see Section 2.3.3,
   - LDOs enabling (ENHV and ENLV) - see Table 3,
   - Balun circuit connection (BAL) - see Section 2.3.4.
3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
5. Connect the source.

To avoid damage to the board, users are urged to follow this procedure.

2.2 Basic configurations

The MPP configuration is not available on the AEM30940 evaluation board. The MPP is by default configured to 50 % of Voc as this ratio optimize the proposed rectifier efficiency.

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	Vovch	Vchrdy	Vovdis	Vhv	Vlv	
H	H	H	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
H	H	L	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
H	L	H	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
H	L	L	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
L	H	H	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
L	H	L	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
L	L	H	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
L	L	L	Custom mode - see Section 2.3.1				1.8 V	

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
H	H	Enabled	Enabled
H	L	Enabled	Disabled
L	H	Disabled	Enabled
L	L	Disabled	Disabled

Table 3: LDOs enabling

SELMPP[1]	SELMPP[0]	Vmpp/Voc
0	0	50%
0	1	65%
1	0	80%
1	1	ZMPP

Table 4: Usage of SELMPP[1:0]

2.3 Advanced configurations

A complete description of the system constraints and configurations is available in Section 8 "System configuration" of the AEM30940 datasheet .
A reminder on how to compute the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found at the e-peas website.

2.3.1 Custom mode

In addition to the pre-defined protection levels, the custom mode allows users to define their own levels via resistors R1 to R4 and to tune the output of the high voltage LDO via resistors R5-R6.
By defining RT = R1+R2+R3+R4 ($1\,M\Omega \leq RT \leq 100\,M\Omega$):

- R1 = RT (1 V / Vovch)
- R2 = RT (1 V / Vchrdy - 1 V / Vovch)
- R3 = RT (1 V / Vovdis - 1 V / Vchrdy)
- R4 = RT (1 - 1 V / Vovdis)

By defining RV = R5+R6 ($1\,M\Omega \leq RV \leq 40\,M\Omega$):

- R5 = RV (1 V / Vhv)
- R6 = RV (1 - 1 V / Vhv)

Make sure the protection levels satisfy the following conditions:

- Vchrdy + 0.05 V ≤ Vovch ≤ 4.5 V
- Vovdis + 0.05 V ≤ Vchrdy ≤ Vovch - 0.05 V
- 2.2 V ≤ Vovdis
- Vhv ≤ Vovdis - 0.3 V

If unused, leave the resistor footprints (R1 to R6) empty.

2.3.2 ZMPP configuration

If this configuration is chosen (see Table 4), the AEM30940 regulate Vsrc at a voltage equals to the product of R1 times the current available at the output of the internal rectifier.

- $10\,\Omega \leq RZMPP \leq 1\,M\Omega$

If unused, leave the resistor footprint R1 empty.

2.3.3 Primary battery configuration

As to the main storage element, the primary battery protection levels have to be defined. To do so, use resistors R7-R8.
By defining RP = R7+R8 ($100\,k\Omega \leq RP \leq 500\,k\Omega$):

- $R7 = \frac{Vprim\_min}{4} \cdot RP \cdot \frac{1}{2.2\,V}$
- R8 = RP - R7

If unused, use a jumper to short each "NoPRIM" 2-pins headers.

2.3.4 Balun circuit configuration

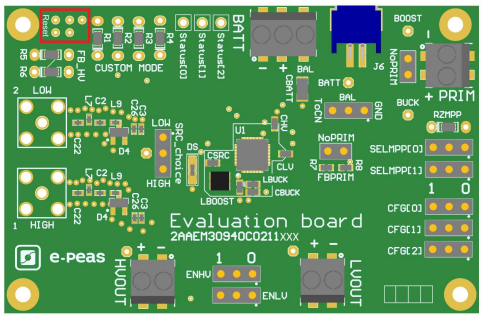
When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (on BATT connector)
- Use a jumper to connect "BAL" to "ToCN"

If unused, use a jumper to connect "BAL" to "GND".

How to reset the AEM30940 evaluation board:

To reset the board, simply disconnect the storage device and the optional primary battery and connect the 6 "Reset" connections (working from the rightmost to the left) to a GND node (i.e. the negative pin of any connector) in order to discharge the internal nodes of the system.



3 Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM30940. To avoid damaging the board, follow the procedure found in Section 2.1 "Safety information". If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:

- Configuration: CFG[2:0] = HLL, BAND 1 connected, ENLV = H, ENHV = H
- Storage element: capacitor (4.7 mF + CBATT)
- Load: 10 kΩ on HVOUT, LVOUT floating
- SRC: current source (1 mA or 100 µA) with voltage compliance (4 V)

Feel free to adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 "Introduction" of AEM30940 datasheet).

3.1 Start-up

The following example allows users to observe the behavior of the AEM30940 in the wake-up mode.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1.

Observations and measurements

- BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 2).
- HLDO/LLDO: Regulated when voltage on BATT first rises above Vchrdy (see Figure 2).
- STATUS[0]: Asserted when the LDOs are ready to be enabled (refer to Section 7.2 "Normal mode" of the AEM30940 datasheet) (see Figure 2).
- STATUS[2]: Asserted each time the AEM30940 performs a MPP evaluation (see Figure 3).

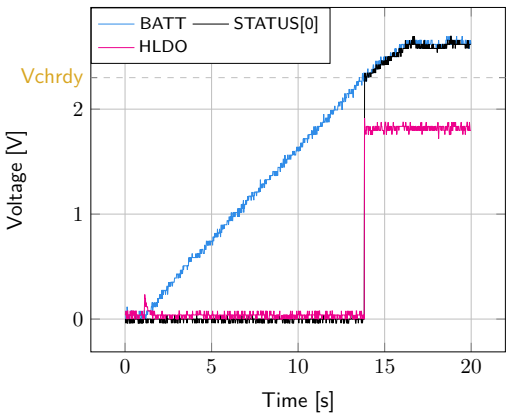


Figure 2: STATUS[0] and HLDO evolution with BATT

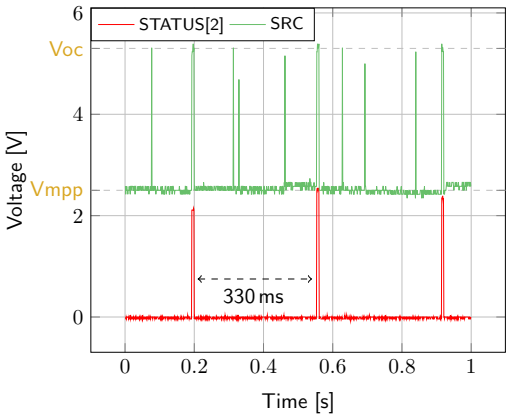


Figure 3: SRC and STATUS[2] while energy is extracted from SRC (BATT under Vovch)

3.2 Shutdown

This test allows users to observe the behavior of the AEM30940 when the system is running out of energy.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing Vovdis (see Figure 4).
- STATUS[0]: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 4).
- STATUS[1]: Asserted for 600 ms when the storage element voltage (BATT) falls below Vovdis (see Figure 4).

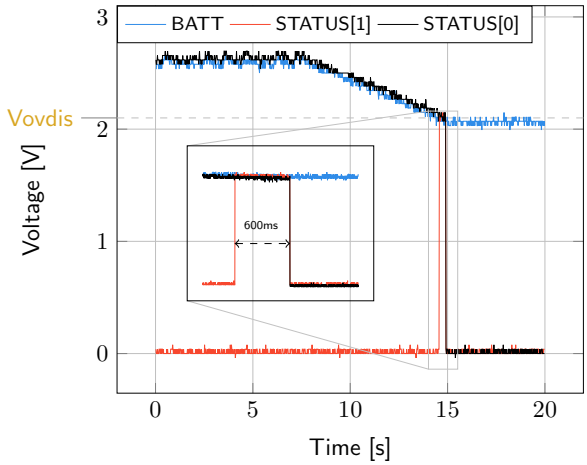


Figure 4: LDOs disabled around 600 ms after BATT reaches Vovdis

3.3 Switching on primary battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1 V coin cell with protection level at 2.4 V, R7 = 68 kΩ and R8 = 180 kΩ).
3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches Vovdis and then rises again to Vchrdy as it is recharged from the primary battery (see Figure 5).
- STATUS[0]: Never de-asserted as the LDOs are still functional (see Figure 5).
- HLDO: Stable and not affected by switching on the primary battery (see Figure 5).

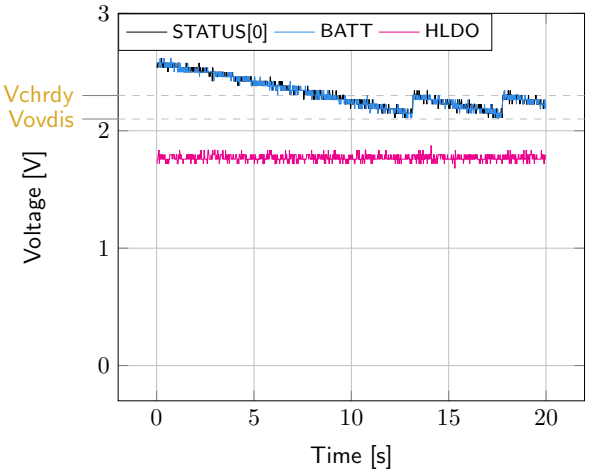


Figure 5: Switching from SRC to the primary battery

3.4 Cold start

The following test allows users to observe the minimum voltage required at SRC to coldstart the AEM30940. Be careful to avoid probing any unnecessary node to avoid leakage current induced by the probe. Make sure to properly reset the board to observe the cold-start behavior.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.
3. SMA connector: Connect your source element.