



# EVQ4415A-QB-00A

High-Efficiency, 1.5A, 36V, 2.2MHz, Synchronous, Step Down Converter Evaluation Board

## DESCRIPTION

The EVQ4415A-QB-00A is an evaluation board for the MP/MPQ4415AGQB.

MP/MPQ4415AGQB is a synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs and one input bypass capacitor. It offers a very compact solution to achieve a 1.5A of continuous output current with excellent load and line regulation over a wide input supply range. The MP/MPQ4415A uses synchronous mode operation to achieve high efficiency over the output current load range.

The EVQ4415A-QB-00A is a fully assembled and tested evaluation board, it generates 3.3V output voltage at load current up to 1.5A from a 4V to 36V input range.

## ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	$V_{IN}$	4 – 36	V
Output Voltage	$V_{OUT}$	3.3	V
Output Current	$I_{OUT}$	1.5	A

## FEATURES

- Wide 4V to 36V Operating Input Range
- 1.5A Continuous Load Current
- 90mΩ High-Side, 50mΩ Low-Side Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 2.2MHz Switching Frequency
- 450kHz to 2.2MHz Frequency Sync
- Forced Continuous Conduction Mode (CCM)
- Internal Soft Start (SS)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) with Valley-Current Detection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-13 (2.5mmx3mm) Package
- CISPR25 Class 5 Compliant
- AEC-Q100 Grade-1

## APPLICATIONS

- Automotive
- Industrial Control Systems
- Medical and Imaging Equipment
- Telecom Applications
- Distributed Power Systems

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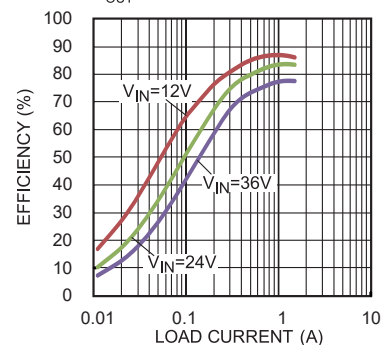
## EVALUATION BOARD



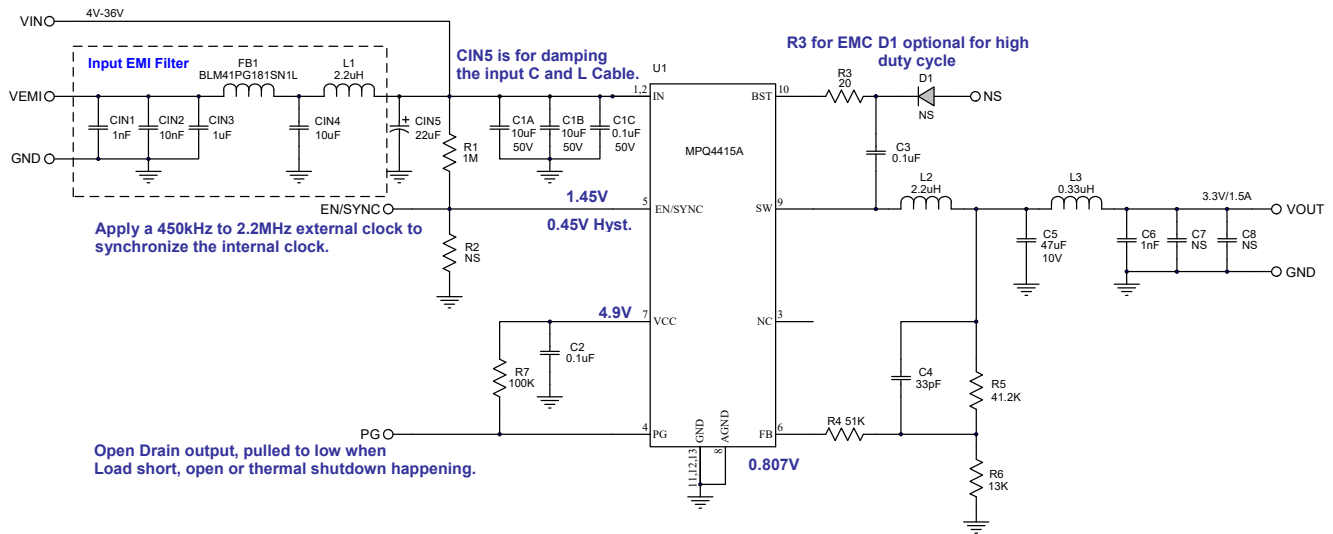
(L x W x H) 2.5" x 2.5" x 0.4"  
(6.4cm x 6.4cm x 1.0cm)

Board Number	MPS IC Number
EVQ4415A-QB-00A	MP/MPQ4415AGQB

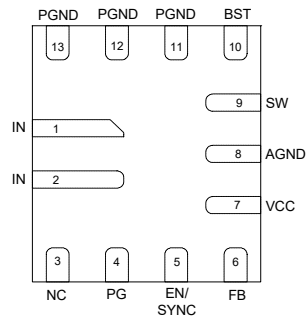
Efficiency vs. Load Current  
 $V_{OUT}=3.3V$



# EVALUATION BOARD SCHEMATIC



### Package reference



### Reference for FB divider selection

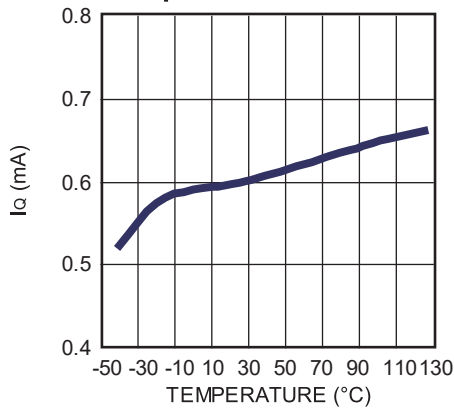
Vo(V)	R6(kΩ)	R5(kΩ)
5	41.2(1%)	7.68(1%)
2.5	41.2(1%)	19.6(1%)
1.8	41.2(1%)	33.5(1%)

**EVQ4415A-QB-00A BILL OF MATERIALS**

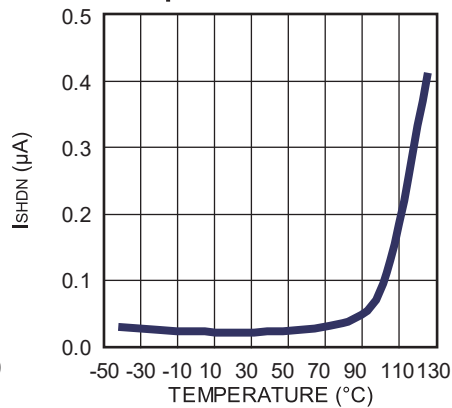
Qty	Ref	Value	Description	Package	Manufacturer	Part Number
1	CIN1	1nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H102KA01D
1	CIN2	10nF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H103JA01D
1	CIN3	1uF	Ceramic Cap., 50V, X7R	1206	muRata	GRM31MR71H105KA88L
1	CIN4	10uF	Ceramic Cap., 50V, X7R	1210	muRata	GRM32ER71H106KA12L
1	CIN5	22uF	Aluminium Cap; 63V	SMD	JiangHai	VTD-63V22
2	C1A, C1B	10μF	Ceramic Cap., 50V, X5R	1206	muRata	GRM31CR61H106KA12L
1	C1C	0.1μF	Ceramic Cap., 50V, X7R	0603	muRata	GRM188R71H104KA93D
2	C2, C3	0.1μF	Ceramic Cap., 16V, X7R	0603	muRata	GRM188R71C104KA01D
1	C4	33pF	Ceramic Cap., 50V, C0G	0603	muRata	GRM1885C1H330JA01D
1	C5	47μF	Ceramic Cap., 10V, X5R	1210	muRata	GRM32ER61A476KE20L
1	C6	1nF	Ceramic Cap., 16V, X7R	0603	muRata	GRM188R71C102KA01D
2	C7, C8	NS				
1	D1	NS				
1	FB1		Magnetic Bead	1806	muRata	BLM41PG181SN1L
2	L1, L2	2.2μH	Inductor, 70mOhm DCR, 3.5A	SMD	Cyntec	VCTA25201B-2R2MS6-89
1	L3	0.33μH	Inductor, 19mOhm DCR, 5.9A	SMD	Cyntec	VCTA20161B-R33MS6-89
1	R1	1M	Film Res., 5%	0603	Yageo	RC0603JR-071ML
1	R3	20	Film Res., 1%	0603	Yageo	RC0603FR-0720RL
1	R4	51k	Film Res., 1%	0603	Yageo	RC0603FR-0751KL
1	R5	13k	Film Res., 1%	0603	Yageo	RC0603FR-0713KL
1	R6	41.2k	Film Res., 1%	0603	Yageo	RC0603FR-0741K2L
1	R7	100k	Film Res., 1%	0603	Yageo	RC0603FR-07100KL
1	R2	NS				
1	U1		Step-Down Regulator	QFN13(2X3)	MPS	MPQ4415AGQB
5	VIN, VEMI, GND, GND, VOU T		2.0 Golden Pin		HZ	
4	PG, GND, EN/ SYN C, GND		2.54mm Test Pin		HZ	

## TYPICAL CHARACTERISTICS

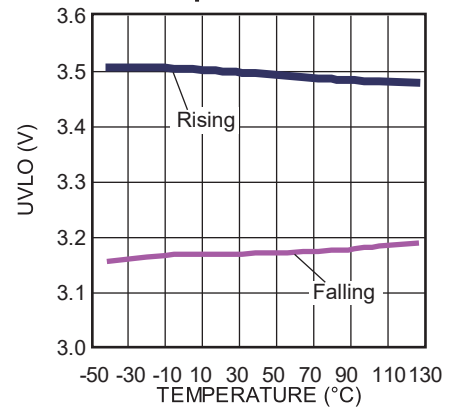
**Quiescent Current vs. Temperature**



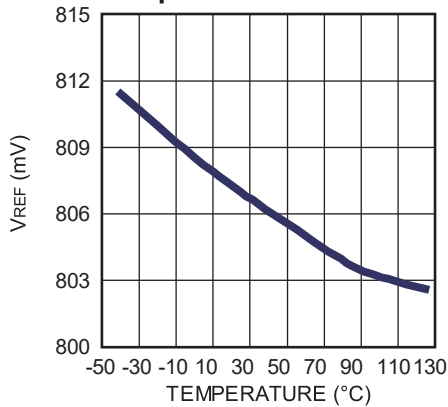
**Shutdown Current vs. Temperature**



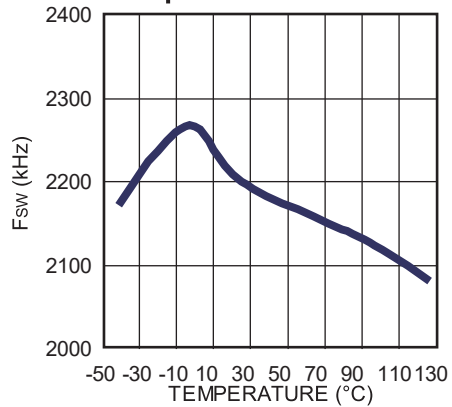
**$V_{IN}$  UVLO Threshold vs. Temperature**



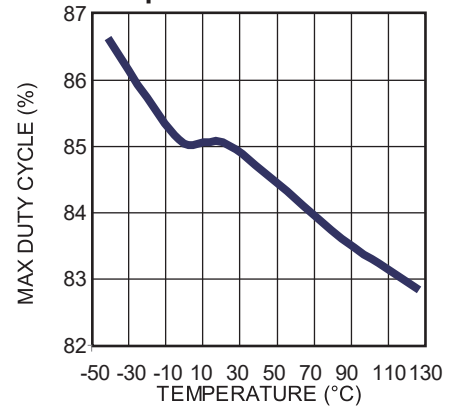
**Feedback Reference vs. Temperature**



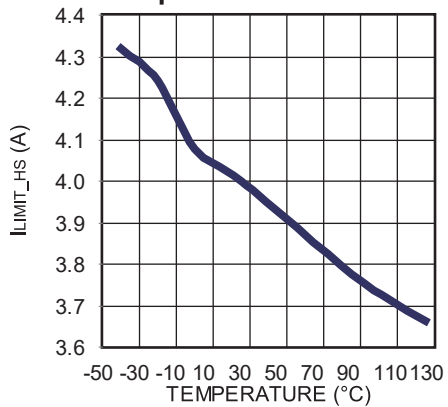
**Switching Frequency vs. Temperature**



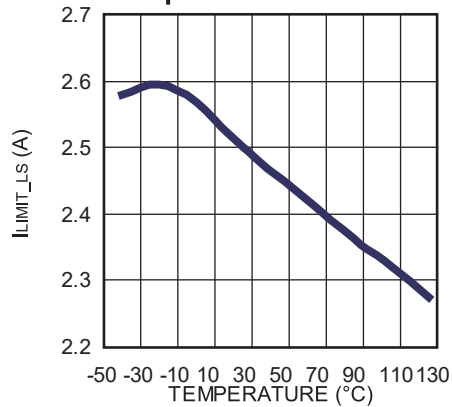
**Max Duty Cycle vs. Temperature**



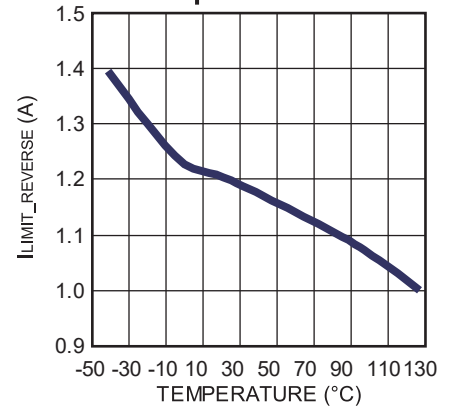
**Current Limit vs. Temperature**

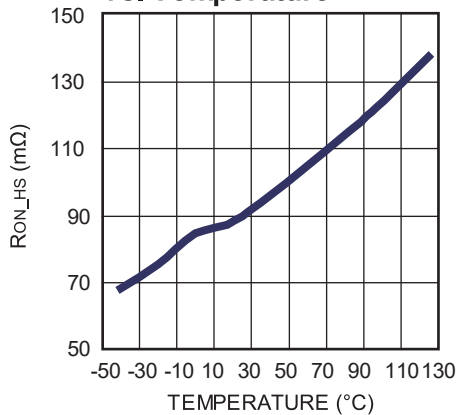
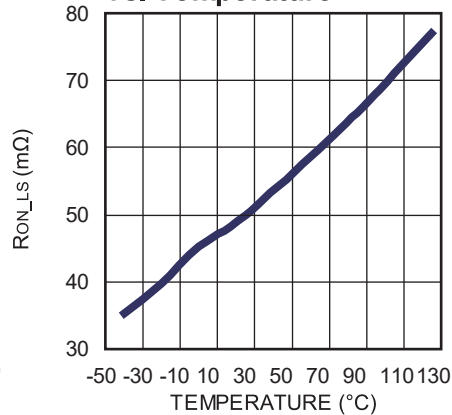
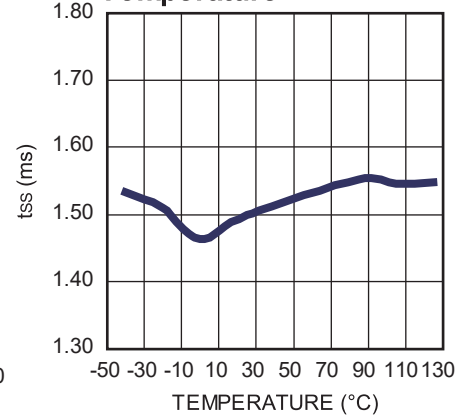
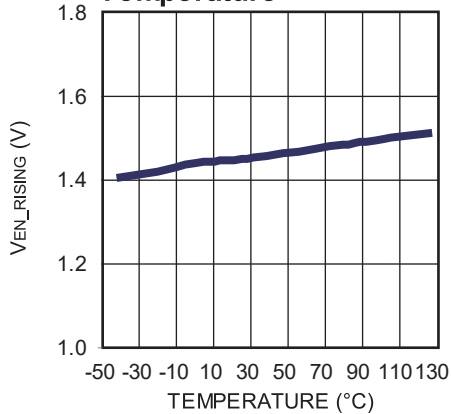
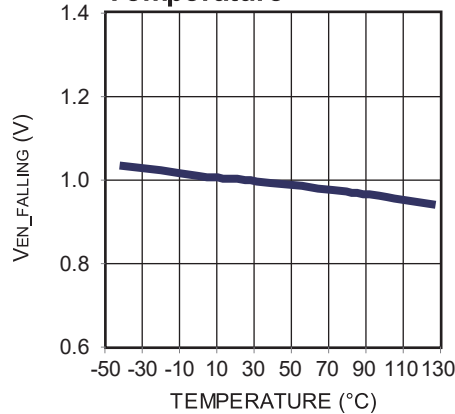
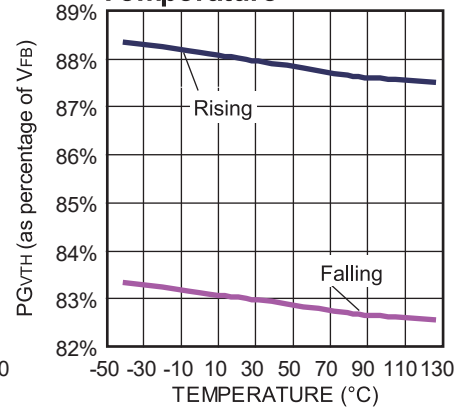
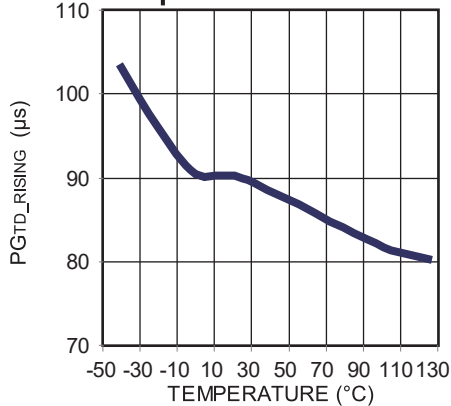
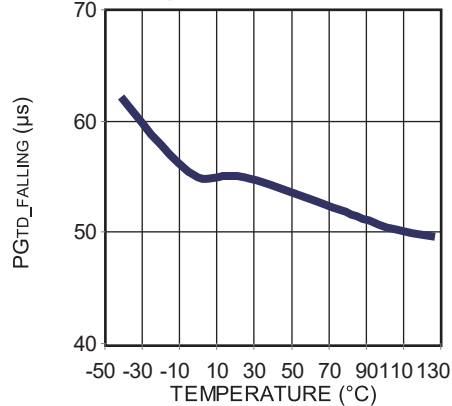


**Valley Current Limit vs. Temperature**



**Reverse Current Limit vs. Temperature**

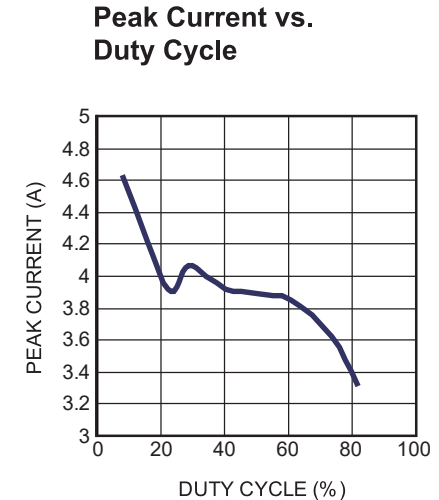
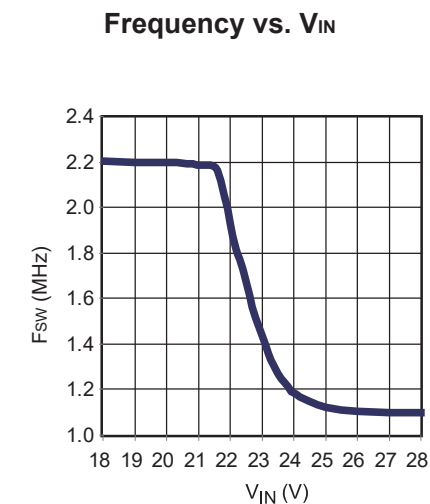
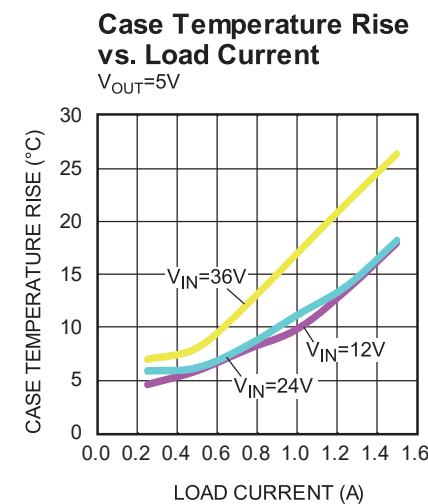
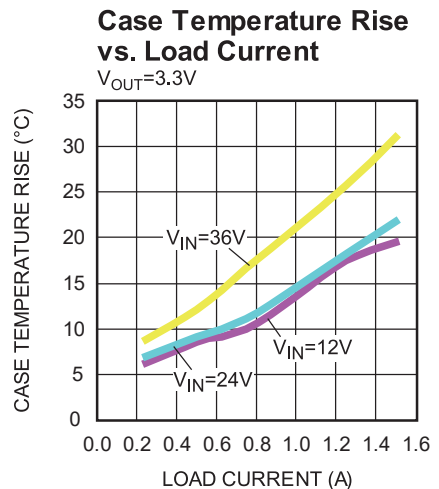
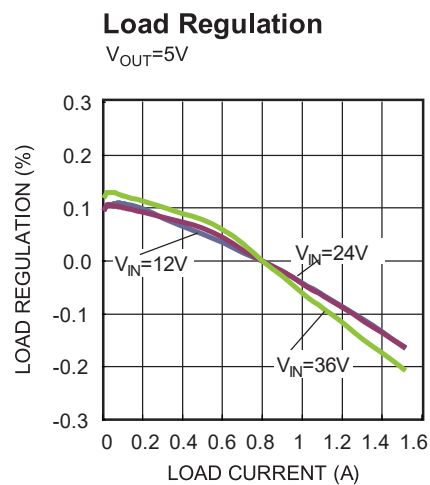
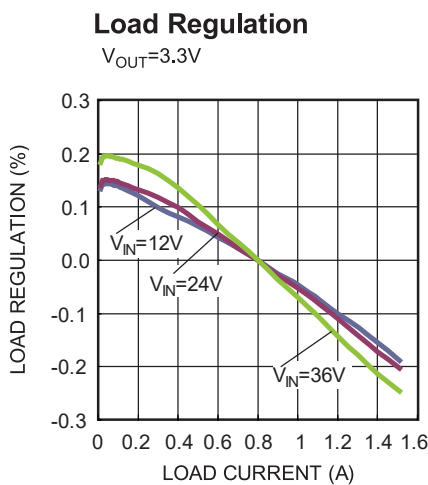
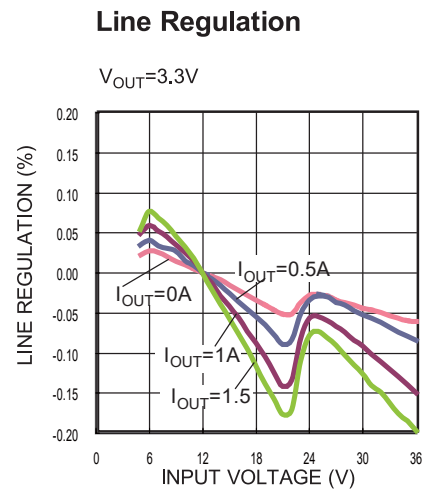
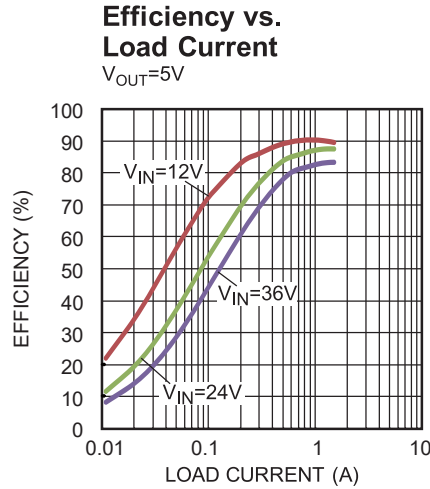
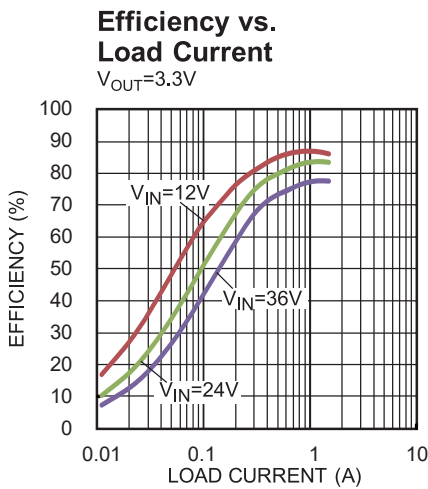


**TYPICAL CHARACTERISTICS (continued)**
**HS-FET On Resistance vs. Temperature**

**LS-FET On Resistance vs. Temperature**

**Soft-Start Time vs. Temperature**

**EN Rising Threshold vs. Temperature**

**EN Falling Threshold vs. Temperature**

**PG Threshold vs. Temperature**

**PG Rising Delay vs. Temperature**

**PG Falling Delay vs. Temperature**


## EVB TEST RESULTS

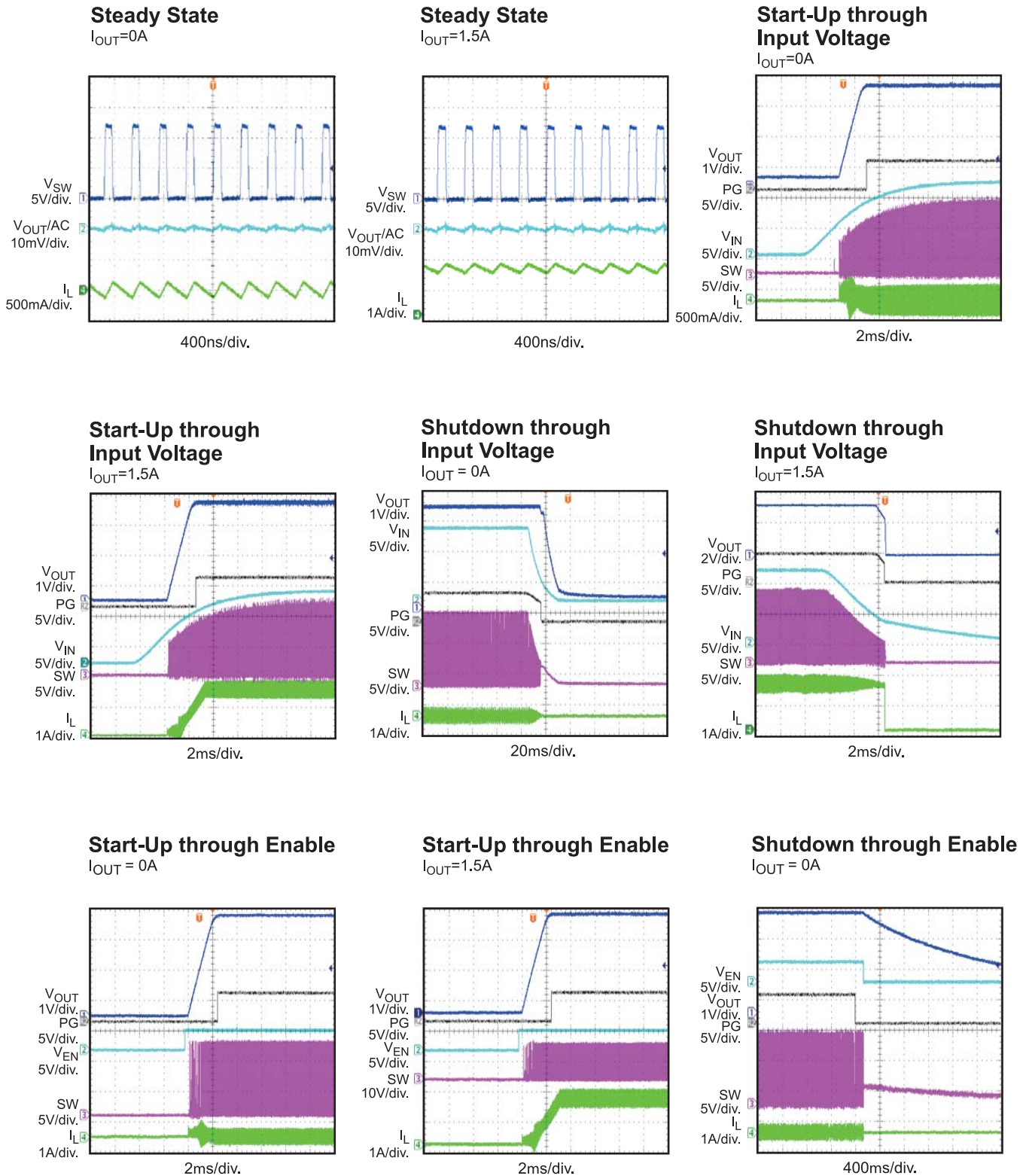
Performance waveforms are tested on the evaluation board.

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$ ,  $F_{SW} = 2.2MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



**EVB TEST RESULTS (continued)**

Performance waveforms are tested on the evaluation board.

 $V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$ ,  $F_{SW} = 2.2MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.


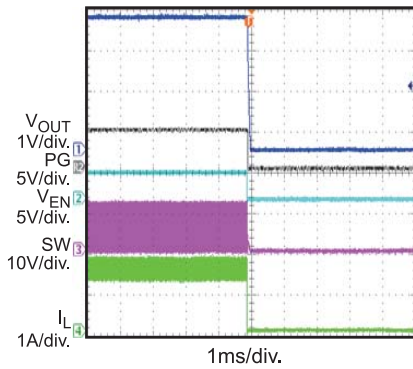
## EVB TEST RESULTS (continued)

Performance waveforms are tested on the evaluation board.

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 2.2\mu H$ ,  $F_{SW} = 2.2MHz$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

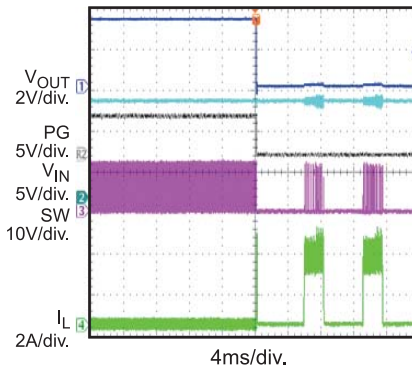
**Shutdown through Enable**

$I_{OUT} = 1.5A$



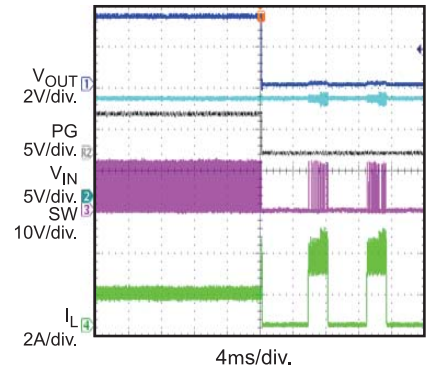
**SCP Entry**

$I_{OUT} = 0A$



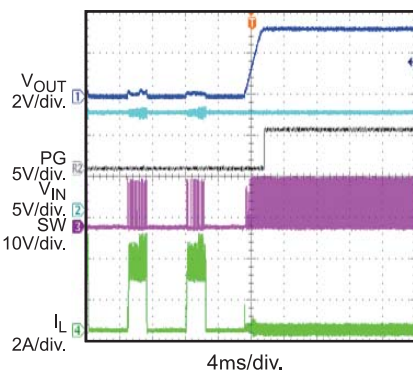
**SCP Entry**

$I_{OUT} = 1.5A$



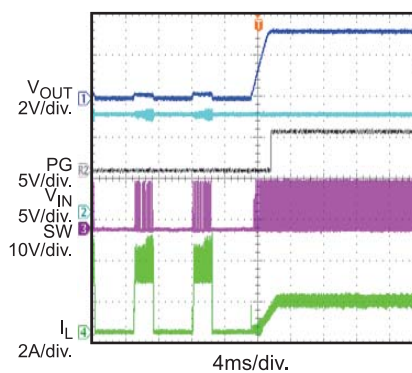
**SCP Recovery**

$I_{OUT} = 0A$

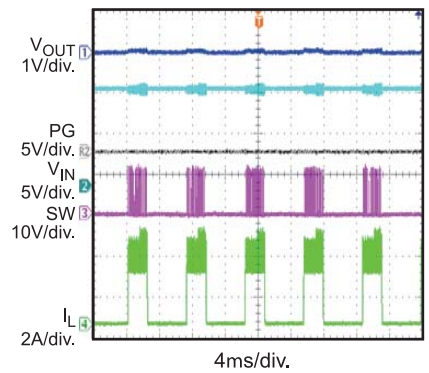


**SCP Recovery**

$I_{OUT} = 1.5A$

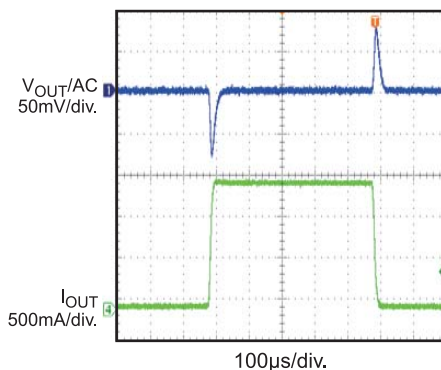


**SCP Steady State**



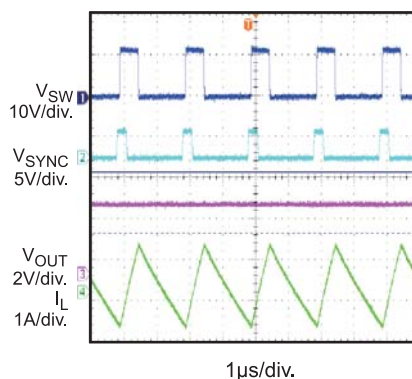
**Load Transient**

$I_{OUT} = 0A-1.5A$



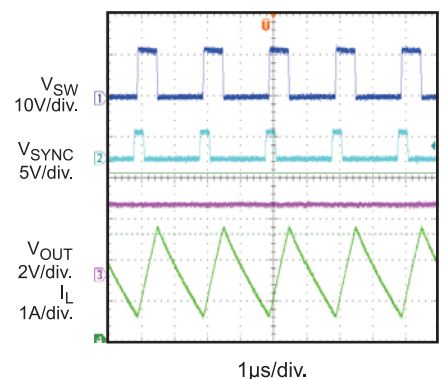
**SYNC Operation**

$f_{SYNC} = 500kHz$ ,  $D = 15\%$ ,  $I_{OUT} = 0A$



**SYNC Operation**

$f_{SYNC} = 500kHz$ ,  $D = 15\%$ ,  $I_{OUT} = 1.5A$





## PRINTED CIRCUIT BOARD LAYOUT

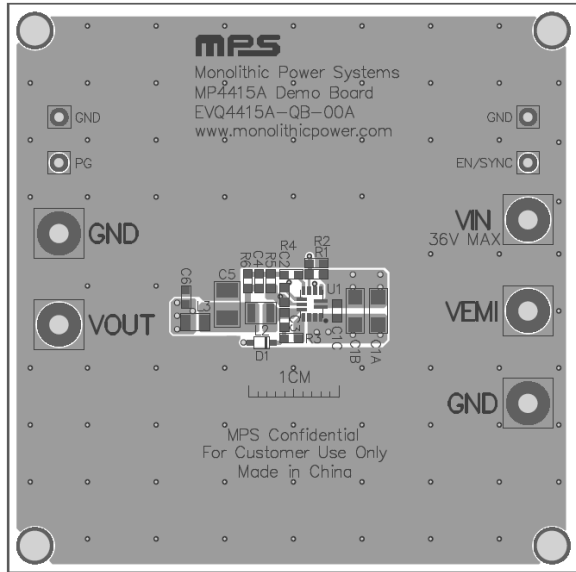


Figure 1: Top Silk Layer and Top Layer

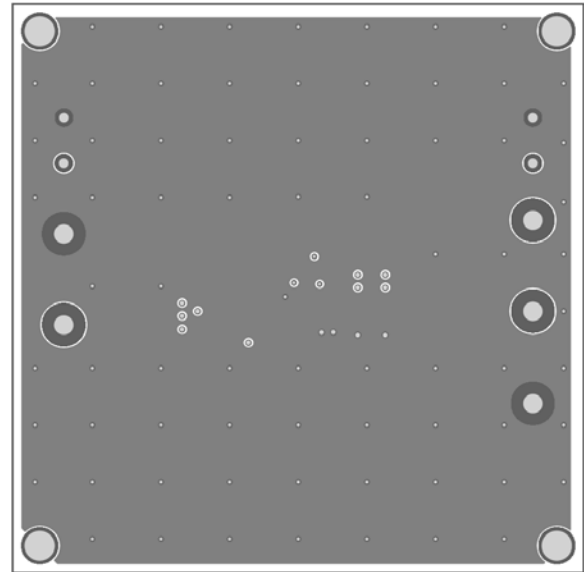


Figure 2: Inner1 Layer

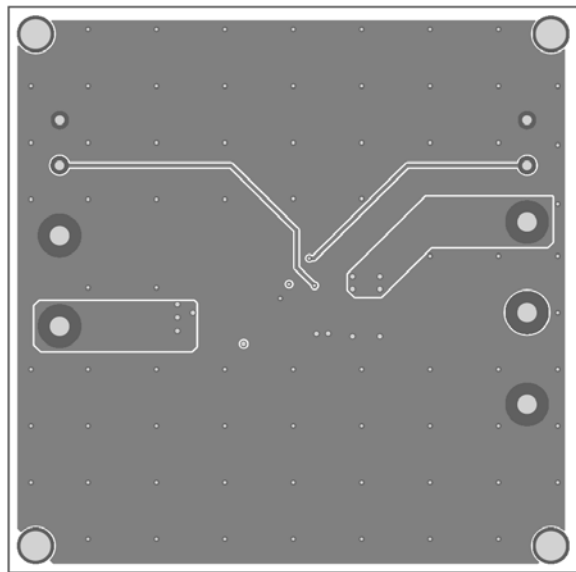


Figure 3: Inner2 Layer

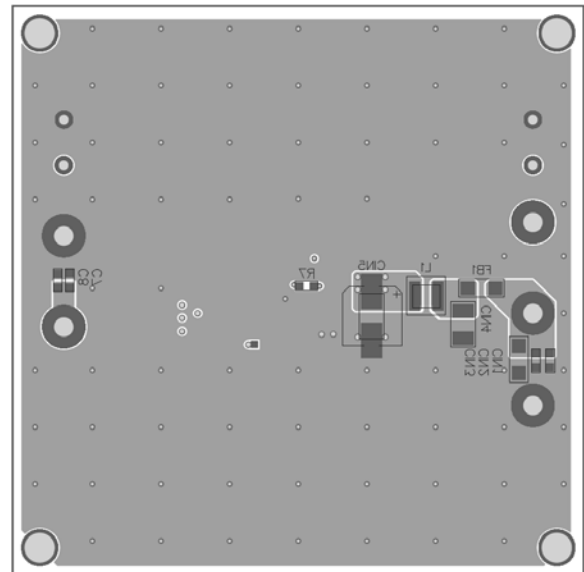


Figure 4: Bottom Silk Layer and Bottom Layer