EZR32HG Wireless MCUs
EZR32HG320 Data Sheet

EZR32HG320 Wireless MCU family with ARM Cortex-M0+ CPU, USB, and sub-GHz Radio

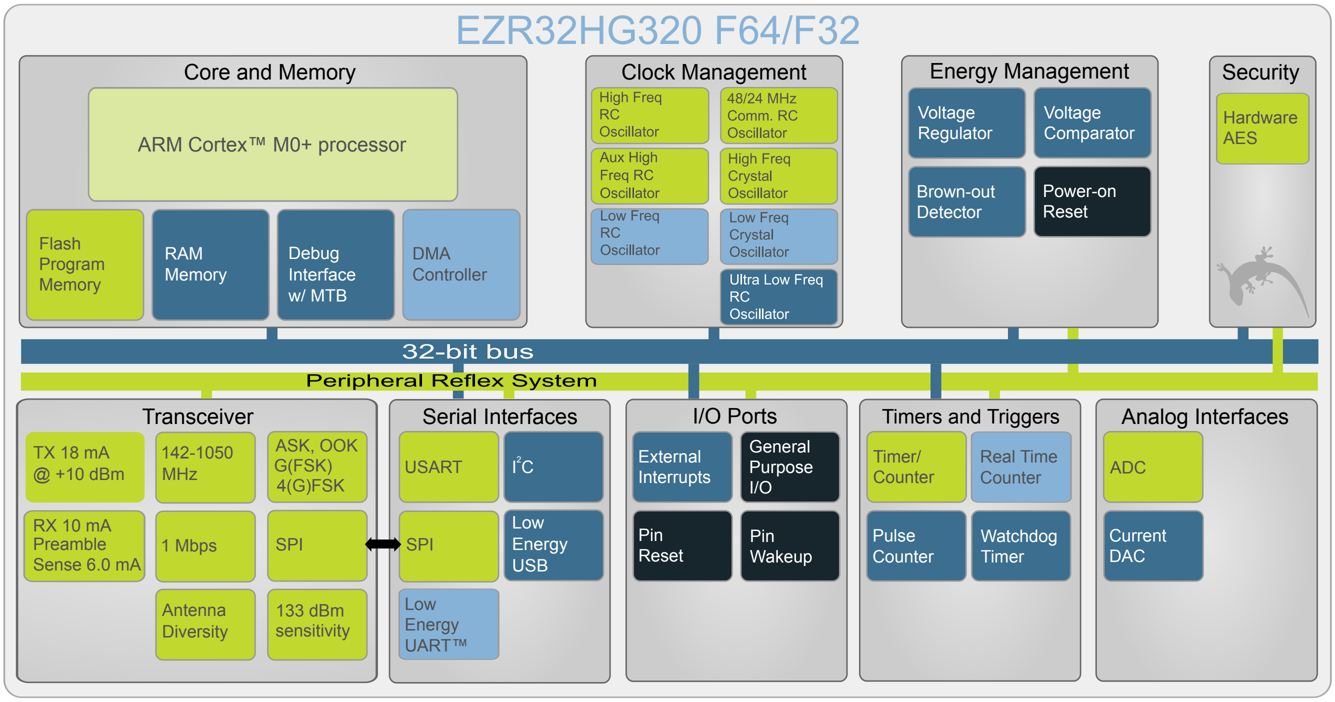
The EZR32HG Wireless MCUs are the latest in Silicon Labs family of wireless MCUs delivering a high performance, low-energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit MCU, the EZR32HG family provides designers the ultimate in flexibility with a family of pin-compatible devices that scale with 64/32 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times of the Silicon Labs energy friendly 32-bit MCUs, combined with the low transmit and receive power consumption of the sub-GHz radio, result in a solution optimized for battery powered applications.

32-Bit ARM Cortex wireless MCUs applications include the following:

- Energy, gas, water and smart metering
- Health and fitness applications
- Consumer electronics
- Alarm and security systems
- Building and home automation

KEY FEATURES

- Silicon Labs' energy efficient 32-bit Wireless MCUs
- Based on ARM Cortex M0 CPU core with 64 kB of flash and 8 kB RAM
- Best-in-class RF performance with EZradio and EZRadioPro transceivers
- Ultra-low power wireless MCU
  - Low transmit and receive currents
  - Ultra-low power standby and sleep modes
  - Fast wake-up time
- Rich set of peripherals including 12-bit ADC and IDAC, multiple communication interfaces (USB, UART, SPI, I2C), multiple GPIO and timers
- AES Accelerator with 128-bit keys



1. Feature List

The HG highlighted features are listed below.

MCU Features

- ARM Cortex-M0+ CPU platform
  - Up to 25 MHz
  - 64/32 kB Flash w/8 kB RAM
  - Hardware AES with 128-bit keys
- Flexible Energy Management System
  - 20 nA @ 3 V Shutoff Mode
  - 0.6 µA @ 3 V Stop Mode
  - 127 µA/MHz @ 3 V Run Mode
- Timers/Counters
  - 3× Timer/Counter
  - 3×3 Compare/Capture/PWM channels
  - Real-Time Counter
  - 16/8-bit Pulse Counter
  - Watchdog Timer
- Communication interfaces
  - 1× USART (UART/SPI)
  - 1× Low Energy UART
  - 1× I2C Interface with SMBus support
  - Universal Serial Bus (USB)
- Ultra low power precision analog peripherals
  - 12-bit 1 Msamples/s ADC
  - On-chip temperature sensor
  - Current Digital to Analog Converter
- Up to 25 General Purpose I/O pins

RF Features

- Frequency Range
  - 142-1050 MHz
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK, OOK
- Receive sensitivity up to -133 dBm
- Up to +20 dBm max output power
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
  - 6 mA @ 1.2 kbps (Preamble Sense)
- Data rate = 100 bps to 1 Mbps
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- IEEE 802.15.4g compliant

System Features

- Power-on Reset and Brown-Out Detector
- Debug Interface
- Temperature range -40 to 85 °C
- Single power supply 1.98 to 3.8 V
- QFN48 package

2. Ordering Information

The table below shows the available EZR32HG320 devices.

Table 2.1. Ordering Information

Ordering	Radio	Flash (kB)	RAM (kB)	Power Amplifier (dBm)	Max Sensitivity (dBm)	Supply Voltage (V)	Package
EZR32HG320FxxR55G-C0	EZRadio	32-64	8	+13	-116	1.98 - 3.8	QFN48
EZR32HG320FxxR60G-C0	EZRadioPro	32-64	8	+13	-126	1.98 - 3.8	QFN48
EZR32HG320FxxR61G-C0	EZRadioPro	32-64	8	+16	-126	1.98 - 3.8	QFN48
EZR32HG320FxxR63G-C0	EZRadioPro	32-64	8	+20	-126	1.98 - 3.8	QFN48
EZR32HG320FxxR67G-C0	EZRadioPro	32-64	8	+13	-133	1.98 - 3.8	QFN48
EZR32HG320FxxR68G-C0	EZRadioPro	32-64	8	+20	-133	1.98 - 3.8	QFN48
EZR32HG320FxxR69G-C0	EZRadioPro	32-64	8	+13 & 20	-133	1.98 - 3.8	QFN48

Table 2.2. Flash Sizes

Example Part Number	Flash Size
EZR32HG320F32R55G	32 kB
EZR32HG320F64R55G	64 kB

Note: Add an "(R)" at the end of the device part number to denote tape and reel option.

Visit www.silabs.com for information on global distributors and representatives.

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3. System Overview

3.1 Introduction

The EZR32HG320 Wireless MCUs are the latest in the Silicon Labs family of wireless MCUs delivering a high-performance, low-energy wireless solution integrated into a small form factor package. By combining a high performance sub-GHz RF transceiver with an energy efficient 32-bit ARM Cortex-M0+, the EZR32HG family provides designers with the ultimate in flexibility with a family of pin-compatible parts that scale from 32 to 64 kB of flash and support Silicon Labs EZRadio or EZRadioPRO transceivers. The ultra-low power operating modes and fast wake-up times combined with the low transmit and receive power consumption of the sub-GHz radio result in a solution optimized for low power and battery powered applications. For a complete feature set and in-depth information on the modules, refer to the EZR32HG Reference Manual.

The EZR32HG320 block diagram is shown below.

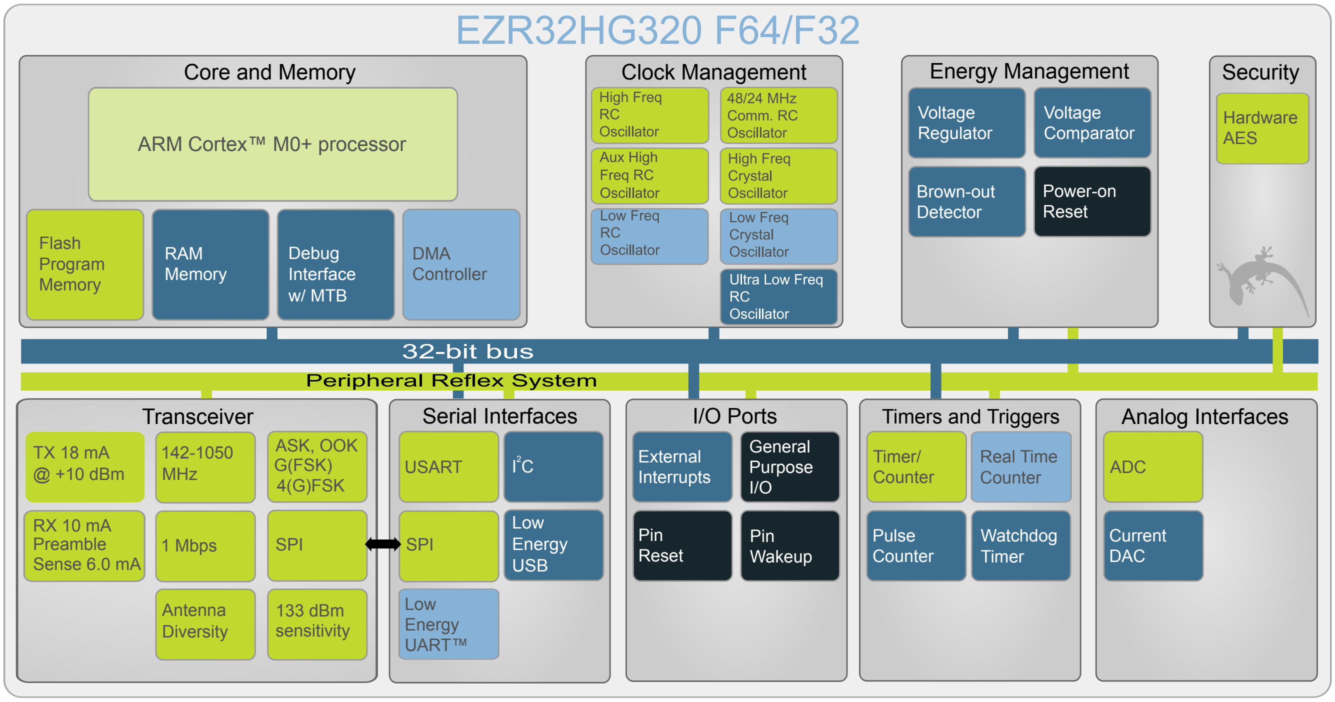


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EZR32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

3.1.2 Debugging Interface (DBG)

These devices include hardware debug support through a 2-pin serial-wire debug interface.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EZR32HG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks: the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

3.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving, for instance, data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μDMA controller licensed from ARM.

3.1.5 Reset Management Unit (RMU)

The Reset Management Unit (RMU) is responsible for handling the reset functionality of the EZR32HG.

3.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manages all the low energy modes (EM) in EZR32HG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

3.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EZR32HG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

3.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may, for example, be caused by an external event, such as an ESD pulse, or by a software failure.

3.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

3.1.10 Universal Serial Bus Controller (USB)

The USB is a full-speed USB 2.0 compliant device controller. The device supports both fullspeed (12 MBit/s) and low speed (1.5 MBit/s) operation. The USB also supports a Low Energy Mode that can be used to lower the current consumption up to 90% by shutting off the clock to the USB Core adn possibly suspending the USHFRCO. The USB device includes an internal dedicated Descriptor-Based Scatter/Garther DMA and supports up to 3 OUT endpoints and 3 IN endpoints, in addition to endpoint 0.

3.1.11 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.12 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

3.1.13 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note *AN0042* is pre-programmed in the device at the factory. The bootloader enables users to program the EZR32 through a UART or a USB CDC class virtual UART without the need for a debuger. The autobaud feature, interface, and commands are described further in the application note.

3.1.14 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique Low Energy Universal Asynchronous Receiver/Transmitter (LEUART™), the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.15 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.16 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator (VCMP) is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.19 Analog to Digital Converter (ADC)

The Analog to Digital Converter (ADC) is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

3.1.20 Current Digital to Analog Converter (IDAC)

The current digital to analog converter (IDAC) can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

3.1.21 Advanced Encryption Standard Accelerator (AES)

The Advanced Encryption Standard Accelerator (AES) performs AES encryption and decryption with 128-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations (i.e., 8- or 16-bit operations are not supported).

3.1.22 General Purpose Input/Output (GPIO)

In the EZR32HG320, there are 25 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

3.1.23 EZRadio® and EZRadioPro® Transceivers

The EZR32HG family of devices is built using high-performance, low-current EZRadio and EZRadioPro RF transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. These devices offer outstanding sensitivity of up to –133 dBm (using EZRadioPro) while achieving extremely low active and standby current consumption. The EZR32HG devices using the EZRadioPro transceiver offer frequency coverage in all major bands and include optimal phase noise, blocking, and selectivity performance for narrow band and licensed band applications, such as FCC Part 90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The active mode TX current consumption of 18 mA at +10 dBm and RX current of 10 mA coupled with extremely low standby current and fast wake times is optimized for extended battery life in the most demanding applications. The EZR32HG devices can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, and ARIB. All devices using the EZRadioPRO tranceiver are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be programmed and configured via Simplicity Studio, available at www.silabs.com.

Communications between the radio and MCU are done over USART and IRQ, which requires the pins to be configured in the following way:

Table 3.1. Radio MCU Communication Configuration

EZR32HG MCU	RF	EZR32HG Function Assignment
PA2	SDN	GPIO Output
PC0	$_n$SEL	US1_CS #5
PC1	SDI	US1_MOSI #5
PC2	SDO	US1_MISO #5
PC3	SCLK	US1_CLK #5
PC4	$_n$IRQ	GPIO_EM4WU6 (GPIO Input with IRQ enabled)

3.1.23.1 EZRadio and EZRadioPRO Transceivers GPIO Configuration

The EZRadio and EZRadioPRO Transceivers have 4 General Purpose Digital I/O pins. These GPIOs may be configured to perform various radio-specific functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.

3.2 Configuration Summary

The features of the EZR32HG320 are a subset of the feature set described in the *EZR32HG Reference Manual*. The table below describes device specific implementation of the features.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_CLK0, CMU_CLK1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
UART0	Full configuration with IrDA and I2S	US0_TX, US0_RX, US0_CLK, US0_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
USARTRF1	Reduced configuration	USRF1_RX, USRF1_TX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7, 6, 5, 4, 1, 0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA
GPIO	25 pins	Available pins are shown in 5.4 GPIO Pinout Overview

3.3 Memory Map

The EZR32HG320 memory map is shown below with RAM and flash sizes for the largest memory configuration.

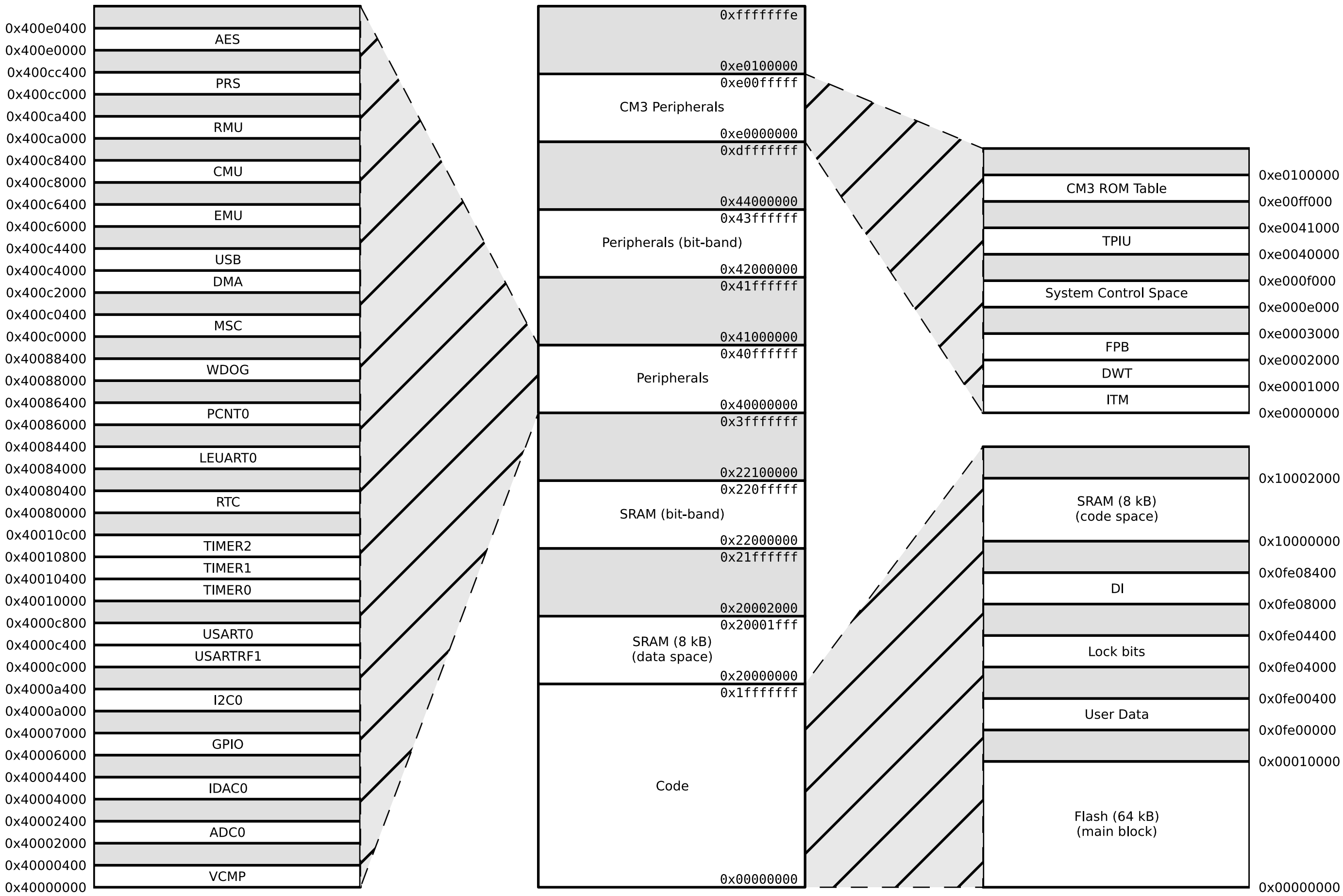


Figure 3.2. EZR32HG320 Memory Map with Largest RAM and Flash Sizes

4. Electrical Specifications

4.1 Test Conditions

4.1.1 Typical Values

The typical data are based on T_{AMB} = 25°C and V_{DD} = 3.0 V, as defined in Table 4.3 General Operating Conditions on page 14, by simulation and/or technology characterisation unless otherwise specified.

4.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 4.3 General Operating Conditions on page 14, by simulation and/or technology characterisation unless otherwise specified.

4.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in the table below may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 4.3 General Operating Conditions on page 14.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-55	—	150[1]	°C
Maximum soldering temperature	T_S	Latest IPC/JEDEC J-STD-020 Standard	—	—	260	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
Voltage on any I/O pin	V_{IOPIN}		-0.3	—	V_{DD}+0.3	V

Note:

1. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.3 Thermal Characteristics

Table 4.2. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}		-40	—	85	°C
Junction temperature value	T_J		—	—	105[1]	°C
Thermal impedance junction to ambient	TI_{JA}	+13/+16 dBm on 2-layer board	—	—	61.8	°C/W
		+20 dBm on 4-layer board	—	—	20.7[2]	°C/W
Storage temperature range	T_{STG}		-55	—	150	°C

Note:
1. Values are based on simulations run on 2-layer and 4-layer PCBs at 0m/s airflow.
2. Based on programmed devices tested for 10000 hours at 150 ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

4.4 General Operating Conditions

Table 4.3. General Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature range	T_{AMB}	-40	—	85	°C
Operating supply voltage	V_{DDOP}	1.98	—	3.8	V
Internal APB clock frequency	f_{APB}	—	—	4825	MHz
Internal AHB clock frequency	f_{AHB}	—	—	4825	MHz

4.5 Current Consumption

Table 4.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash.	24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	148	158	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	153	163	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	161	172	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	163	174	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	127	137	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	129	139	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	131	140	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	134	143	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	137	145	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	136	144	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	139	148	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	142	150	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	146	154	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	184	196	µA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	194	208	µA/MHz

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EM1}	EM1 current	24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C	—	64	68	µA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	67	71	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	85	91	µA/MHz
		24 MHz USHFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	86	92	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	51	55	µA/MHz
		24 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	52	56	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	53	57	µA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	54	58	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	56	59	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	57	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	58	61	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	59	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	64	68	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	67	71	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	106	114	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	114	126	µA/MHz
I_{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} = 25°C	—	0.9	1.35	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} = 85°C	—	1.6	3.50	µA
I_{EM3}	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD} = 3.0 V, T_{AMB} = 25°C	—	0.6	0.90	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V_{DD} = 3.0 V, T_{AMB} = 85°C	—	1.2	2.65	µA
I_{EM4}	EM4 current	V_{DD} = 3.0 V, T_{AMB} = 25°C	—	0.02	0.035	µA
		V_{DD} = 3.0 V, T_{AMB} = 85°C	—	0.18	0.480	µA

4.5.1 EM0 Current Consumption

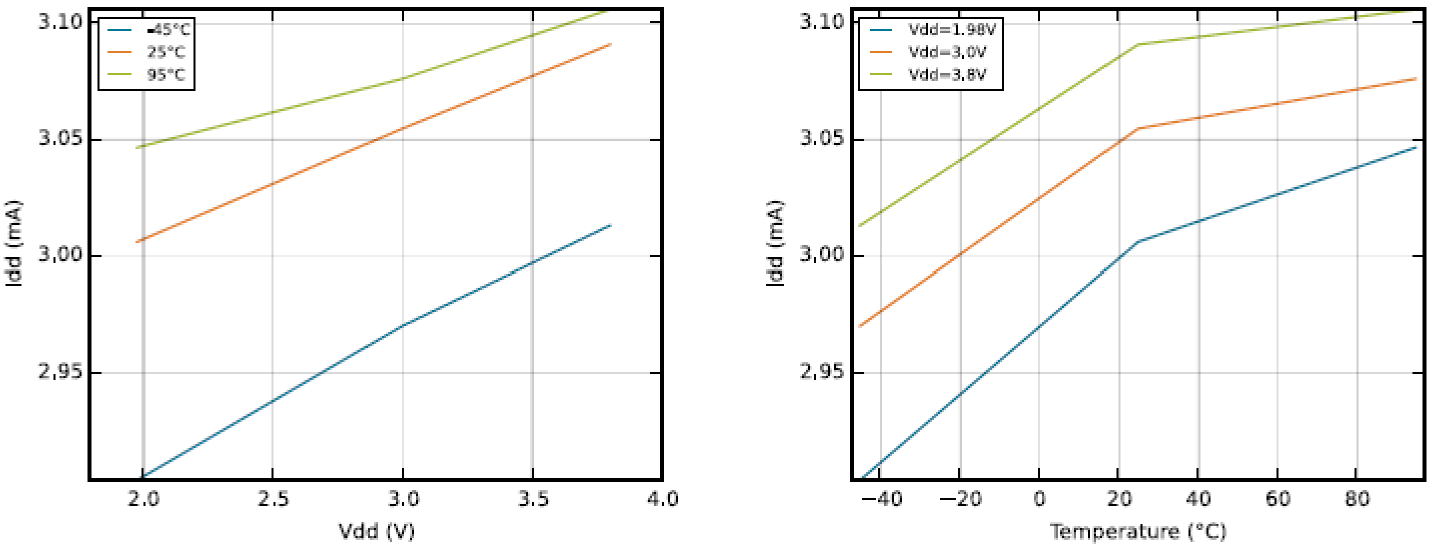


Figure 4.1. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 24 MHz

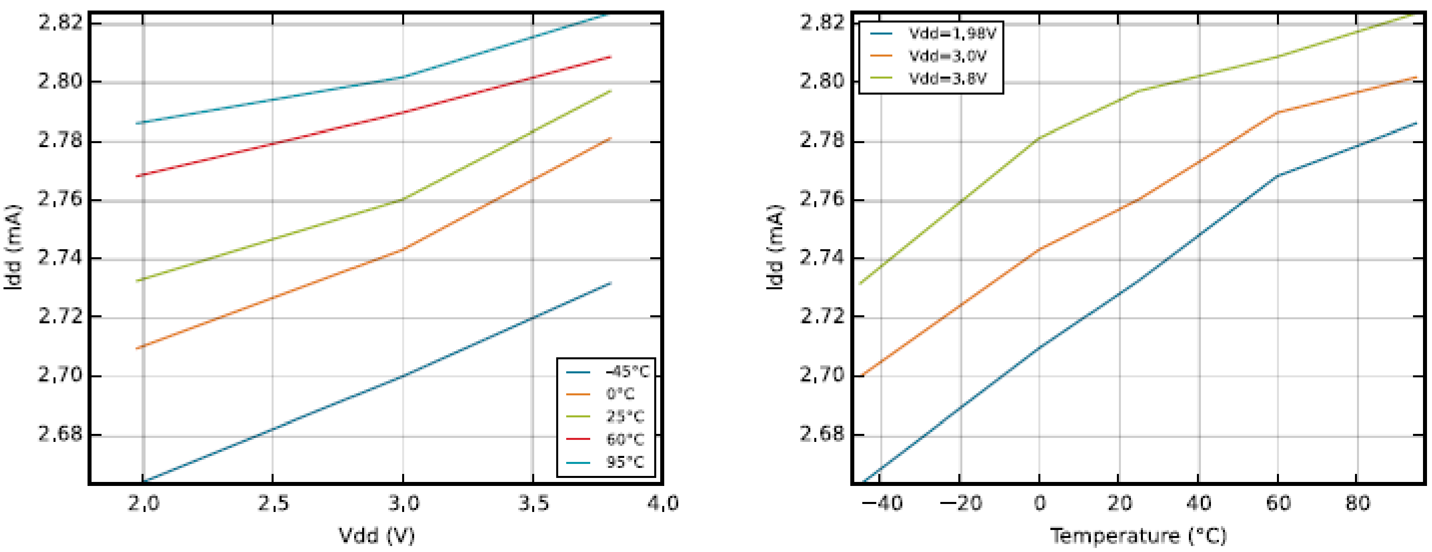


Figure 4.2. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 21 MHz

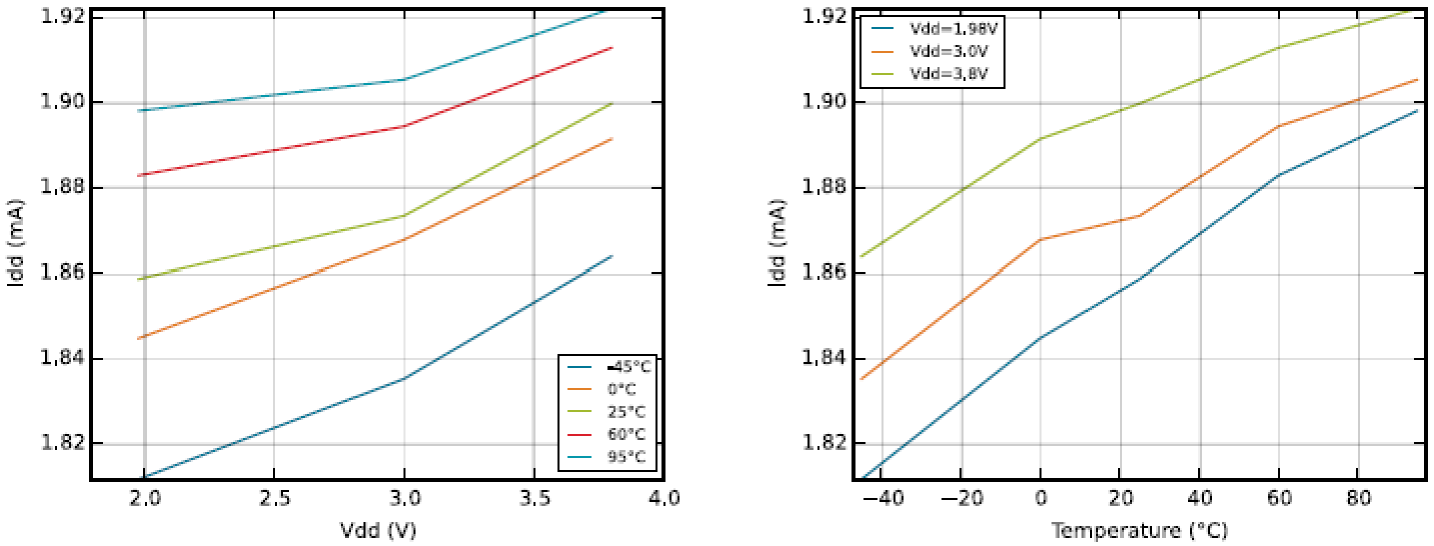


Figure 4.3. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 14 MHz

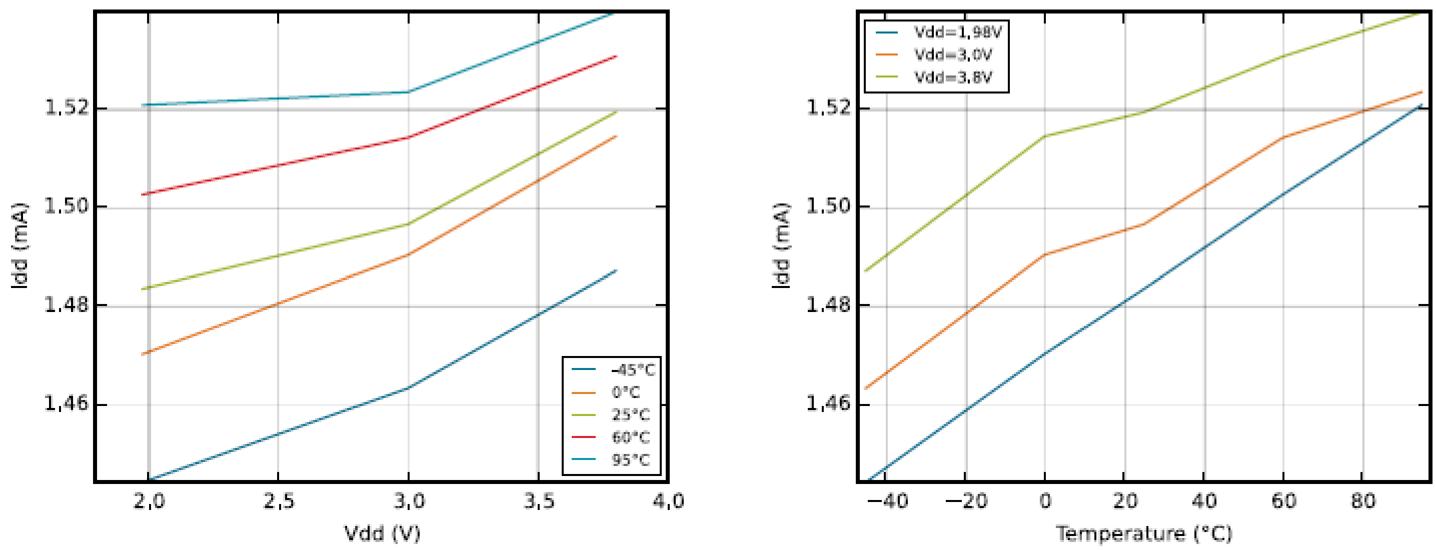


Figure 4.4. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 11 MHz

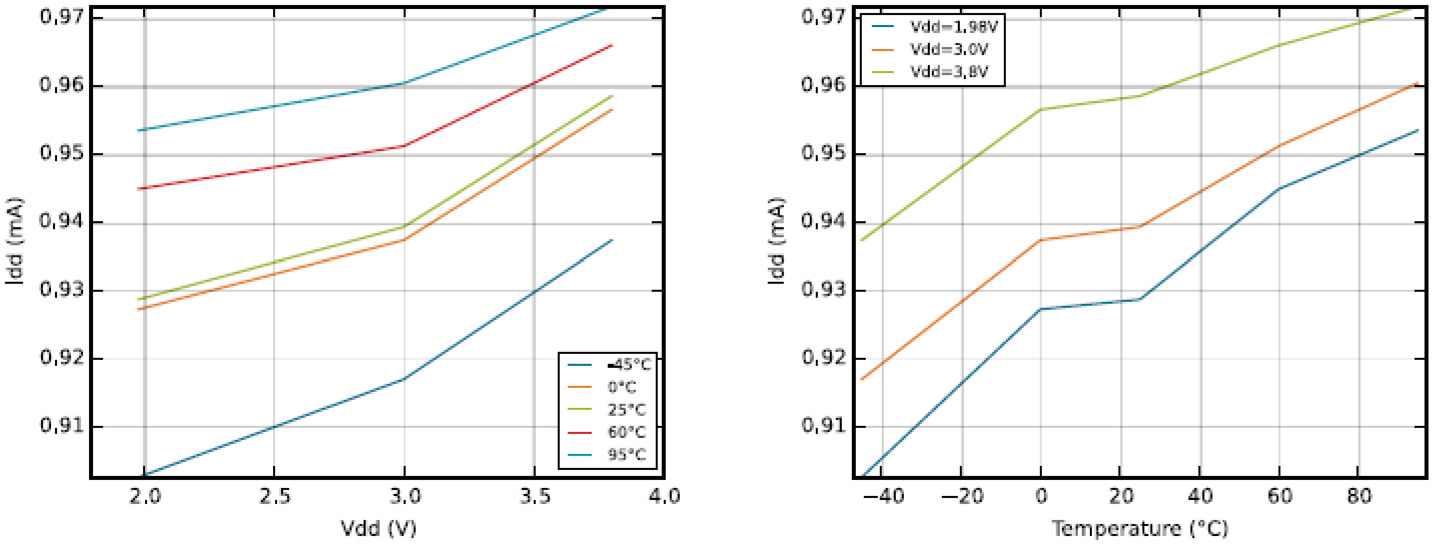


Figure 4.5. EM0 Current Consumption while Executing Prime Number Calculation Code from Flash with HFRCO Running at 6.6 MHz

4.5.2 EM1 Current Consumption

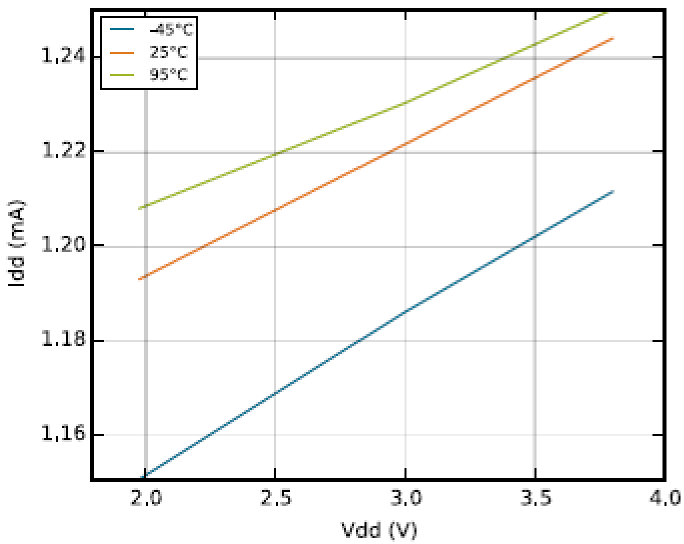


Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 24 MHz

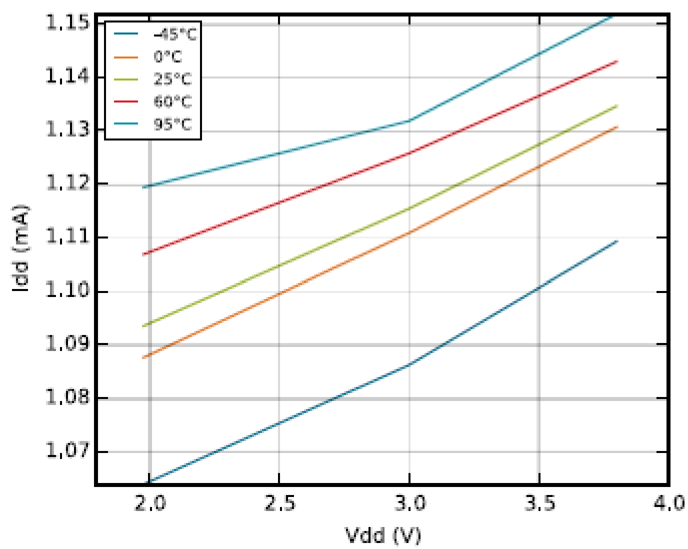


Figure 4.7. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 21 MHz

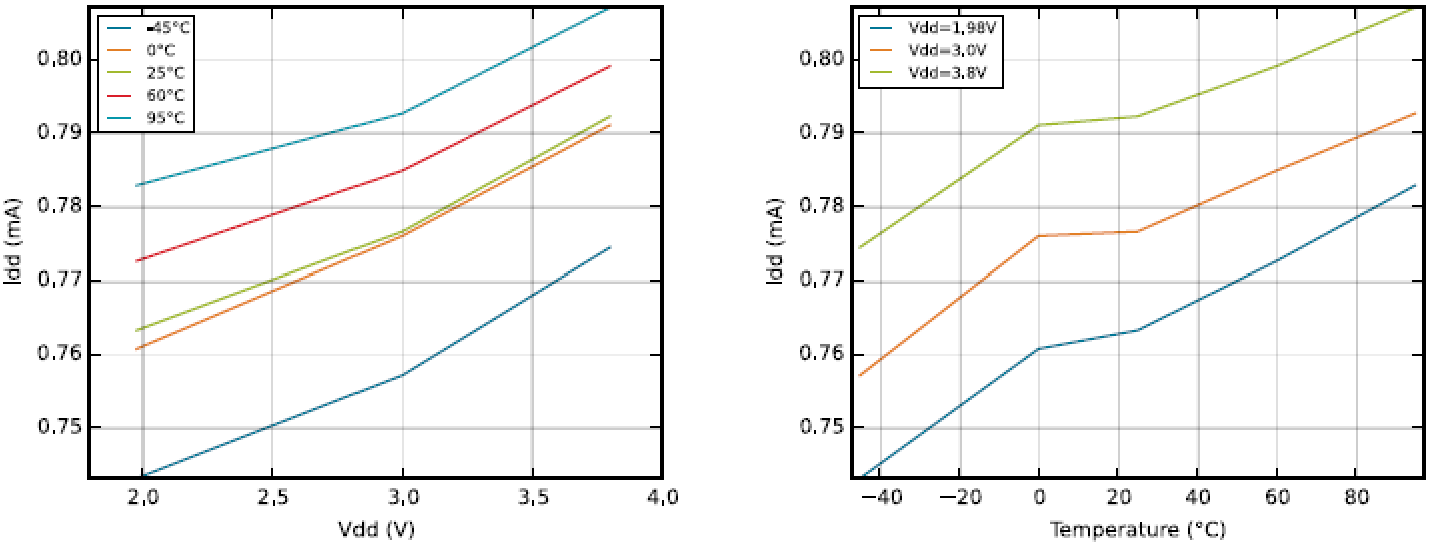


Figure 4.8. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 14 MHz

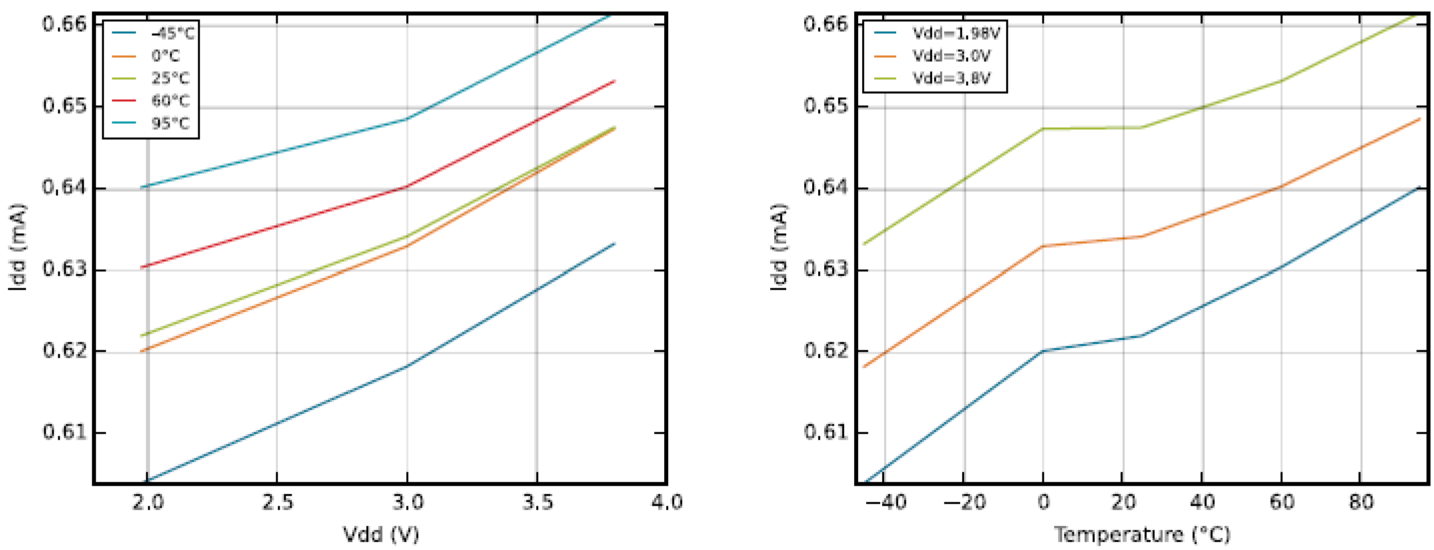


Figure 4.9. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz

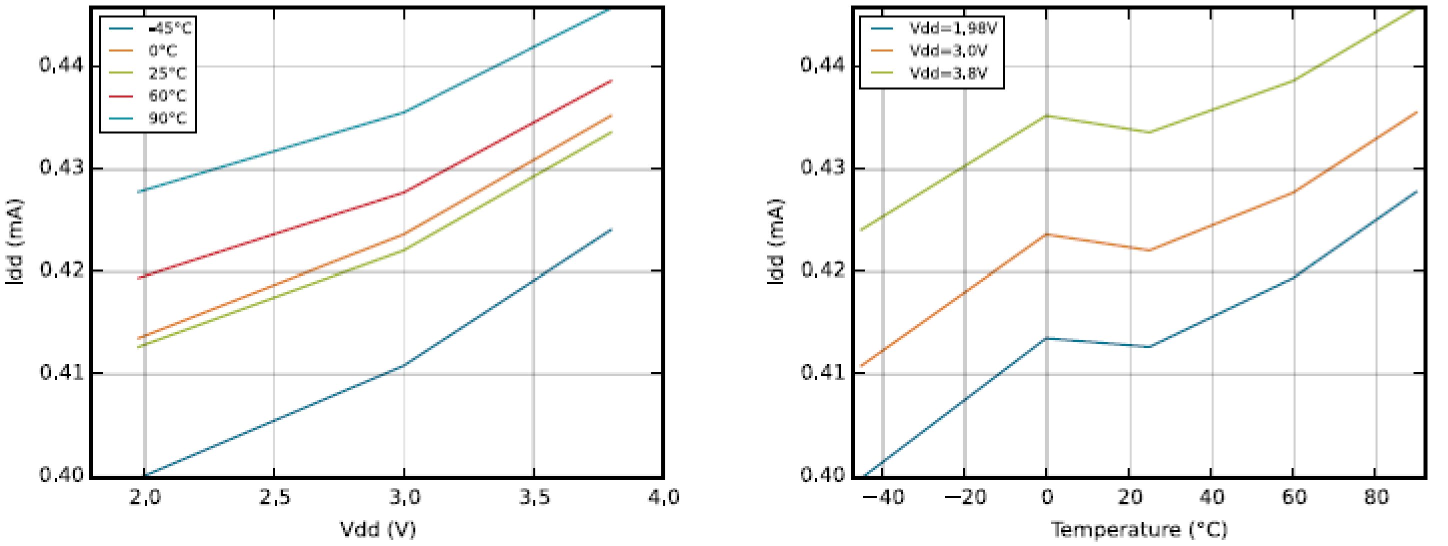


Figure 4.10. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz

4.5.3 EM2 Current Consumption

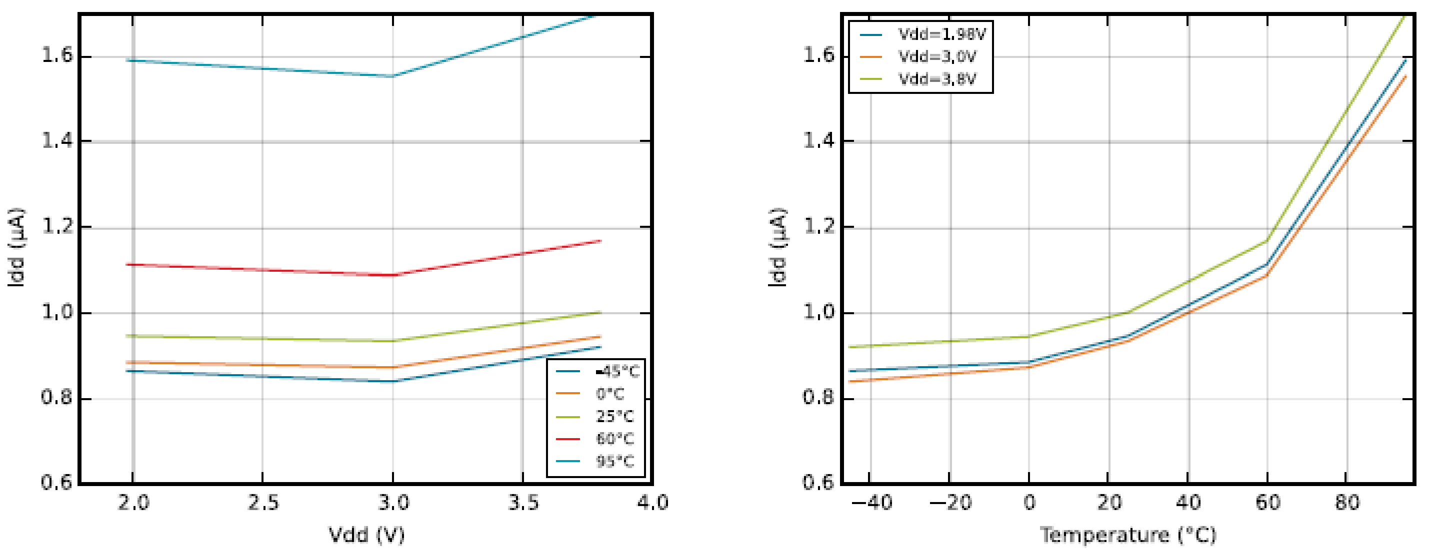


Figure 4.11. EM2 Current Consumption, RTC Prescaled to 1 kHz, 32.768 kHz LFRCO

4.5.4 EM3 Current Consumption

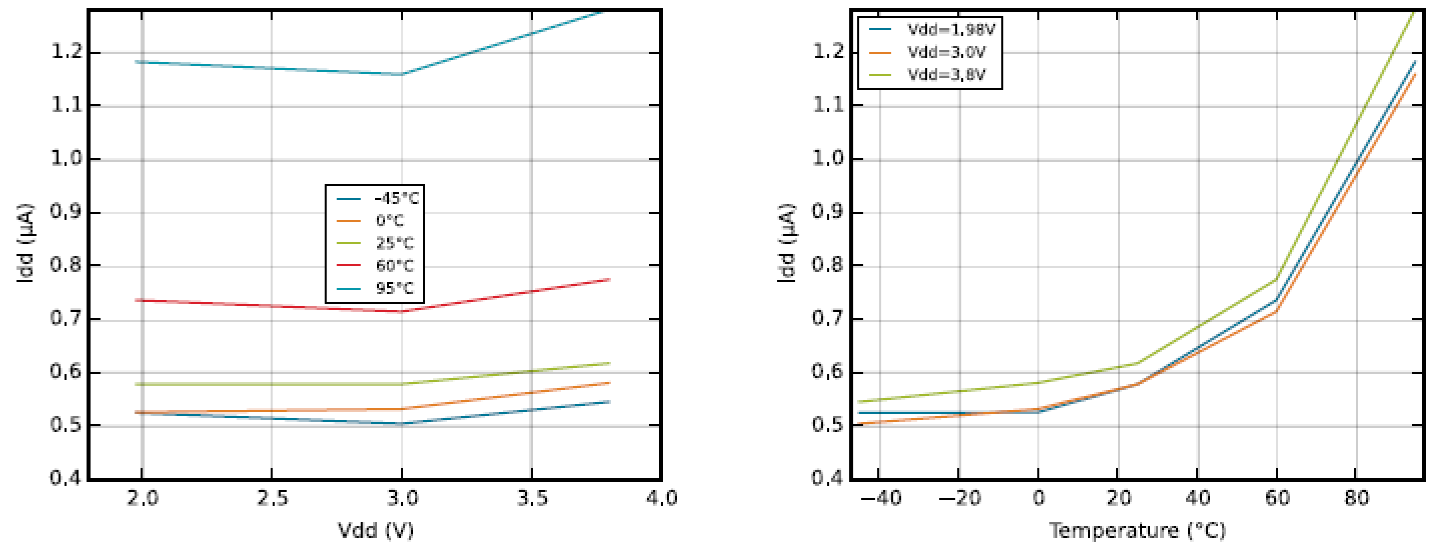


Figure 4.12. EM3 Current Consumption

4.5.5 EM4 Current Consumption

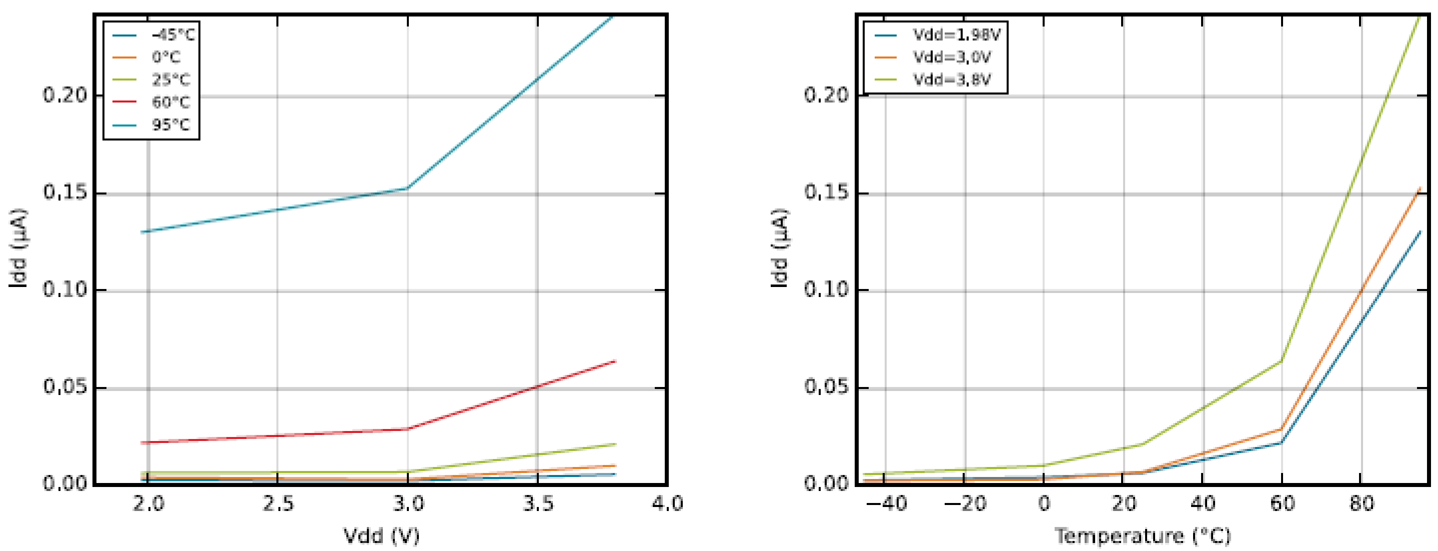


Figure 4.13. EM4 Current Consumption

4.6 Transitions between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.5. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	µs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	µs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	µs

4.7 Power Management

The EZR32HG requires the AVDD_x, VDD_DREG, RFVDD_x and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, see the application note, AN0002.0: EFM32 and EZR32 Wireless MCU Series 0 Hardware Design Considerations.

Table 4.6. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage	EM0	1.74	—	1.96	V
		EM2	1.71	1.86	1.98	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage		—	1.85	—	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	µs
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	µF
C_{USB_VREGO}	USB voltage regulator out decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND	—	1	—	µF
C_{USB_VREGI}	USB voltage regulator in decoupling capacitor.	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND	—	4.7	—	µF

4.8 Flash

Table 4.7. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:

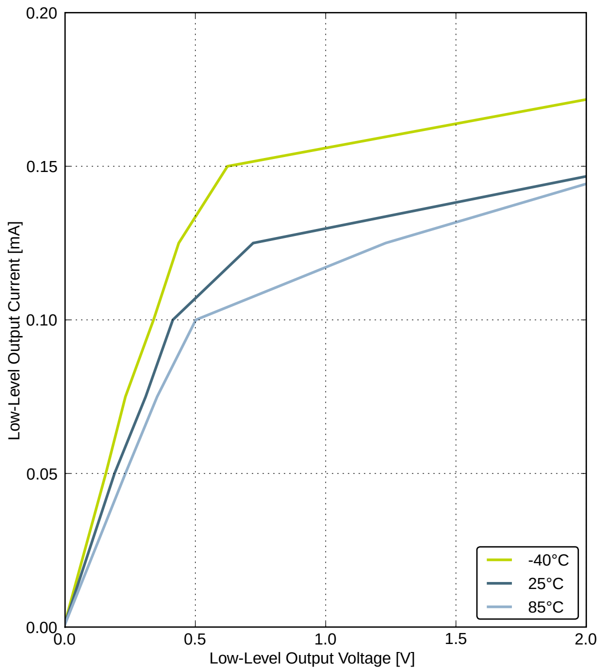
1. Measured at 25 ºC.

4.9 General Purpose Input Output

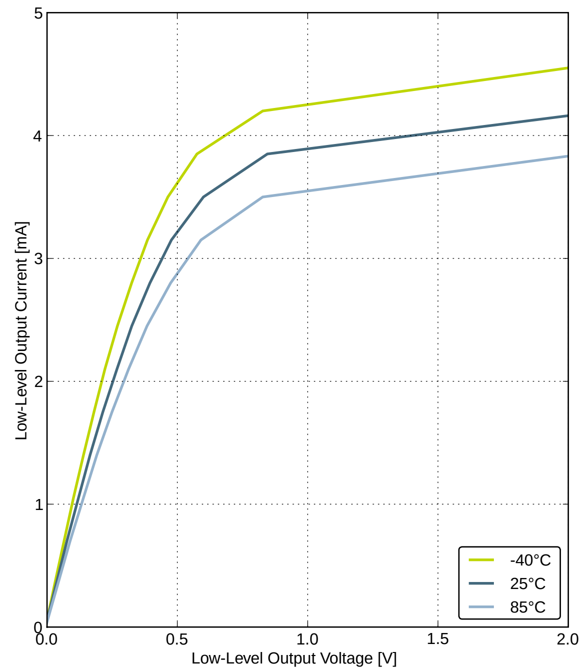
Table 4.8. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	0.30 V_{DD}	V
Input high voltage	V_{IOIH}		0.70 V_{DD}	—	—	V
Output high voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.80 V_{DD}	—	V
		Sourcing 0.1 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.90 V_{DD}	—	V
		Sourcing 1 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.85 V_{DD}	—	V
		Sourcing 1 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.90 V_{DD}	—	V
		Sourcing 6 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75 V_{DD}	—	—	V
		Sourcing 6 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60 V_{DD}	—	—	V
		Sourcing 20 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80 V_{DD}	—	—	V

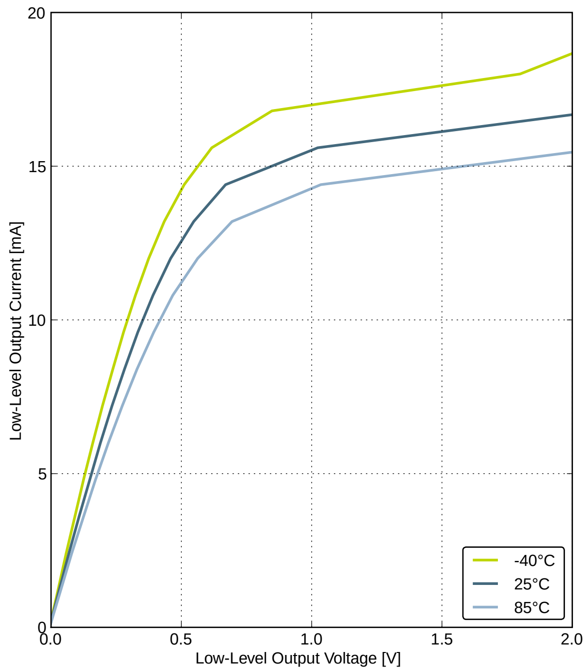
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output low voltage (Production test condition = 3.0 V, DRIVE-MODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.20 V_{DD}	—	V
		Sinking 0.1 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.10 V_{DD}	—	V
		Sinking 1 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW	—	0.05 V_{DD}		V
		Sinking 6 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.30 V_{DD}	V
		Sinking 6 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	0.20 V_{DD}	V
		Sinking 20 mA, V_{DD} = 1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.35 V_{DD}	V
		Sinking 20 mA, V_{DD} = 3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	0.25 V_{DD}	V
Input leakage current	I_{IOLEAK}	High Impedance IO connected to GROUND or Vdd	—	±0.1	±40	nA
I/O pin pull-up resistor	R_{PU}		—	40	—	kΩ
I/O pin pull-down resistor	R_{PD}		—	40	—	kΩ
Internal ESD series resistor	R_{IOESD}		—	200	—	Ω
Pulse width of pulses to be removed by the glitch suppression filter	$t_{IOGLITCH}$		10	—	50	ns
Output fall time	t_{IOOF}	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C_L = 12.5-25 pF.	20+0.1 C_L	—	250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C_L = 350-600 pF	20+0.1 C_L	—	250	ns
I/O pin hysteresis (V_{IOTHR+} - V_{IOTHR-})	V_{IOHYST}	V_{DD} = 1.98 - 3.8 V	0.10 V_{DD}	—	—	V



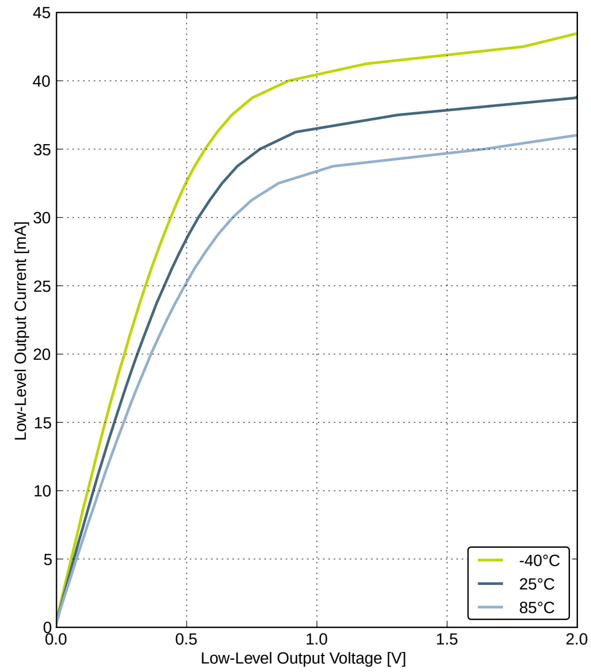
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

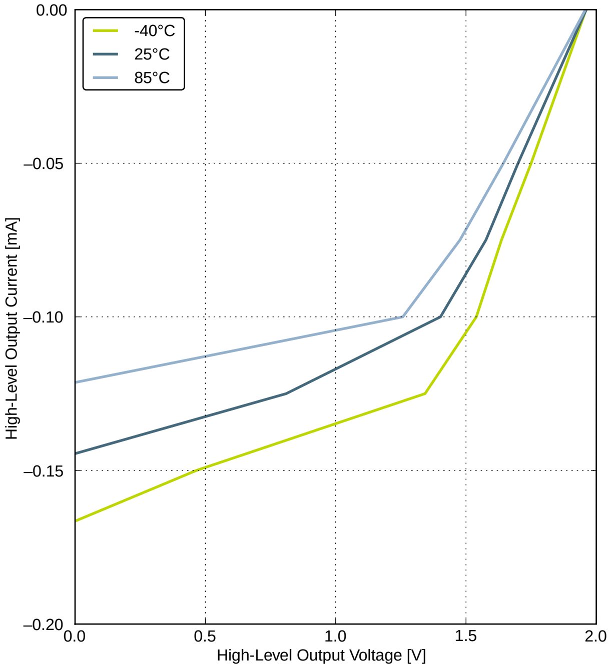


GPIO_Px_CTRL DRIVEMODE = STANDARD

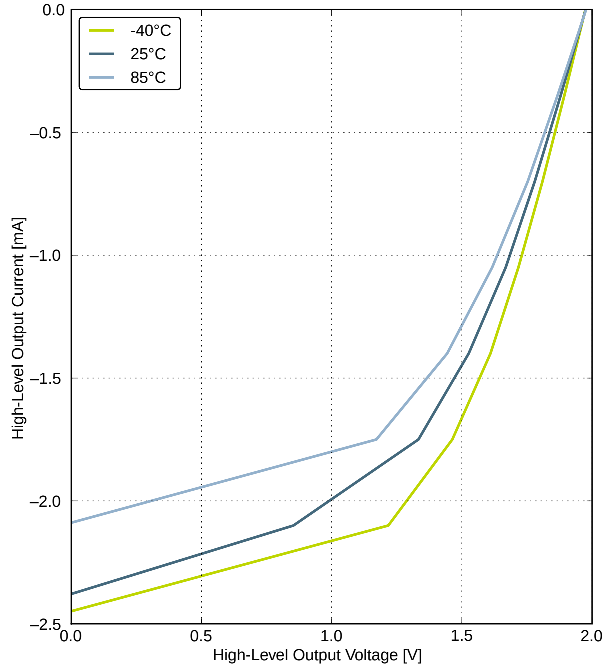


GPIO_Px_CTRL DRIVEMODE = High

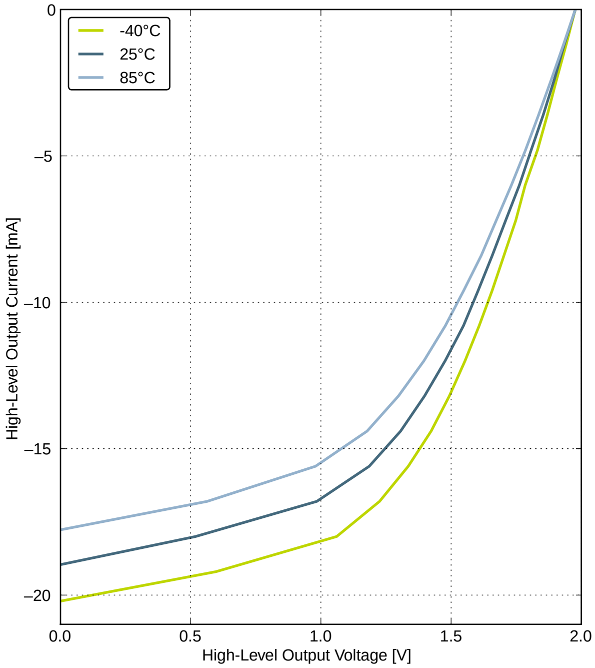
Figure 4.14. Typical Low-Level Output Current, 2 V Supply Voltage



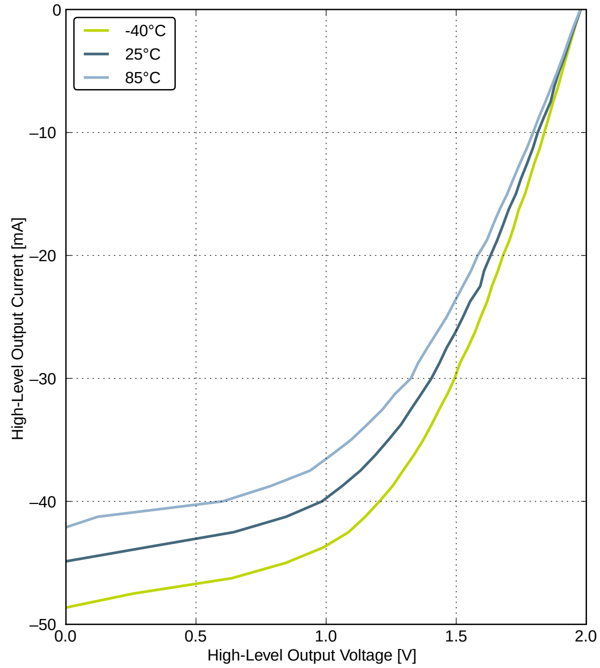
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

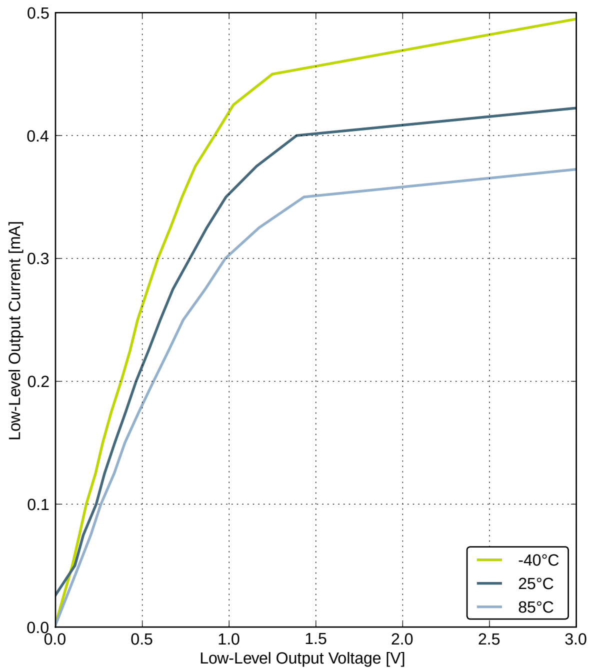


GPIO_Px_CTRL DRIVEMODE = STANDARD

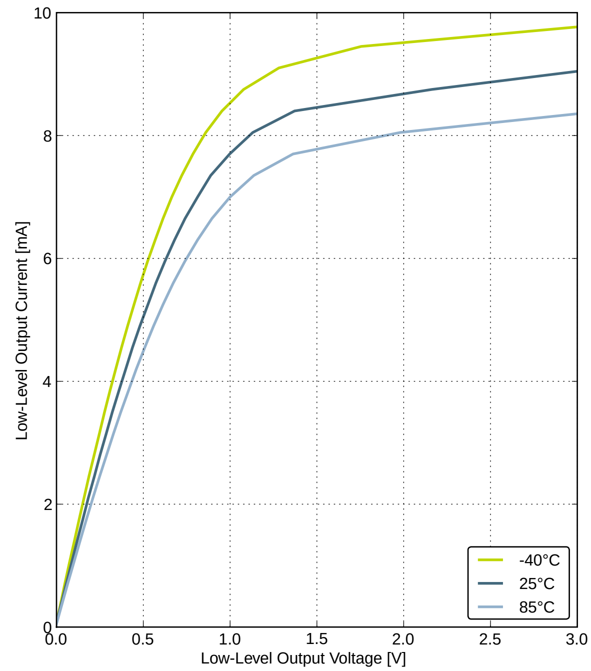


GPIO_Px_CTRL DRIVEMODE = High

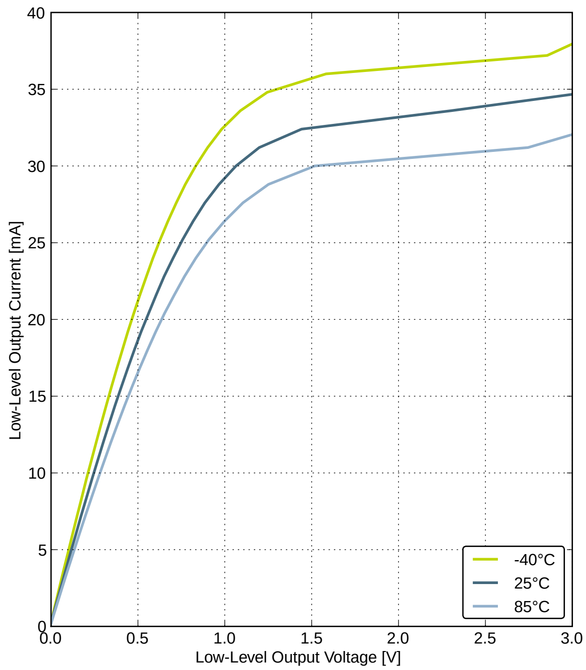
Figure 4.15. Typical High-Level Output Current, 2 V Supply Voltage



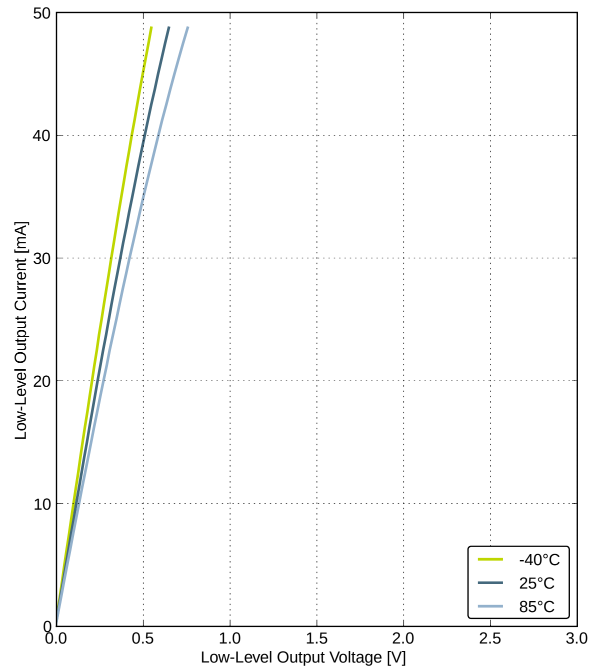
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = High

Figure 4.16. Typical Low-Level Output Current, 3 V Supply Voltage

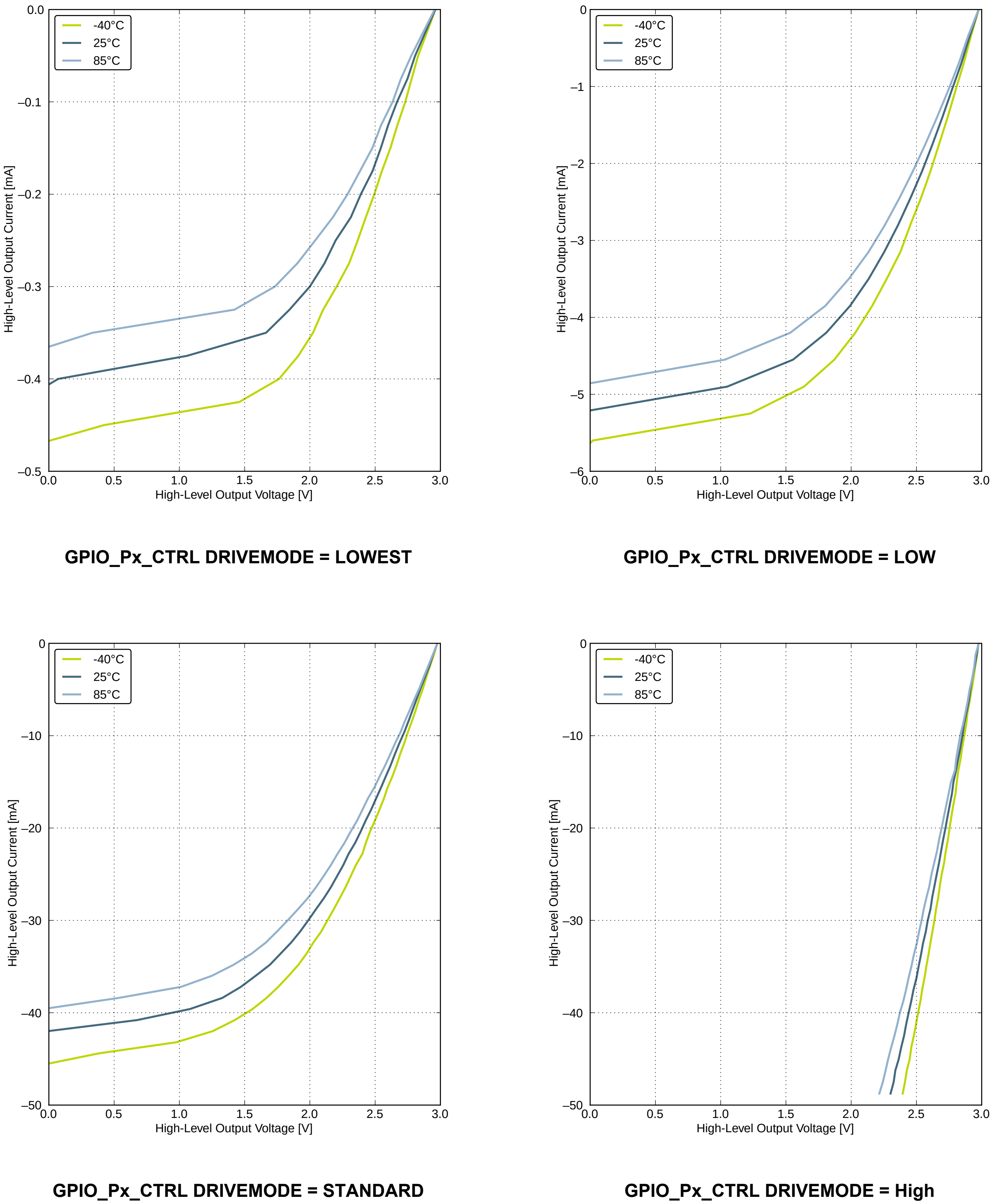
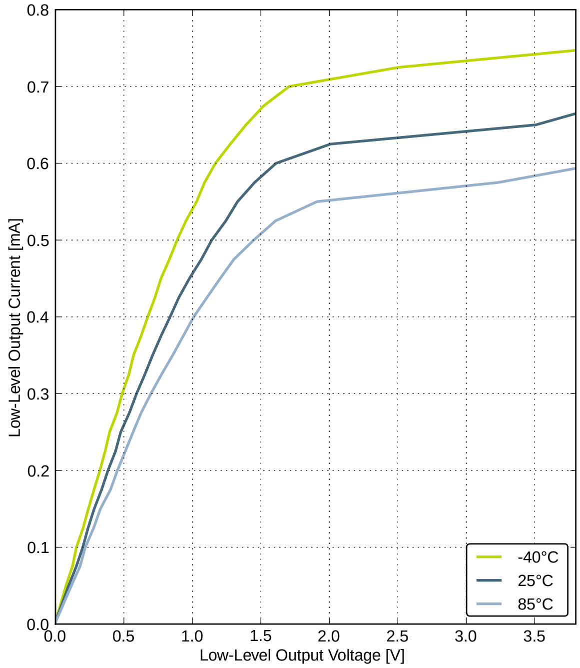
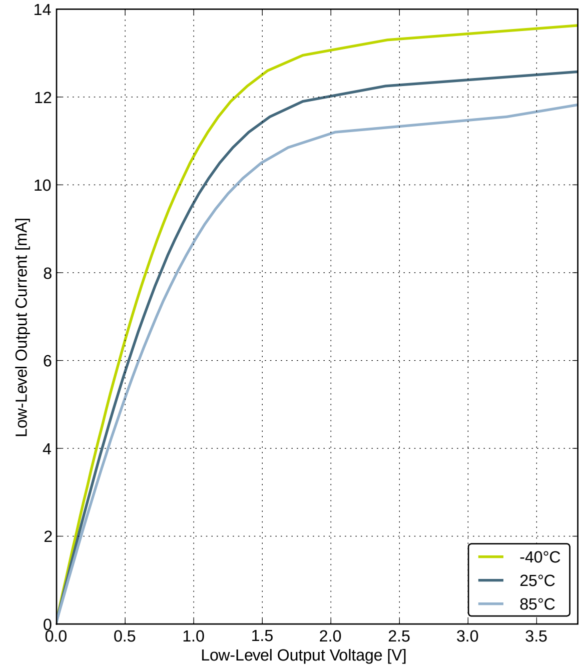


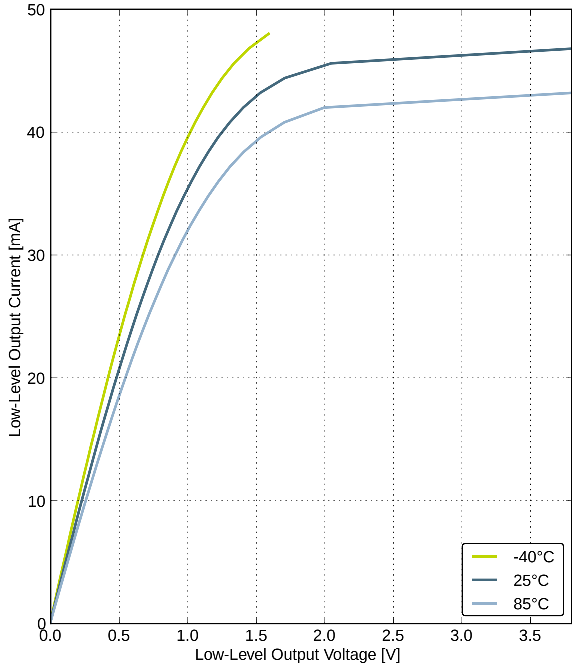
Figure 4.17. Typical High-Level Output Current, 3 V Supply Voltage



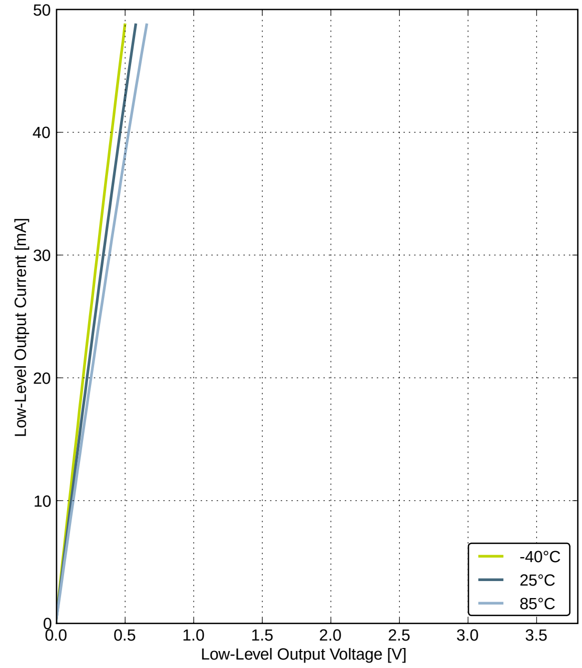
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

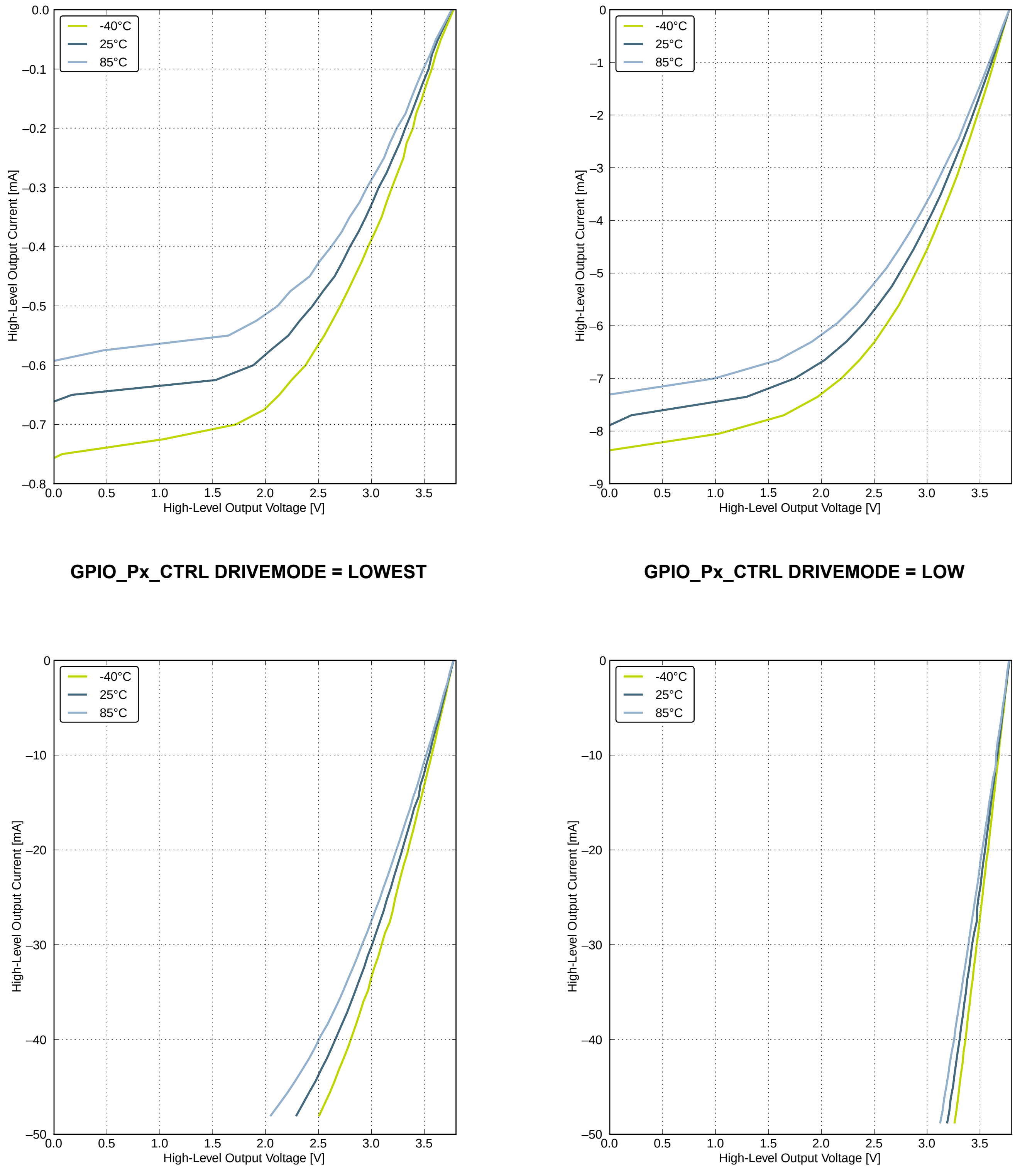


GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = High

Figure 4.18. Typical Low-Level Output Current, 3.8 V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW

GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = High

Figure 4.19. Typical High-Level Output Current, 3.8 V Supply Voltage

4.10 Oscillators

4.10.1 LFXO

Table 4.9. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported nominal crystal frequency	f_{LFXO}		31.3	32.768	34.3	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	30	120	kΩ
Supported crystal external load range	C_{LFXOL}		X[1]5	—	25	pF
Duty cycle	DC_{LFXO}		48	50	53.5	%
Current consumption for core and buffer after startup	I_{LFXO}	ESR=30 kΩ, C_L=10 pF, LFXOBOOST in CMU_CTRL is 1	—	190	—	nA
Start- up time	t_{LFXO}	ESR=30 kΩ, C_L=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1	—	1100	—	ms

Note:

1. See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio.

For safe startup of a given crystal, the Configurator tool in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, refer to application note, AN0016.0: EFM32 Oscillator Design Considerations.

4.10.2 HFXO

Table 4.10. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported frequency, any mode	f_{HFXO}		4	—	25	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 25 MHz	—	30	100	Ω
		Crystal frequency 4 MHz	—	400	1500	Ω
The transconductance of the HFXO input transistor at crystal startup	g_{mHFXO}	HFXOBOOST in CMU_CTRL equals 0b11	20	—	—	ms
Supported crystal external load range	C_{HFXOL}		5	—	25	pF
Current consumption for HFXO after startup	I_{HFXO}	4 MHz: ESR=400 Ohm, C_L=20 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	85	—	µA
		25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	165	—	µA
Startup time	t_{HFXO}	25 MHz: ESR=30 Ohm, C_L=10 pF, HFXOBOOST in CMU_CTRL equals 0b11	—	785	—	µs

4.10.3 LFRCO

Table 4.11. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency , V_{DD}= 3.0 V, T_{AMB}=25 °C	f_{LFRCO}		31.3	32.768	34.3	kHz
Startup time not including software calibration	t_{LFRCO}		—	150	—	µs
Current consumption	I_{LFRCO}		—	361	492	nA
Frequency step for LSB change in TUNING value	$TUNESTEP_{LFRCO}$		—	202	—	Hz

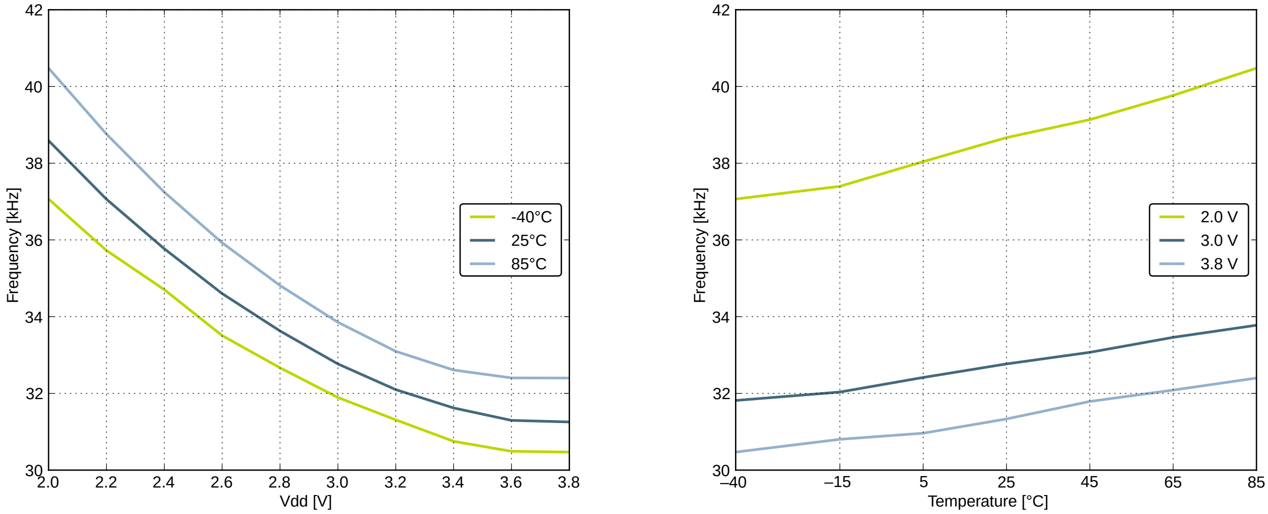


Figure 4.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage

4.10.4 HFRCO

Table 4.12. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, V_{DD} = 3.0 V, T_{AMB} = 25°C	24 MHz frequency band	23.28	24.0	24.72	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{HFRCO\_settling}$	Settling time after start-up	f_{HFRCO} = 14 MHz	—	0.6	—	Cycles
I_{HFRCO}	Current consumption	f_{HFRCO} = 24 MHz	—	158	184	µA
		f_{HFRCO} = 21 MHz	—	143	175	µA
		f_{HFRCO} = 14 MHz	—	113	140	µA
		f_{HFRCO} = 11 MHz	—	101	125	µA
		f_{HFRCO} = 6.6 MHz	—	84	105	µA
		f_{HFRCO} = 1.2 MHz	—	27	40	µA
$TUNESTEP_{HFRCO}$	Frequency step for LSB change in TUNING value	24 MHz frequency band	—	66.8[1]	—	kHz
		21 MHz frequency band	—	52.8[1]	—	kHz
		14 MHz frequency band	—	36.9[1]	—	kHz
		11 MHz frequency band	—	30.1[1]	—	kHz
		7 MHz frequency band	—	18.0[1]	—	kHz
		1 MHz frequency band	—	3.4	—	kHz

Note:

1. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 21 MHz across operating conditions.

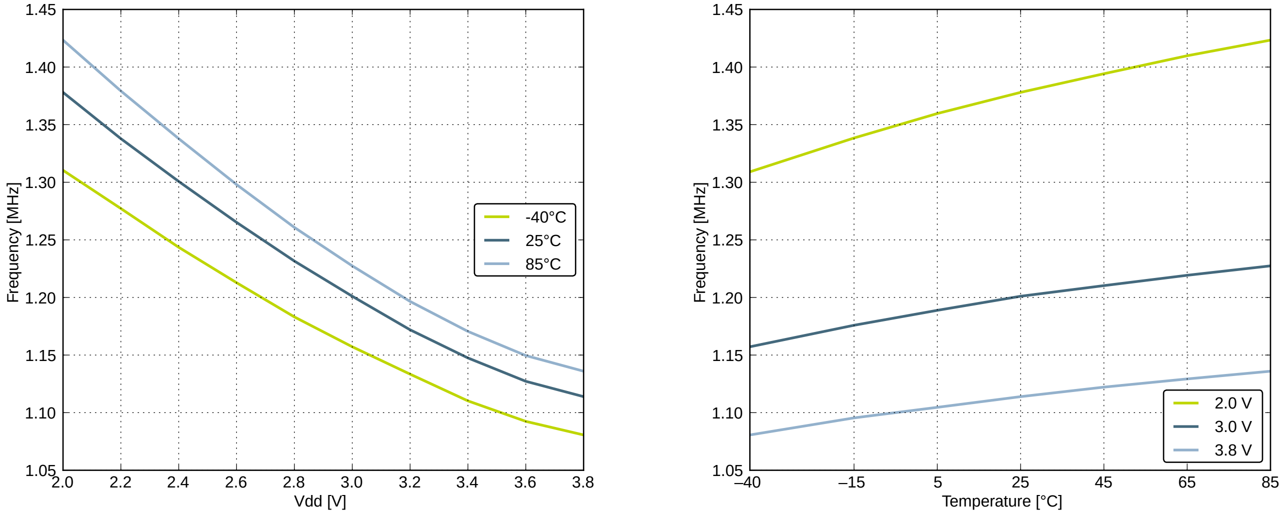


Figure 4.21. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

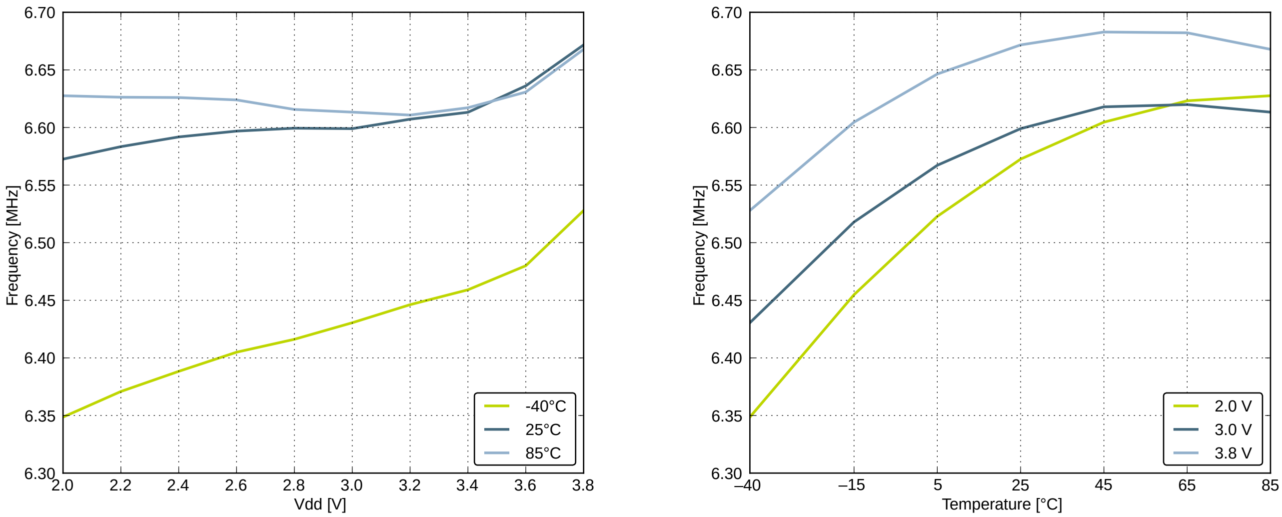


Figure 4.22. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

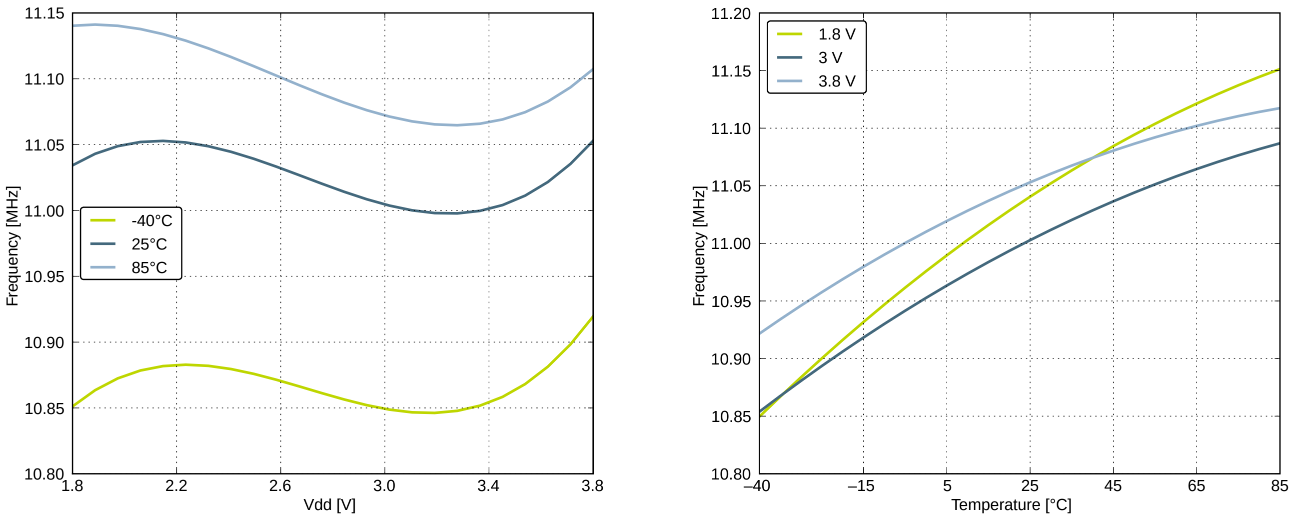


Figure 4.23. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

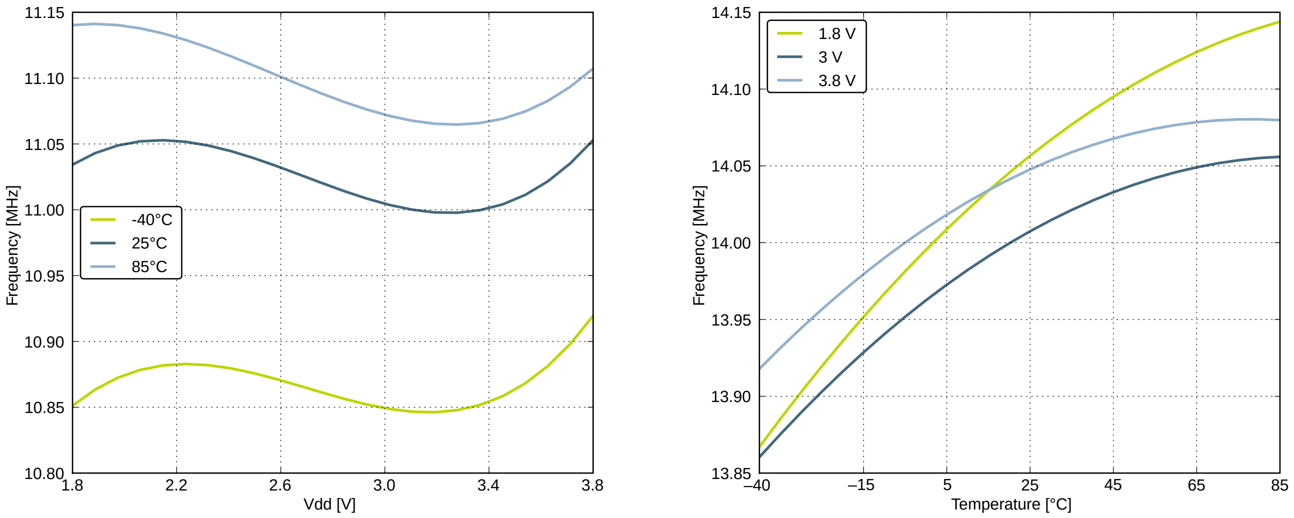


Figure 4.24. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

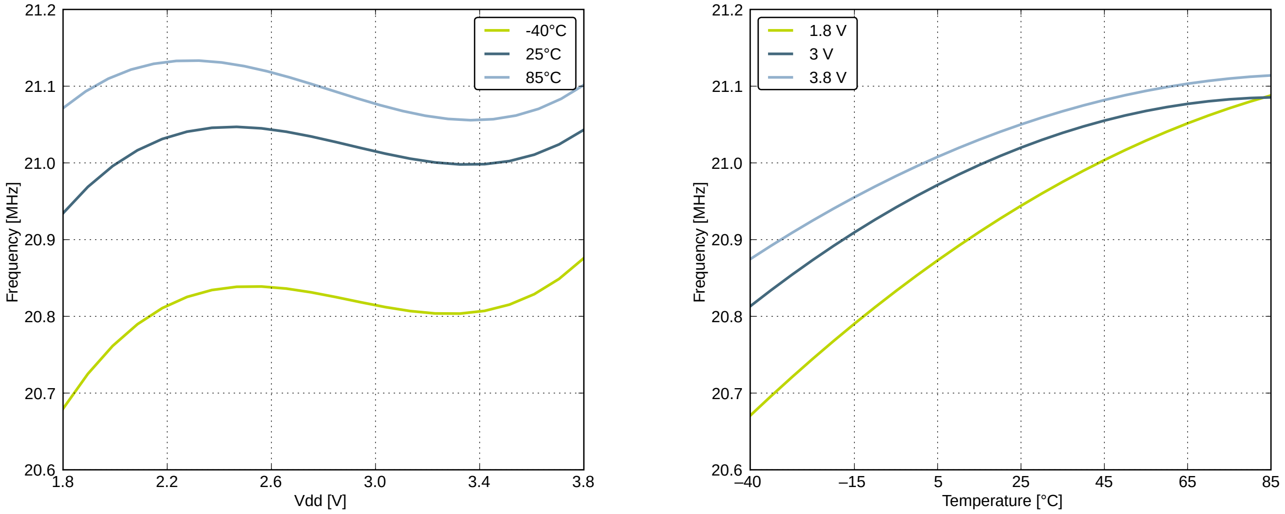


Figure 4.25. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

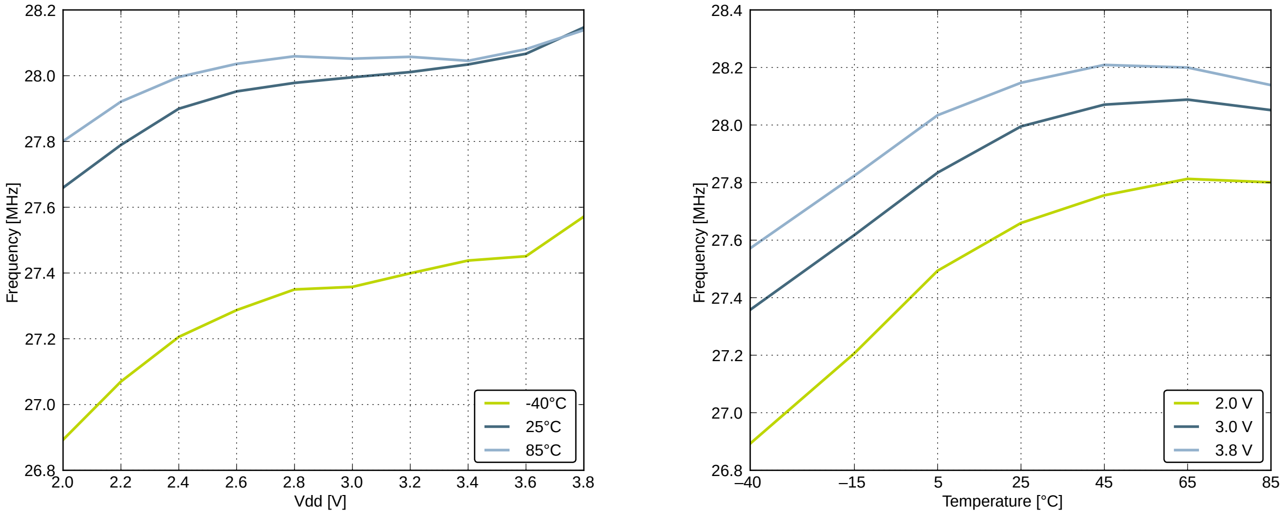


Figure 4.26. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature

4.10.5 AUXHFRCO

Table 4.13. AUXHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{AUXHFRCO}$	Oscillation frequency, V_{DD}= 3.0 V, T_{AMB}=25°C	21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40	6.60	6.80	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
$t_{AUXHFRCO\_settling}$	Settling time after start-up	$f_{AUXHFRCO}$ = 14 MHz	—	0.6	—	Cycles
$TUNESTEP_{AUXHFRCO}$	Frequency step for LSB change in TUNING value	21 MHz frequency band	—	52.8	—	kHz
		14 MHz frequency band	—	36.9	—	kHz
		11 MHz frequency band	—	30.1	—	kHz
		7 MHz frequency band	—	18.0	—	kHz
		1 MHz frequency band	—	3.4	—	kHz

4.10.6 USHFRCO

Table 4.14. USHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{USHFRCO}$	Oscillation frequency	No Clock Recovery, Full Temperature and Supply Range, 48 MHz band	47.10	48.00	48.90	MHz
		No Clock Recovery, Full Temperature and Supply Range, 24 MHz band	23.73	24.00	24.32	MHz
		No Clock Recovery, 25°C, 3.3V, 48 MHz band	47.50	48.00	48.50	MHz
		No Clock Recovery, 25°C, 3.3V, 24 MHz band	23.86	24.00	24.16	MHz
		USB Active with Clock Recovery, Full Temperature and Supply Range	47.88	48.00	48.12	MHz
$TC_{USHFRCO}$	Temperature coefficient	3.3V	—	0.0175	—	%/°C
$VC_{USHFRCO}$	Supply voltage coefficient	25°C	—	0.0045	—	%/V
$I_{USHFRCO}$	Current consumption	$f_{USHFRCO}$ = 48 MHz	1.21	1.36	1.48	mA
		$f_{USHFRCO}$ = 24 MHz	0.81	0.92	1.02	mA

4.10.7 ULFRCO

Table 4.15. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	25 °C, 3 V	0.7		1.75	kHz
Temperature coefficient	TC_{ULFRCO}		—	0.05	—	%/°C
Supply voltage coefficient	VC_{ULFRCO}		—	-18.2	—	%/V

4.11 Analog Digital Converter (ADC)

Table 4.16. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single-ended	0	—	V_{REF}	V
		Differential	$-V_{REF}/2$	—	$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single-ended and differential		1.25	—	V_{DD}	V
$V_{ADCREFIN\_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0	—	V_{DD} - 1.1	V
$V_{ADCREFIN\_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625	—	V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0	—	V_{DD}	V
I_{ADCIN}	Input current	2 pF sampling capacitors	—	<100	—	nA
$CMRR_{ADC}$	Analog input common mode rejection ratio		—	65	—	dB
I_{ADC}	Average active current	1 Msamples/s, 12 bit, external reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	735[1]	—	µA
		1 Msamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	760[1]	—	µA
		500 Ksamples/s, 12 bit, external reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	346[1]	—	µA
		500 Ksamples/s, 12 bit, internal 1.25V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	354[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 00b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	52[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 01b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	50[1]	—	µA
		10 kSamples/s, 12 bit, internal 1.25 V reference, WARMUP = 10b, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	54[1]	—	µA
I_{ADCREF}	Current Consumption of internal voltage refer-ene	Internal voltage reference	—	65	—	µA
C_{ADCIN}	Input capacitance		—	2	—	pF

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{ADCIN}	Input ON resistance		300	—	800	Ω
$R_{ADCFILT}$	Input RC filter resistance		—	10	—	kΩ
$C_{ADCFILT}$	Input RC filter/decoupling capacitance		—	250	—	fF
$I_{ADCBIASIN}$	Input bias current	VSS < VIN < VDD	-40	—	40	nA
$I_{ADCOFFSETIN}$	Input offset current	VSS < VIN < VDD	-40	—	40	nA
f_{ADCCLK}	ADC Clock Frequency	BIASPROG=0x747	—	—	7	MHz
		BIASPROG=0xF4B	—	—	13	MHz
$t_{ADCCONV}$	Conversion time	6-bit	7	—	—	ADCCLK Cycles
		8-bit	11	—	—	ADCCLK Cycles
		12-bit	13	—	—	ADCCLK Cycles
t_{ADCACQ}	Acquisition time	Programmable	1	—	256	ADCCLK Cycles
$t_{ADCACQVDD3}$	Required acquisition time for VDD/3 reference		2	—	—	µs
$t_{ADCSTART}$	Startup time of reference generator and ADC core	NORMAL mode	—	5	—	µs
		KEEPADCWARM mode	—	1	—	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SNR_{ADC}	Signal-to-Noise Ratio (SNR)	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	59	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	67	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK= 13 MHz, BIASPROG =0xF4B	63	69	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	70	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	67	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SNR_{ADC}	Signal-to-Noise Ratio (SNR)	200 kSamples/s, 12 bit, differential, V_{DD} reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	63	69	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	—	70	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$SINAD_{ADC}$	Signal-to-Noise And Distortion Ratio (SINAD)	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	58	—	dB
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	62	—	dB
		1 MSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	63	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	66	—	dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	62	68	—	dB
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	68	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	61	—	dB
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	62	—	dB
		200 kSamples/s, 12 bit, single-ended, VDD reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5V reference, ADC_CLK= 7 MHz, BIASPROG = 0x747	—	66	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$SINAD_{ADC}$	Signal-to-Noise And Distortion Ratio (SINAD)	200 kSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	62	68	—	dB
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	69	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	1 MSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	75	—	dBc
		1 MSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	76	—	dBc
		1 MSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	76	—	dBc
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	78	—	dBc
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	—	77	—	dBc
		1 MSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK= 13 MHz, BIASPROG = 0xF4B	—	76	—	dBc
		1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference, ADC_CLK = 13 MHz, BIASPROG = 0xF4B	68	79	—	dBc
		1 MSamples/s, 12 bit, differential, 5 V reference, ADC_CLK =13 MHz, BIASPROG = 0xF4B	—	79	—	dBc
		200 kSamples/s, 12 bit, single-ended, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	75	—	dBc
		200 kSamples/s, 12 bit, single-ended, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	75	—	dBc
		200 kSamples/s, 12 bit, single-ended, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	76	—	dBc
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, 5 V reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	—	78	—	dBc

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$SFDR_{ADC}$	Spurious-Free Dynamic Range (SFDR)	200 kSamples/s, 12 bit, differential, V_{DD} reference, ADC_CLK = 7 MHz, BIASPROG = 0x747	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference,ADC_CLK = 7 MHz, BIASPROG = 0x747	—	79	—	dBc
$V_{ADCOFFSET}$	Offset voltage	After calibration, single-ended	—	0.3	—	mV
		After calibration, differential	-4	0.3	4	mV
$TGRAD_{ADCTH}$	Thermometer output gradient		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/ °C
DNL_{ADC}	Differential non-linearity (DNL)	V_{DD}= 3.0 V, external 2.5V reference	-1	±0.7	4	LSB
INL_{ADC}	Integral non-linearity (INL), End point method	V_{DD}= 3.0 V, external 2.5V reference	—	±1.6	±3	LSB
MC_{ADC}	Missing codes	V_{DD}= 3.0 V, external 2.5 V reference	—	—	3	LSB
$GAIN_{ED}$	Gain error drift	1.25 V reference	—	0.01[2]	0.033[3]	%/°C
		2.5 V reference	—	0.01[2]	0.03[3]	%/°C
$OFFSET_{ED}$	Offset error drift	1.25 V reference	—	0.00[2]	0.06[3]	LSB/°C
		2.5 V reference	—	0.00[2]	0.04[3]	LSB/°C
V_{REF}	VREF voltage	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
V_{REF_VDRIFT}	VREF voltage drift	1.25 V reference	-12.4	2.9	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.7	35.2	mV/V
V_{REF_TDRIFT}	VREF temperature drift	1.25 V reference	-132	272	677	μV/°C
		2.5 V reference	-231	545	1271	μV/°C
I_{VREF}	VREF current consumption	1.25 V reference	—	67	114	μA
		2.5 V reference	—	55	82	μA
V_{REF_MATCH}	ADC and DAC VREF matching	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Includes required contribution from the voltage reference.
2. Typical numbers given by abs(Mean) / (85 - 25).
3. Max number given by (abs(Mean) + 3x stddev) / (85 - 25).

The integral non-linearity (INL) and differential non-linearity (DNL) parameters are explained in the following figures.

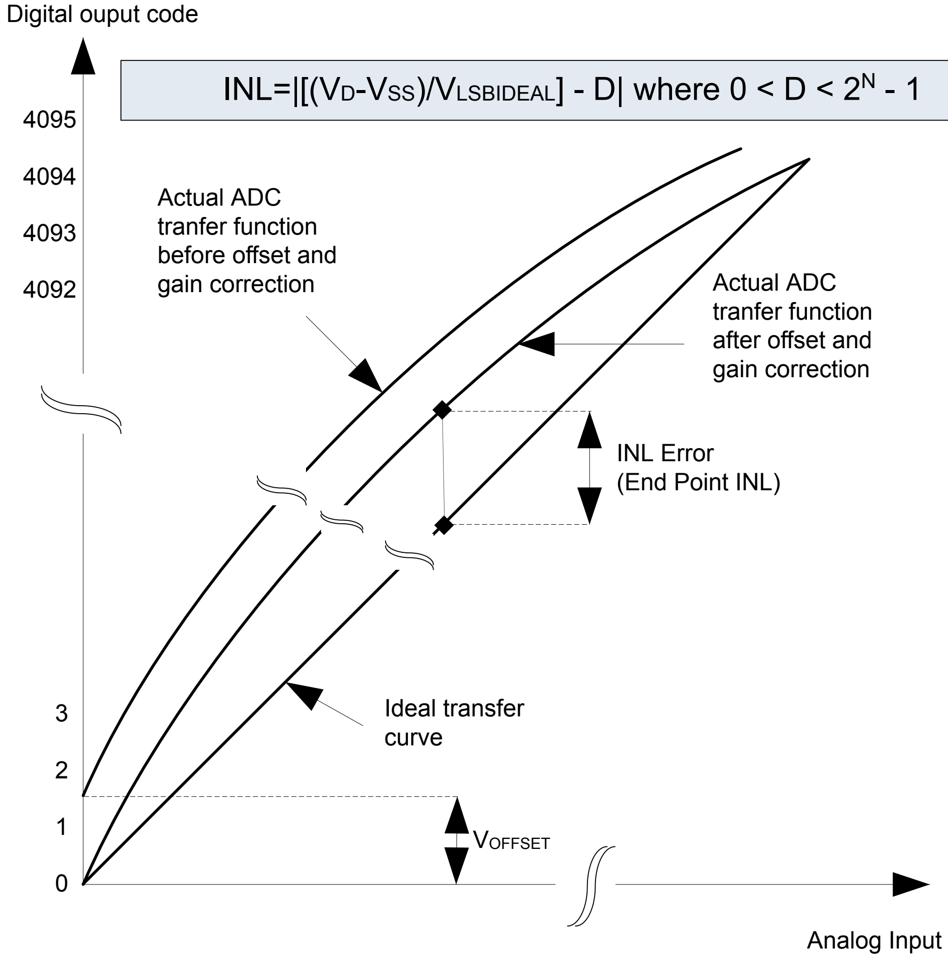


Figure 4.27. Integral Non-Linearity (INL)

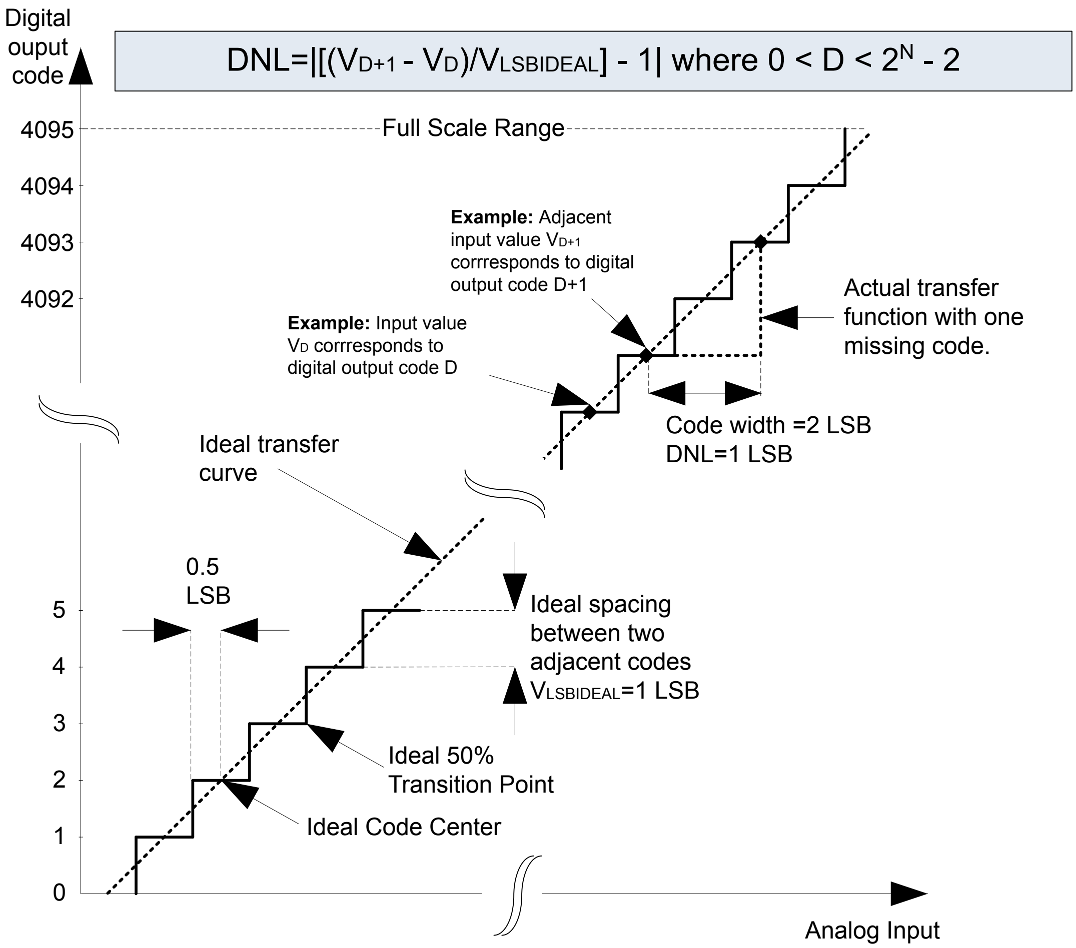
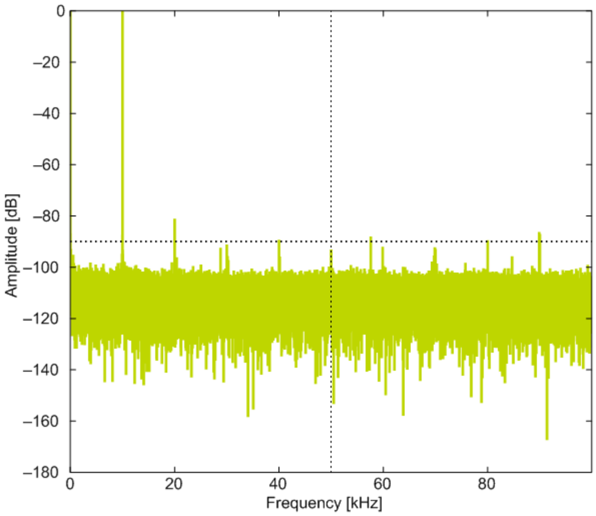
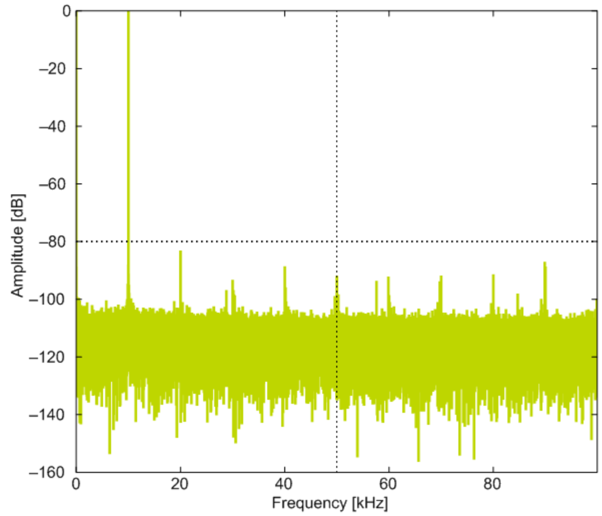


Figure 4.28. Differential Non-Linearity (DNL)

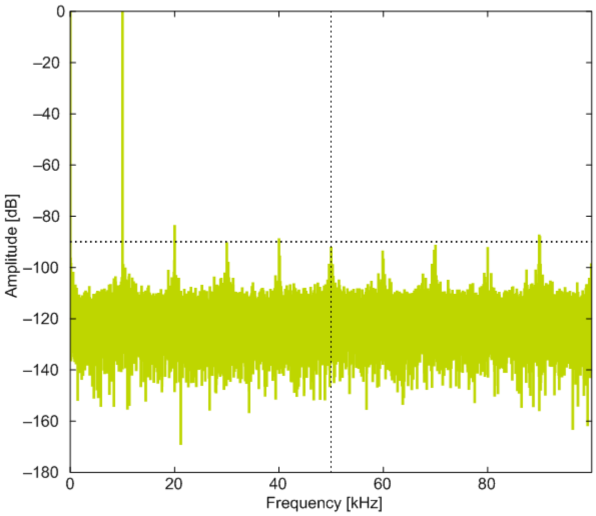
4.11.1 Typical Performance



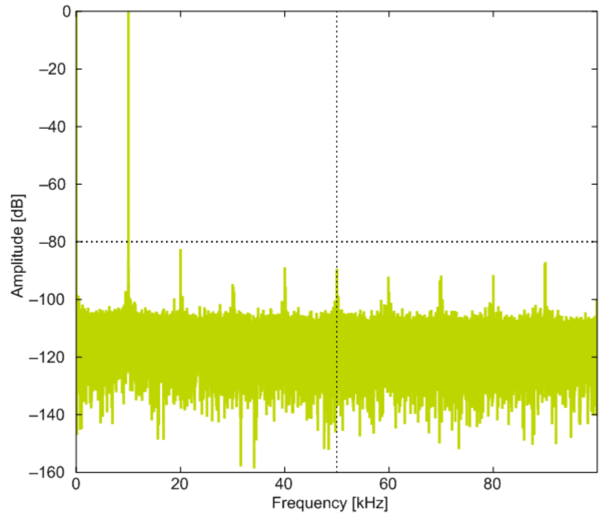
1.25 V Reference



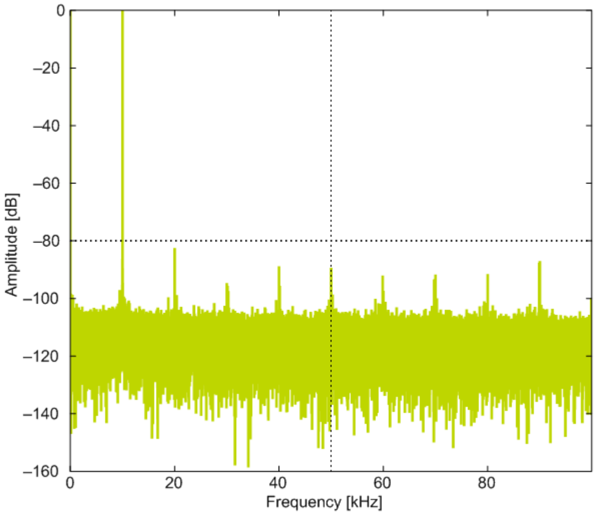
2.5 V Reference



2XVDDVSS Reference

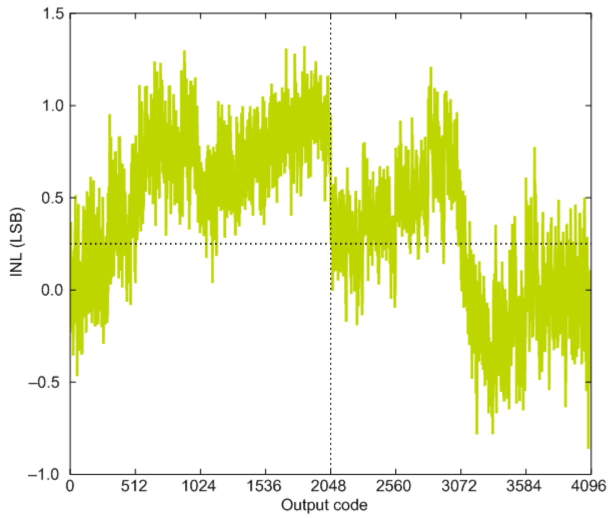


5VDIFF Reference

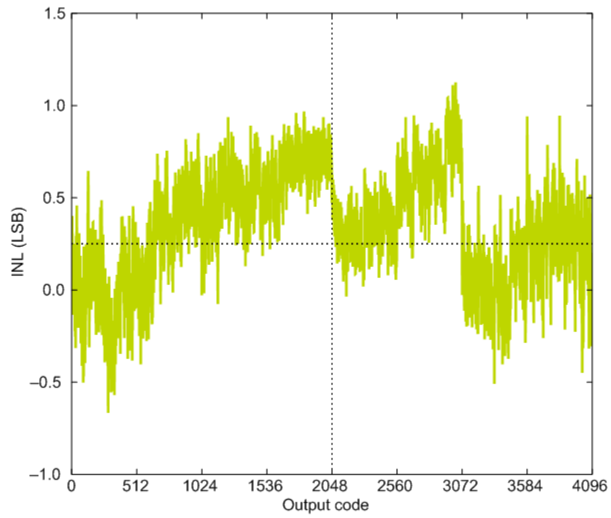


V_{DD} Reference

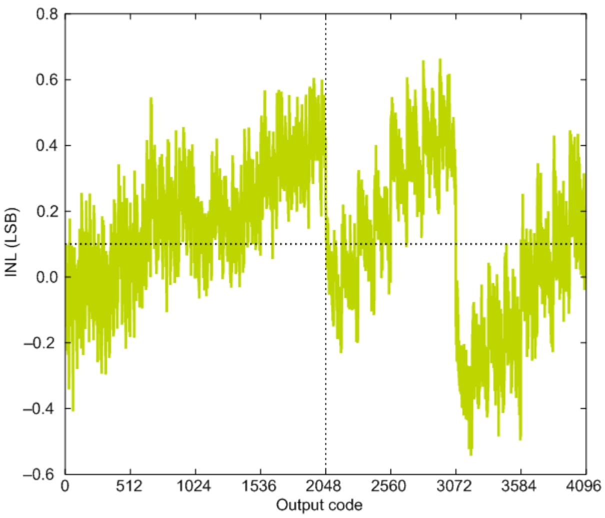
Figure 4.29. ADC Frequency Spectrum, V_{DD} = 3 V, Temp = 25 °C



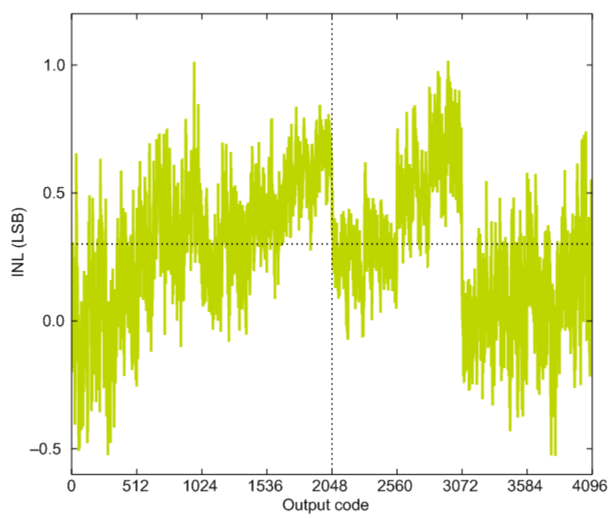
1.25 V Reference



2.5 V Reference



2XVDDVSS Reference



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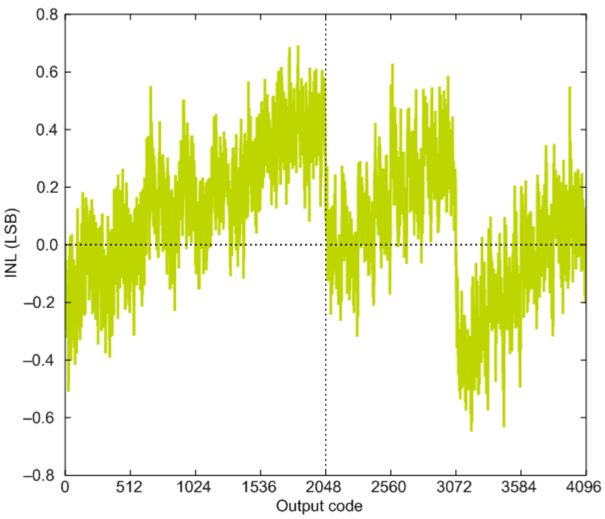
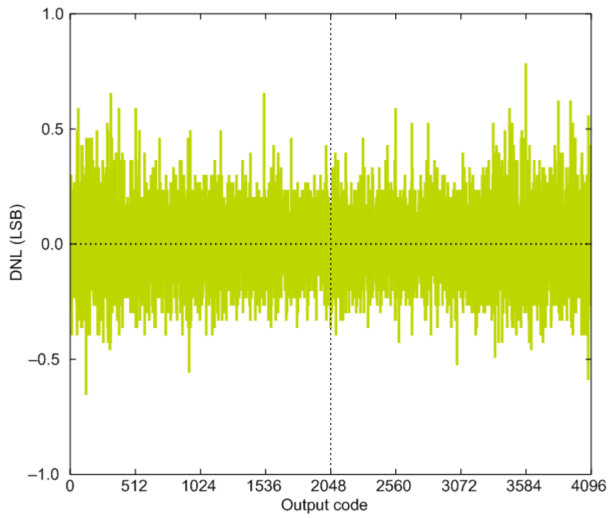
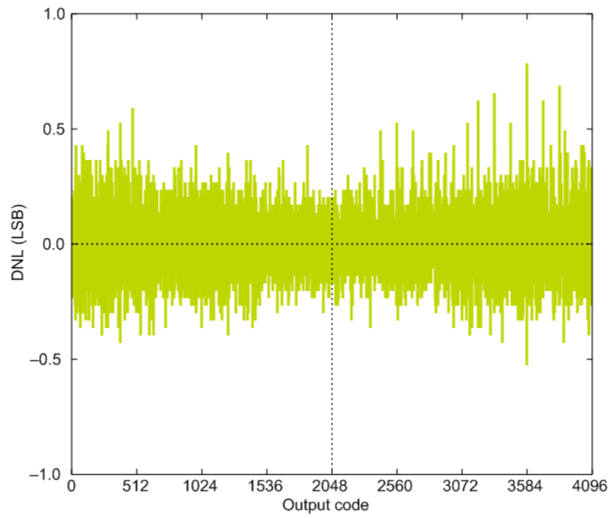


VDD Reference

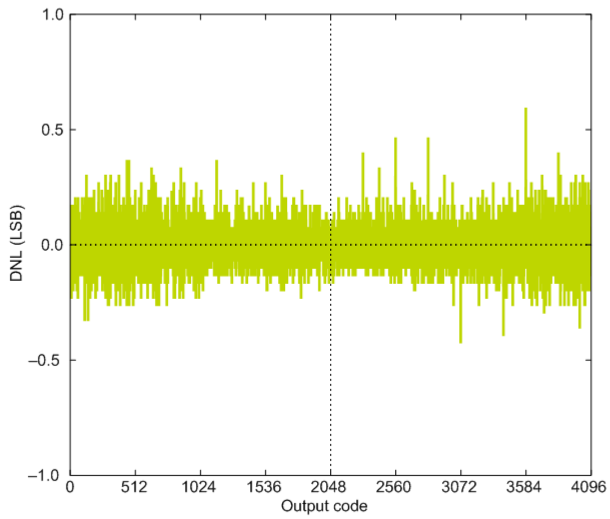
Figure 4.30. ADC Integral Linearity Error vs Code, V_{DD} = 3 V, Temp = 25 °C



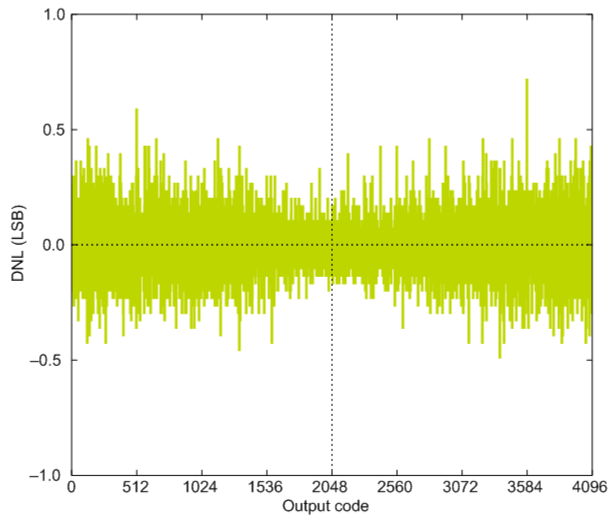
1.25 V Reference



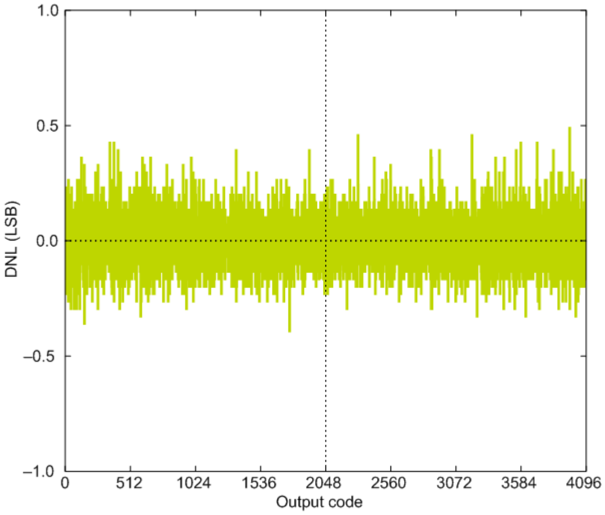
2.5 V Reference



2XVDDVSS Reference

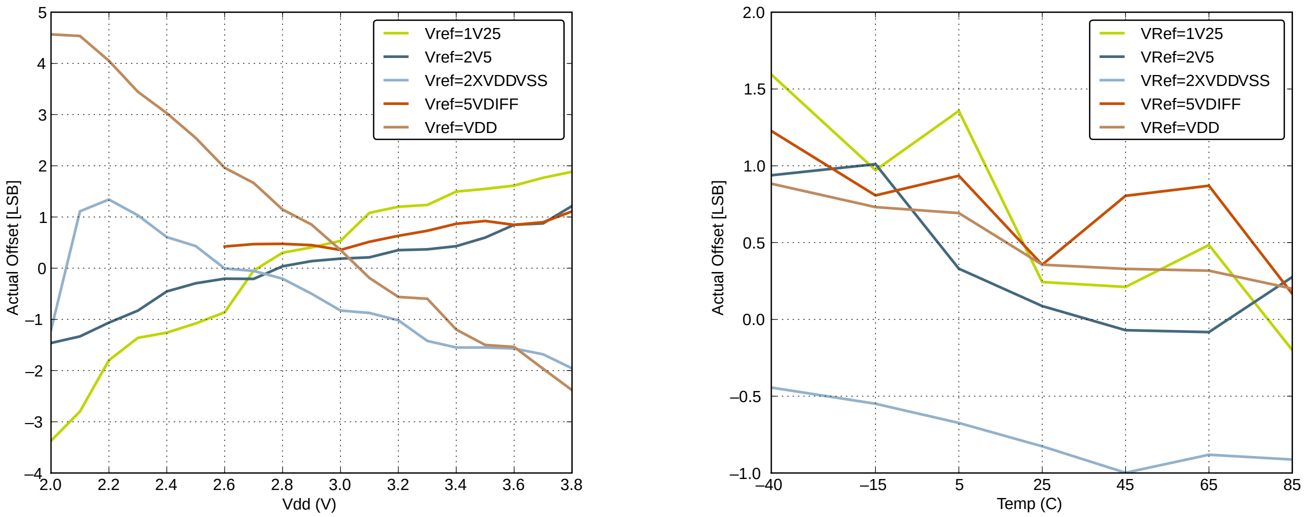


5VDIFF Reference



V_{DD} Reference

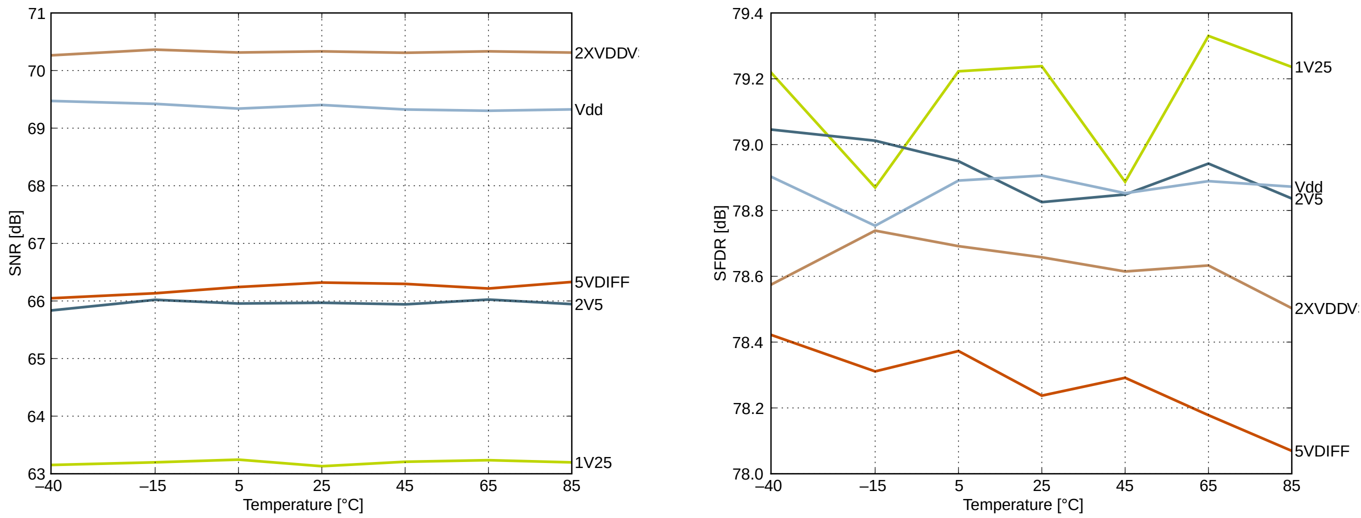
Figure 4.31. ADC Differential Linearity Error vs Code, V_{DD} = 3 V, Temp = 25 °C



Offset vs Supply Voltage, Temp = 25 °C

Offset vs Temperature, V_{DD} = 3 V

Figure 4.32. ADC Absolute Offset, Common Mode = V_{DD}/2



Signal to Noise Ratio (SNR) **Spurious-Free Dynamic Range (SFDR)**

Figure 4.33. ADC Dynamic Performance vs Temperature for all ADC References, V_{DD} = 3 V

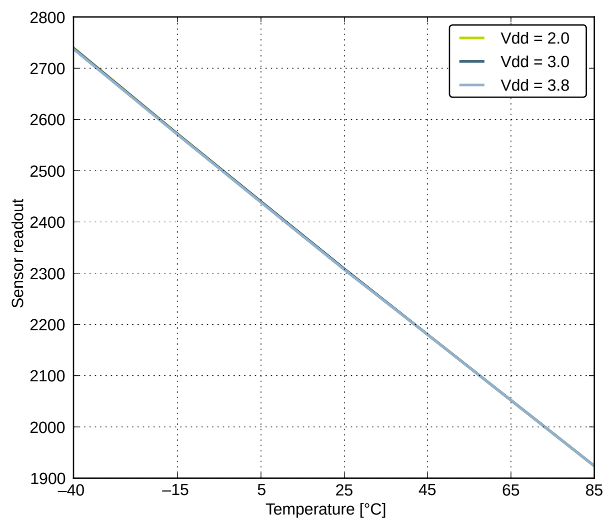


Figure 4.34. ADC Temperature Sensor Readout

4.12 Current Digital Analog Converter (IDAC)

Table 4.17. IDAC Range 0 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	13.0	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	0.85	—	µA
Step size	I_{STEP}		—	0.05	—	µA
Current drop at high impedance load	I_D	$V_{IDAC\_OUT} = V_{DD}$ - 100mV	—	0.79	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0V, STEPSEL=0x10	—	0.3	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	11.7	—	nA/V

Table 4.18. IDAC Range 0 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	15.1	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	0.85	—	µA
Step size	I_{STEP}		—	0.05	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200 mV	—	0.30	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	0.2	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	12.5	—	nA/V

Table 4.19. IDAC Range 1 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	14.4	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	3.2	—	µA
Step size	I_{STEP}		—	0.1	—	µA
Current drop at high impedance load	I_D	$V_{IDAC\_OUT} = V_{DD}$ - 100mV	—	0.75	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	0.7	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	38.4	—	nA/V

Table 4.20. IDAC Range 1 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	19.4	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	3.2	—	µA
Step size	I_{STEP}		—	0.1	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200 mV	—	0.32	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	0.7	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	40.9	—	nA/V

Table 4.21. IDAC Range 2 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	17.3	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	8.5	—	µA
Step size	I_{STEP}		—	0.5	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = V_{DD} - 100mV	—	1.22	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	2.8	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	96.6	—	nA/V

Table 4.22. IDAC Range 2 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	29.3	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	8.5	—	µA
Step size	I_{STEP}		—	0.5	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200 mV	—	0.62	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	2.8	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	94.4	—	nA/V

Table 4.23. IDAC Range 3 Source

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	18.7	—	µA
		Duty-cycled	—	10	—	nA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	33.9	—	µA
Step size	I_{STEP}		—	2.0	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = V_{DD} - 100 mV	—	3.54	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	10.9	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	159.5	—	nA/V

Table 4.24. IDAC Range 3 Sink

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Active current with STEPSEL=0x10	I_{IDAC}	EM0, default settings	—	62.5	—	µA
Nominal IDAC output current with STEPSEL=0x10	I_{0x10}		—	34.1	—	µA
Step size	I_{STEP}		—	2.0	—	µA
Current drop at high impedance load	I_D	V_{IDAC_OUT} = 200 mV	—	1.75	—	%
Temperature coefficient	TC_{IDAC}	V_{DD} = 3.0 V, STEPSEL=0x10	—	10.9	—	nA/°C
Voltage coefficient	VC_{IDAC}	T = 25 °C, STEPSEL=0x10	—	148.6	—	nA/V

Table 4.25. IDAC

Parameter	Symbol	Min	Typ	Max	Unit
Start-up time, from enabled to output settled	$t_{IDACSTART}$	—	40	—	µs

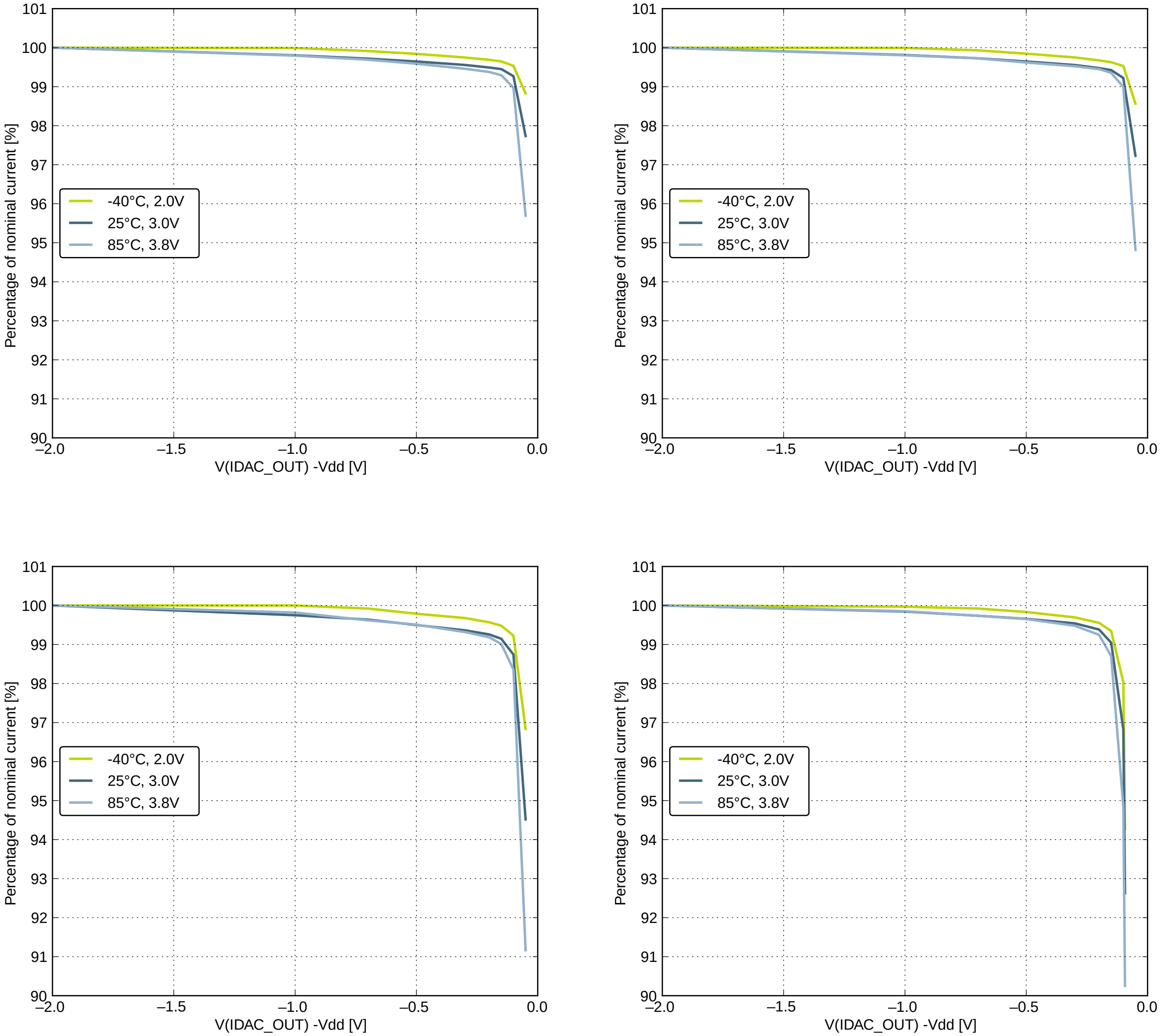


Figure 4.35. IDAC Source Current as a Function of Voltage on IDAC_OUT

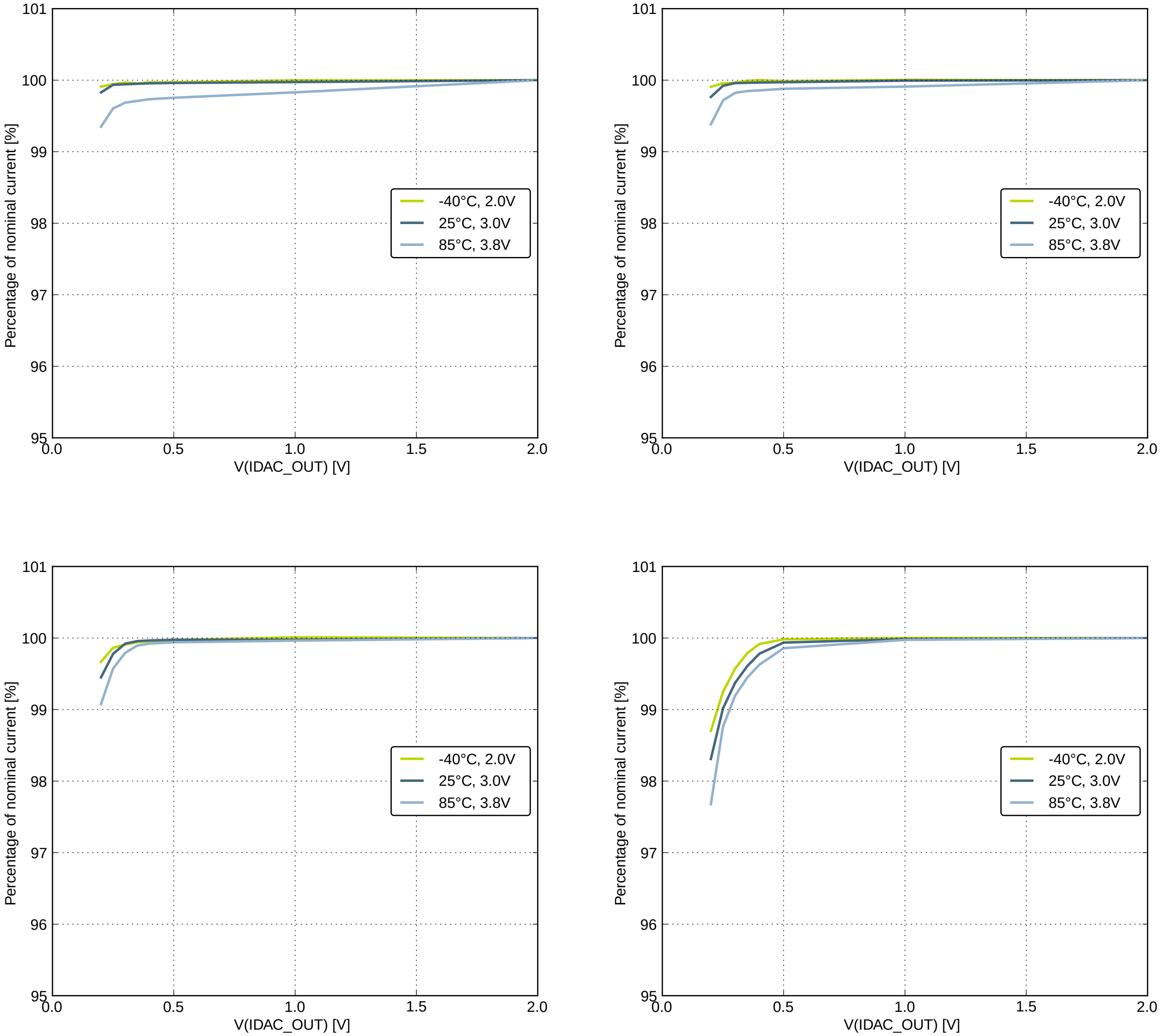


Figure 4.36. IDAC Sink Current as a Function of Voltage from IDAC_OUT

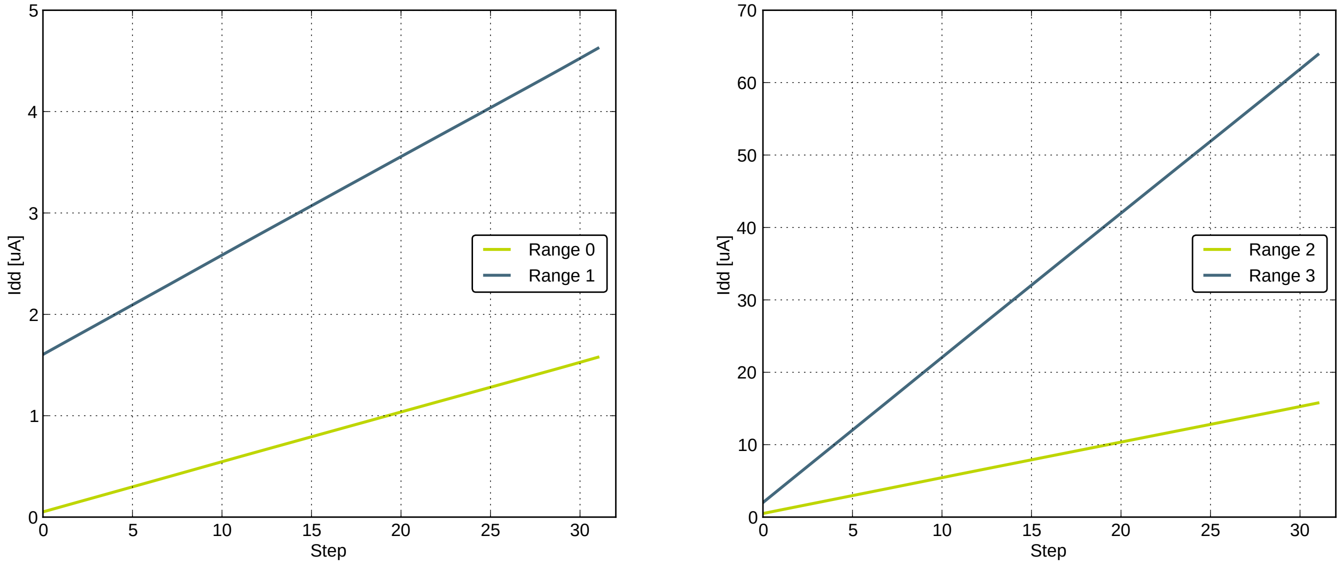


Figure 4.37. IDAC Linearity

4.13 Voltage Comparator (VCMP)

Table 4.26. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{VCMPIN}		—	V_{DD}	—	V
VCMP Common Mode voltage range	V_{VCMPCM}		—	V_{DD}	—	V
Active current	I_{VCMP}	BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register	—	0.30.2	0.60.8	μA
		BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0.	—	2222	3535	μA
Startup time reference generator	$t_{VCMPREF}$	NORMAL	—	10	—	μs
Offset voltage	$V_{VCMPOFFSET}$	single-ended	—	10	—	mV
		Differential	—	10	—	mV
VCMP hysteresis	$V_{VCMPHYST}$		—	6117	210—	mV
Startup time	$t_{VCMPSTART}$		—	—	10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation: $V_{DD\ Trigger\ Level}$=1.667 V+0.034 ×TRIGLEVEL

4.14 I2C

Table 4.27. I2C Standard-Mode (Sm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	100 [1]	kHz
SCL clock low time	t_{LOW}	4.7	—	—	µs
SCL clock high time	t_{HIGH}	4.0	—	—	µs
SDA set-up time	$t_{SU,DAT}$	250	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	3450[2, 3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	4.0	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	4.0	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	4.7	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EZR32HG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450 * 10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.28. I2C Fast-Mode (Fm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	400[1]	kHz
SCL clock low time	t_{LOW}	1.3	—	—	µs
SCL clock high time	t_{HIGH}	0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$	100	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	900[2, 3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.6	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	1.3	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EZR32HG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900 * 10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.29. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	1000[1]	kHz
SCL clock low time	t_{LOW}	0.5	—	—	µs
SCL clock high time	t_{HIGH}	0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$	50	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	0.26	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	0.5	—	—	µs

Note:

1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EZR32HG Reference Manual.

4.15 USB

The USB hardware in the EZR32HG320 passes all tests for USB 2.0 Full Speed certification. The test report will be distributed with application note *AN0046 - USB Hardware Design Guide* when ready.

Table 4.30. USB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{USBOUT}	USB regulator output voltage		3.1	3.4	3.7	V
I_{USBOUT}	USB regulator output current	BIASPROG=0, T_{AMB}=25°C	55.7	79.4	104.1	mA
		BIASPROG=1, T_{AMB}=25°C	66.0	95.9	126.4	mA
		BIASPROG=2, T_{AMB}=25°C	94.6	146.5	188.1	mA
		BIASPROG=3, T_{AMB}=25°C	80.4	128.3	176.0	mA

4.16 Radio

All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated. The data was collected while running off the internal RC oscillator (HFRCO).

4.16.1 EZRadioPRO (R6x) DC Electrical Characteristics

Measured on direct-tie RF evaluation board.

Table 4.31. EZRadioPro DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Saving Modes	$I_{shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	4000	nA
	$I_{standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	9000	nA
	$I_{SleepRC}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	740	10000	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal	—	1.7	—	μA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	μA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
Preamble Sense Mode Current	I_{psm}	Duty cycing during preamble search, 1.2 kbps, 4 byte preamble	—	6	—	mA
		Fixed 1s wakeup interval, 50 kbps, 5 byte preamble	—	10	—	μA
TUNE Mode Current	I_{TuneRX}	RX Tune, High Performance Mode	—	7.6	—	mA
	I_{TuneTX}	TX Tune, High Performance Mode	—	7.8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode, 915 MHz, 40 kbps	—	13.7	22	mA
	I_{RXL}	Low Power Mode, 915 MHz, 40 kbps	—	11.1	—	mA
TX Mode Current (R69)	I_{TX_+20}	+20 dBm output power, class-E match, 915 MHz, 3.3 V	—	93	108	mA
	I_{TX_+13}	+13 dBm output power, class-E match, 868/915 MHz, 3.3 V	—	22	—	mA
TX Mode Current (R63, R68)	I_{TX_+20}	+20 dBm output power, class-E match, 915 MHz, 3.3 V	—	93	108	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	69	80	mA
	I_{TX_+13}	+13 dBm output power, class-E match, 915 MHz, 3.3 V	—	44.5	60	mA
TX Mode Current (R60, R67)	I_{TX_+10}	+10 dBm output power, class-E match, 868/915 MHz, 3.3 V	—	19.7	—	mA
	I_{TX_+10}	+10 dBm output power, class-E match, 169 MHz, 3.3 V	—	18	—	mA
	I_{TX_+13}	+13 dBm output power, class-E match, 868/915 MHz, 3.3 V	—	22	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Mode Current (R61)	I_{TX_+16}	+16 dBm output power, class-E match, 868 MHz, 3.3 V	—	43	55	mA
	I_{TX_+13}	+13 dBm output power, switched-current match, 868 MHz, 3.3 V	—	33.5	40	mA

4.16.2 EZRadioPRO (R6x) Synthesizer AC Electrical Characteristics

Table 4.32. EZRadioPro Synthensizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution	$F_{RES-1050}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	μs
Phase Noise	$L_{(fM)}$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	–108	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	–115	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	–135	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	–143	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	–94	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	–97	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	–122	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	–135	dBc/Hz

4.16.3 EZRadioPRO (R6x) Receiver AC Electrical Characteristics

For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.

Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 4.33. EZRadioPro Receiver AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		850	—	1050	MHz
			350	—	525	MHz
			284		350	MHz
			142	—	175	MHz
RX Sensitivity 169 MHz (R68, R67)3	$P_{RX\_0.1}$	(BER < 0.1%) (100 bps, GFSK, BT = 0.5, Δf = ±100 Hz)	—	–133	—	dBm
RX Sensitivity 169 MHz (R60, R61, R63)3	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	–129	—	dBm
RX Sensitivity 169 MHz (R60, R61, R63, R67, R68)3	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–110.7	–108	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–106	–104	dBm
	P_{RX_125}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–99	–96	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–89	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–110	–107	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–103	–100	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–97	–93	dBm
RX Sensitivity 915/868 MHz (R68, R67)3	$P_{RX\_0.1}$	(BER < 0.1%) (100 bps, GFSK, BT = 0.5, Δf = ±100 Hz)	—	–132	—	dBm
RX Sensitivity 915 MHz (R60, R61, R63, R69)3	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	–127	—	dBm
RX Sensitivity 868 MHz (R60, R61, R63, R69)3		(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250 Hz)	—	–127	—	dBm
RX Sensitivity 868 MHz (R60, R61, R63, R67, R68, R69)3	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109.9	—	dBm
RX Sensitivity 915 MHz (R60, R61, R63, R67, R68, R69)3		(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109.4	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity 915/868 MHz (R60, R61, R63, R67, R68, R69)3	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–104	–102	dBm
	P_{RX_125}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	–92	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110.6	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–88.7	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–108	–104	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–101	–97	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–96	–91	dBm
RX Channel Bandwidth (R60, R61, R63)	BW		1.1	—	850	kHz
RX Channel Bandwidth (R68, R67)			0.2	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from –110 dBm to -90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity, 169 MHz	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–69	–59	dB
±1-Ch Offset Selectivity, 450 MHz			—	–60	–50	dB
±1-Ch Offset Selectivity, 868 / 915 MHz			—	–52.5	–45	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–79	–68	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	–86	–75	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection (IF = 468.75 kHz)	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. RF = 460 MHz	30	40	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 460 MHz	40	55	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 915 MHz	30	45	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 915 MHz	40	52	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 169 MHz	35	45	—	dB
		With image rejection calibration. Rejection at the image frequency. RF = 169 MHz	45	60	—	dB

Note:

1. BER sensitivity measure using GPIO3 for data and GPIO1 for data clock. Use of other GPIO pins could result in degraded sensitivity.
2. When in HFXO mode sensitivity will degrade at multiples of HFXO crystal frequency. Values in data sheet do not include spurious channel values.

4.16.4 EZRadioPRO (R6x) Transmitter AC Electrical Characteristics

The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).

Default API setting for modulation deviation resolution is double the typical value specified.

Output power is dependent on matching components and board layout.

Table 4.34. EZRadioPro Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution	$F_{RES-1050}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Typical Output Power Range (R63)	P_{TX63}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+20	dBm
Typical Output Power Range (R61)	P_{TX61}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–40		+16	dBm
Typical Output Power Range (R60)	P_{TX60}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+12.5	dBm
Typical Output Power Range (R68)	P_{TX68}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+20	dBm
Typical Output Power Range (R69)	P_{TX69}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+20	dBm
Typical Output Power Range (R67)	P_{TX67}	Typical Output Power Range at 3.3 V with Class E mtch optimized for best PA efficiency	–20	—	+12.5	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power Variation (R63, R68, R69)		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm
Output Power Variation (R60, R67)		At 10 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	9	10	11	dBm
Output Power Variation (R63, R68)		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
Output Power Variation (R60, R67)		At 10 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	9.5	10	10.5	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	0.4	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	3	dB
TX RF Output Level Variation vs. Frequency	$\Delta P\text{-}RF_{FREQ}$	Measured across 902–928 MHz	—	0.6	1.7	dB
Transmit Modulation Filtering	B×T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

4.16.5 EZRadioPRO (R6x) Radio Auxillary Block Specifications

Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.

XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 4.35. EZRadioPro Auxiliary Block Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Range	$XTAL_{RANGE}$		25	–	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	–	300	–	uS
30 MHz XTAL Cap Resolution	$30M_{RES}$		–	70	–	fF
32 kHz XTAL Start-Up Time	t_{32K}		–	2	–	sec
32 kHz Accuracy using Internal RC Oscillator	$32KRC_{RES}$		–	2500	–	ppm
POR Reset Time	t_{POR}		–	–	6	ms

4.16.6 EZRadio (R55) DC Electrical Characteristics

Table 4.36. EZRadio DC Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Saving Modes	$I_{shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	—	nA
	$I_{standby}$	Register values maintained	—	40	—	nA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
	$I_{SPIActive}$	SPI active state	—	1.5	—	mA
TUNE Mode Current	I_{TuneRX}	RX Tune	—	6.8	—	mA
	I_{TuneTX}	TX Tune	—	7.1	—	mA
RX Mode Current	I_{RX}	Measured at 40 kbps, 20 kHz deviation, 315 MHz	—	10.9	—	mA
TX Mode Current	I_{TX}	+10 dBm output power, measured on direct tie RF evaluation board at 868 MHz	—	19	—	mA
		+13 dBm output power, measured on direct tie RF evaluation board at 868 MHz	—	24	—	mA

4.16.7 EZRadio (R55) Synthesizer AC Electrical Characteristics

Table 4.37. EZRadio Synthensizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
Synthesizer Frequency Resolution	$F_{RES-960}$	850-960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	420-525 MHz	—	57.2	—	Hz
	$F_{RES-350}$	283-350 MHz	—	38.1	—	Hz
Phase Noise	$L_{(fM)}$	ΔF = 10 kHz, 915 MHz	—	100	—	dBc/Hz
		ΔF = 100 kHz, 915 MHz	—	102.1	—	dBc/Hz
		ΔF = 1 MHz, 915 MHz	—	123.5	—	dBc/Hz
		ΔF = 10 MHz, 915 MHz	—	136.6	—	dBc/Hz

4.16.8 EZRadio (R55) Receiver AC Electrical Characteristics

Table 4.38. EZRadio Receiver AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
RX Sensitivity 915 MHz	P_{RX_2}	(BER < 0.1%) (2.4 kbps, GFSK, BT = 0.5, Δf = ±30 kHz, 114 kHz RX BW)	—	-115	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±25 kHz, 114 kHz RX BW)	—	-107.6	—	dBm
	P_{RX_128}	(BER < 0.1%) (128 kbps, GFSK, BT = 0.5, Δf = ±70 kHz, 305 kHz RX BW)	—	-102.4	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 1 kbps, 185 kHz Rx BW, OOK, PN15 data)	—	-113.5	—	dBm
		(BER < 0.1%, 40 kbps, 185 kHz BW, OOK, PN15 data)	—	-102.7	—	dBm
RX Sensitivity 434 MHz	P_{RX_2}	(BER < 0.1%) (2.4 kbps, GFSK, BT = 0.5, DF = ±30 kHz, 114 kHz Rx BW)	—	-116	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, DF = ±25 kHz, 114 kHz Rx BW)	—	-108	—	dBm
	P_{RX_128}	(BER < 0.1%) (128 kbps, GFSK, BT = 0.5, DF = ±70 kHz, 305 kHz Rx BW)	—	-103	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 1 kbps, 185 kHz Rx BW, OOK, PN15 data)	—	-113	—	dBm
		(BER < 0.1%, 40 kbps, 185 kHz BW, OOK, PN15 data)	—	-102	—	dBm
RX Channel Bandwidth	BW		40	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from -110 dBm to -90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX channel BW = 58 kHz, channel spacing = 100 kHz	—	-50	—	dB
±2-Ch Offset Selectivity	$C/I_{2\text{-}CH}$		—	-56	—	dB
Blocking 200 kHz−1 MHz	$200K_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER, <0.1%. Interferer is CW and desired is modulated with 1.2 kbps ΔF = 5.2 kHz GFSK with BT = 0.5, RX channel BW = 58 kHz	—	-56	—	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$		—	-71	—	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	-71	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection	Im_{REJ}	Rejection at the image frequency IF = 468 kHz	—	40	—	dB

Note:

1. BER sensitivity measure using GPIO3 for data and GPIO1 for data clock. Use of other GPIO pins could result in degraded sensitivity.
2. When in HFXO mode sensitivity will degrade at multiples of HFXO crystal frequency. Values in data sheet do not include spurious channel values.

4.16.9 EZRadio (R55) Transmitter AC Electrical Characteristics

The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).

Conducted measurements based on RF evaluation board. Output power and emissions specifications are dependent on transmit frequency, matching components, and board layout.

Table 4.39. EZRadio Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		284	—	350	MHz
			350	—	525	MHz
			850	—	960	MHz
(G)FSK Data Rate	DR_{FSK}		1.0	—	500	kbps
OOK Data Rate	DR_{OOK}		0.5	—	120	kbps
Modulation Deviation Range	Δf_{960}	850-960 MHz	—	—	500	kHz
	Δf_{525}	350-525 MHz	—	—	500	kHz
	Δf_{350}	284-350 MHz	—	—	500	kHz
Modulation Deviation Resolution	$F_{RES-960}$	850-960 MHz	—	114.4	—	Hz
	$F_{RES-525}$	420-525 MHz	—	57.2	—	Hz
	$F_{RES-420}$	350-420 MHz	—	45.6	—	Hz
	$F_{RES-350}$	284-350 MHz	—	38.1	—	Hz
Output Power Range	P_{TX}	Measured at 434 MHz, 3.3 V, Class E match	-20	—	+13	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	—	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	-40 to +85 °C	—	2.3	—	dB
TX RF Output Level Variation vs. Frequency	$\Delta P\text{-}RF_{FREQ}$	Measured across 902-928 MHz	—	0.6	—	dB
Transmit Modulation Filtering	B×T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

4.16.10 EZRadio (R55) Radio Auxiliary Block Specifications

XTAL Range tested in production using an external clock source (similar to using a TCXO).

Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested by bench characterization.

Table 4.40. EZRadio Auxilliary Block Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
XTAL Range	$XTAL_{RANGE}$		25		32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	300	—	us
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	Ff
POR Reset Time	t_{POR}		—	—	6	ms

4.16.11 Radio Digital I/O Specification

6.7 ns is typical for GPIO0 rise time.

Assuming V_{DD} = 3.3 V, drive strength is specified at V_{OH} (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.

2.4 ns is typical for GPIO0 fall time.

Table 4.41. EZRadio/Pro Digital I/O Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD_RF} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD_RF} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< VDD	-1	—	1	uA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	uA
Drive Strength for Output Low Level3	I_{OmaxLL}	DRV[1:0] = LL	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	1.13	—	mA
Drive Strength for Output High Level3	I_{OmaxLL}	DRV[1:0] = LL	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.96	—	mA
Drive Strength for Output High Level for GPIO3	I_{OmaxLL}	DRV[1:0] = LL	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL	—	1.7	—	mA
	I_{OmaxHH}	DRV[1:0] = HH	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD_RF} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD_RF} x 0.2	V

4.17 Digital Peripherals

Table 4.42. Digital Peripherals

Parameter	Symbol	Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	7.5	—	µA/MHz
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	150	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	6.25	—	µA/MHz
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	8.75	—	µA/MHz
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	100	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	100	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	2.5	—	µA/MHz
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	5.31	—	µA/MHz
PRS current	I_{PRS}	PRS idle current	—	2.81	—	µA/MHz
DMA current	I_{DMA}	Clock enable	—	8.12	—	µA/MHz

5. Pinout and Package

Note: Refer to the application note, AN0002.0: EFM32 and EZR32 Wireless MCU Series 0 Hardware Design Considerations, for guidelines on designing Printed Circuit Boards (PCB's) for the EZR32HG320.

5.1 Pinout

The EZR32HG320 pinout is shown in below. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

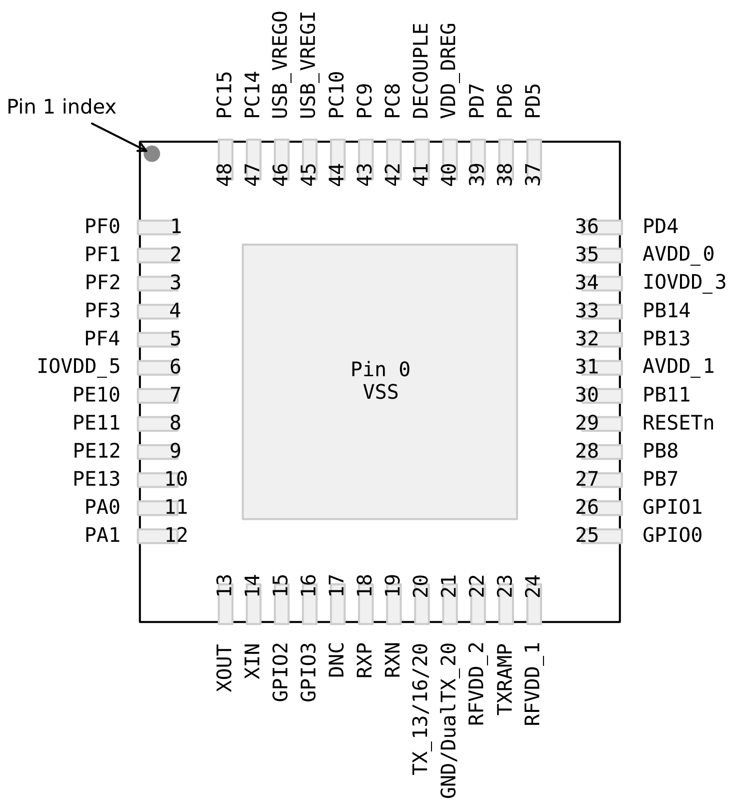


Figure 5.1. Pinout (top view, not to scale)

5.2 Pin Descriptions

Table 5.1. Device Pinout

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PF0		TIM0_CC0 #5	LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0
2	PF1		TIM0_CC1 #5	LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0 GPIO_EM4WU3
3	PF2		TIM0_CC2 #5/6 TIM2_CC0 #3	LEU0_TX #4	CMU_CLK0 #3 PRS_CH0 #3 GPIO_EM4WU4
4	PF3		TIM0_CDTI0 #5		PRS_CH0 #1
5	PF4		TIM0_CDTI1 #5		PRS_CH1 #1
6	IOVDD_5	Digital IO power supply 5.			
7	PE10		TIM1_CC0 #1	US0_TX #0	PRS_CH2 #2
8	PE11		TIM1_CC1 #1	US0_RX #0	PRS_CH3 #2
9	PE12	ADC0_CH0	TIM1_CC2 #1 TIM2_CC1 #3	US0_RX #3 US0_CLK #0/6 I2C0_SDA #6	CMU_CLK1 #2 PRS_CH1 #3
10	PE13	ADC0_CH1	TIM2_CC2 #3	US0_TX #3 US0_CS #0/6 I2C0_SCL #6	PRS_CH2 #3 GPIO_EM4WU5
11	PA0		TIM0_CC1 #6 TIM0_CC0 #0/1/4 PCNT0_S0IN #4	USB_DMPU #0 LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
12	PA1		TIM0_CC0 #6 TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
13	XOUT	EZRadio peripheral crystal oscillator output. Connect to an external 26/30 MHz crystal or leave floating if driving the XOUT pin with an external signal source.			
14	XIN	EZRadio peripheral crystal oscillator input. Connect to an external 26/30 MHz crystal or to an external clock source. If using an external clock source with no crystal, dc coupling with a nominal 0.8 VDC level is recommended with a minimum ac amplitude of 700 mVpp. Refer to AN417 for more details about using an external clock source.			
15	GPIO2	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			
16	GPIO3	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			
17	DNC	Do not connect.			
18	RXP	Differential RF Input Pin of the LNA. See application schematic for example matching network.			
19	RXN	Differential RF Input Pin of the LNA. See application schematic for example matching network.			
20	TX_13/16/20	Transmit Output Pin. +13 dBm for EZR32HG320FXXR55, R60, R67 and R69, +16 dBm for EZR32HG320FXXR61, and +20 dBm for EZR32HG320FXXR63 and R68 variants. The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.			
21	GND/DualTX_20	+20 dBm for EZR32HG320FXXR69 variant.			

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
22	RFVDD_2	+1.8 to +3.6 V Supply Voltage Input to Internal Regulators for the Radio. The recommended VDD supply voltage is +3.3 V.			
23	TXRAMP	Programmable Bias Output with Ramp Capability for External FET PA.			
24	RFVDD_1	+1.8 to +3.6 V Supply Voltage Input to Internal Regulators for the Radio. The recommended VDD supply voltage is +3.3 V.			
25	GPIO0	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			
26	GPIO1	General Purpose Digital I/O for the radio. May be configured to perform various EZRadio functions, including Clock Output, FIFO Status, POR, Wake-up Timer, TRSW, AntDiversity control, etc.			
27	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4	
28	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4	
29	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
30	PB11	IDAC0_OUT	TIM1_CC2 #3 PCNT0_S1IN #4		CMU_CLK1 #3
31	AVDD_1	Analog power supply 1.			
32	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
33	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
34	IOVDD_3	Digital IO power supply 3.			
35	AVDD_0	Analog power supply 0.			
36	PD4	ADC0_CH4		LEU0_TX #0	
37	PD5	ADC0_CH5		LEU0_RX #0	
38	PD6	ADC0_CH6	TIM1_CC0 #4 PCNT0_S0IN #3	USRF1_RX #2 I2C0_SDA #1	BOOT_RX
39	PD7	ADC0_CH7	TIM1_CC1 #4 PCNT0_S1IN #3	USRF1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 BOOT_TX
40	VDD_DREG	Power supply for on-chip voltage regulator.			
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
42	PC8		TIM2_CC0 #2	US0_CS #2	
43	PC9		TIM2_CC1 #2	US0_CLK #2	GPIO_EM4WU2
44	PC10		TIM2_CC2 #2	US0_RX #2	
45	USB_VREGI				
46	USB_VREGO				
47	PC14		TIM0_CDTI1 #1/6 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 LEU0_TX #5 USB_DM	PRS_CH0 #2
48	PC15		TIM0_CDTI2 #1/6 TIM1_CC2 #0	US0_CLK #3 LEU0_RX #5 USB_DP	PRS_CH1 #2

5.3 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do no have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to the LOCATION 0.

Table 5.2. Alternate Functionality Overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ADC0_CH0	PE12							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PE13							Analog to digital converter ADC0, input channel number 1.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PD6							Bootloader RX.
BOOT_TX	PD7							Bootloader TX.
CMU_CLK0			PD7	PF2				Clock Management Unit, clock output number 0.
CMU_CLK1	PA1		PE12	PB11				Clock Management Unit, clock output number 1.
DBG_SWCLK	PF0							Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1							Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
I2C0_SCL	PA1	PD7				PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6				PF0	PE12	I2C0 Serial Data input / output.
IDAC0_OUT	PB11							IDAC0 output.
LEU0_RX	PD5	PB14		PF1	PA0	PC15		LEUART0 Receive input.
LEU0_TX	PD4	PB13		PF0	PF2	PC14		LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN				PD6	PA0			Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14			PD7	PB11			Pulse Counter PCNT0 input number 1.
PRS_CH0	PA0	PF3	PC14	PF2				Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4	PC15	PE12				Peripheral Reflex System PRS, channel 1.
PRS_CH2			PE10	PE13				Peripheral Reflex System PRS, channel 2.
PRS_CH3			PE11	PA0				Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0			PA0	PF0	PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1				PF1	PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2						PF2	PF2	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0						PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1		PC14				PF4	PC14	Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2		PC15					PC15	Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0			PC8	PF2				Timer 2 Capture Compare input / output channel 0.
TIM2_CC1			PC9	PE12				Timer 2 Capture Compare input / output channel 1.
TIM2_CC2			PC10	PE13				Timer 2 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9	PC15	PB13	PB13	PE12	USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14	PE13	USART0 chip select input / output.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US0_RX	PE11		PC10	PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10			PE13	PB7			USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PC14							USB D- pin.
USB_DMPU	PA0							USB D- Pullup control.
USB_DP	PC15							USB D+ pin.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VRE-GO							USB Decoupling for internal 3.3 V USB regulator and regulator output
USRF1_RX[1]			PD6					USARTRF1 Asynchronous Receive. USARTRF1 Synchronous mode Master Input / Slave Output (MISO).
USRF1_TX[1]			PD7					USARTRF1 Asynchronous Transmit.Also used as receive input in half duplex communication. USARTRF1 Synchronous mode Master Output / Slave Input (MOSI).

Note:

1. The USART1 peripheral is shared between the radio and the external (asynchronous) communication and it is not possible to simultaneously use USART1 for external communication and communication with the radio. It is possible but not recommended to alternate between the two functions. If this is done certain precautions in timing and data must be taken. To use USART1 for communicating with the radio, see pins/location# in Radio MCU Communication Configuration table.

5.4 GPIO Pinout Overview

The specific GPIO pins available in EZR32HG320 are shown in the GPIO pinout table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Table 5.3. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	PC15	PC14	-	-	-	PC10	PC9	PC8	-	-	-	-	-	-	-	-
Port D	-	-	-	-	-	-	-	-	PD7	PD6	PD5	PD4	-	-	-	-
Port E	-	-	PE13	PE12	PE11	PE10	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	PF4	PF3	PF2	PF1	PF0

5.5 QFN48 Package

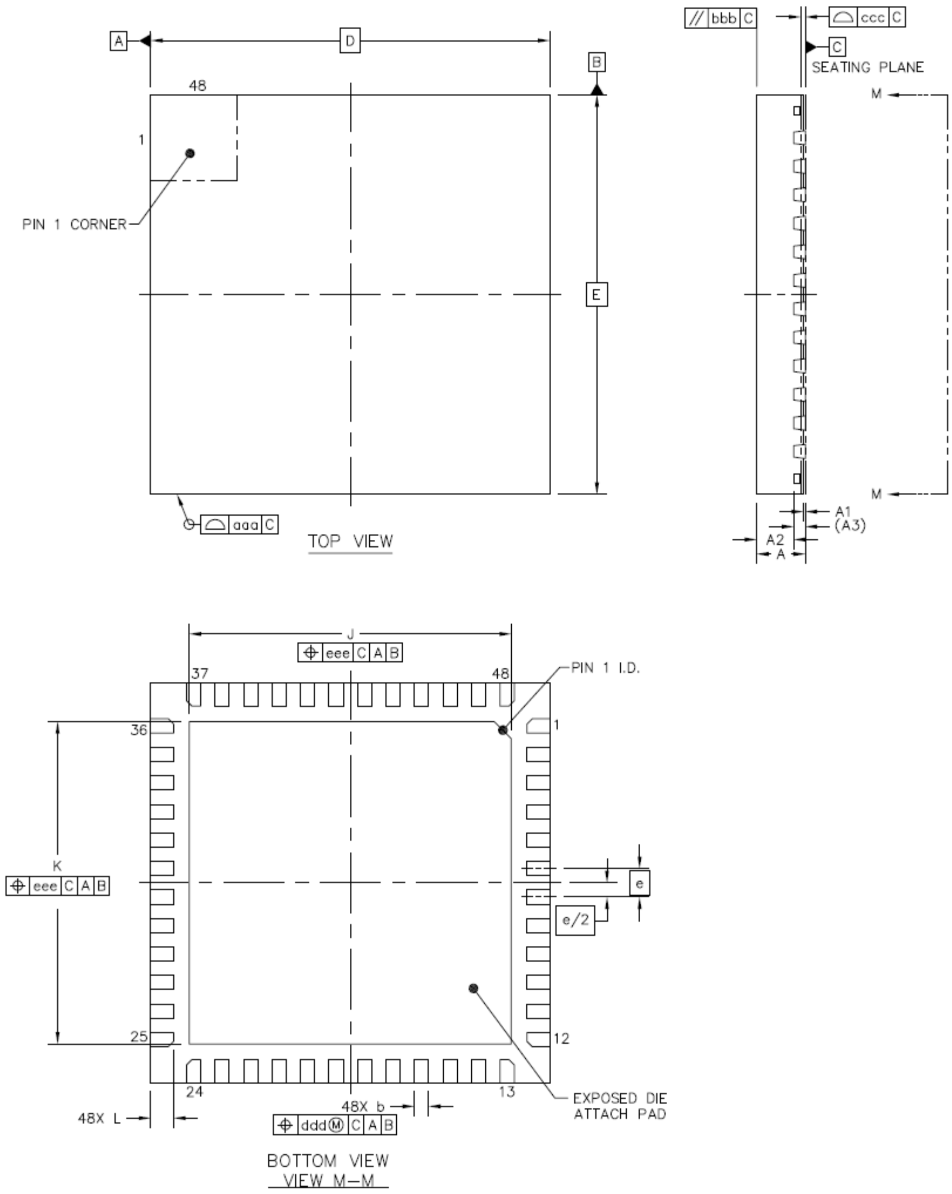


Figure 5.2. QFN48

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 5.4. QFN48 (Dimensions in mm)

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A2	---	0.65	0.67
A3	0.203 REF		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
J	5.55	5.65	5.75
K	5.55	5.65	5.75
e	0.50 BSC		
L	0.35	0.40	0.45
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
eee	0.10		

The QFN48 Package uses Matte Tin plated leadframe. All EZR32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx

6. PCB Layout and Soldering

6.1 Recommended PCB Layout

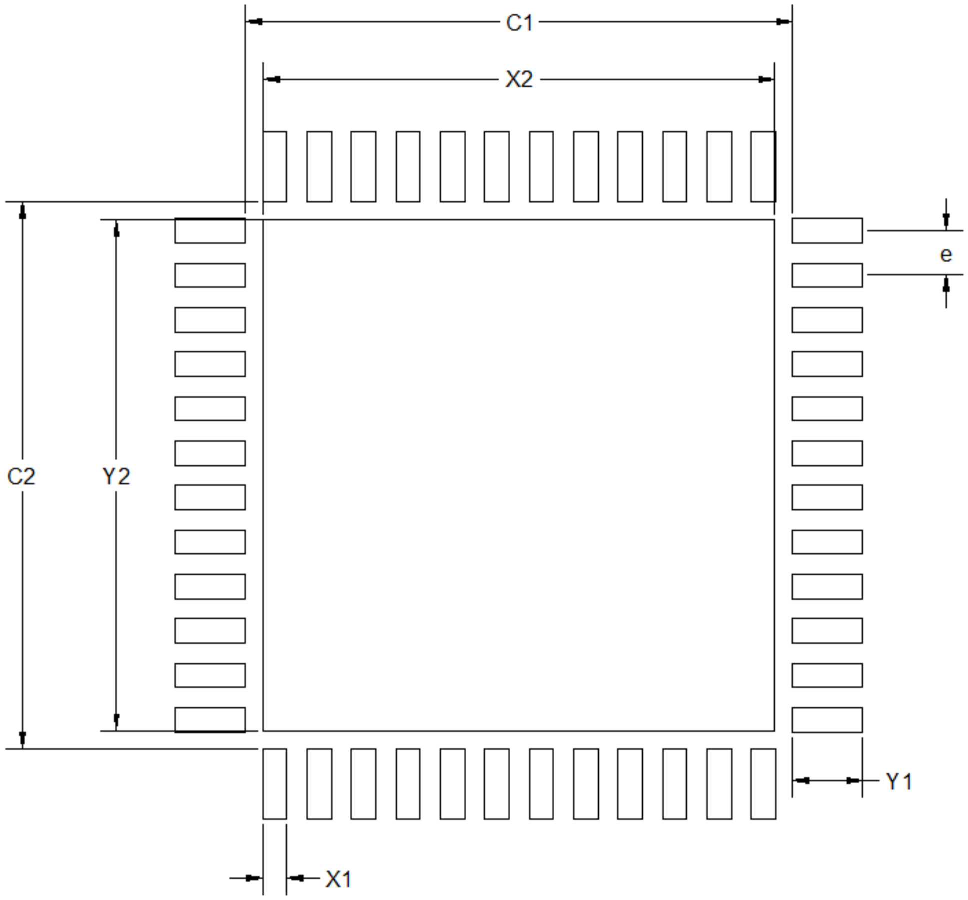


Figure 6.1. PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (Dimensions in mm)

Dimension	MIN	MAX
C1	6.05	6.25
C2	6.05	6.25
e	0.50 BSC	
X1	0.17	0.37
X2	5.65	5.85
Y1	0.69	0.89
Y2	5.65	5.85

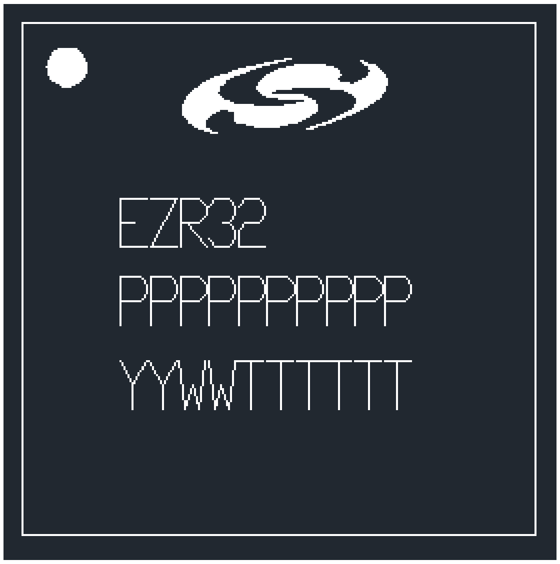
Dimension	MIN	MAX
Note: **General** 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. 4. A 4x4 array of 1.1 mm square openings on 1.3 mm pitch should be used for the center ground pad. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

6.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

7. Top Marking

The top marking is illustrated and explained below.



Mark Method:	Laser	
Logo Size:	Top center	
Font Size:	0.71 mm Left-Justified	
Line 1 Marking:	FFFFFFFFFF = Family Part Number (EZR32)EZR32	Refer to the line marking instruction from assembly PO.

Line 2 Marking:	PPPPPPPPPP = Part Number
	• P_1P_2: HG = Happy Gecko
	• $P_3P_4P_5$: 320 (USB)
	• P_6P_7: Flash Size
	  • FD = 32
	  • FE = 64
		• P_8P_9: Radio
		  • 55 = EZRadio +13 dBm, -116 sensitivity
		  • 60 = EZRadioPRO +13 dBm, -129-126 sensitivity
		  • 61 = EZRadioPRO +16 dBm, -129-126 sensitivity
		  • 63 = EZRadioPRO +20 dBm, -129-126 sensitivity
		  • 67 = EZRadioPRO +13 dBm, -133 sensitivity
		  • 68 = EZRadioPRO +20 dBm, -133 sensitivity
		  • 69 = EZRadioPRO +13 & 20 dBm, -133 sensitivity
		• P_{10}: Temperature Range
		  • G = -40 — 85 °C

Line 3 Marking:	YY = Year	Assigned by the Assembly House.
	WW = Work Week	Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order from assembly PO.
Line 4 Marking:	Circle = 1.3 mm diameter; center justified	"e3" Pb-Free Symbol
	Gecko Logo; right justified	Gecko Logo height = 1.90 mm

8. Revision History

Revision 1.2

April, 2020

- In 4.11 Analog Digital Converter (ADC):
  - Updated test conditions, updated specifications, and added footnote for average active current.
  - Added input bias current.
  - Added input offset current.
  - Updated ADC clock frequency.
  - Input ON resistance (R_{ADCIN}) changed from 1 MΩ minimum to 300 Ω minimum and 800 Ω maximum.
  - Updated SNR, SINAD and SFDR.
  - Updated offset voltage.
  - Updated missing codes specification (MC_{ADC}).
  - Added gain error drift and offset error drift.
  - Removed ADC internal voltage reference.
  - Added VREF output voltage, VREF voltage drift, VREF temperature drift, VREF current consumption, and ADC and DAC VREF matching.

Revision 1.1

August, 2019

- Updated Ordering Information table for the release of revision C devices
- Added footnote to USRF1_TX and USRF1_RX in Alternate Functionality Overview table
- Updated PCB Land Pattern Dimensions table to fix typographical error
- New formatting throughout

Revision 1.0

- Added R69 content

Revision 0.4

- Removed content currently documented the RFI database:
  - Environmental Table from the Electrical Specifications chapter
  - Moisture Sensitivity Level in the Soldering Information section

Revision 0.3

- Updated Current Consumption table
- Updated Power Management table
- Revised text describing LFXO Oscillator: “energyAware Designer” to “Configurator tool”
- Updated HFXO oscillator table, fHXFO parameter changed: “Supported nominal crystal Frequency” to “Supported frequency, any mode”
- Updated LFRCO table
- Updated HFRCO table
- Updated AUXHFRCO table
- Updated USHFRCO table
- Updated ADC table
- Added USB electrical table

Revision 0.2

- Initial Release