DESCRIPTION

This document describes the specifications for the F1130 Dual Path RF Receiver consisting of RF amplifier with bypass, DSA, RF Mixer and IF amplifier in each signal path. Applications include Multi-mode, Multi-carrier BaseStation Receivers. F1130 supports the following frequencies: RF from 400MHz to 1100MHz, LO from 500MHz to 1300MHz, and IF from 25MHz to 400MHz. Refer to the Part # Matrix below describing the complete series.

The F1130 RF front-end offers 19dB gain with 3.5dB NF and +37dBm OIP3 performance. The digital step attenuator provides 30dB adjustment range in 2dB steps via the SPI interface controller. For strong signal conditions, each RF amplifier can be bypass controlled via the SPI interface. The RF front-end output and mixer input signals are bonded to separate pins to allow interstage image-reject filtering.

Each of the dual mixer paths provide 9 dB power gain, 10.3dB NF and +36dBm OIP3 performance. An external LO signal is applied to the mixer LO port.

This device is packaged in a 7 x 7 mm, 48-pin Thin QFN with 50 ohm single-ended RF & LO inputs and 200 ohm differential IF output impedance for ease of integration into the receiver lineup.

COMPETITIVE ADVANTAGE

The on-chip 4-bit RF digital step attenuator (DSA) has very low insertion loss and low distortion.

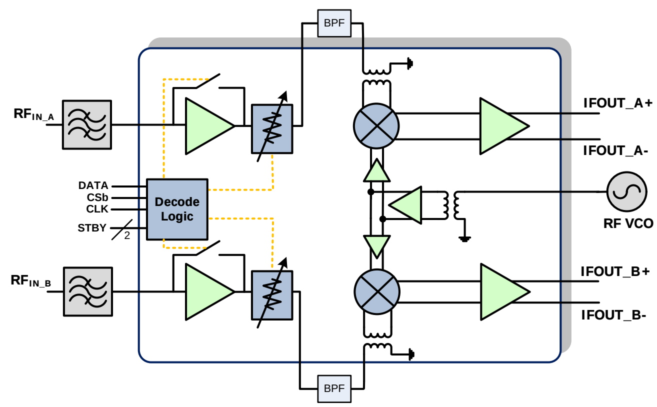
The F1130 has very low power consumption thus allowing it to be packaged in very compact 7x7 solution

- ✓ GlitchFree™ Technology
- ✓ Extremely accurate with low distortion
- ✓ Very small solution area

FEATURES

- Dual Path for Diversity / MIMO
- Glitch-Free™ Technology
- RF: 400MHz to 1100MHz
- LO: 500MHz to 1300MHz
- IF: 25MHz to 400MHz
- Bypassable RF amplifiers for strong signal conditions
- 19dB RF front-end power gain
- +37dBm RF front-end OIP3 (Bypass OFF)
- +43dBm RF front-end OIP3 (Bypass ON)
- 3.5dB front-end NF AT 900MHz
- 9dB mixer power gain (HS LO)
- +36dBm mixer OIP3
- 50Ω RF and LO impedance
- 200Ω differential IF output impedance
- Independent CHA, CHB path standby mode
- 30dB gain control range, 2dB steps
- 3 bit SPI control
- Total I_{CC} = 360mA
- 7 x 7 mm, 48-pin VFQFPN package

FUNCTIONAL BLOCK DIAGRAM



PART# MATRIX

Part#	RF freq range (MHz)	UTRA bands	IF freq range (MHz)	LO freq range (MHz)
F1130	400 - 1100	5,6,8,12,13,14,1718,19,20, 26	25 – 400	500 - 1300
F1180	1400 - 2700	1,2,3,4,7,9,10, 11,15,16,21,23, 24,25,33,34,35, 36,37,39,40,41	25 – 400	1350 - 2900

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
VCC to GND	V_{CC}	-0.3	+5.5	V
SPI DATA, SPI LE, SPI CLK, STBY_A, STBY_B	V_{Logic}	-0.3	V_{cc} + 0.25	V
IFOUT_A+, IFOUT_A-, IFOUT_B+, IFOUT_B-,	I_{IF}	1.00	V_{cc} + 0.30	V
LO_IN, RFIN_A, RFIN_B, MIXRFIN_A, MIXRFIN_B	V_{Cntl}	-0.3	+0.30	V
LO_BIAS	V_{LO}	+2.1	+4.0	V
RFA_BIAS, RFB_BIAS	V_{RFIN}	-0.3	+1.50	V
RFAMP_BIAS, IFA_BIAS, IFB_BIAS	V_{Bias}	-0.3	+2.20	V
Maximum RF Input Power – Bypass OFF (1hr < duration < 2hr @ Tcase = 105C)	P_{RFIN_A} P_{RFIN_B}		+24	dBm
Maximum RF Input Power – Bypass ON (1hr < duration < 2hr @ Tcase = 105C)	P_{RFIN_A} P_{RFIN_B}		+24	dBm
Maximum RF Input Power to Mixer (1hr < duration < 2hr @ Tcase = 105C)	P_{RFMIX_A} P_{RFMIX_B}		+21	dBm
Continuous Power Dissipation	P_{diss}		2.15	W
Junction Temperature	T_j		+150	°C
Storage Temperature Range	T_{st}	-65	+150	°C
Lead Temperature (soldering, 10s)			+260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			2000 (Class 2)	Volts
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			250 (Class C3)	Volts

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	32 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	3 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1130 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{CC}	All VCC pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
RF Freq Range	F_{RF}		400		1100	MHz
LO Freq Range	F_{LO}		500		1300	MHz
LO Power	P_{LO}		-3		+3	dBm
IF Freq Range	F_{IF}		25		400	MHz
RF Amplifier Source Impedance	Z_{RFIN_A} Z_{RFIN_B}	Single Ended		50		Ω
RF Amplifier Load Impedance	Z_{RFOUT_A} Z_{RFOUT_B}	Single Ended		50		Ω
Mixer RF Source Impedance	$Z_{MXRRFIN\_A}$ $Z_{MXRRFIN\_B}$	Single Ended		50		Ω
Mixer LO Source Impedance	$Z_{MXRLOIN\_A}$ $Z_{MXRLOIN\_B}$	Single Ended		50		Ω
Mixer IF Load Impedance	$Z_{MXRIFOUT\_A}$ $Z_{MXRIFOUT\_B}$	Differential		200		Ω

F1130 SPECIFICATION

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
General						
Logic Input High	V_{IH}	All Control Pins	***1.17***			V
Logic Input Low	V_{IL}	All Control Pins			***0.67***	V
Logic Current	I_{IH}, I_{IL}	All Control Pins	***-120***		***+120***	µA
Standby Mode Logic	STBY	STBY = V_{IH} or Floating	Power OFF			
		STBY = V_{IL}	Power ON			
Supply Current	I_{CC_ON}	Bypass OFF, 2 Channels		***360***	***410***[1]	mA
	I_{CC_OFF1}	Bypass ON, 1 Channels (CHA or CHB)		***295***	***330***	
	I_{CC_OFF2}	Bypass ON, 2 Channels (CHA and CHB)		***230***	***260***	
	I_{CC_STBY}	Standby Mode		***20***	***26***	
RF Switching time[3]	τ_{RF}	10% to 90% risetime		250		ns
DSA Settling time[3]	τ_{SET}	10% to 90% risetime		100		ns
Turn ON time[3]	τ_{ON}	10% to 90% risetime		225		ns
Turn OFF time[3]	τ_{OFF}	10% to 90% risetime		25		ns
Control Interface	SPI_{BIT}			14		bit
Serial Clock Speed	SPI_{CLK}				***24***	MHz

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).
Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

F1130 SPECIFICATION (CONTINUED)

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF VGA – Bypass OFF						
Gain[4]	G_{VGA}		***17.5***	***19***	***20.5***	dB
Gain Flatness	G_{VGA_FLAT}	F_{RF} = 400 MHz to 110 MHz over any 100 MHz bandwidth		± 0.3		dB
Gain Variation	G_{VGA_T}	T_{case} =-40 to +105 °C		-0.4 to +0.2		dB
Noise Figure	NF_{VGA}			3.5		dB
Input 1 dB Power Compression	$IP1dB_{LBVGA}$			0		dBm
Output Third Order Intercept Point	$OIP3_{VGA}$	Pout = 0 dBm/Tone, 1 MHz tone separation	34[2]	37		dBm
RF VGA – Bypass ON						
Gain	G_{BYPASS}		***-3.5***	***-2.5***		dB
Gain Flatness	G_{BYPASS_FLAT}	F_{RF} = 400 MHz to 1100 MHz over any 100 MHz bandwidth		± 0.2		dB
Gain Variation	G_{BYPASS_T}	T_{case} =-40 to +105 °C		± 0.25		dB
Input 1 dB Power Compression	$IP1dB_{LBBYPASS}$			22		dBm
Output Third Order Intercept Point	$OIP3_{BYPASS\_0}$	Attenuation = 0dB 1 MHz tone separation	40	43		dBm
Output Third Order Intercept Point	$OIP3_{BYPASS\_6}$	Attenuation = 6dB 1 MHz tone separation	34	37		dBm
RF VGA – Bypass ON or OFF						
DSA Gain Control Range	DSA_{RANGE}			30		dB
DSA Gain Step	DSA_{STEP}			2		dB
Gain Accuracy	DSA_{ACC}		***±(0.05 + 0.04*ATTN) Max***			dB
Channel Isolation	ISO_{A-B} ISO_{B-A}	RFA Input to RFB Output RFB Input to RFA Output	46	52		dB
VGA Input Match	$S11_{VGA}$			-15		dB
VGA Output Match	$S22_{VGA}$			-15		dB
Isolation between VGA RFout and Mixer RFin	$ISO_{VGA/MIX}$	No Connection between ports	47	50		dB

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).
Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

F1130 Specification (continued)

Specifications apply at V_{CC} = +5.00V, T_{CASE} = +25°C, F_{RF} = 900MHz, F_{IF} = 199MHz, F_{LO} = 1099MHz, P_{LO} = 0dBm, For bypass ON, RF VGA input = +5dBm, for Bypass OFF, RF VGA input = -20dBm/tone, Attenuator = 0dB, STBY_A, STBY_B = GND unless otherwise noted. Trace, Connector, and external transformer losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Mixer						
Gain	G_{MXR}		***8***	***9***	***10***	dB
Gain Flatness	G_{MXR_FLAT}	F_{RF} = 1400 MHz to 2700 MHz over any 100 MHz bandwidth		± 0.2		dB
IF Gain Flatness Bandwidth	G_{IF_FLAT1}	Fixed LO Flatness = 0.5 dB		200		MHz
	G_{IF_FLAT2}	Fixed LO Flatness = 0.8 dB		300		MHz
Gain Variation	G_{MXR_T}	T_{case} =-40 to +105 °C		± 0.8		dB
Noise Figure	NF_{MXR}			10.3		dB
Blocking Noise Figure	NF_{MXR_BLK}	+75 MHz offset Pin (Blocker) = + 4dBm		17.5		dB
Input 1 dB Compression	$IP1dB_{MXR}$		***7***	***9***		dBm
Output Third Order Intercept Point	$OIP3_{MXR}$	1 MHz tone separation	33	36		dBm
Output Second Order Intercept Point	$OIP2_{MXR}$	1 MHz tone separation		58		dBm
2RF – 2LO rejection	$2x2_{MXR}$	F_{RF} – F_{IF}/2		68		dBc
3RF – 3LO rejection	$3x3_{MXR}$	Frequency = F_{RF} – 2*F_{IF}/3		70		dBc
Second Harmonic	$HD2_{MXR}$			65		dBc
Third Harmonic	$HD3_{MXR}$			80		dBc
Settling Time	τ_{MXR_SET}	Pin = -13 dBm STBY VIH to VIL Time for IF to settle to 0.1 dB of final value		170		ns
Mixer RF Input Match	$S11_{MXR\_RF}$			-15		dB
Mixer LO Input Match	$S11_{MXR\_LO}$			-15		dB
Mixer IF Output Match	$S22_{MXR\_IF}$			-13		dB
Channel Isolation	ISO_{IF}	IFOUT_A to IFOUT_B		70		dBc
RF to IF Isolation	ISO_{RI}	Pin = -10 dBm Ratio of IF level to RF leakage at IF port		36		dBc
LO to RF Leakage	ISO_{LR}			-47		dBm
LO to IF Leakage	ISO_{LI}			-37		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Speeds are measured after SPI programming is completed (data latched with LE = HIGH).
Note 4: Gain across the entire frequency band is affected by the inclusion of the RF switch.

Serial Control Mode

Data is clocked in LSB first via serial mode. Serial data is formatted as a 14-bit word. The 14-bit word contains logic for bypass mode, 4-bit attenuator setting, and guard bit. Each word contains the following sequence:

Table 1 - 14 Bit SPI Word Sequence

D13	RX Path 2 bypass mode
D12	Guard bit
D11	RX Path 1 bypass mode
D10	Guard bit
D9	Attenuator 2
D8	Attenuator 2
D7	Attenuator 2
D6	Attenuator 2
D5	Guard bit
D4	Attenuator 1
D3	Attenuator 1
D2	Attenuator 1
D1	Attenuator 1
D0	Guard bit

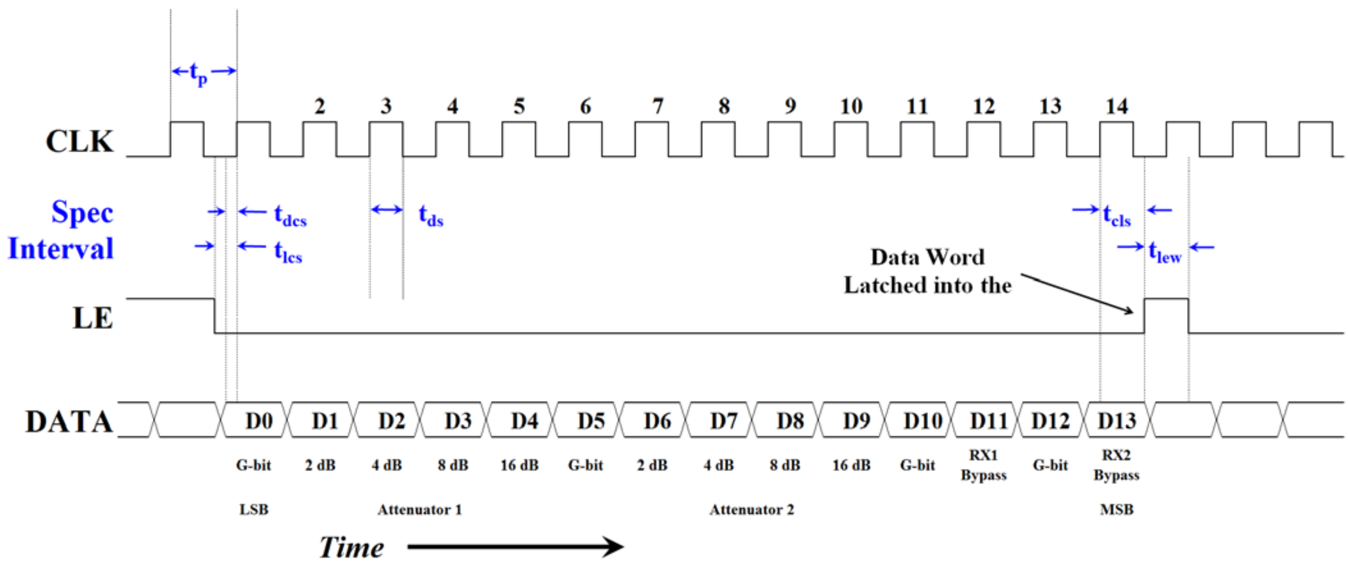


Figure 1 - Serial Register Timing Diagram

Table 2 - SPI Preset Timing Parameters Calcuated for 24 MHz

Parameter	Symbol	Min	Typ	Max	Units
Clock Period (Frequency)	t_p			41.66 (24)	ns (MHz)
Data Setup	t_{ds}		20.83		ns
Data to CLK Setup Time	t_{dcs}	5			ns
LE to CLK Setup Time	t_{lcs}	5			ns
CLK to LE Setup Time	t_{cls}	5			ns
LE Pulse Time	t_{lew}		20		ns

Table 3 – Attenuator Data Word Bit Sequence

Attenuation Setting	Attenuator 1 D4, D3, D2, D1	Attenuator 2 D9, D8, D7, D6
Insertion Loss	0000	0000
2 dB	0001	0001
4 dB	0010	0010
6 dB	0011	0011
8 dB	0100	0100
10 dB	0101	0101
12 dB	0110	0110
14 dB	0111	0111
16 dB	1000	1000
18 dB	1001	1001
20 dB	1010	1010
22 dB	1011	1011
24 dB	1100	1100
26 dB	1101	1101
28 dB	1110	1110
30 dB	1111	1111

Table 4 - RF Bypass Data Word Bit Sequence

RF Switch ByPass Mode	RX1 D11	RX2 D13
OFF	0	0
ON	1	1

PIN 8 LATCH ENABLE (LE):

When LE is high (> VIH), the CLK input is disabled. Renesas recommends keeping LE high to reduce F1130 sensitivity to CLK bus noise when SPI is not being programmed. When LE is low (< VIL), the DATA word can be programmed into the shift registers. The programmed word is then latched into F1130 on the LE rising edge (refer to Figure 1). End of data occurs after 14^{th} bit.

DEFAULT REGISTER SETTING:

After power on, the default setting for the VGA is Bypass OFF mode with attenuation set to 30 dB. This means the amplifier is in the signal path with maximum attenuation.

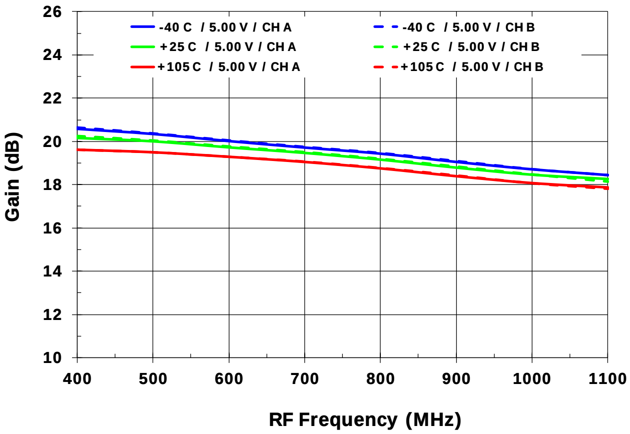
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

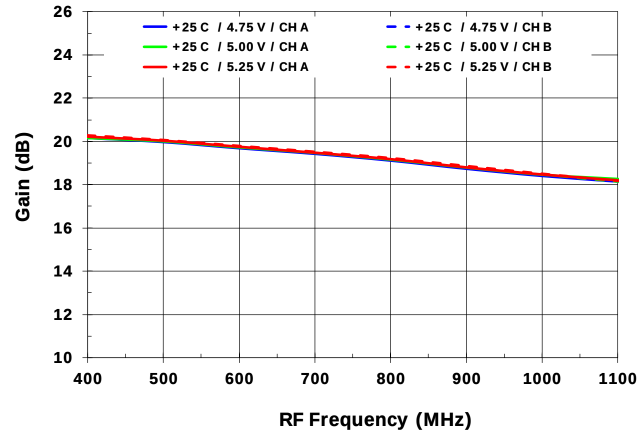
- **V_{CC} = +5.00 V**
- **T_{CASE} = +25 °C**
- **F_{RF} = 900 MHz**
- **F_{IF} = 199 MHz**
- **F_{LO} = 1100 MHz**
- **P_{LO} = 0 dBm**
- **RF VGA output = -5 dBm/tone**
- **RF Mixer output = 0 dBm/tone**
- **Attenuator = 0 dB**
- **STBY_A, STBY_B = GND**

VGA BYPASS OFF: TYPICAL OPERATING CONDITIONS (- 1 -)

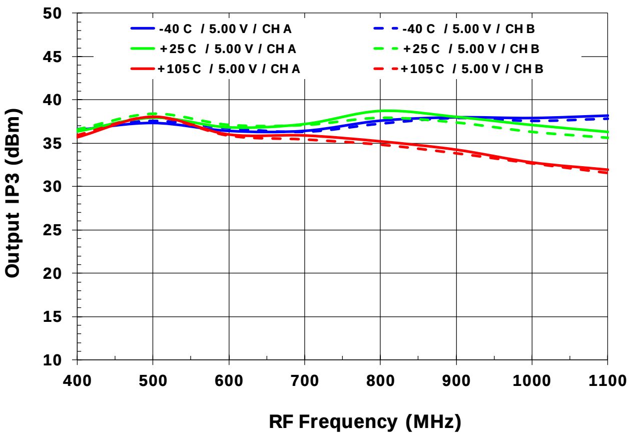
Gain vs. T_{case} [G_{VGA}]



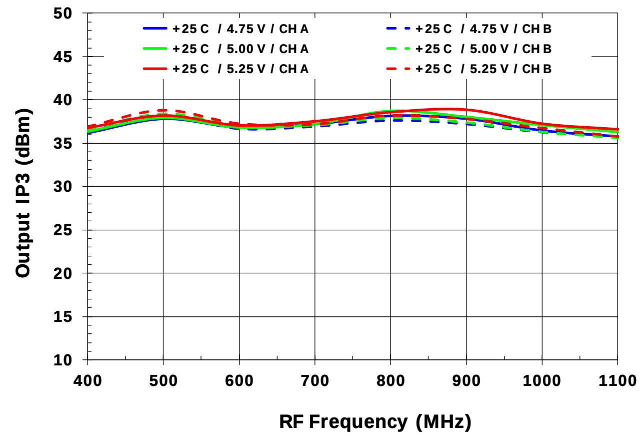
Gain vs. V_{cc} [G_{VGA}]



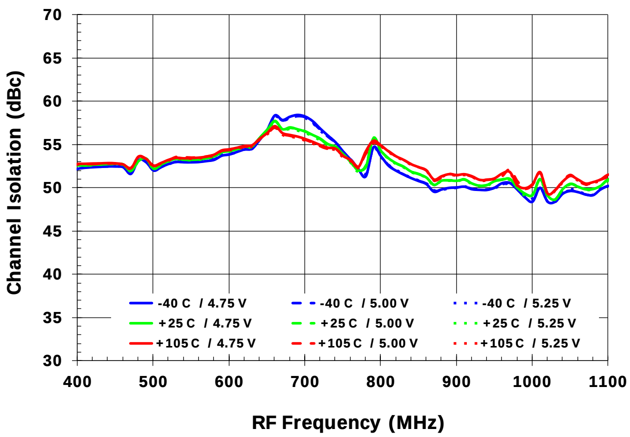
Output IP3 vs. T_{case} [$OIP3_{VGA}$]



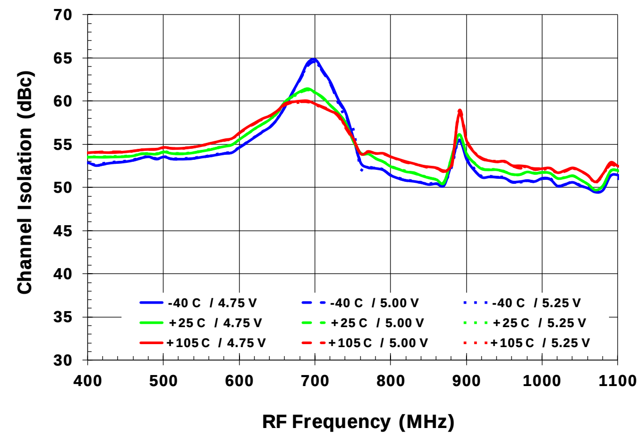
Output IP3 vs. V_{cc} [$OIP3_{VGA}$]



Channel Isolation vs. T_{case} & V_{cc} [ISO_{A-B}]

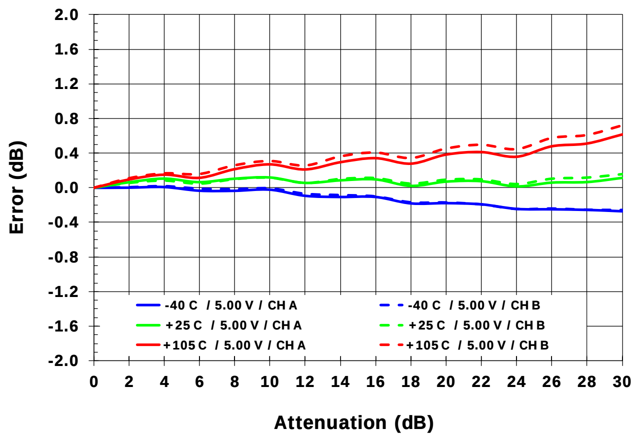


Channel Isolation vs. T_{case} & V_{cc} [ISO_{B-A}]

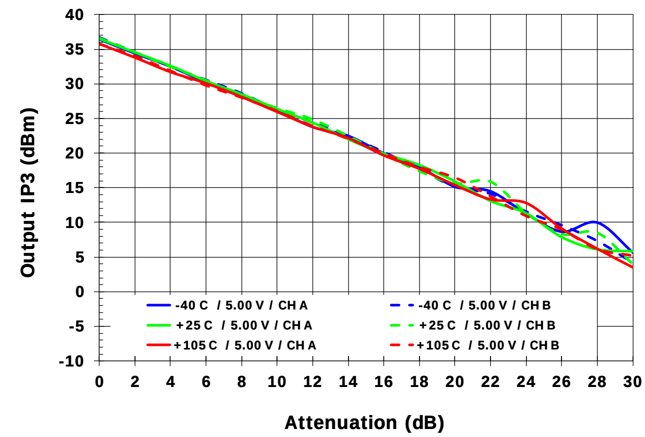


VGA BYPASS OFF: TYPICAL OPERATING CONDITIONS (- 2 -)

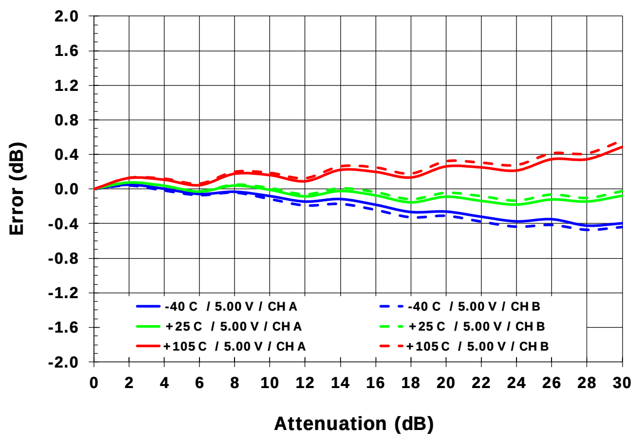
Gain Accuracy [DSA_{ACC} 400 MHz]



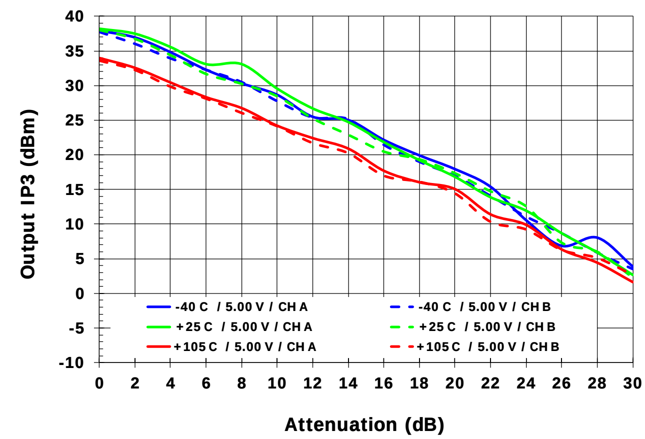
OIP3 vs. Attenuation [400 MHz]



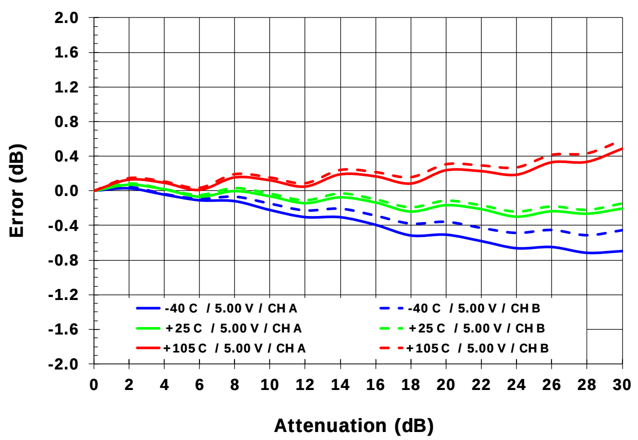
Gain Accuracy [DSA_{ACC} 900 MHz]



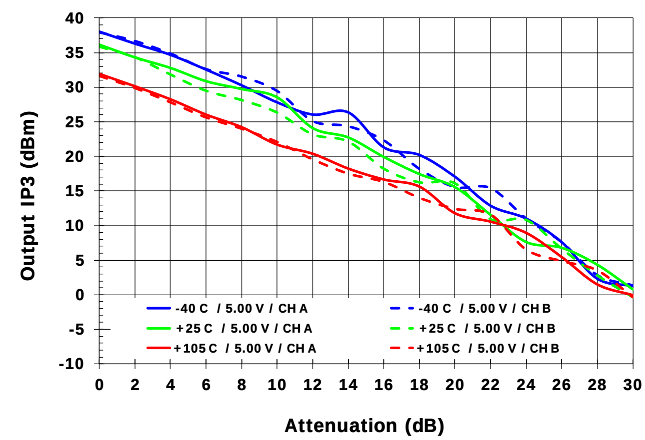
OIP3 vs. Attenuation [900 MHz]



Gain Accuracy [DSA_{ACC} 1100 MHz]

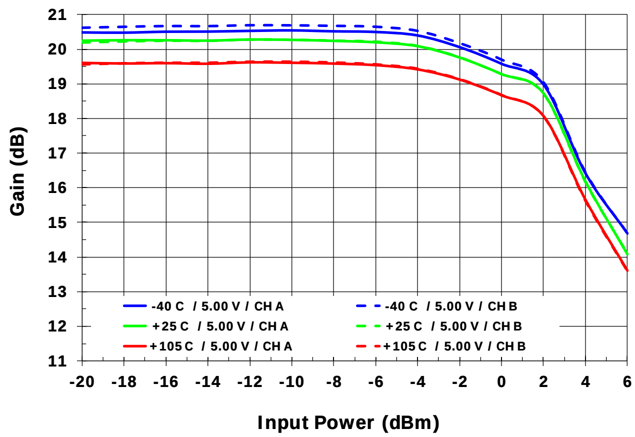


OIP3 vs. Attenuation [1100 MHz]

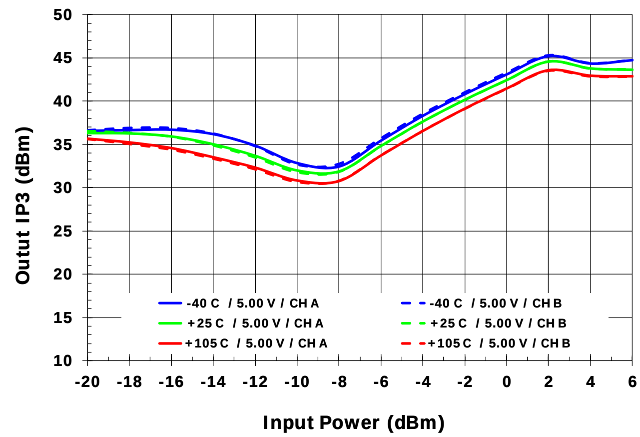


VGA Bypass OFF: Typical Operating Conditions (- 3 -)

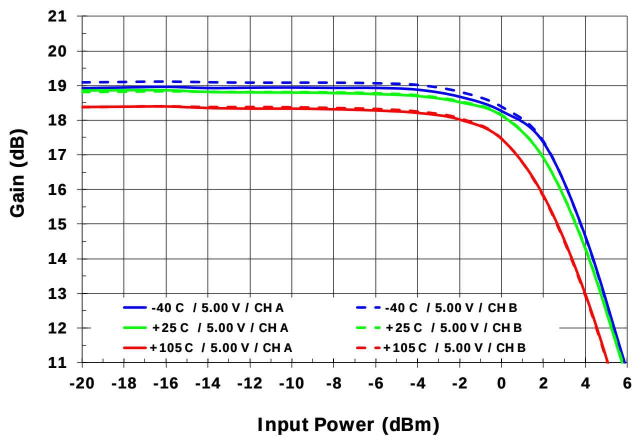
Gain vs. Input Power [400 MHz]



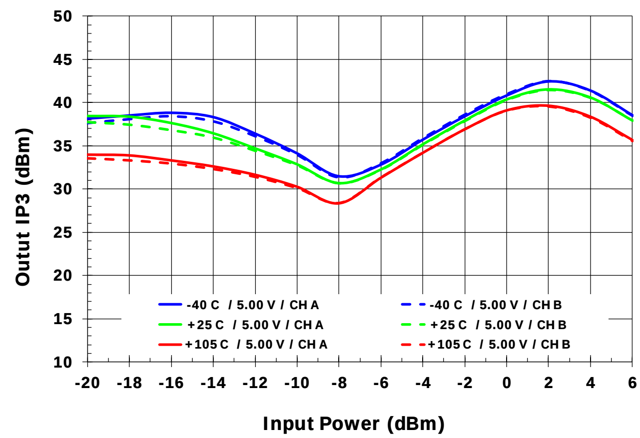
OIP3 vs. Input Power [400 MHz]



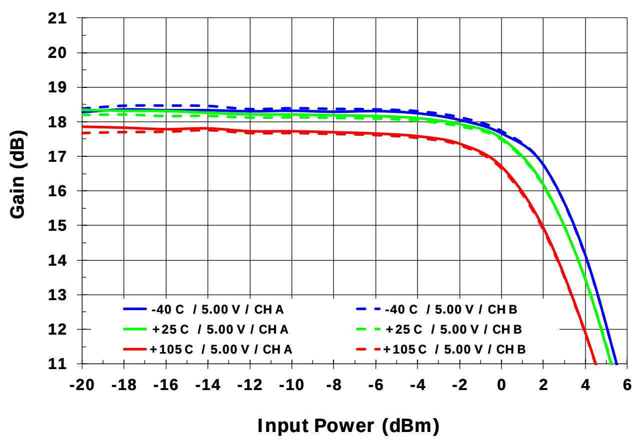
Gain vs. Input Power [900 MHz]



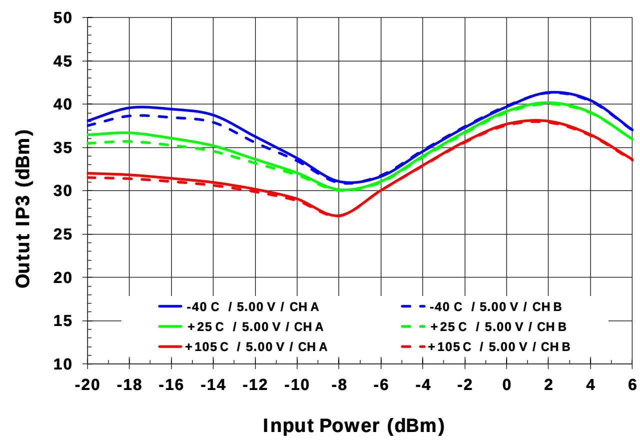
OIP3 vs. Input Power [900 MHz]



Gain vs. Input Power [1100 MHz]

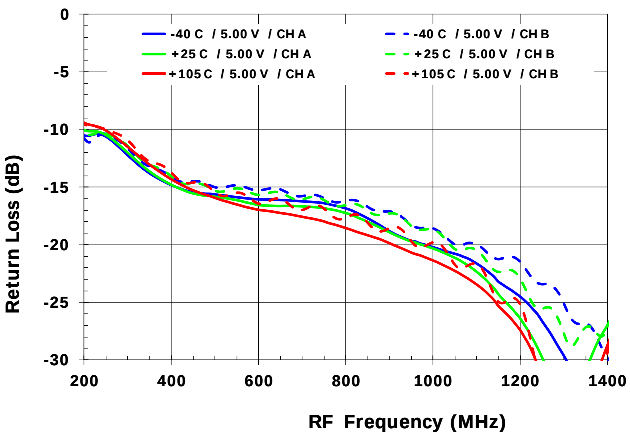


OIP3 vs. Input Power [1100 MHz]

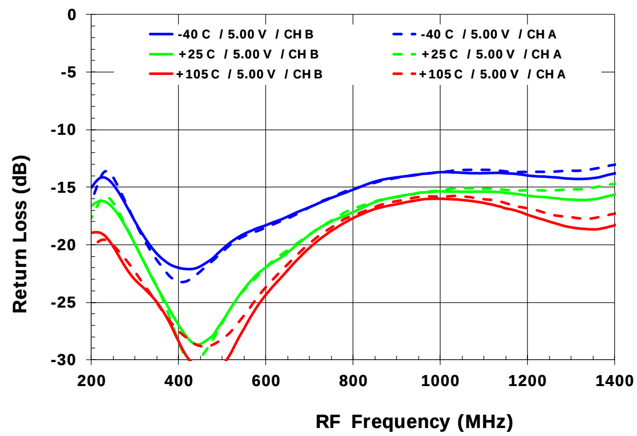


VGA BYPASS OFF: TYPICAL OPERATING CONDITIONS (- 4 -)

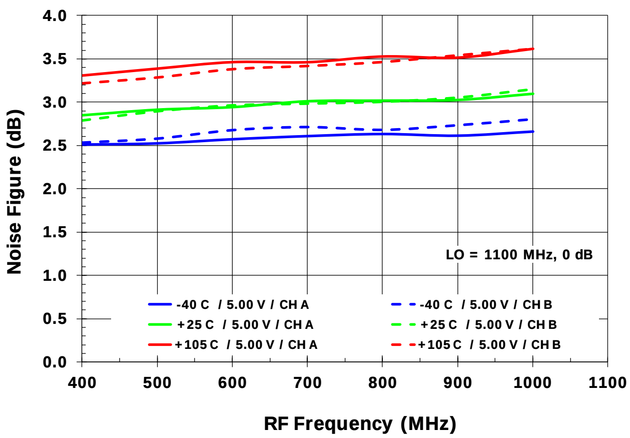
Input Match – [S11$_{VGA}$]



Output Match – [S22$_{VGA}$]

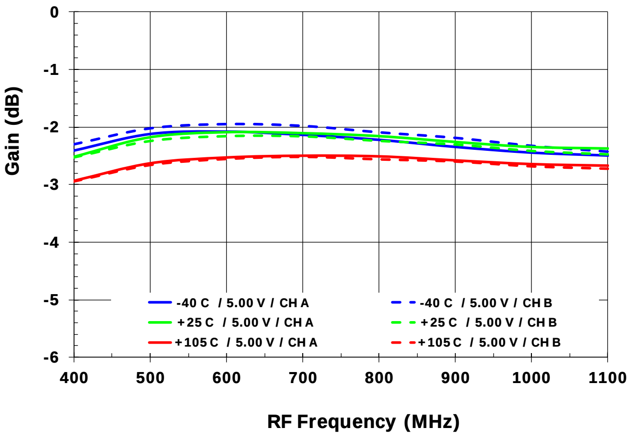


Noise Figure [NF$_{VGA}$]

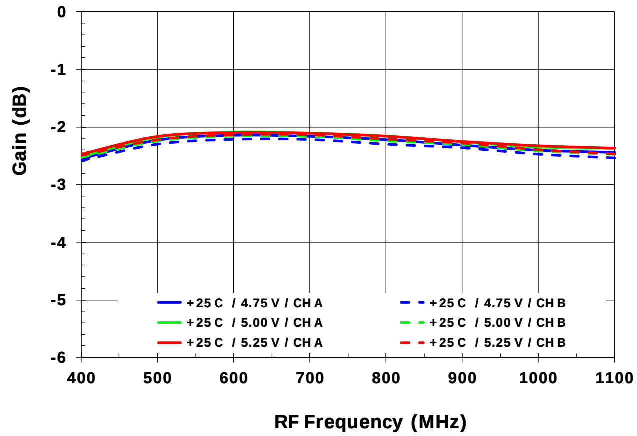


VGA BYPASS ON: TYPICAL OPERATING CONDITIONS (- 5 -)

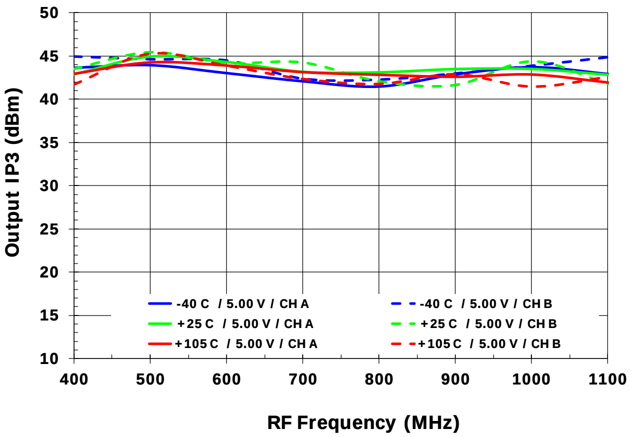
Gain vs. T_{case} [G_{BYPASS}]



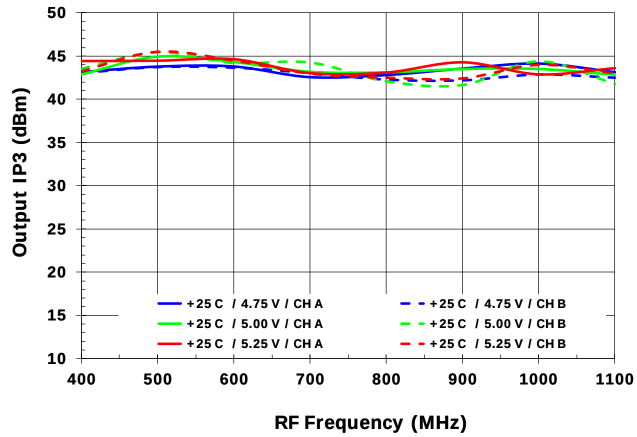
Gain vs. V_{cc} [G_{BYPASS}]



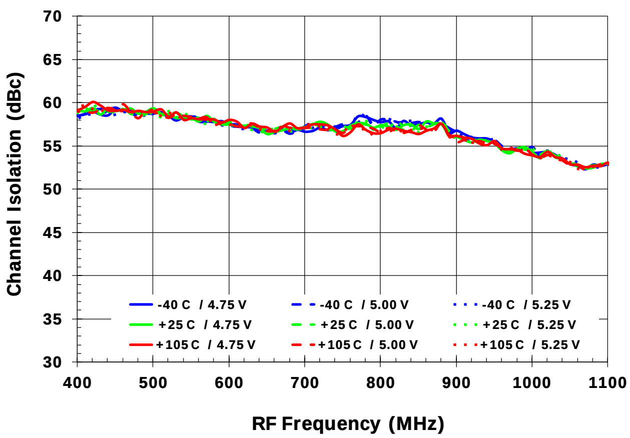
Output IP3 vs.T_{case} [$OIP3_{BYPASS\_0}$]



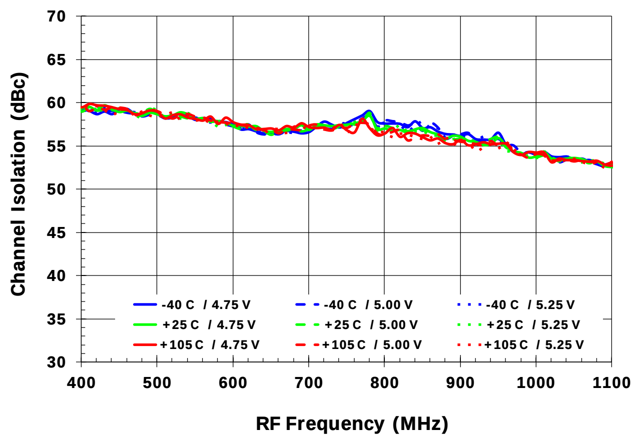
Output IP3 vs.V_{cc} [$OIP3_{BYPASS\_0}$]



Channel Isolation vs. T_{case} & V_{cc} [ISO_{A-B}]

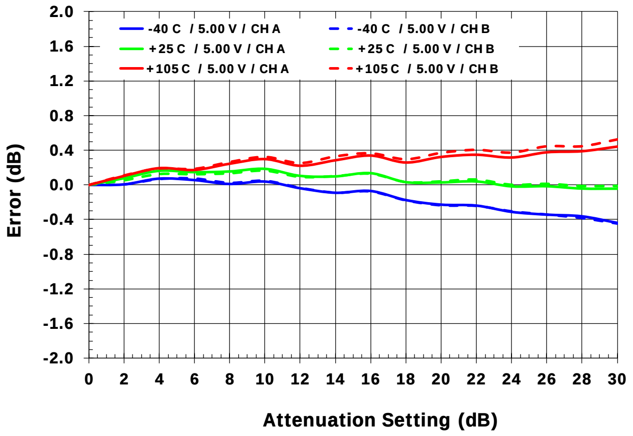


Channel Isolation vs. T_{case} & V_{cc} [ISO_{B-A}]

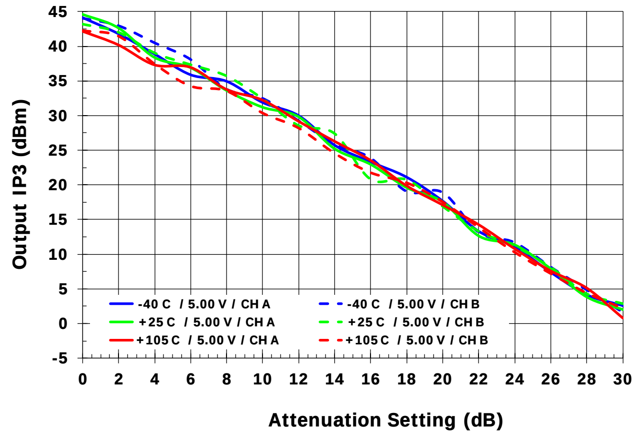


VGA BYPASS ON: TYPICAL OPERATING CONDITIONS (- 6 -)

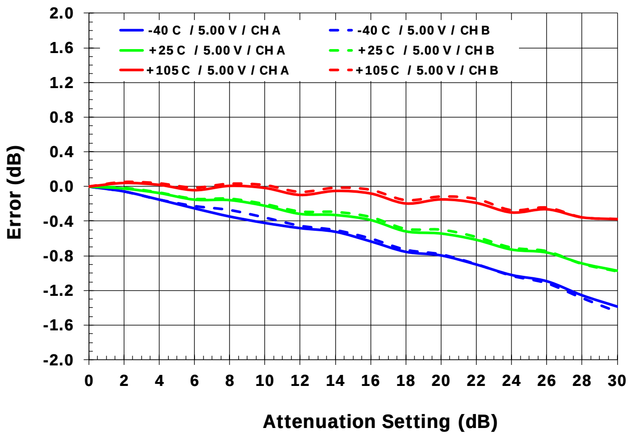
Gain Accuracy [DSA_{ACC} 400 MHz]



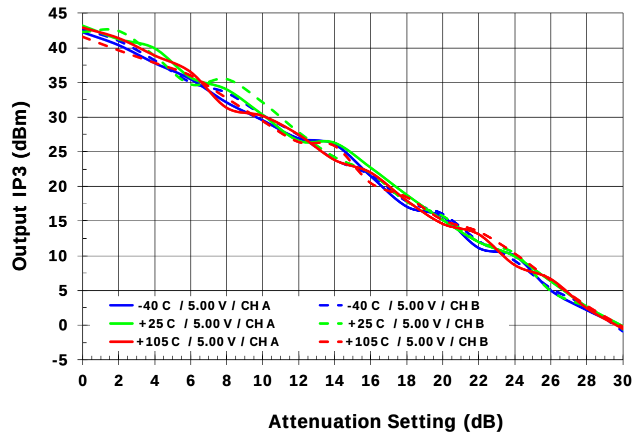
OIP3 vs. Attenuation [400 MHz]



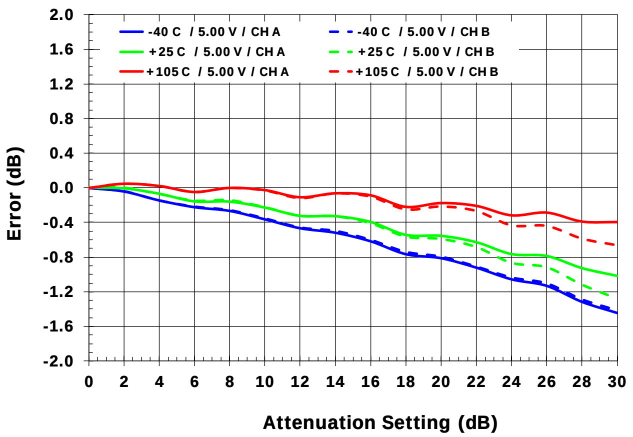
Gain Accuracy [DSA_{ACC} 900 MHz]



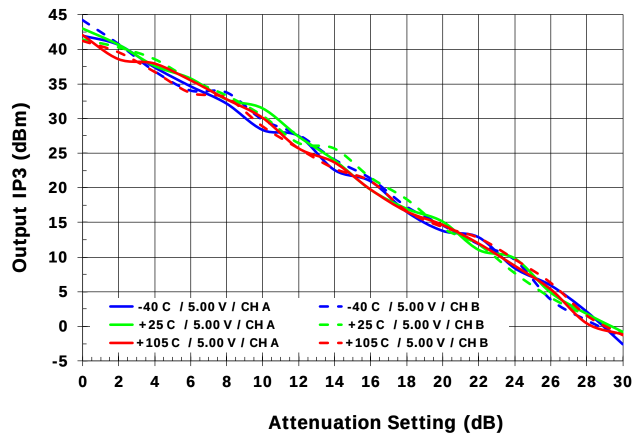
OIP3 vs. Attenuation [900 MHz]



Gain Accuracy [DSA_{ACC} 1100 MHz]

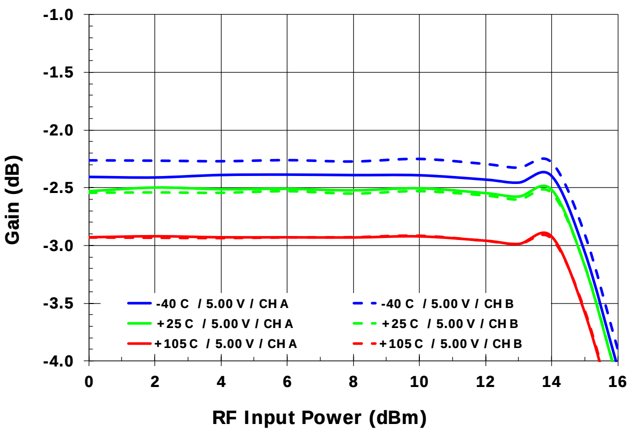


OIP3 vs. Attenuation [1100 MHz]

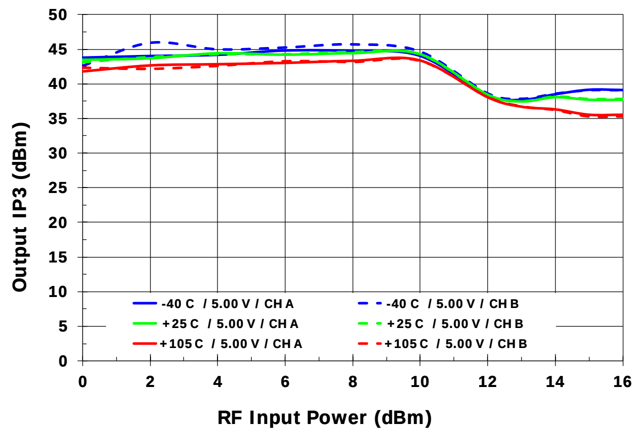


VGA BYPASS ON: TYPICAL OPERATING CONDITIONS (- 7 -)

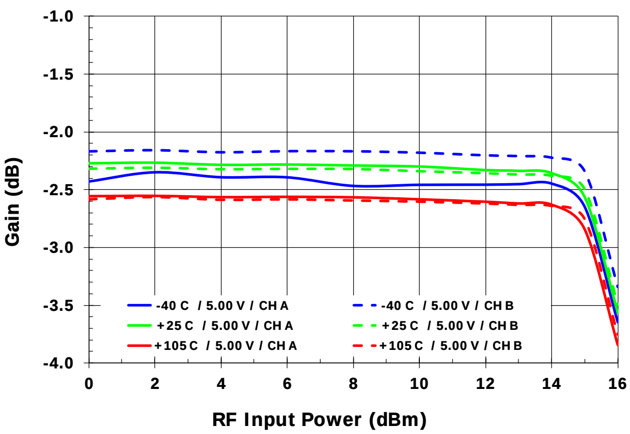
Gain vs. Input Power [400 MHz]



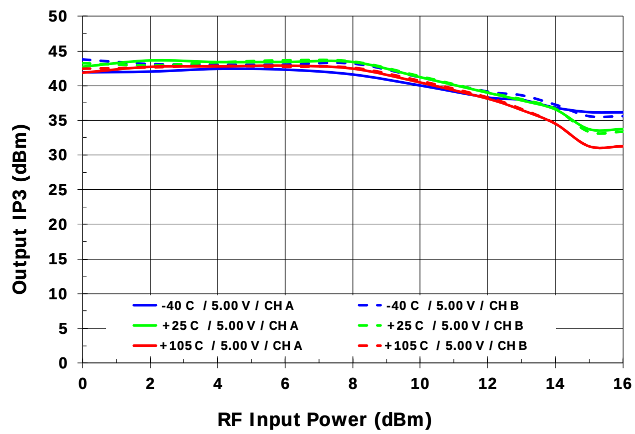
OIP3 vs. Input Power [400 MHz]



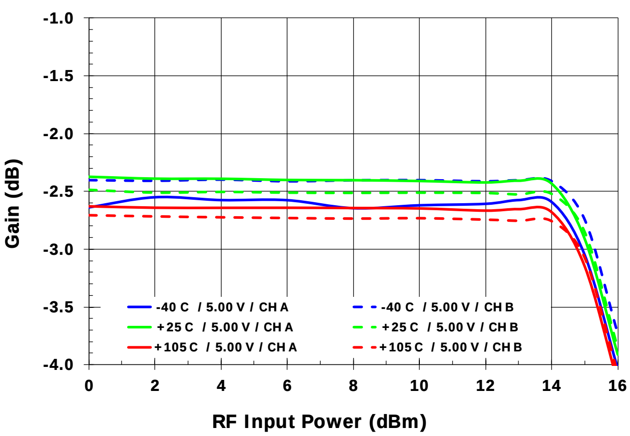
Gain vs. Input Power [900 MHz]



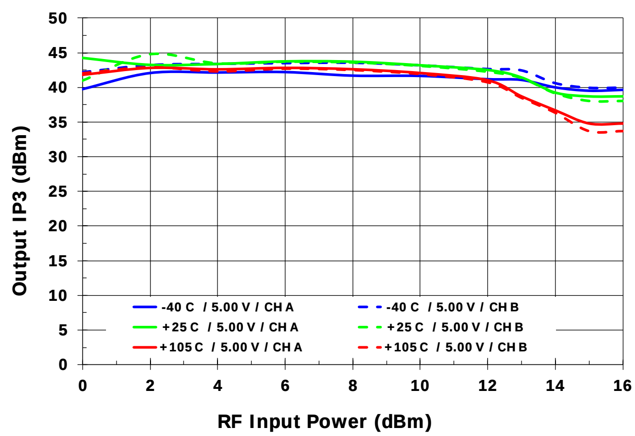
OIP3 vs. Input Power [900 MHz]



Gain vs. Input Power [1100 MHz]

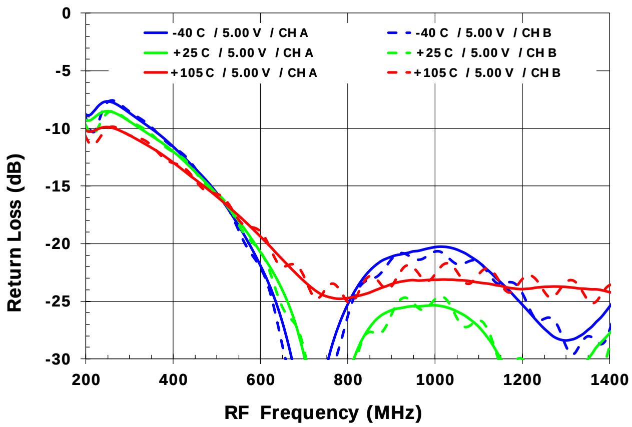


OIP3 vs. Input Power [1100 MHz]

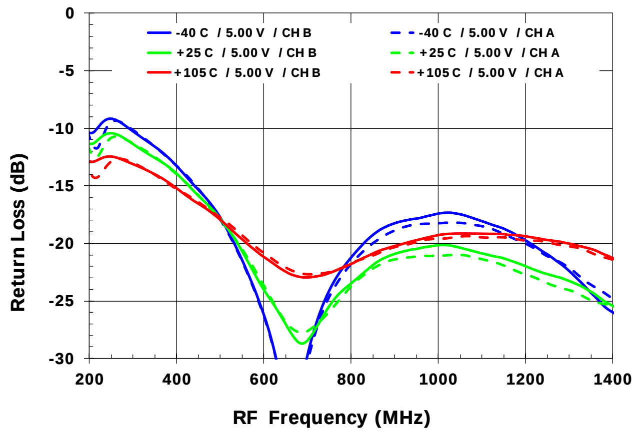


VGA BYPASS ON: TYPICAL OPERATING CONDITIONS (- 8 -)

Input Match - S11 VGA

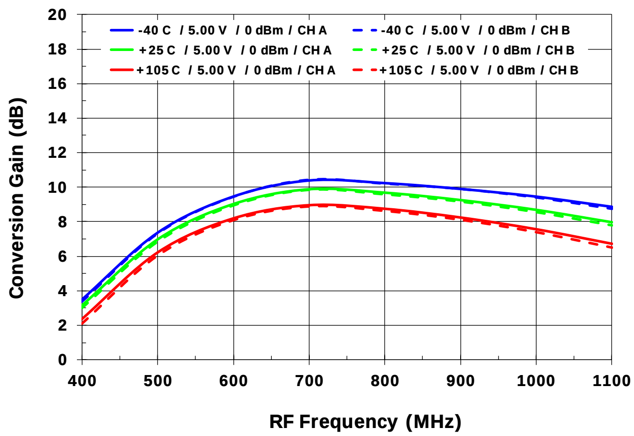


Output Match - S22 VGA

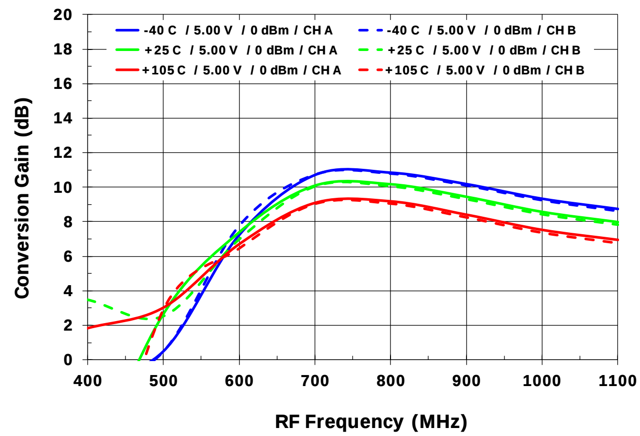


MIXER: TYPICAL OPERATING CONDITIONS (- 9 -)

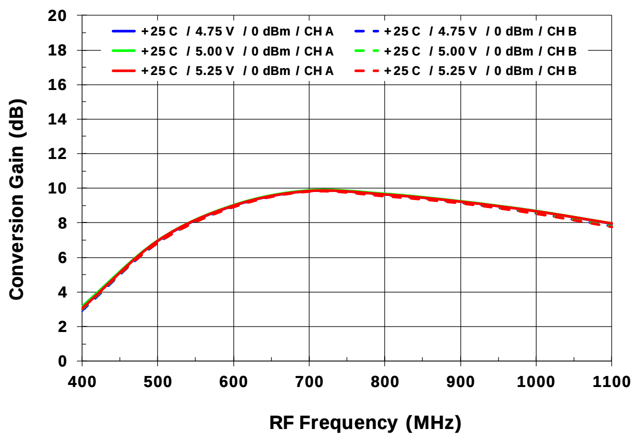
Gain vs. T_{case} [G_{MXR}, HS Injection]



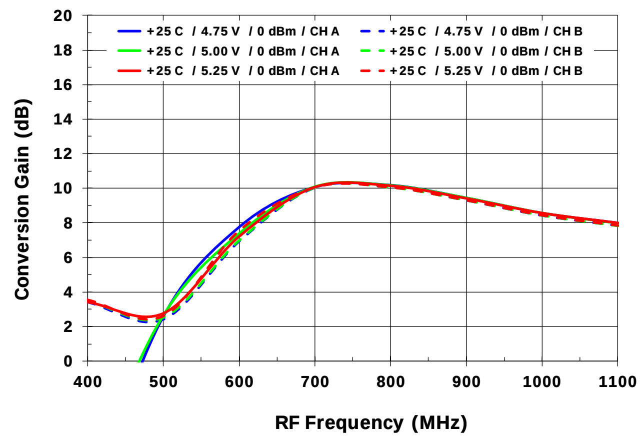
Gain vs. T_{case} [G_{MXR}, LS Injection]



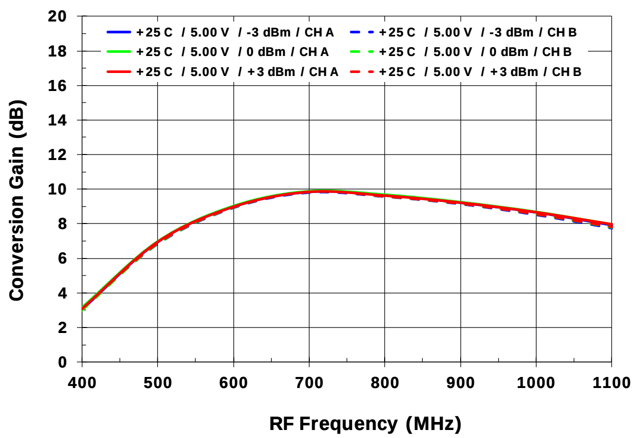
Gain vs. V_{cc} [G_{MXR}, HS Injection]



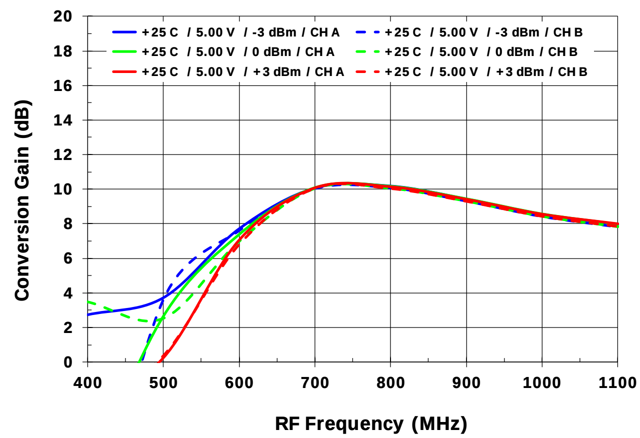
Gain vs. V_{cc} [G_{MXR}, LS Injection]



Gain vs. LO Power [G_{MXR}, HS Injection]

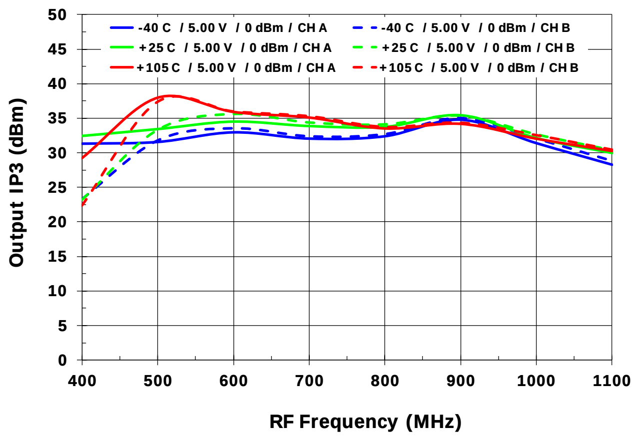


Gain vs. LO Power [G_{MXR}, LS Injection]

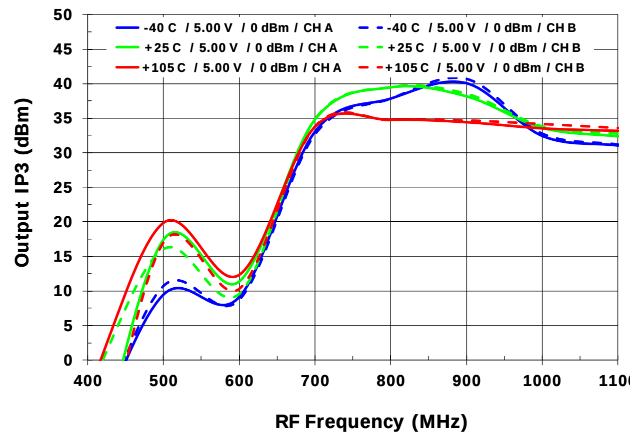


MIXER: TYPICAL OPERATING CONDITIONS (- 10 -)

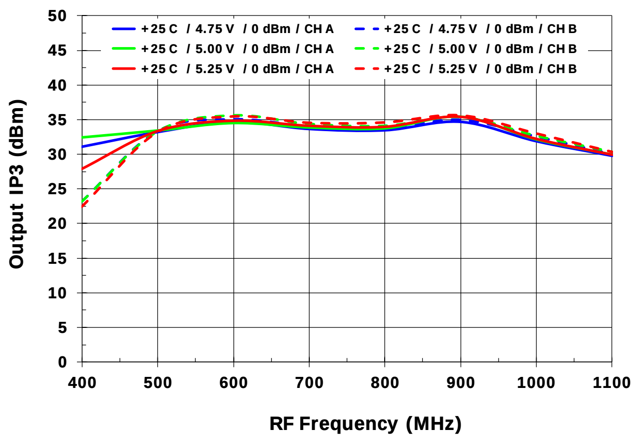
OIP3 vs. T_{case} [$OIP3_{MXR}$, HS injection]



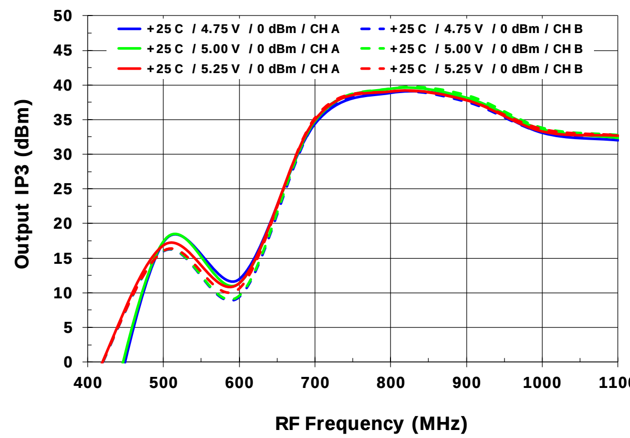
OIP3 vs. T_{case} [$OIP3_{MXR}$, LS injection]



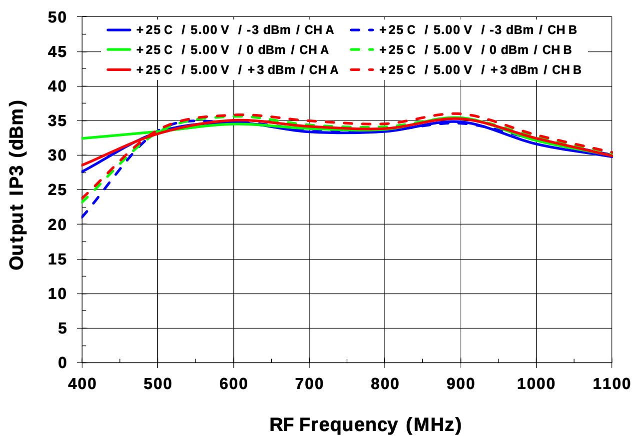
OIP3 vs. V_{cc} [$OIP3_{MXR}$, HS injection]



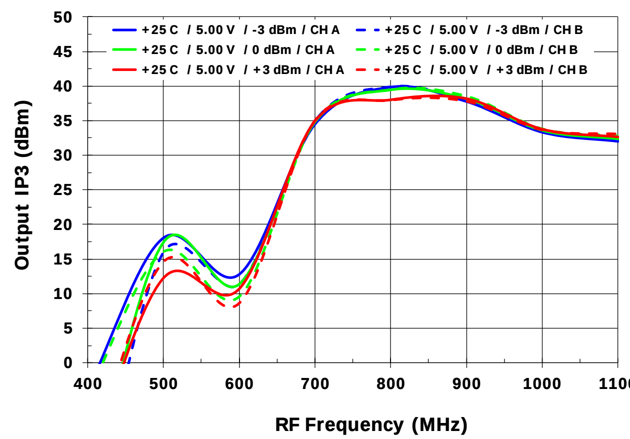
OIP3 vs. V_{cc} [$OIP3_{MXR}$, LS injection]



OIP3 vs. LO Power [$OIP3_{MXR}$, HS injection]

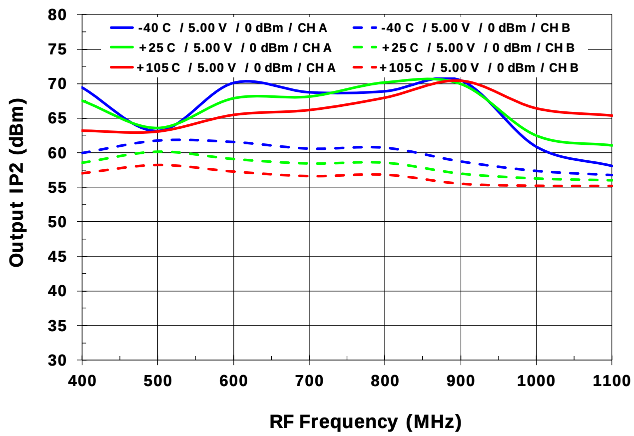


OIP3 vs. LO Power [$OIP3_{MXR}$, LS injection]

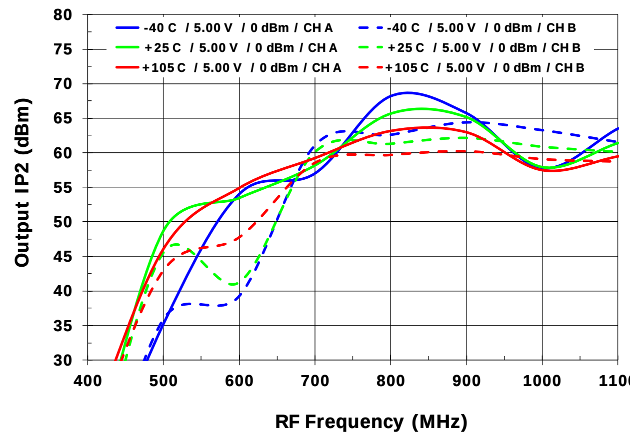


MIXER: TYPICAL OPERATING CONDITIONS (- 11 -)

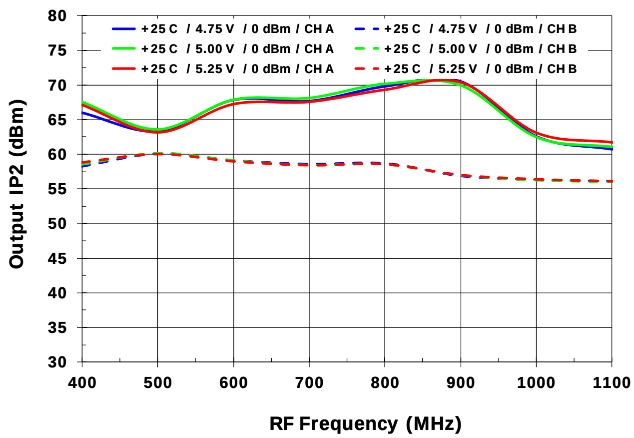
OIP2 vs. T_{case} [$OIP2_{MXR}$, HS injection]



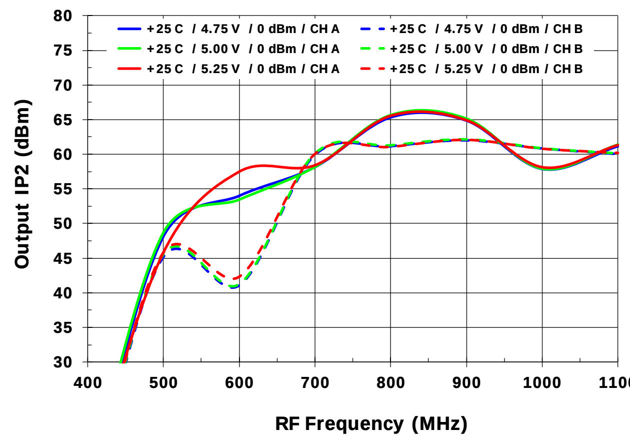
OIP2 vs. T_{case} [$OIP2_{MXR}$, LS injection]



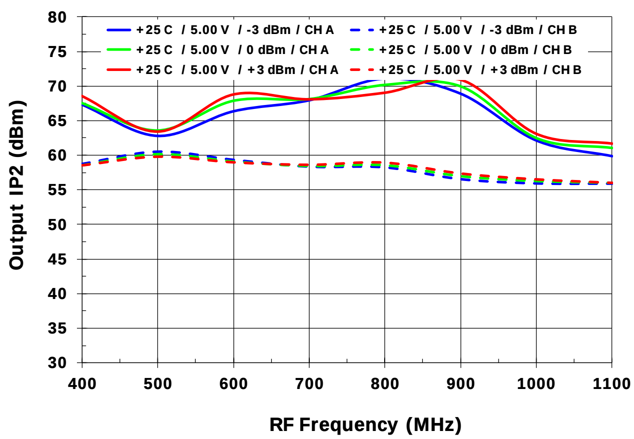
OIP2 vs. V_{cc} [$OIP2_{MXR}$, HS injection]



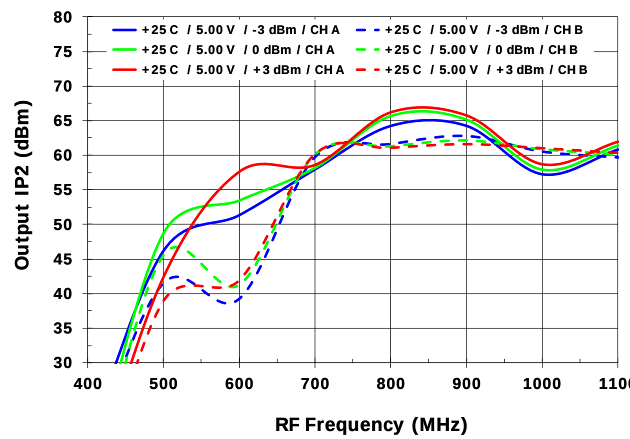
OIP2 vs. V_{cc} [$OIP2_{MXR}$, LS injection]



OIP2 vs. LO Power [$OIP2_{MXR}$, HS injection]

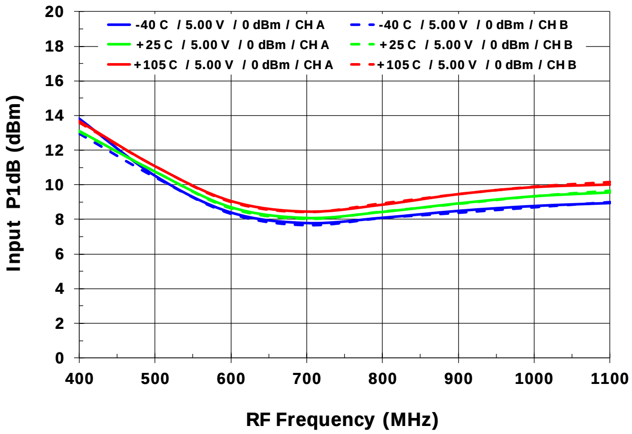


OIP2 vs. LO Power [$OIP2_{MXR}$, LS injection]

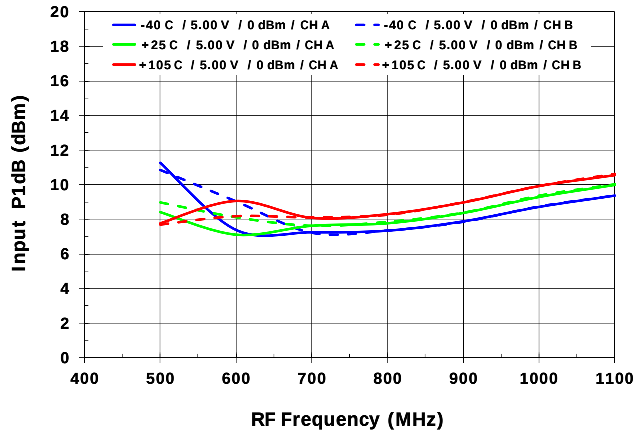


MIXER: TYPICAL OPERATING CONDITIONS (- 12 -)

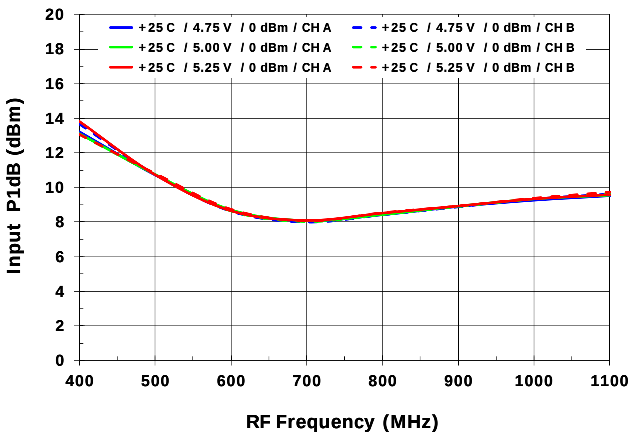
IP1dB vs. T_{case} [$IP1dB_{MXR}$, HS injection]



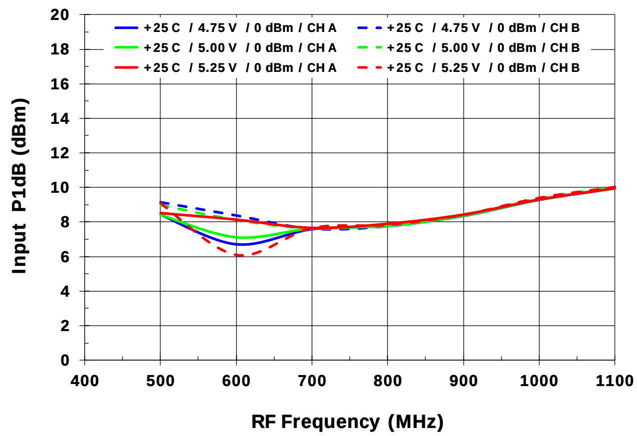
IP1dB vs. T_{case} [$IP1dB_{MXR}$, LS injection]



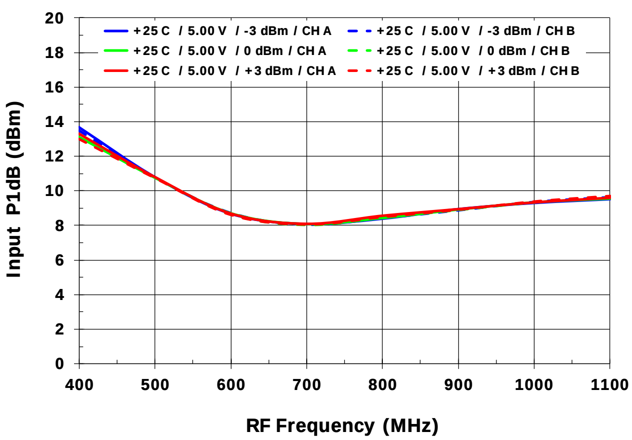
IP1dB vs. V_{cc} [$IP1dB_{MXR}$, HS injection]



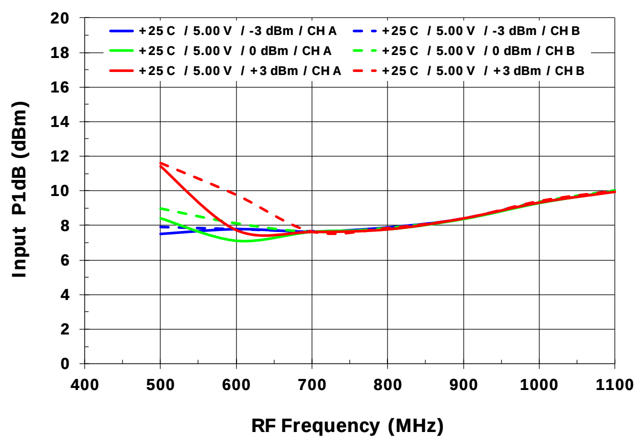
IP1dB vs. V_{cc} [$IP1dB_{MXR}$, LS injection]



IP1dB vs. LO Power [$IP1dB_{MXR}$, HS injection]

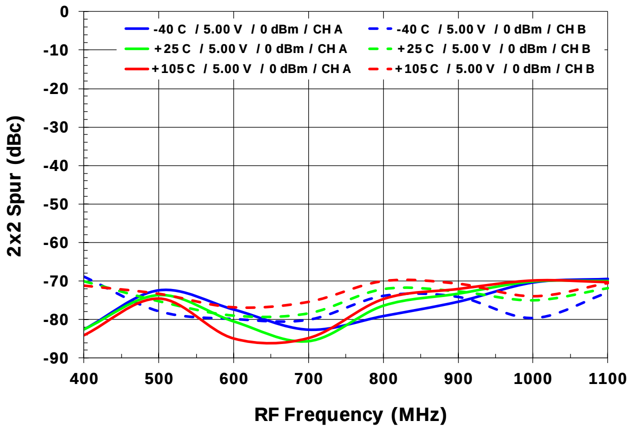


IP1dB vs. LO Power [$IP1dB_{MXR}$, LS injection]

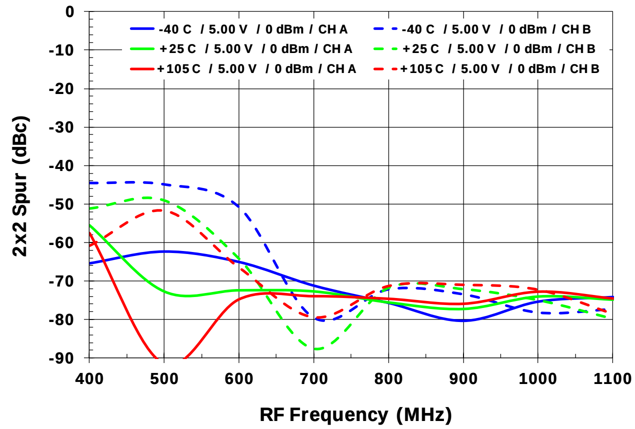


MIXER: TYPICAL OPERATING CONDITIONS (- 13 -)

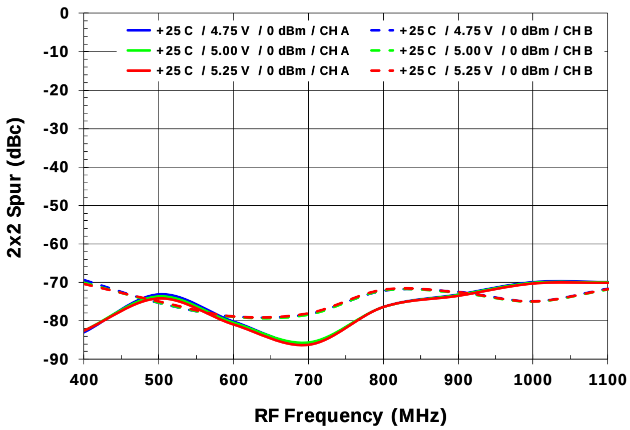
2x2 Rejection vs. T_{case} [$2x2_{MXR}$, HS rejection]



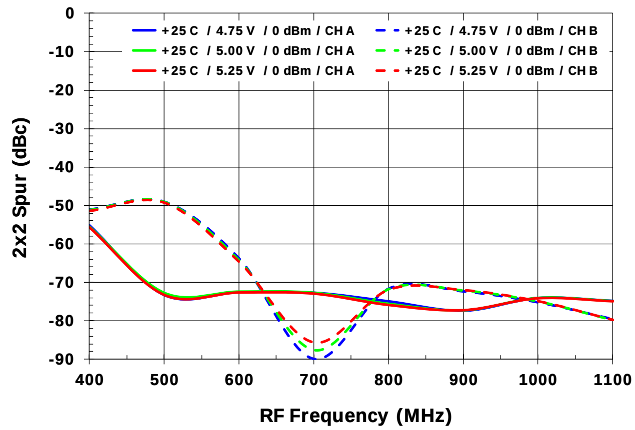
2x2 Rejection vs. T_{case} [$2x2_{MXR}$, LS rejection]



2x2 Rejection vs. V_{cc} [$2x2_{MXR}$,HS rejection]

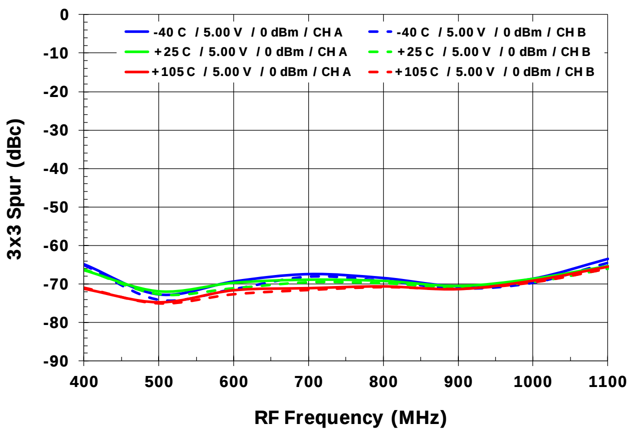


2x2 Rejection vs. V_{cc} [$2x2_{MXR}$, LS rejection]

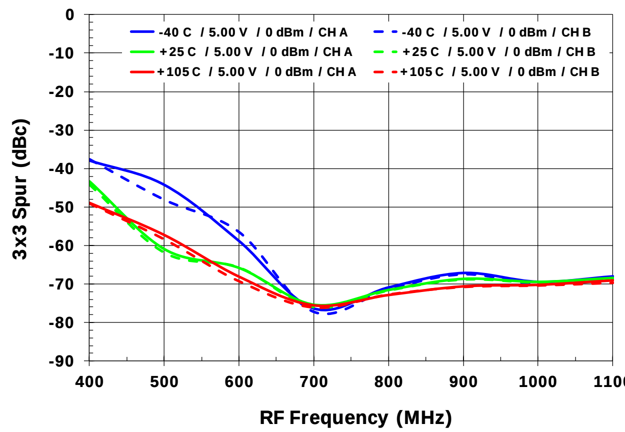


MIXER: TYPICAL OPERATING CONDITIONS (- 14 -)

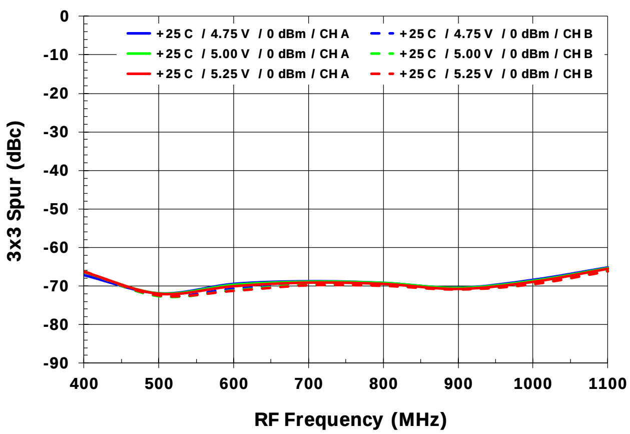
3x3 Rejection vs. T_{case} [$3x3_{MXR}$, HS rejection]



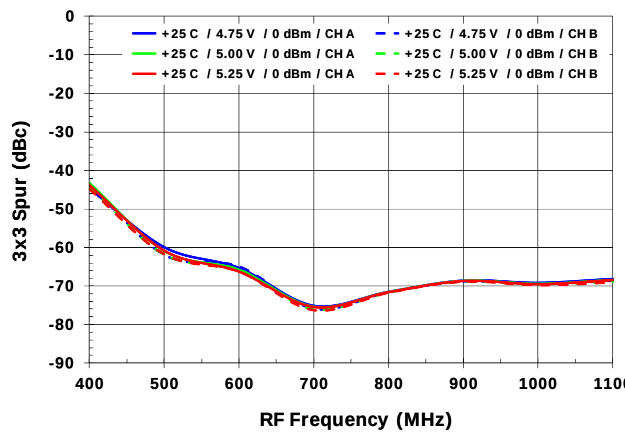
3x3 Rejection vs. T_{case} [$3x3_{MXR}$, LS rejection]



3x3 Rejection vs. V_{cc} [$3x3_{MXR}$, HS rejection]

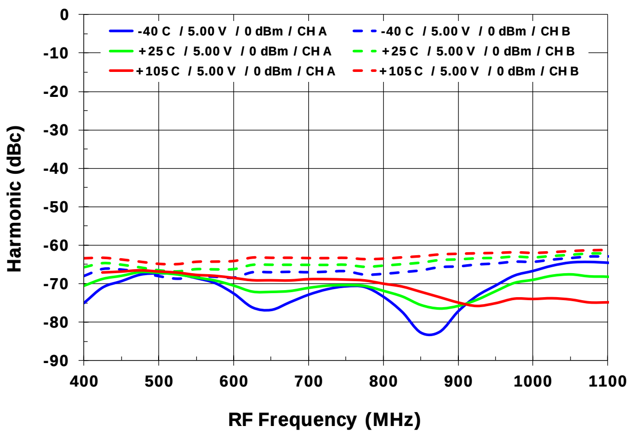


3x3 Rejection vs. V_{cc} [$3x3_{MXR}$, LS rejection]

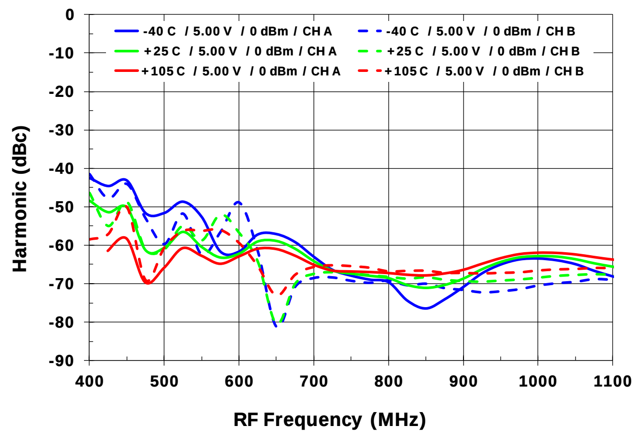


MIXER: TYPICAL OPERATING CONDITIONS (- 15 -)

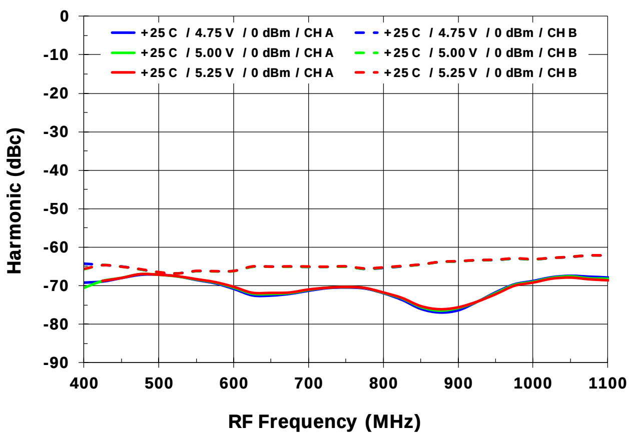
HD2 vs. T_{case} [$HD2_{MXR}$, HS injection]



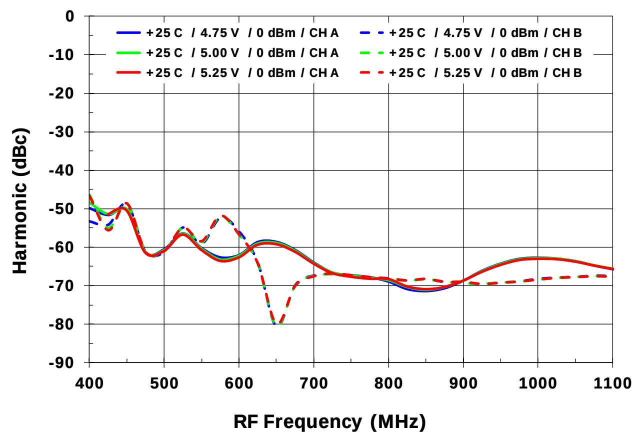
HD2 vs. T_{case} [$HD2_{MXR}$, LS injection]



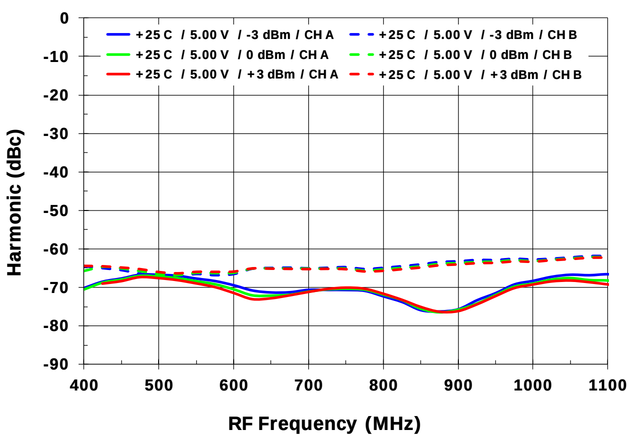
HD2 vs. V_{cc} [$HD2_{MXR}$, HS injection]



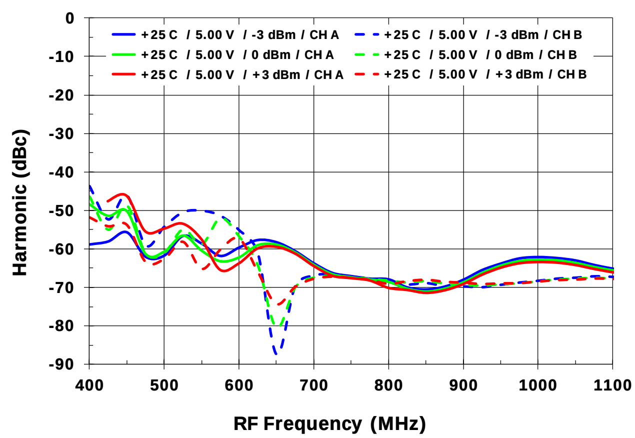
HD2 vs. V_{cc} [$HD2_{MXR}$, LS injection]



HD2 vs. LO Power [$HD2_{MXR}$, HS injection]

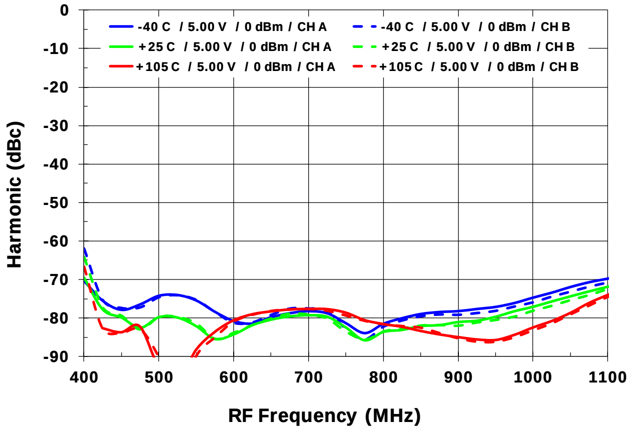


HD2 vs. LO Power [$HD2_{MXR}$, LS injection]

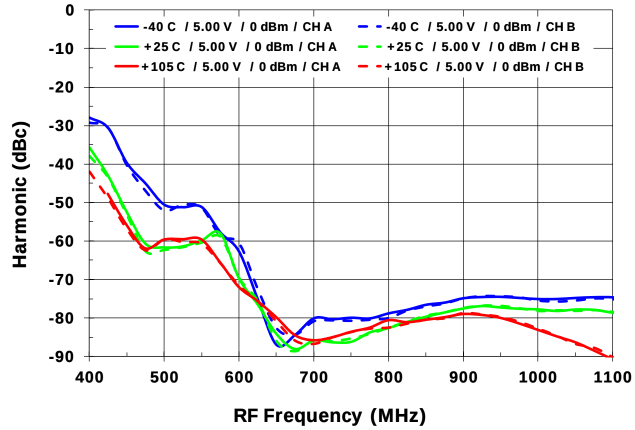


MIXER: TYPICAL OPERATING CONDITIONS (- 16 -)

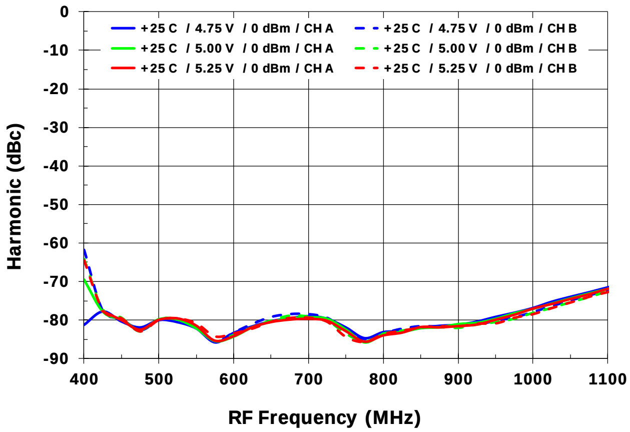
HD3 vs. T_{case} [$HD3_{MXR}$, HS injection]



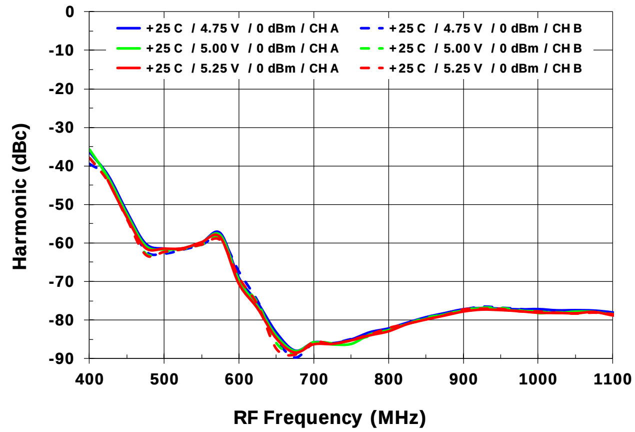
HD3 vs. T_{case} [$HD3_{MXR}$, LS injection]



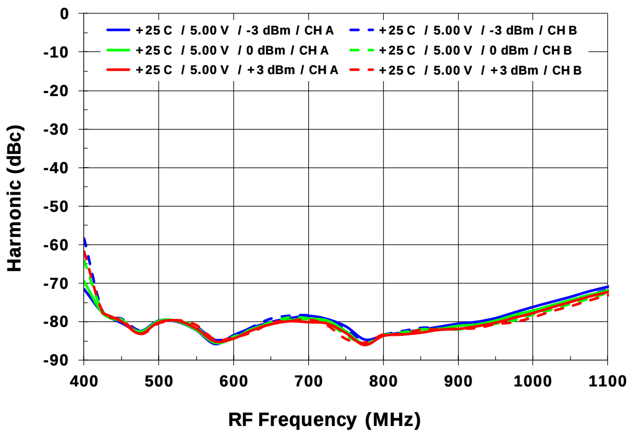
HD3 vs. V_{cc} [$HD3_{MXR}$, HS injection]



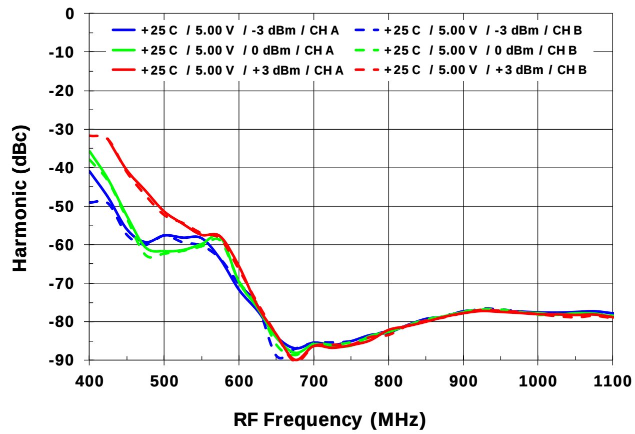
HD3 vs. V_{cc} [$HD3_{MXR}$, LS injection]



HD3 vs. LO Power [$HD3_{MXR}$, HS injection]

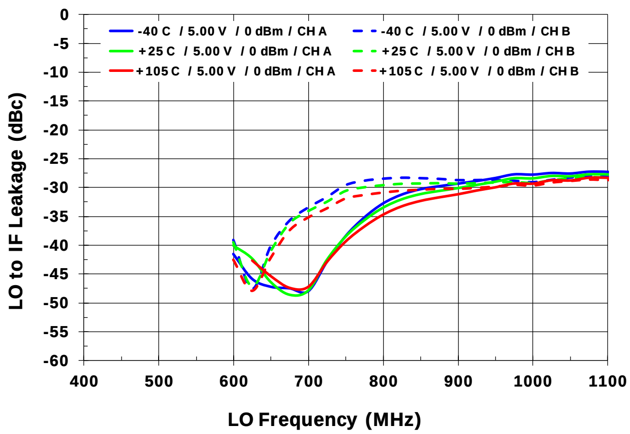


HD3 vs. LO Power [$HD3_{MXR}$, LS injection]

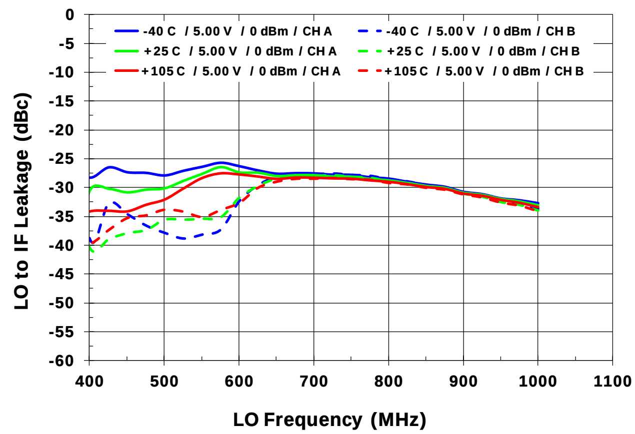


MIXER: TYPICAL OPERATING CONDITIONS (- 17 -)

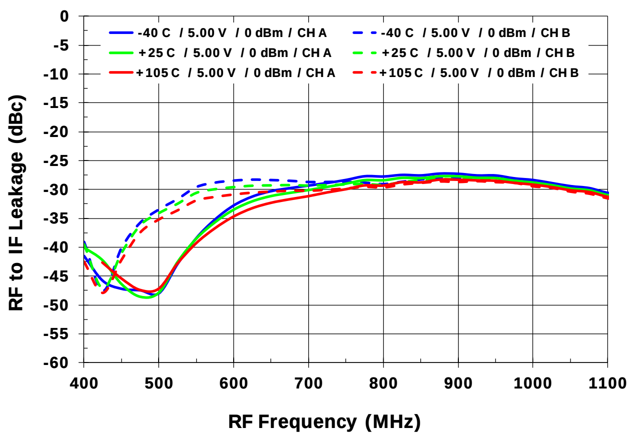
LO to IF Leakage vs. T_{case} [ISO_{LI}, HS injection]



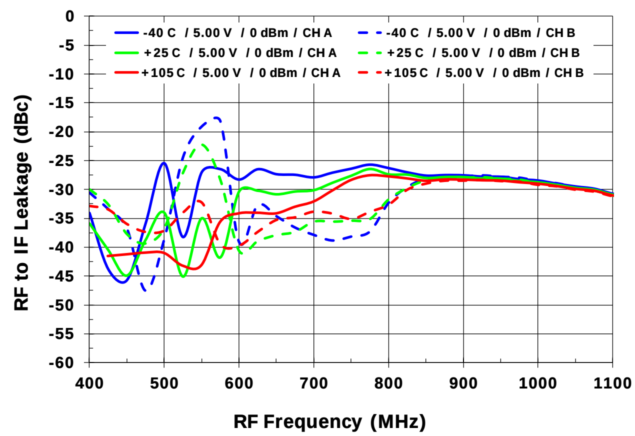
LO to IF Leakage vs. T_{case} [ISO_{LI}, LS injection]



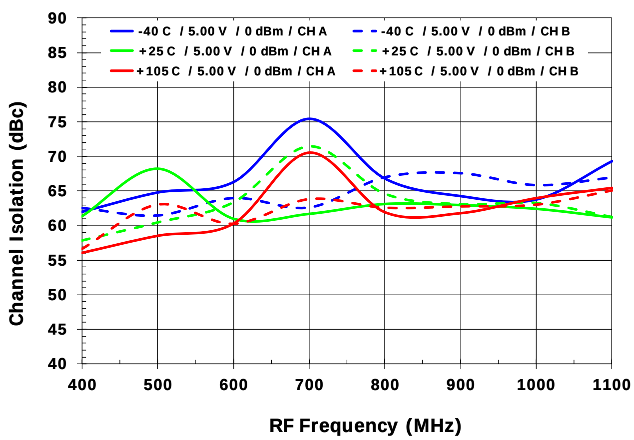
RF to IF Rejection vs. T_{case} [ISO_{RI}, HS injection]



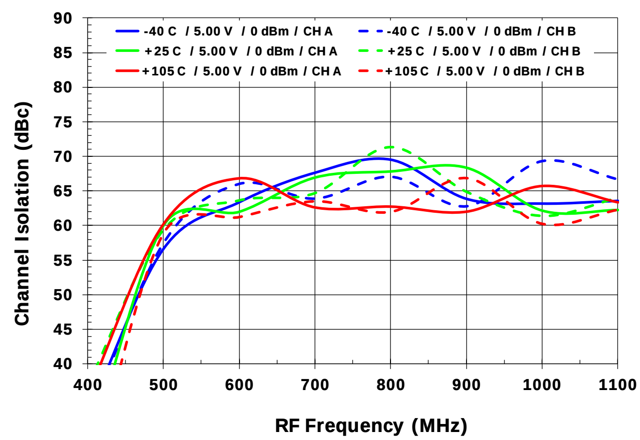
RF to IF Rejection vs. T_{case} [ISO_{RI}, LS injection]



Channel Isolation vs. T_{case} [ISO_{IF}, HS injection]

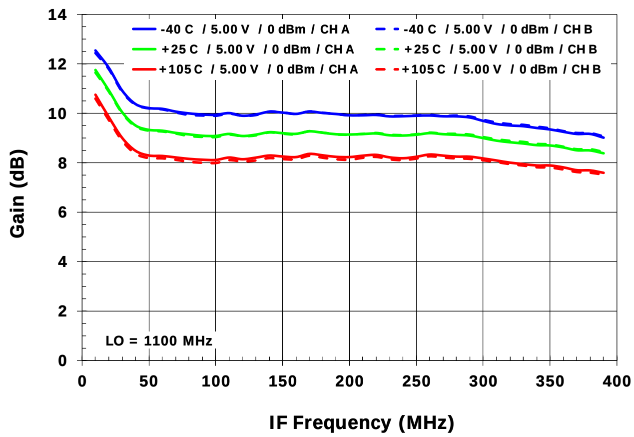


Channel Isolation vs. T_{case} [ISO_{IF}, LS injection]

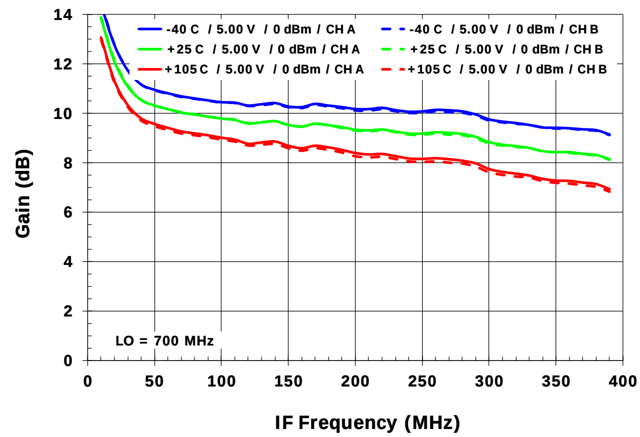


MIXER: TYPICAL OPERATING CONDITIONS (- 18 -)

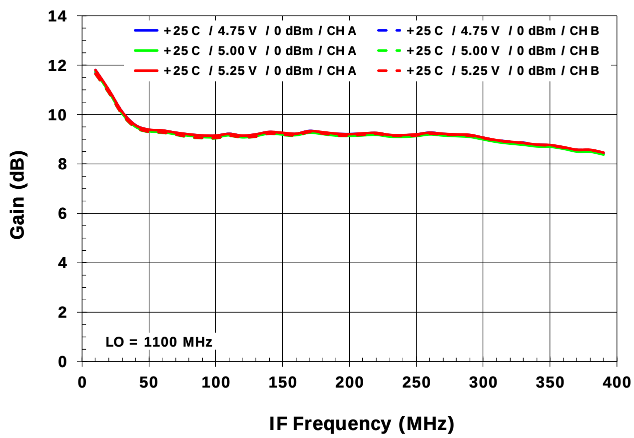
IF Gain flatness vs. T_{case} [G_{MXR_T}, HS injection]



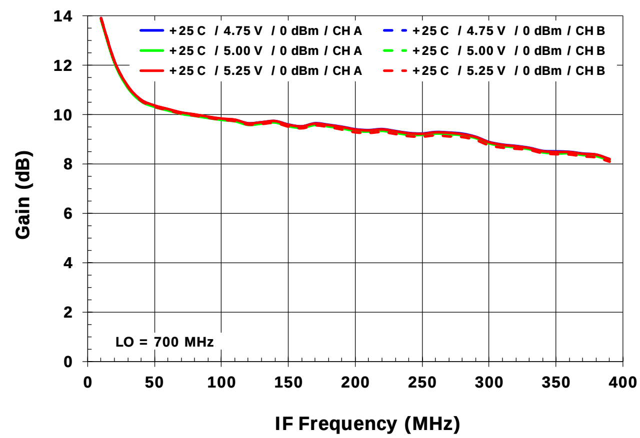
IF Gain flatness vs. T_{case} [G_{MXR_T}, LS injection]



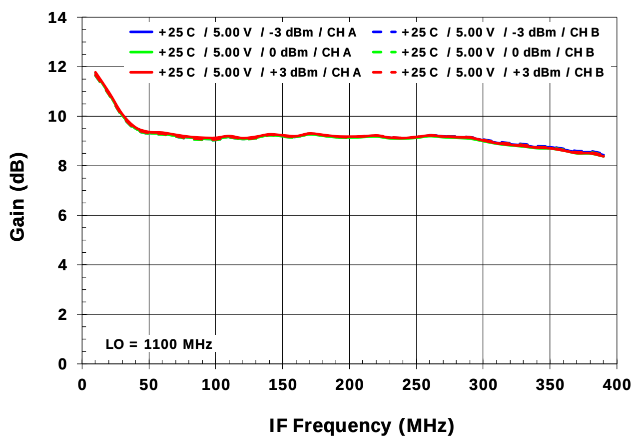
IF Gain flatness vs. V_{cc} [G_{MXR_T}, HS injection]



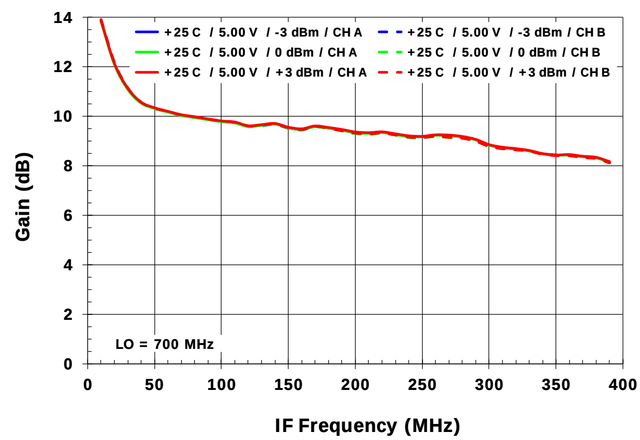
IF Gain flatness vs. V_{cc} [G_{MXR_T}, LS injection]



IF Gain flatness vs. LO Power [G_{MXR_T}, HS injection]

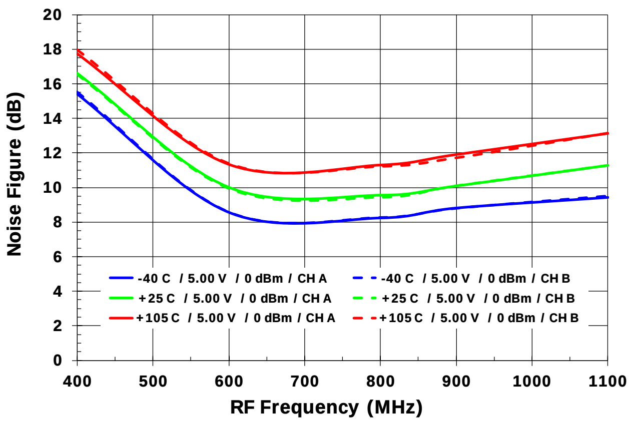


IF Gain flatness vs. LO Power [G_{MXR_T}, LS injection]

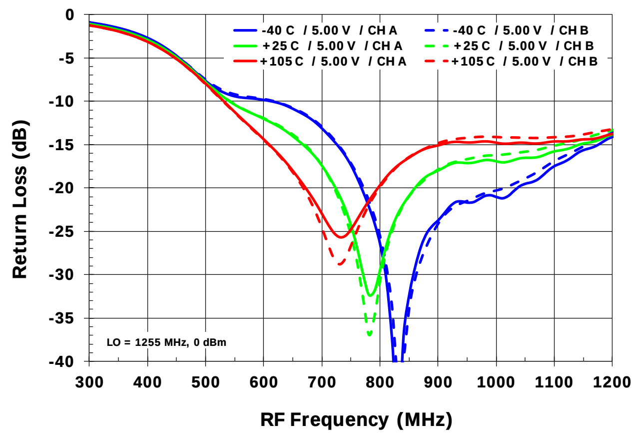


MIXER: TYPICAL OPERATING CONDITIONS (- 19 -)

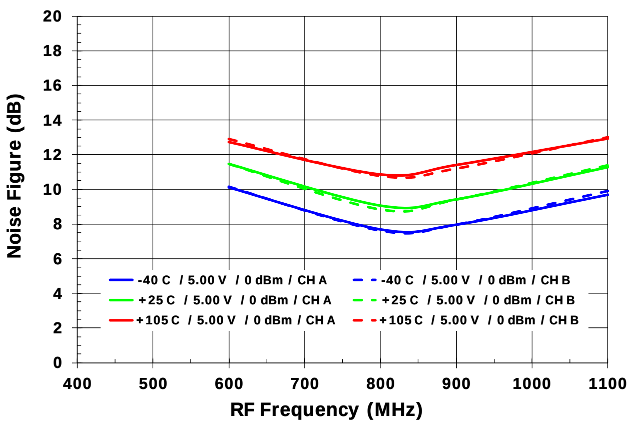
Noise Figure vs.T_{case} [NF_{MXR}, HS Injection]



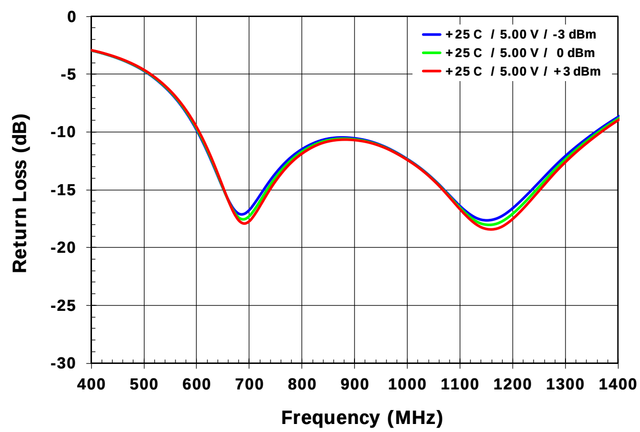
Mixer RF Input Return Loss [$S11_{MXR\_RF}$]



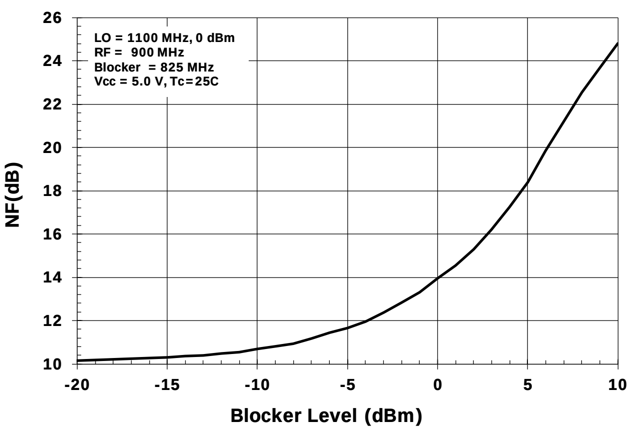
Noise Figure vs.T_{case} [NF_{MXR} LS, Injection]



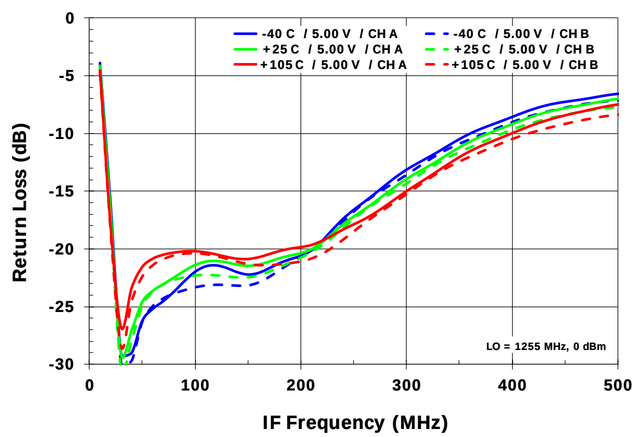
Mixer LO Port Return Loss [$S11_{MXR\_LO}$]



Noise Figure with Blocker [NF_{MXR_BLK}]

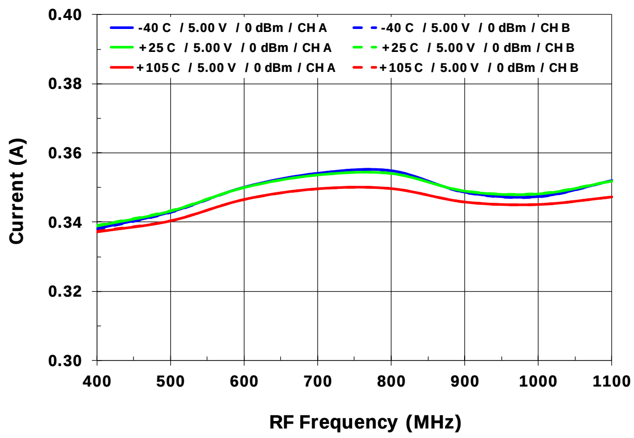


Mixer IF Output Return Loss [$S22_{MXR\_IF}$]

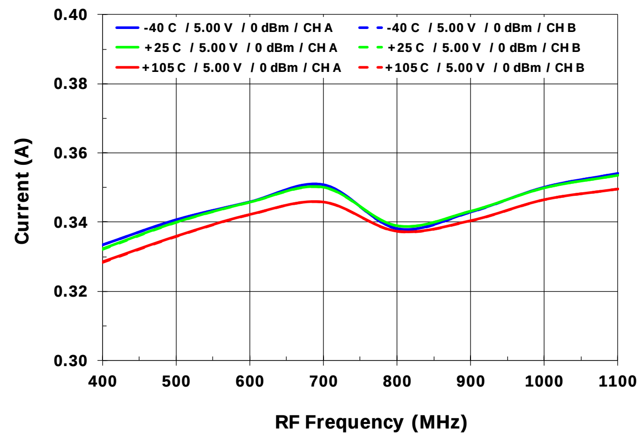


MIXER: TYPICAL OPERATING CONDITIONS (- 20 -)

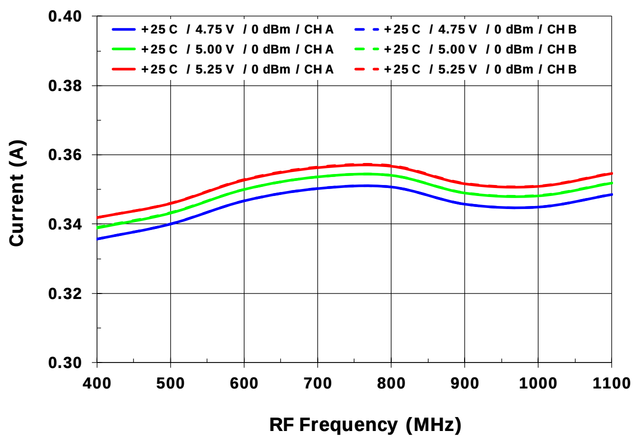
Current Consumption vs. T_{case} [HS injection]



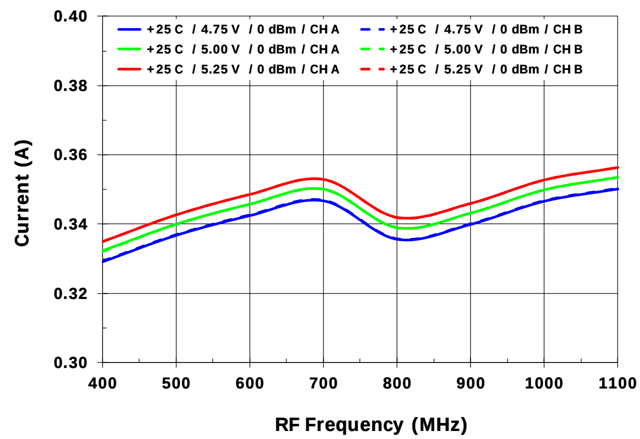
Current consumption vs. T_{case} [LS injection]



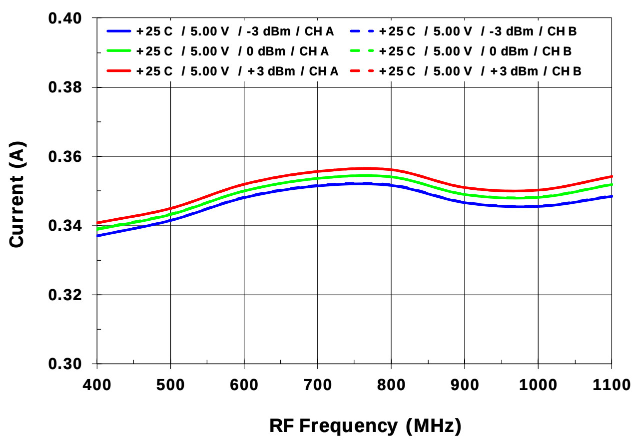
Current consumption vs. V_{cc} [HS injection]



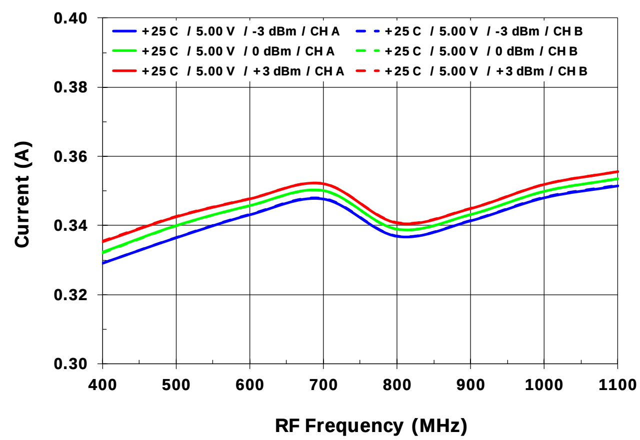
Current consumption vs. V_{cc} [LS injection]



Current consumption vs. LO Power [HS injection]

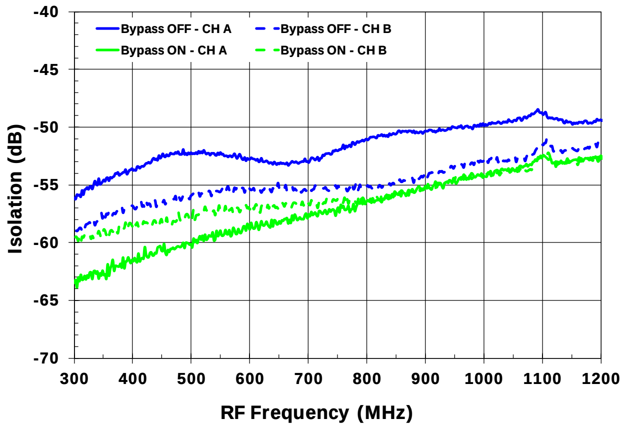


Current consumption vs. LO Power [LS injection]



VGA & MIXER: TYPICAL OPERATING CONDITIONS (- 21 -)

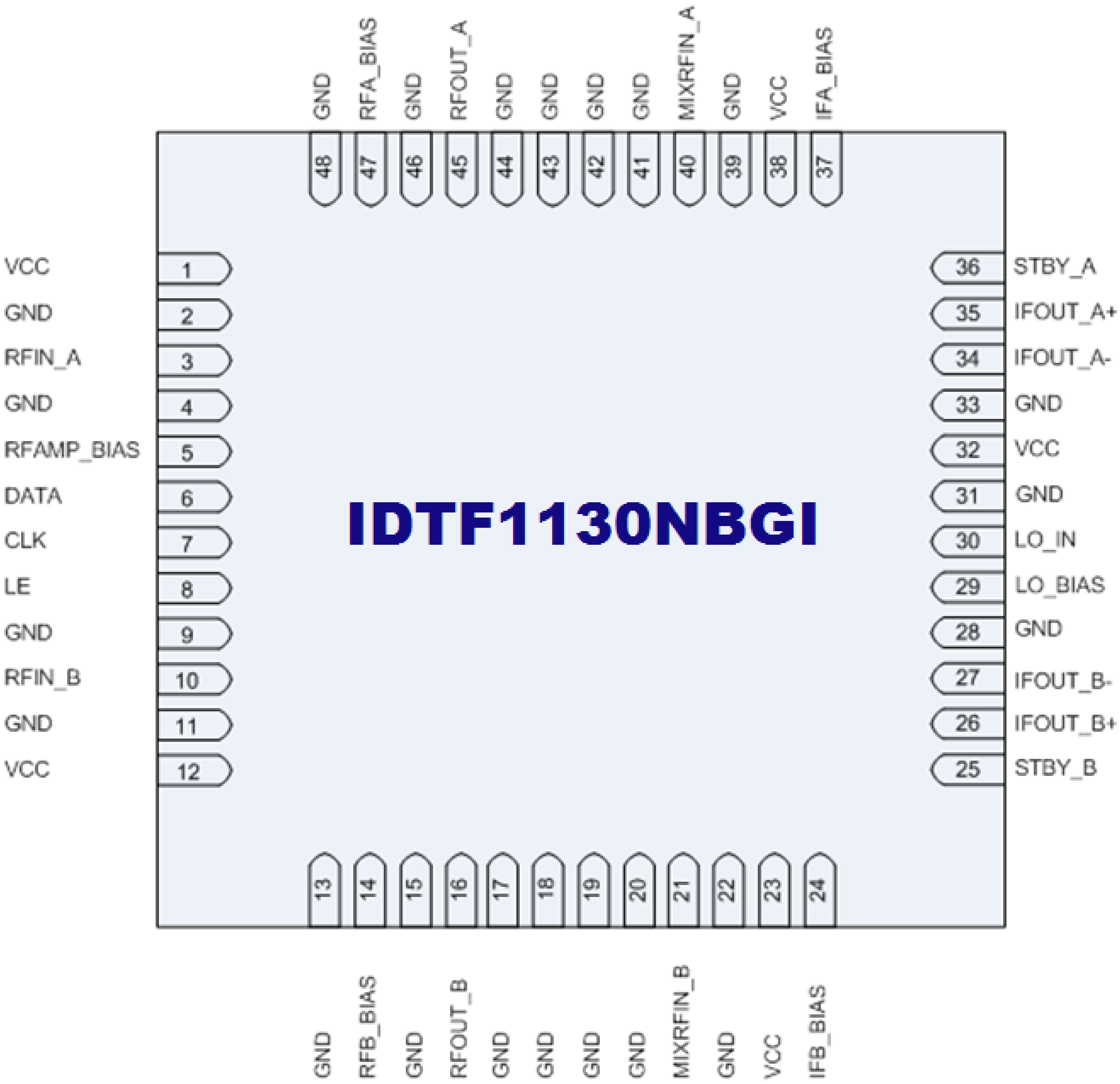
RF Amplifier to Mixer Isolation



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

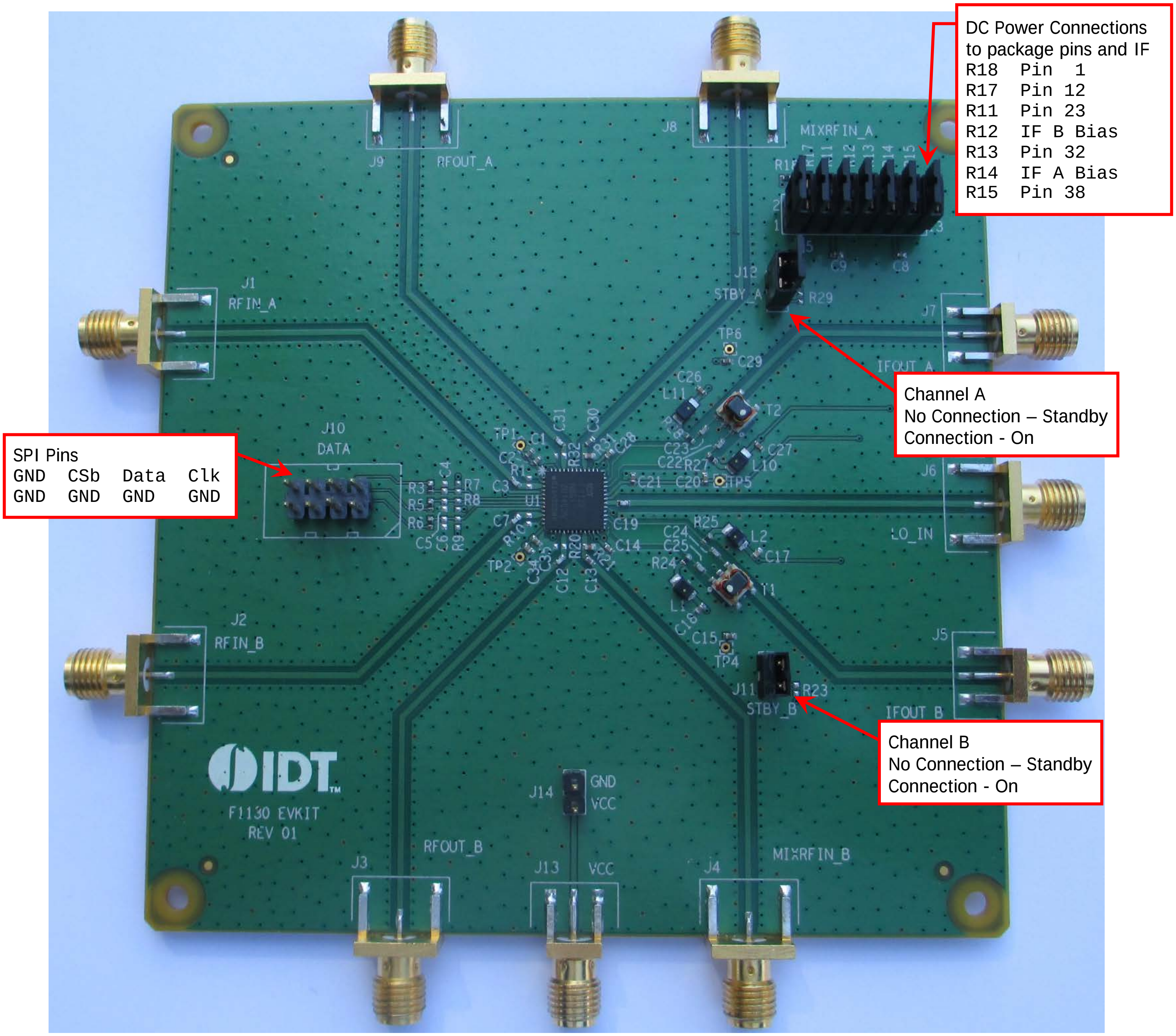
Pin Diagram



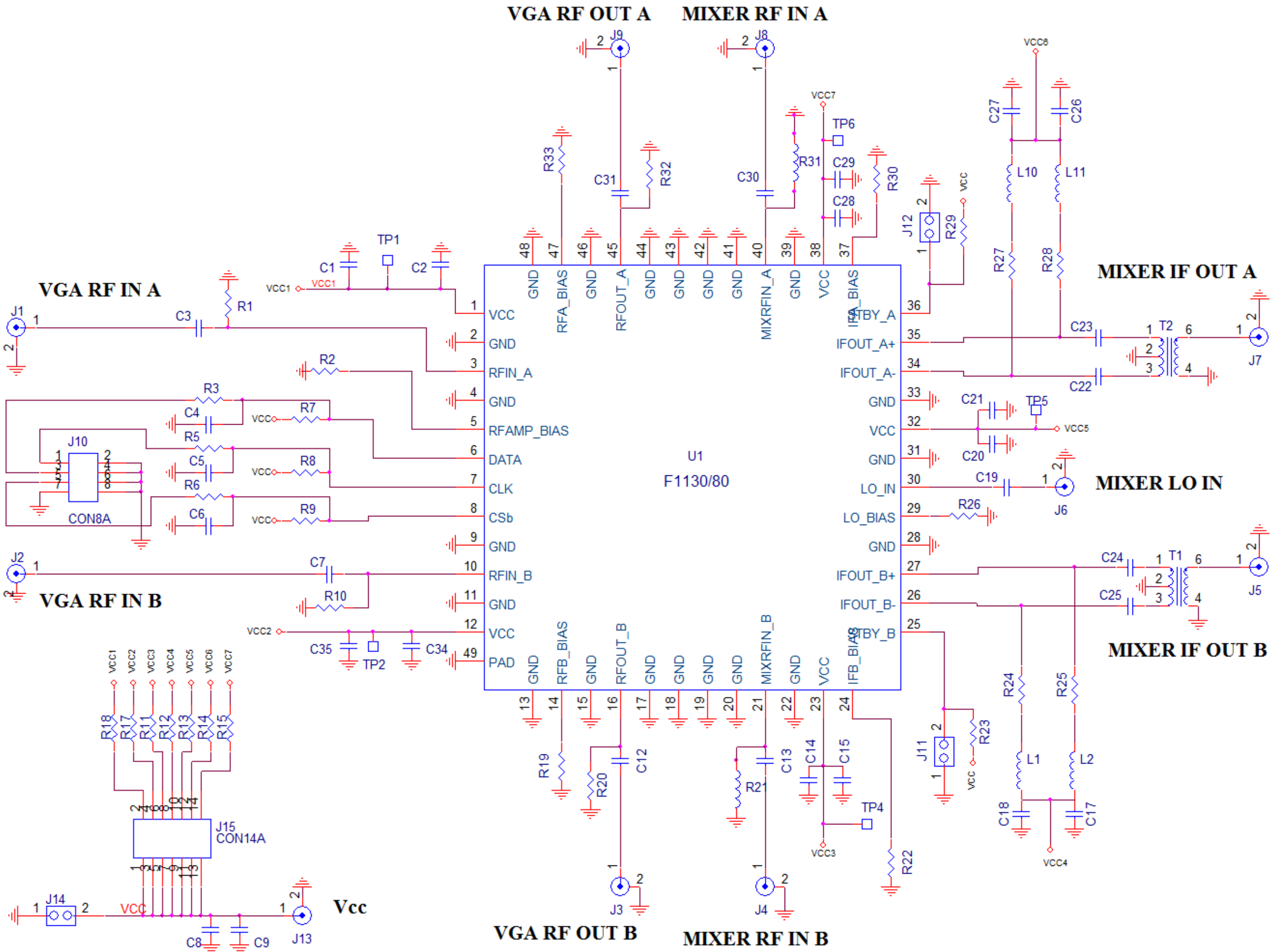
PIN DESCRIPTION

Pin	Name	Function
1, 12, 23, 32, 38	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
2, 4, 9, 11, 13, 15, 17, 18, 19, 20, 22, 28, 31, 33, 39, 41, 42, 43, 44, 46, 48	GND	Ground these pins.
3	RFIN_A	Channel-A VGA RF Input. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
5	RFAMP_BIAS	Connect a resistor to GND (refer to BOM)
6	SPI Data	Data: 1.8V CMOS compatible.
7	SPI CLK	Clock: 1.8V CMOS compatible.
8	SPI LE	Latch Enable: 1.8V CMOS compatible. See Serial Interface Section for pin description.
10	RFIN_B	Channel-B VGA RF Input. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
14	RFB_BIAS	Connect a resistor to GND (refer to BOM).
16	RFOUT_B	Channel-B VGA RF Output. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
21	MIXRFIN_B	Channel-B Mixer RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin.
24	IFB_BIAS	Connect a resistor to GND (refer to BOM).
25	STBY_B	Standby Diversity Channel (Low = device power ON, High or Floating = device power OFF with SPI still powered ON)
26	IFOUT_B+	Channel-B Mixer Differential IF- Output. Connect pullup inductor from this pin to VCC.
27	IFOUT_B-	Channel-B Mixer Differential IF+ Output. Connect pullup inductor from this pin to VCC.
29	LO_BIAS	Connect a resistor to GND (refer to BOM).
30	LO_IN	Mixer Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor.
34	IFOUT_A-	Channel-A Mixer Differential IF- Output. Connect pullup inductor from this pin to VCC.
35	IFOUT_A+	Channe-Al Mixer Differential IF+ Output. Connect pullup inductor from this pin to VCC.
36	STBY_A	Standby Main Channel (Low = device power ON, High = device power OFF with SPI still powered ON).
37	IFA_BIAS	Connect a resistor to GND (refer to BOM).
40	MIXRFIN_A	Channel-A Mixer RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin.
45	RFOUT_A	Channel-A RF VGA Output. Internally matched to 50Ω. AC coupled. DO NOT apply DC to this pin. Place coupling capacitor as close to the pin as possible.
47	RFA_BIAS	Connect a resistor to GND (refer to BOM).
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

EVKIT PICTURE



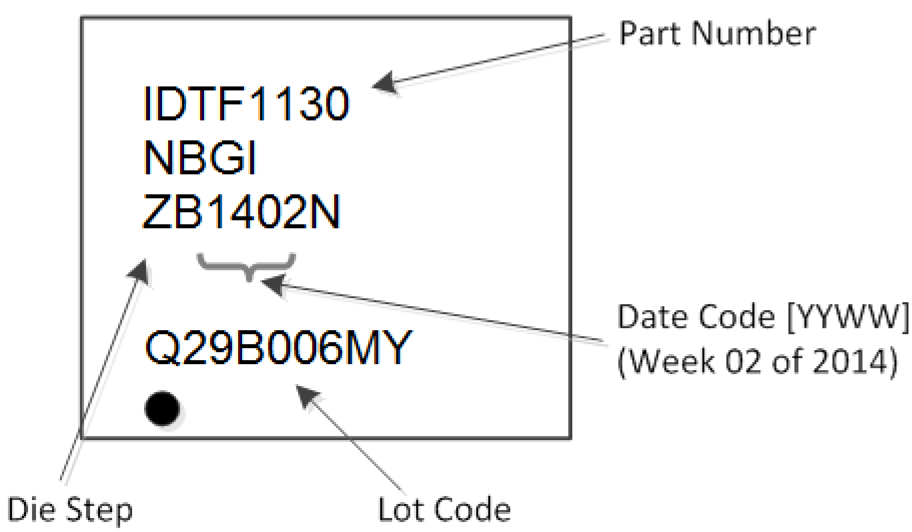
EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C2, 8, 14, 17, 20, 26, 28, 34	8	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MuRata
2	C1, 9, 15, 18, 21, 27, 29, 35	8	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	MuRata
3	C3, 7, 12, 19, 31	5	CAP CER 200PF 50V 5% C0G 0402	GRM1555C1H201JA01D	MuRata
4	C22-25	4	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	MuRata
5	C13, 30	2	CAP CER 8PF 50V C0G 0402	GRM1555C1H8R0DZ01D	MuRata
6	R2	1	RES 7.50K OHM 1/10W 1% 0402 SMD	ERJ-2RKF7501X	Panasonic
7	R3, 5, 6	3	RES 3.00K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3001X	Panasonic
8	R19, 26, 33	3	RES 3.24K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3241X	Panasonic
9	R22, 30	2	RES 62.0 OHM 1/10W 1% 0402 SMD	ERJ-2RKF62R0X	Panasonic
10	R11-15, 17, 18, 24, 25, 27, 28	11	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic
11	L1, 2, 10, 11	4	0805LS (2012) Ceramic Chip Inductor	0805LS-102XJLB	Coilcraft
12	R21, 31	2	0402CS Ceramic Chip Inductor	0402CS-20NXJLU	Coilcraft
13	T1, 2	2	4:1 Center Tap Balun	TC4-1TG2+	Mini Circuits
14	J11, 2, 14	3	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M
15	J10	1	CONN HEADER VERT DBL 4POS GOLD	67997-108HLF	FCI
16	J15	1	CONN HEADER VERT DBL 7POS GOLD	67996-114HLF	FCI
17	J1-4, 6, 8, 9	7	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson
18	J5, 7, 13	3	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson
19	U1	1	Dual Path RF Receiver 400-1100MHz	AV650B00_5ZNA	Renesas
20		1	Printed Cicuit Board	F1130 EVKIT REV 01	
21			Bill Of Material		
22	C4-6 R1, 7-10, 20, 23, 29, 32	0	Do Not Populate	N/A	N/A

TOP MARKINGS



APPLICATIONS INFORMATION

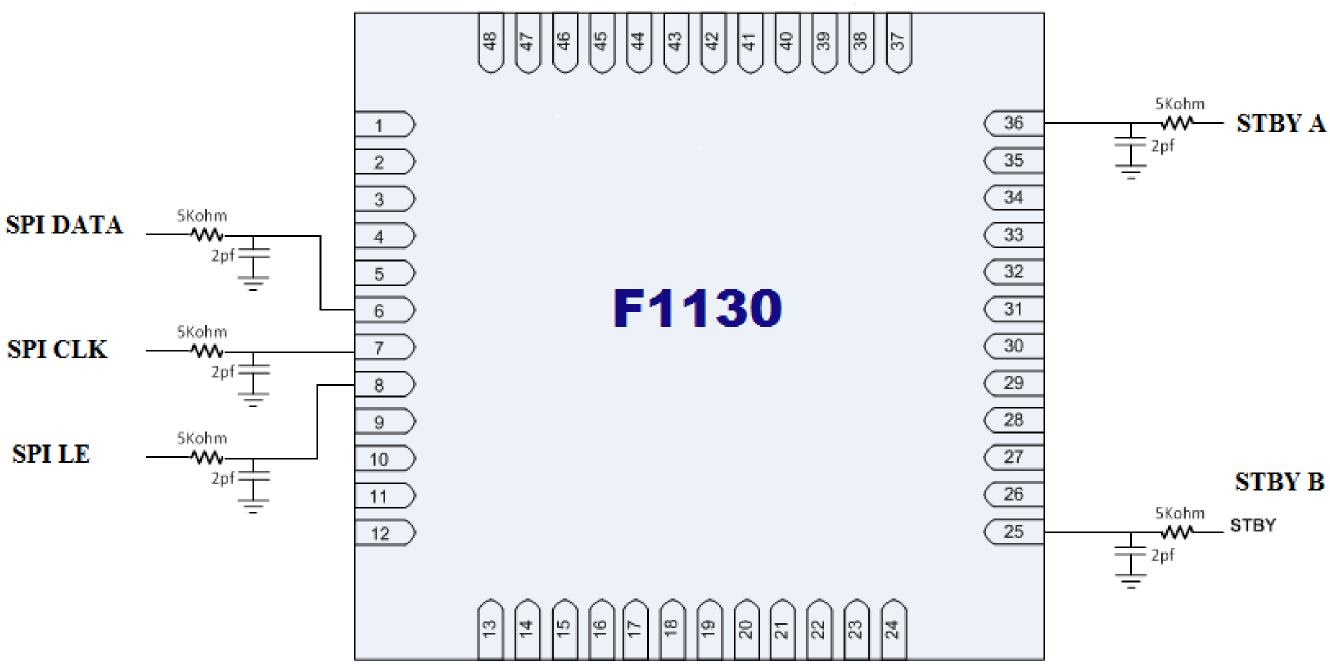
F1130 has been optimized for use in high performance RF applications from 1400MHz to 2700MHz.

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to SPI and control pins 6, 7, 8, 25, and 36 as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to overload the control line.



F1130 Digital Pin Voltage & Resistance Values (pins not connected)

The following table list the resitance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC these same pins to should have the measured voltage to ground.

Pin	Name	DC voltage (volts)	Resistance (ohms)
6	DATA	5	57K
7	CLK	5	57K
8	LE	5	57K
25	STBY_B	5	57K
36	STBY_A	5	57K

ORDERING INFORMATION

Part Number	Package Description	Carrier Type	Temperature Range
F1130NBGI	48-VFQFPN, 7 × 7 mm	Tape and Reel	-40°C to +85°C
F1130NBGI8		Tray	

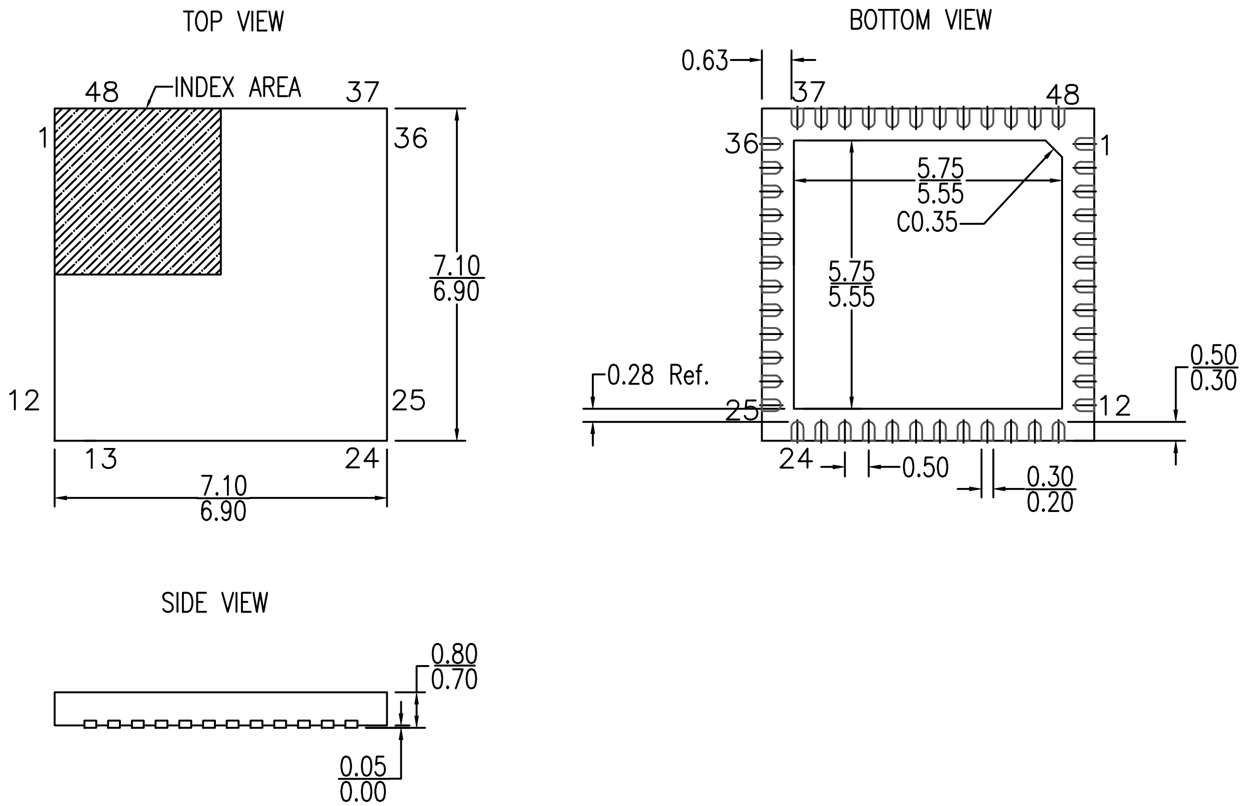
REVISION HISTORY

Revision Date	Description
February 8, 2022	Rebranded to Renesas.
April 13, 2015	Initial release.

48-VFQFPN, Package Outline Drawing

7.0 x 7.0 x 0.75 mm Body, Epad 5.65 x 5.65 mm, 0.5mm Pitch

NBG48P1, PSC-4228-01, Rev 02, Page 1

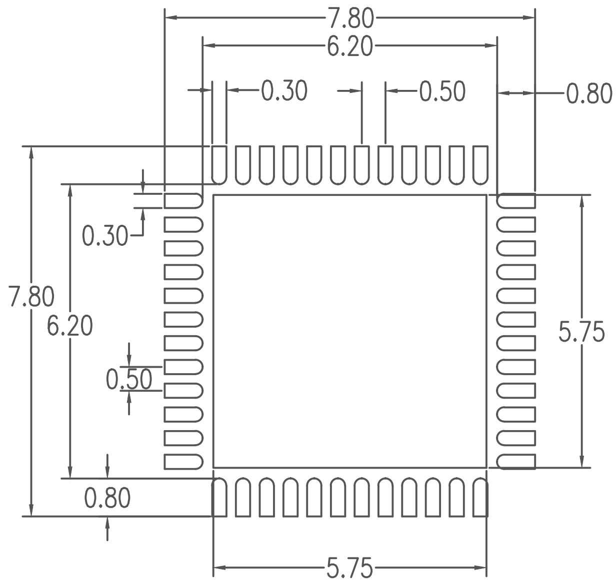


NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.

48-VFQFPN, Package Outline Drawing

7.0 x 7.0 x 0.75 mm Body, Epad 5.65 x 5.65 mm, 0.5mm Pitch

NBG48P1, PSC-4228-01, Rev 02, Page 2



RECOMMENDED LAND PATTERN RECOMMENDATION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 10, 2018	Rev 02	Correct VFQFP-N to VFQFPN, Remove Black Package Code
Sept 27, 2017	Rev 01	New Format