DESCRIPTION

This document describes the preliminary specification for the F1375 **D**igital **P**re-**D**istortion Demodulator for PA linearization. This series of devices is offered in two frequency variants to cover common UTRA bands.

COMPETITIVE ADVANTAGE

In typical basestation transmitters digital pre-distortion is employed to improve the Transmitter performance. The signal out of the PA is sampled and the incoming Tx chain I&Q data is pre-distorted to counteract the distortion inherent in the PA. The PA signal is adjusted via a digital step attenuator to a lower level and then sub-sampled at an IF frequency of ~200 MHz which necessitates the need for a highly linear demodulator to downmix to quadrature IF from the Transmit frequency. By sampling IF_I and IF_Q independently and then digitally combining these signals, an effective doubling of the sample rate can be achieved. Any distortion in this path will degrade the performance of the DPD algorithm. By utilizing an ultra-linear demodulator w/integrated DSA such as the F1375, the ACLR and/or power consumption of the full Tx system can be improved significantly.

- ✓ DPD full path ACLR: ⇓ **1 dB**
- ✓ Icc: DPD function Power Consumption ⇓ **40%**
- ✓ Zero-Distortion™ Demod eliminates 2 IF amps
- ✓ Integrates 2 BPFs, 2 Baluns, SP2T RF switch
- ✓ Glitch-Free™ gain control

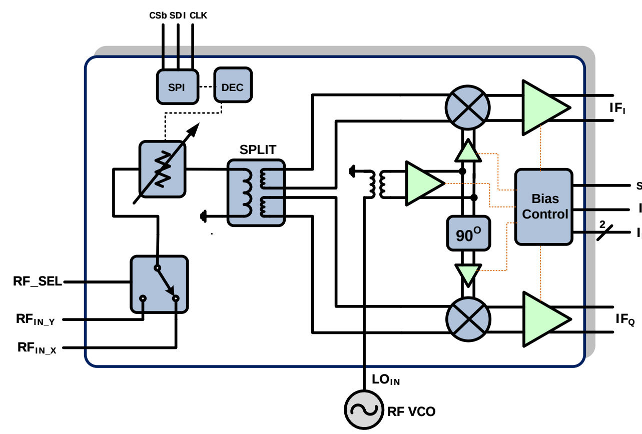
PART# MATRIX

Part#	RF range	UTRA bands	IF freq range	Typ. Gain	Injection
F1325	550 - 1150	5,6,8,12,13, 14,17	20 - 350	8.2	High Side or Low Side
F1375	1300 - 2900	1,2,3,4,9,10 7,21, 24, 38	20 - 500	9	High Side or Low Side

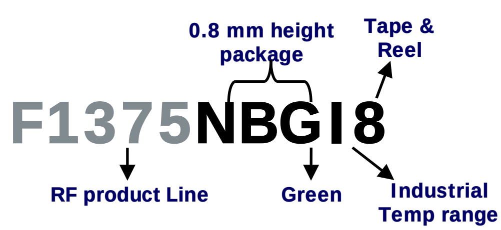
FEATURES (I OR Q PATH)

- Wide flat performance IF BW
- Wide RF and LO BWs (~ 1.6 GHz)
- Ideal for Multi-Carrier Systems
- Drives ADC directly
- Ultra linear +40 dBm $IP3_O$
- Low Noise Figure
- Excellent ACLR performance
- **100Ω** output impedance
- Fully integrated DPD demodulator
- 6 x 6 mm 36-pin package
- Standby Mode w/Fast Recovery
- I_{CC}: 270 mA

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
SW_Latch, DATA, CSb, CLK, RF_SEL	0V to 3.6V
STBY	0V to V_{CC}
IF_I+, IF_I-, IF_Q+, IF_Q-	1V to (Vcc + 0.3V)
LO_IN	-0.3V to +0.3V
RF_INX, RF_INY	-0.3V to +0.3V
IF_BiasI, IF_BiasQ to GND	-0.3V to +1.2V
LO_ADJ to GND	2.1V to 4.0V
RF Input Power (Into RFIN_X or RFIN_Y)	**+27 dBm**
Continuous Power Dissipation	2.5W
θ_{JA} (Junction – Ambient)	+40°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +105°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Moisture Sensitivity Level	**1**
Lead Temperature (soldering, 10s)	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

F1375 SPECIFICATION

See typical application circuit. Specifications apply at V_{CC} = +5.0V, T_C = 25C, **F_{RF} = 2100 MHz**, **F_{LO} = 1900 MHz**, Gain = G_{MAX}, P_{LO} = 0 dBm, T_C= +25°C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF input trace losses de-embedded.

Parameter	Comment	Symbol	Min	Typ	Max	Units
Logic Input High	For STBY, DATA, CSb, CLK, SB_Latch	V_{IH}	***1.1***			V
Logic Input Low	For STBY, DATA, CSb, CLK, SB_Latch	V_{IL}			***0.5***	V
Logic Current	V_H = 2.3V, V_L = 0V	I_{IH}, I_{IL}	***-100***		***+10***	µA
Supply Voltage(s)	All V_{CC} (operating range)	V_{CC}		4.75 to 5.25		V
Temperature Range	Operating Range	T_{CASE}	-40		+105	degC
Supply Current	Total V_{CC}	I_{SUPP}		***270***	***300***	mA
Supply Current	Standby Mode: STBY > V_{IH}	I_{STBY}		***26***	***30***	mA
RF Freq Range	Sets LO freq range	F_{RF}	1450		2700	MHz
IF center Freq Range	Sets LO freq range	F_{IF}	100		300	MHz
Oversample RF Range	▪ Measure Gain at I&Q ▪ Gain setting = G_{MAX} ▪ F_{LO} = 1800 MHz, 2920 MHz ▪ Gain Delta < 2.5 dB	F_{RFD}	***1300***		***2900***	MHz
Oversample IF Range	▪ Measure Gain at I&Q ▪ Gain setting = G_{MAX} ▪ F_{LO} = 1800 MHz, 2920 MHz ▪ Gain Delta < 2.5 dB	F_{IFD}	***20***		***500***	MHz
IF Linearity BW	▪ IP3O > +36 dBm ▪ P_{IN} = -8 dBm per tone ▪ Gain setting = G_{MAX}	IF_{LIN}	100		300	MHz
RF Linearity BW	▪ IF Freq = 200 MHz ▪ IP3O > +35 dBm ▪ P_{IN} = -8 dBm per tone ▪ Gain setting = G_{MAX}	RF_{LIN}	1600		2700	MHz
LO Freq Range		F_{LOH}	1300		2900	MHz
LO Power		P_{LO}		-3 to +3		dBm
RF Input Impedance	Single Ended (RL > 10 dB)	Z_{RF}		50		Ω
IF Output Impedance	Differential (RL > 10 dB)	Z_{IF}		100		Ω
LO port Impedance	Single Ended (RL > 10 dB)	Z_{LO}		50		Ω
Gain maximum	▪ From RF_INX to I+,I- & Q+,Q- ▪ Gain setting = G_{MAX} ▪ Pin = -8 dBm	G_{MAX}	***7.6***[1]	***9***	***10.4***	dB
Gain minimum	▪ From RF_INX to I+,I ▪ Gain setting = G_{MIN} ▪ Pin = +14 dBm	G_{Min}	***-17.5***	***-16.5***	***-15.5***	dB

F1375 SPECIFICATION - CONTINUED

See typical application circuit. Specifications apply at V_{CC} = +5.0V, T_C = 25C, **F_{RF} = 2100 MHz**, **F_{LO} = 1900 MHz**, Gain = G_{MAX}, P_{LO} = 0 dBm, T_C= +25°C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF input trace losses de-embedded.

Parameter	Comment	Symbol	Min	Typ	Max	Units
Noise Figure	▪ From RF_INX to I+,I- out ▪ Gain setting = G_{MAX}	NF		18.2		dB
Output IP3 – G_{MAX}	▪ Measured at I+,I- and Q+,Q- ▪ P_{IN} = -8 dBm per tone ▪ 5 MHz Tone Separation ▪ Gain setting = G_{MAX}	$IP3_{MAX}$	***36***	***40***		dBm
Output IP3 – G_{-15}	▪ Measured at I+,I- and Q+,Q- ▪ P_{IN} = +7 dBm per tone ▪ 5 MHz Tone Separation ▪ Gain setting = G_{-15}	$IP3_{-15}$	38[2]	41		dBm
2nd Harmonic	▪ Measured at I+,I- and Q+,Q- ▪ P_{IN} = -8 dBm ▪ Gain setting = G_{MAX}	H2	-60	-75		dBc
Output IP2	▪ Measured at I+,I- and Q+,Q- ▪ P_{IN} = -8 dBm per tone ▪ 5 MHz Tone Separation ▪ Gain setting = G_{MAX}	$IP2_O$	50	60		dBm
Input compression	▪ Measured at I+,I- and Q+,Q- ▪ P_{IN} = +4 dBm ▪ Gain setting = G_{MAX}	C		***0.3***	***1***	dB
Gain Ripple	▪ RF = 1800 to 2280 MHz ▪ IF = 20 to 500 MHz	Ripple		1.5		dB
Quadrature Amplitude Balance	▪ LO = 1900MHz	BAL_G	***-0.3***		***0.3***	dB
Quadrature Phase Balance	▪ LO = 1900MHz ▪ Measure with 20 GSa/sec scope	BAL_Φ	-2.3		0	degrees
Amplitude Balance over environmentals	▪ Tc = -40C to 105C ▪ LO drive = -3 dBm to +3 dBm ▪ Measure with 20 GSa/sec scope	$BAL_{G\Delta}$	-0.5		+0.5	dB
Quadrature Phase Balance over environmentals	▪ Tc = -40C to 105C ▪ LO drive = -3 dBm to +3 dBm ▪ Measure with 20 GSa/sec scope	$BAL_{\Phi\Delta}$	-3		+1	degrees
LO to IF leakage	▪ Output balun not de-embedded	ISO_{LI}		-30	-25	dBm
LO to RF leakage		ISO_{LR}		-42		dBm
RF to IF isolation	▪ RF leakage at IF relative to IF level ▪ Output balun not de-embedded	ISO_{RI}		-47	-43	dBc
Attenuator Range		Range		25.5		dB

F1375 SPECIFICATION - CONTINUED

See typical application circuit. Specifications apply at V_{CC} = +5.0V, T_C = 25C, **F_{RF} = 2100 MHz**, **F_{LO} = 1900 MHz**, Gain = G_{MAX}, P_{LO} = 0 dBm, T_C= +25°C, STBY = GND unless otherwise noted. Full Lineup measured through to I or Q path. IF Transformers and RF input trace losses de-embedded.

Parameter	Comment	Symbol	Min	Typ	Max	Units
Attenuator Glitching	▪ Step from 15.5 to 16 dB ▪ Step from 16 to 15.5 dB ▪ Measure maximum excursion	$ATTN_G$		0.5		dB
Attenuator Step Accuracy		DNL		0.2		dB
Attenuator Abs. Accuracy	0.5dB to 25.5dB range	INL		***0.2***	***1***	dB
Attenuator Resolution		LSB		0.5		dB
Serial Clock Speed	SPI 3 wire bus	F_{CLOCK}		***20***	***50***	MHz
Data to Clock Setup	SPI 3 wire bus	T_S	3			ns
Data to Clock Hold	SPI 3 wire bus	T_H	3			ns
Clock to CS Setup	SPI 3 wire bus	T_{EN}	3			ns
Clock Pulse Width	SPI 3 wire bus	T_W	5			ns
RF Switch Isolation	▪ F_{RF} < 2.0 GHz ▪ RF_INX selected	ISO_{RFSW}		-47		dBc
RF Switch and attenuator settling times[3]						
EN bit on	• LO_INA: 1900MHz, 0dBm • RF_INX: 2100MHz, -8dBm	EN_{ON}		100		
EN bit off		EN_{OFF}		50		
RF switched X to Y (no Y signal)		RF_{SWXY}		150		
RF switched Y to X (no Y signal)		RF_{SWYX}		200		
Attenuator switched 0dB to 25.5dB (max)		ATT_{SETL}		300		
Attenuator switched 25.5dB (max) to 0dB				300		
Attenuator switched 15.5dB to 16dB				250		
Attenuator switched 16dB to 15.5dB				250		

SPECIFICATION NOTES:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test
2 – All other Items in min/max columns are Guaranteed by Design Characterization
3 – Excludes SPI write time

POWER-ON SEQUENCE

The power-on sequence ensures F1375 works in default mode once powered on. If the F1375 is programmed after applying DC power, the following power-on sequence is not needed. Note: To use power on sequence, SW_LATCH cannot be grounded permanently.

The power-on sequence should be:

1. CSb & SW_LATCH must be set low at power-on
2. Once powered on, first set SW_LATCH high, then set CSb high
3. Proceed with normal programming.

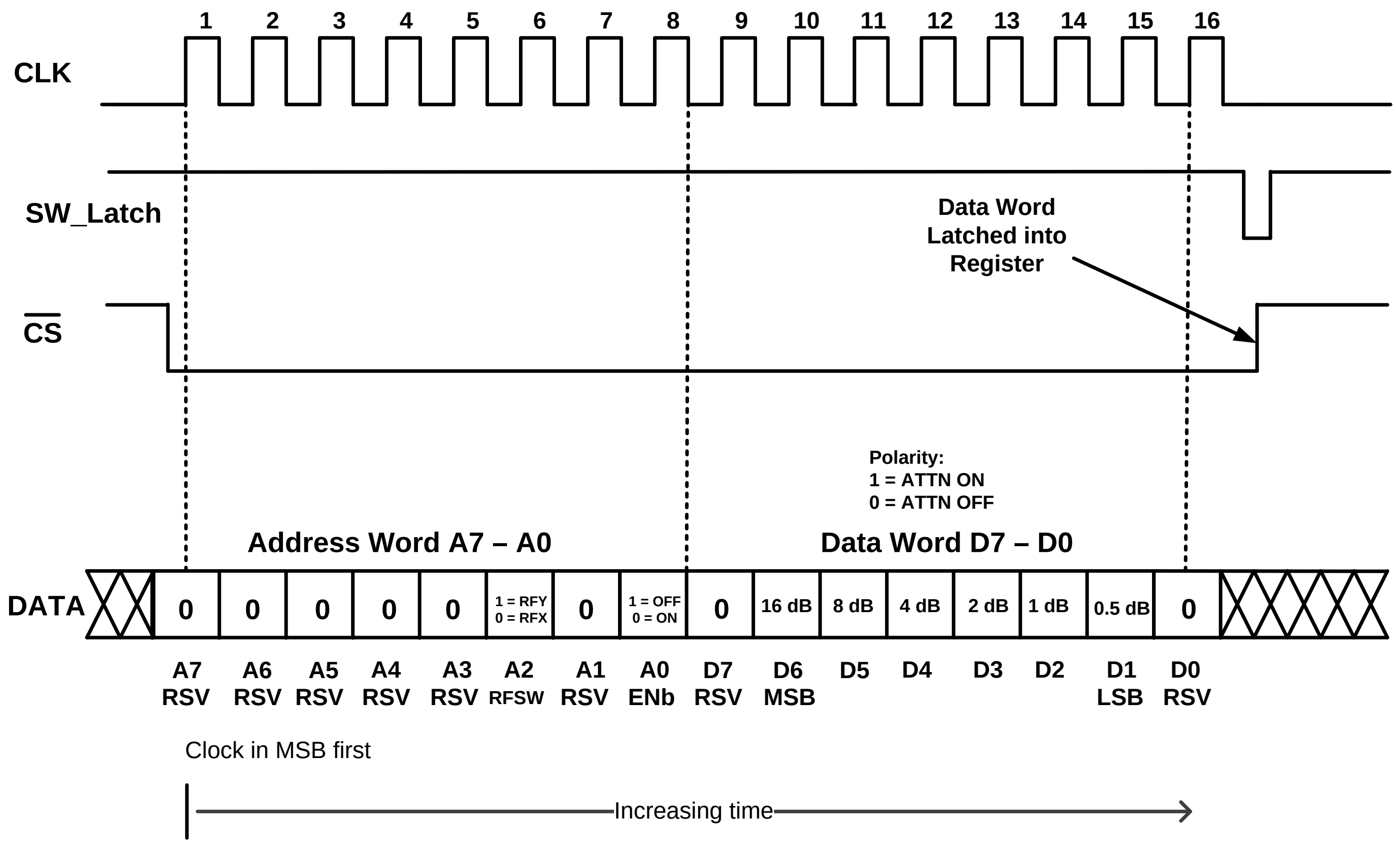
The default state after using power-on sequence:

- Maximum attenuation
- RF_INX selected
- Normal operation (not Standby Mode)

SERIAL PROGRAMMING

The device is programmed via the serial port by asserting Chip Select (CSb). Note: Most-Significant-Bit first, where the Address Word is the Most-Significant-Byte.

Serial mode timing diagram high level:

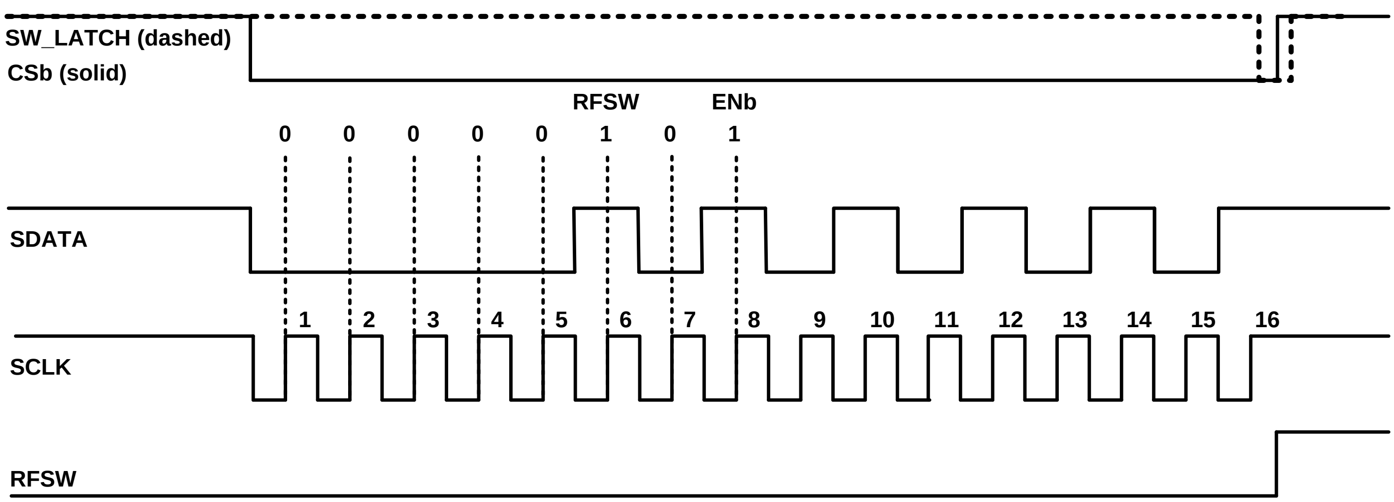


To program the Serial Interface:

If CSb is de-asserted (set to high), the serial interface will ignore the CLK line. Once CSb is asserted (set to low), the serial interface will recognize the CLK and any data present on DATA will be clocked into the registers with each rising CLK edge. After the 16th CLK cycle, and before the 17th CLK cycle, CSb must be de-asserted to successfully program the part with the desired bytes. If CSb is de-asserted before the 16th CLK cycle, or after the 17th CLK cycle, there is no guarantee that the correct bytes will be programmed and the user will have to re-program the interface in accordance with the aforementioned procedure.

SW_LATCH Programming Sequence

- When SW_LATCH is pinned high during the programming sequence, "RFSW" and "ENb" registers cannot be programmed and therefore will not toggle.
- If SW_LATCH is pinned low during the programming sequence, the "RFSW" and "ENb" register will toggle. This can be prevented with the "Programming Sequence" below.



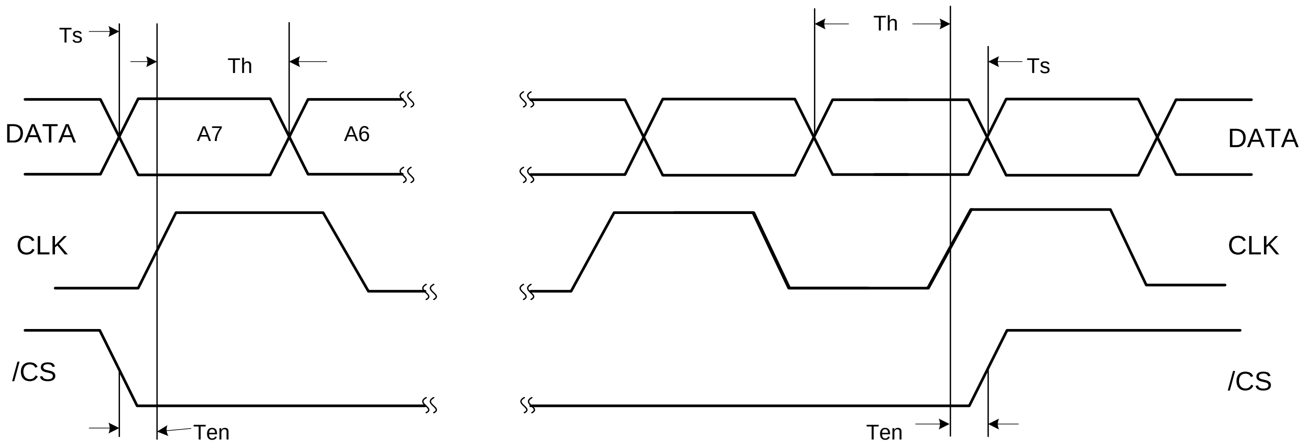
Sequence for Programming Registers A<2>:A<0>

1) SW_Latch = 1; CSb = 0
2) *CLK in 8- or 16-bit word, do not de-assert (pull high) CSb*
3) Set SW_LATCH = 0 while CSb = 0 remains)
4) With SW_Latch = 0, set CSb = 1
5) Set SW_Latch = 1
6) Program complete

Special Note Regarding Phase of I & Q:

- When LO is high-side injected, IF_I leads IF_Q by 90 degrees
- When LO is low-side injected, IF_Q leads IF_I by 90 degrees

SERIAL MODE TIMING DIAGRAM ZOOM:



- Data is shifted with the rising edge of CLK when /CS is low
- The rising edge of /CS latches data into the device

LOGIC TRUTH TABLE:

STBY	SW_LATCH	MODE	WRITE ACCESS
0	0	Operating Mode	A2:A0 Enabled, D7:D0 Enabled
0	1	Operating Mode	A2:A0 Disabled, D7:D0 Enabled
1	0	Off	A2:A0 Enabled, D7:D0 Enabled
1	1	Off	A2:A0 Disabled, D7:D0 Enabled

F1375 Attenuation Table

The F1375 gain/attenuation setting is controlled by 6 bits in the data word. The device provides an added attenuation range from 0 dB to 25.5 dB in 0.5 dB steps. A “high” or “1” bit corresponds to attenuation stepped IN, while a “low” or “0” bit corresponds to attenuation stepped OUT.

F1375 DPD Demodulator - Attenuation Table (Data Word D7-D0)

BINARY	HEX	Added Atten (dB)		BINARY	HEX	Added Atten (dB)
00000000	00	0		00110100	34	13
00000010	02	0.5		00110110	36	13.5
00000100	04	1		00111000	38	14
00000110	06	1.5		00111010	3A	14.5
00001000	08	2		00111100	3C	15
00001010	0A	2.5		00111110	3E	15.5
00001100	0C	3		01000000	40	16
00001110	0E	3.5		01000010	42	16.5
00010000	10	4		01000100	44	17
00010010	12	4.5		01000110	46	17.5
00010100	14	5		01001000	48	18
00010110	16	5.5		01001010	4A	18.5
00011000	18	6		01001100	4C	19
00011010	1A	6.5		01001110	4E	19.5
00011100	1C	7		01010000	50	20
00011110	1E	7.5		01010010	52	20.5
00100000	20	8		01010100	54	21
00100010	22	8.5		01010110	56	21.5
00100100	24	9		01011000	58	22
00100110	26	9.5		01011010	5A	22.5
00101000	28	10		01011100	5C	23
00101010	2A	10.5		01011110	5E	23.5
00101100	2C	11		01100000	60	24
00101110	2E	11.5		01100010	62	24.5
00110000	30	12		01100100	64	25
00110010	32	12.5		01100110	66	25.5

Because the first and last bits of the Data Word are not presently used by the F1375, two additional hex character pairs exists for each of those in this table. For example, data words of either H00, H80, or H01 (binary “00000000,” “10000000,” or 00000001) will place the F1375 in its minimum attenuation state. Likewise, data words of either H66, HE6, or H67 (binary “01100110” or “11100110” or “01100111”) will place the F1375 in its maximum attenuation state of 25.5 added attenuation.

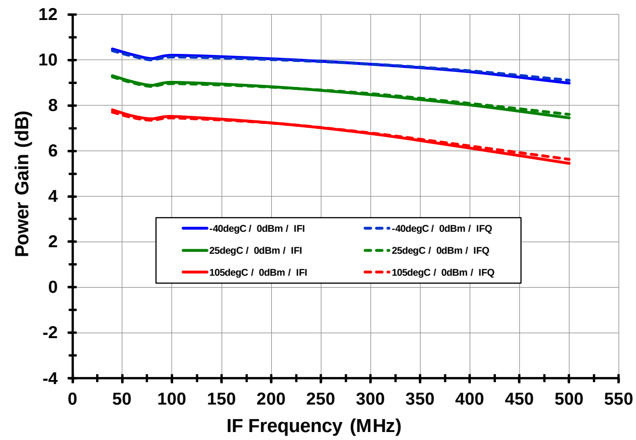
TYPICAL OPERATING CONDITIONS

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply

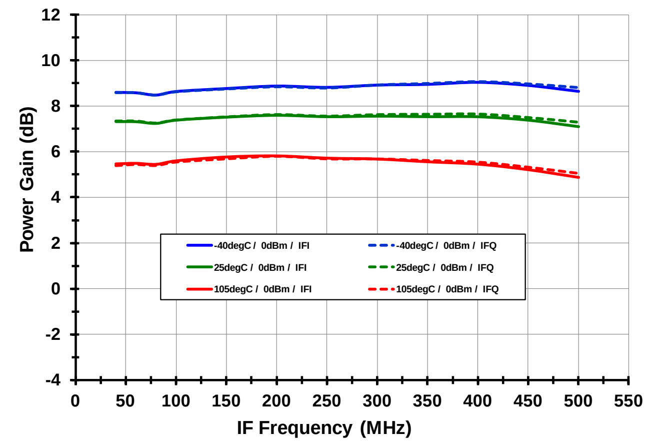
- **IF = 200 MHz**
- **Tone spacing = 5 MHz**
- **Pin = - 8 dBm / Tone**
- **Pout ~ 1 dBm / Tone**
- **RF_X, IF_Q selected**
- **Minimum Attenuation selected (0 dB ATTN)**
- **V_{CC} = 5.00 V**
- **LO level = 0 dBm**
- **Case Temperature = 25C**
- **All Temperatures are Case Temperature (T_{CASE})**
- **Output Transformers are de-embedded**
- **Input RF trace losses are de-embedded**

TOCs F1375 [Gain, IP3$_O$, IP2$_O$, Fixed LO vs Temp] (-1-)

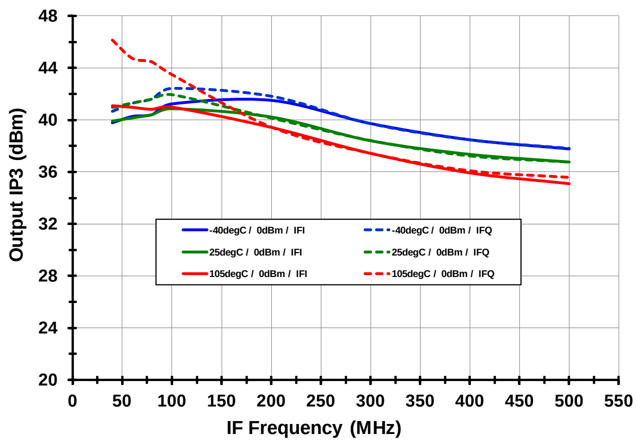
Gain [LO = 1.80 GHz, Low Side Injection]



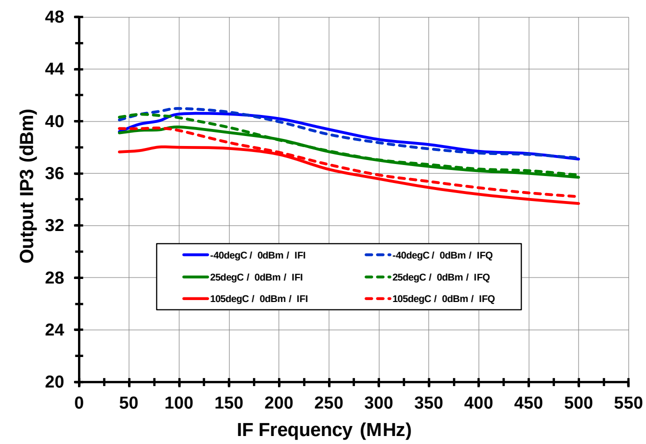
Gain [LO = 2.92 GHz, High Side Injection]



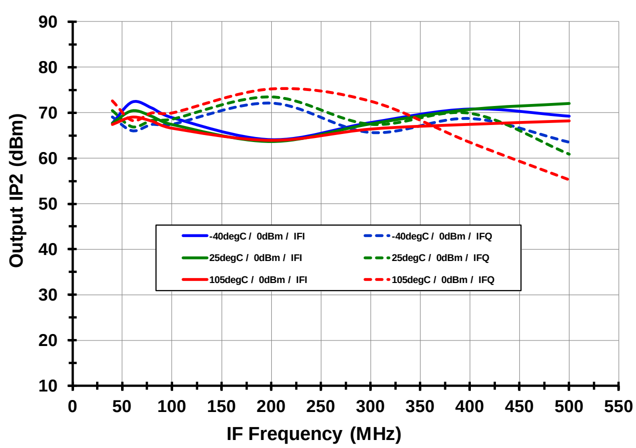
IP3$_O$ [LO = 1.80 GHz, Low Side Injection]



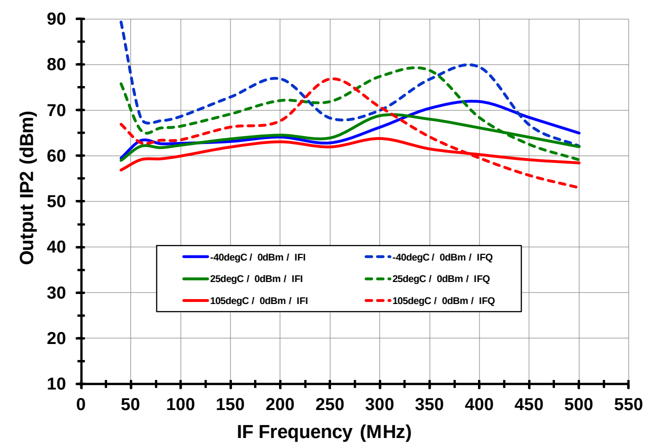
IP3$_O$ [LO = 2.92 GHz, High Side Injection]



IP2$_O$ [LO = 1.80 GHz, Low Side Injection]

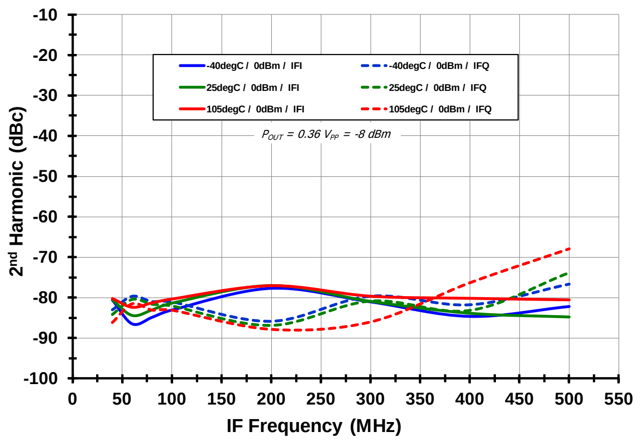


IP2$_O$ [LO = 2.92 GHz, High Side Injection]

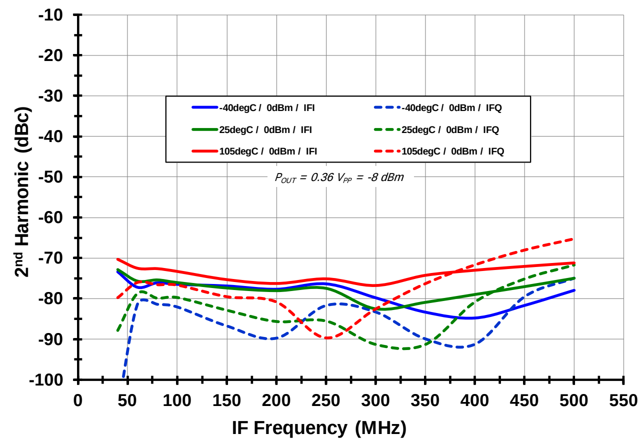


TOCs F1375 [H2 Fixed LO vs Temp, Transformer loss, RF Trace Loss] (-2-)

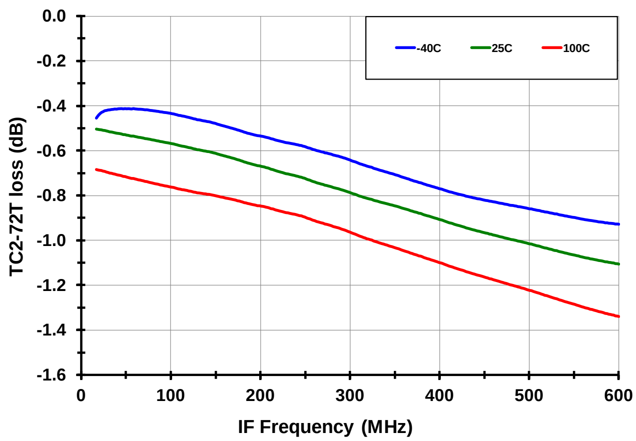
H2 [LO = 1.8 GHz, Low Side Injection]



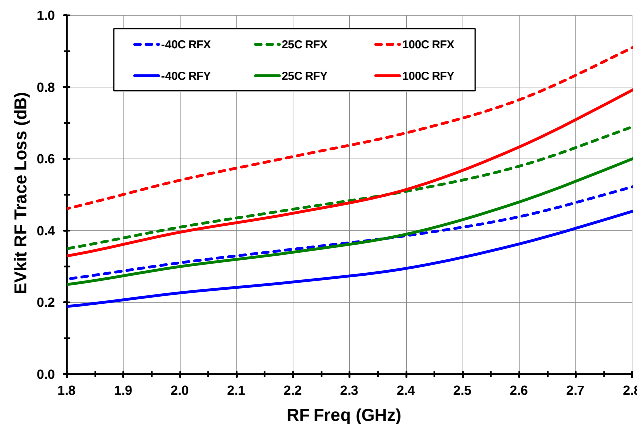
H2 [LO = 2.92 GHz, High Side Injection]



IF Transformer Loss

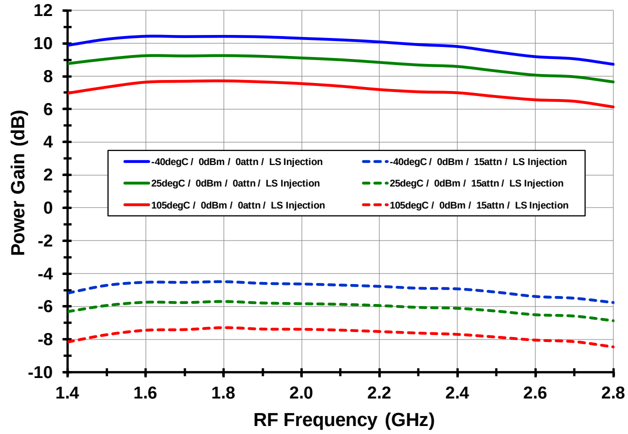


EVKit RF Trace Loss

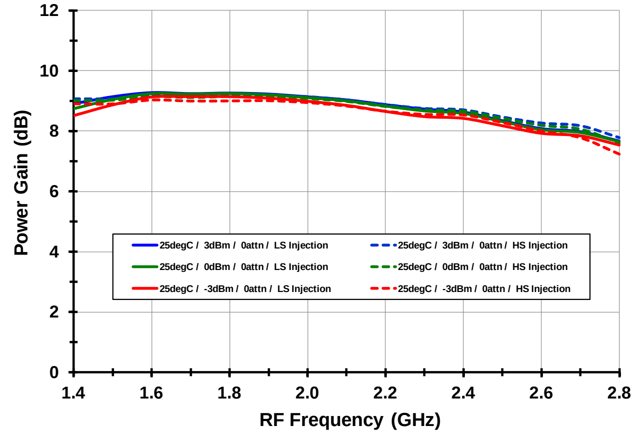


TOCs F1375 [Fixed IF = 200MHz Gain, IP3$_O$, IP2$_O$] (-3-)

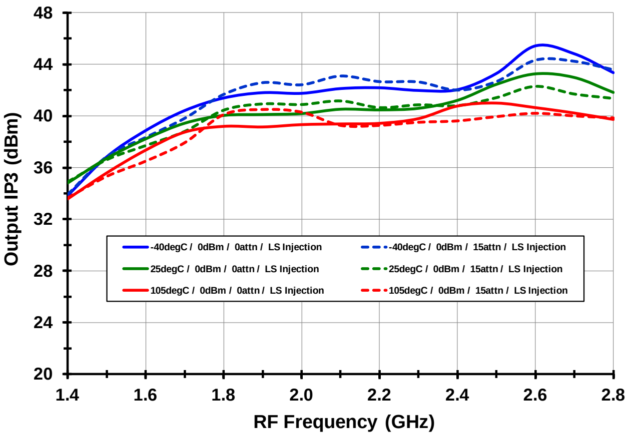
Gain [vs. Tcase]



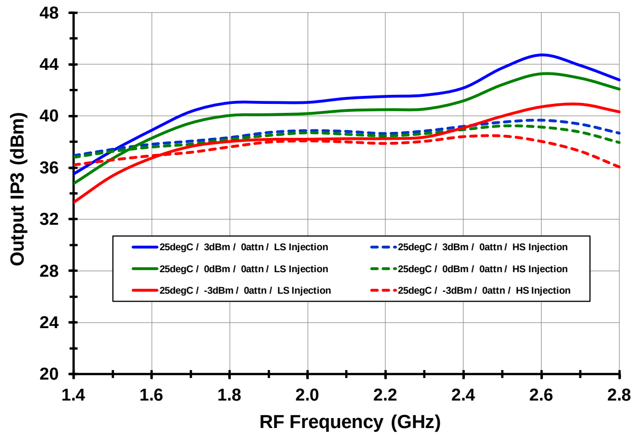
Gain [vs. LO Level]



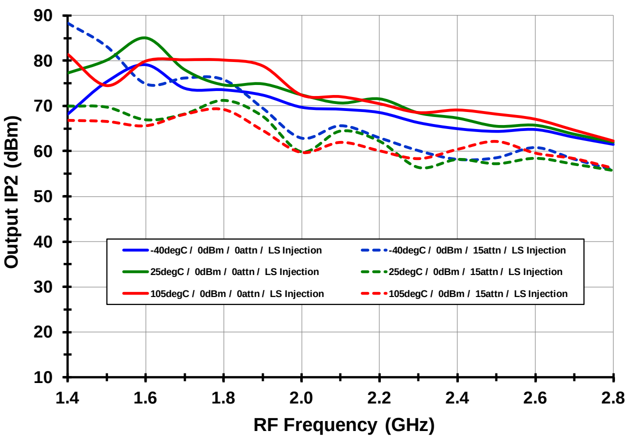
IP3$_O$ [vs. Tcase]



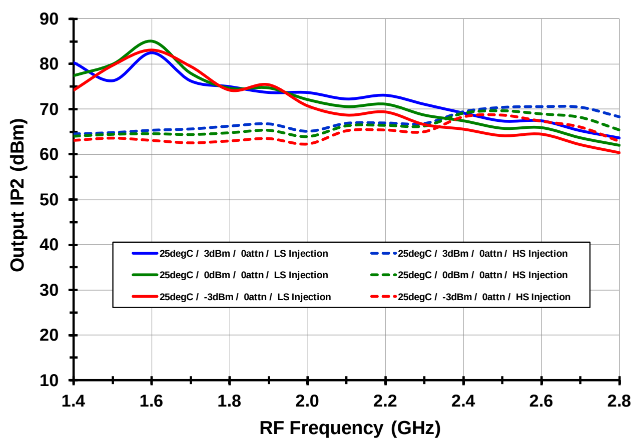
IP3$_O$ [vs. LO Level]



IP2$_O$ [vs. Tcase]

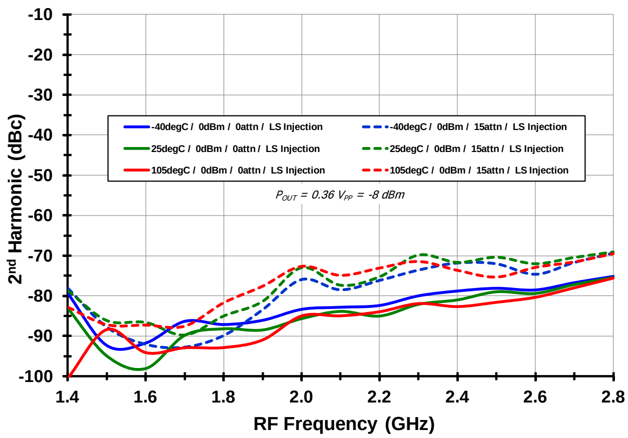


IP2$_O$ [vs. LO Level]

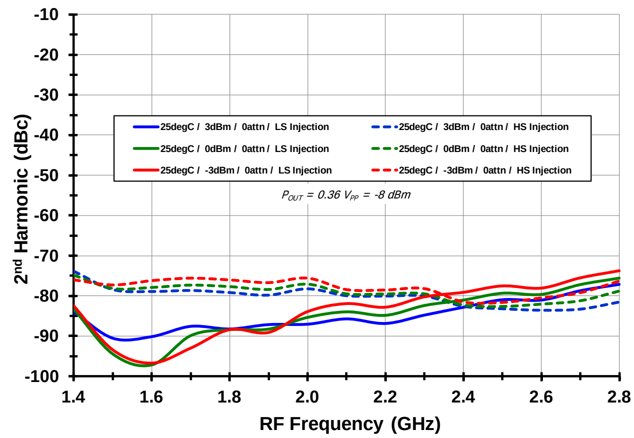


TOCs F1375 [Fixed IF = 200MHz, H2, LO – IF Leakage, ICC] (-4-)

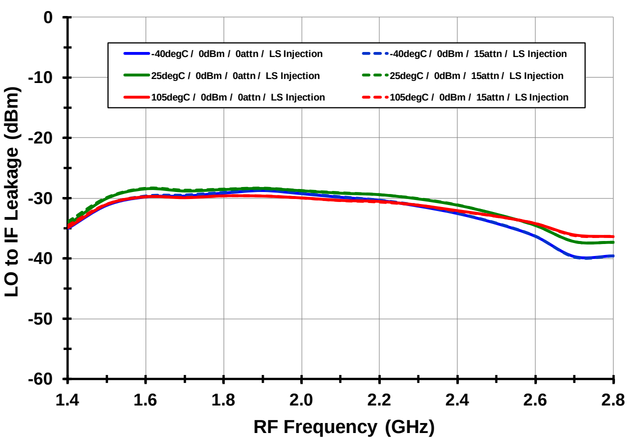
H2 [vs. Tcase]



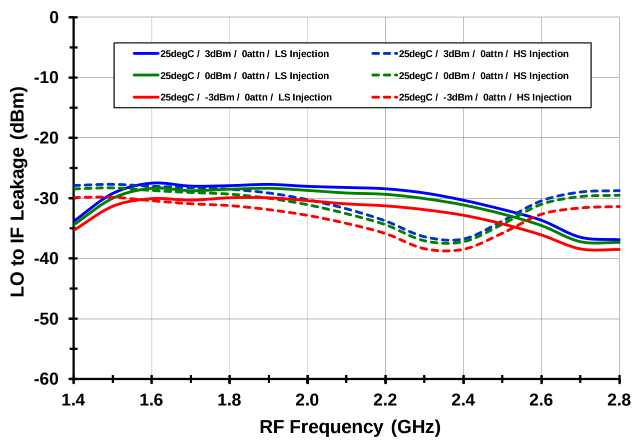
H2 [vs. LO Level]



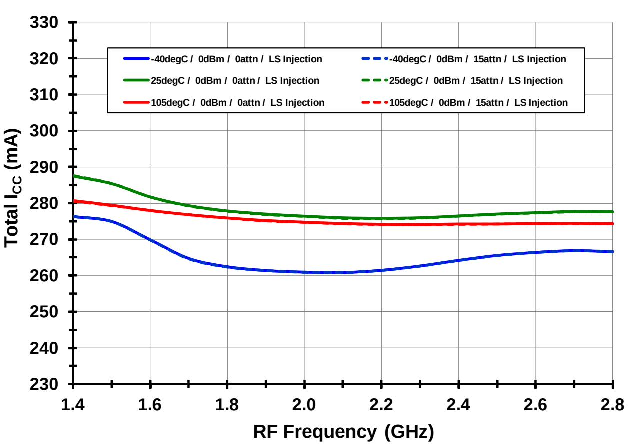
LO - IF [vs. Tcase]



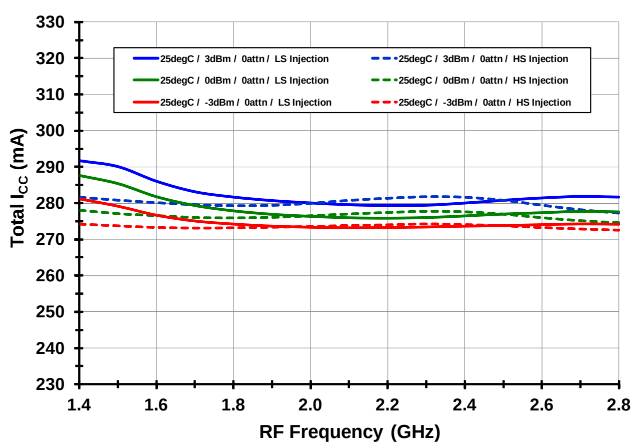
LO - IF [vs. LO Level]



I_{CC} [vs. Tcase]

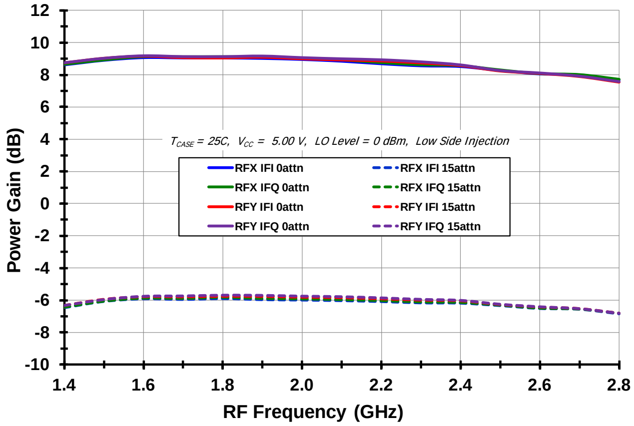


I_{CC} [vs. LO Level]

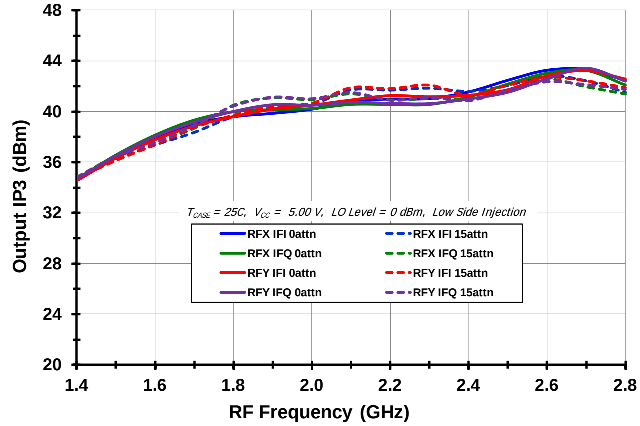


TOCs F1375 [Fixed IF Configuration, Gain, IP3O, IP2O, H2, Leakage] (-5-)

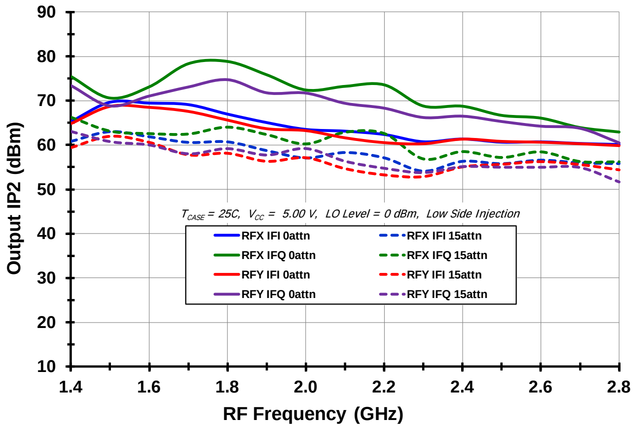
Gain



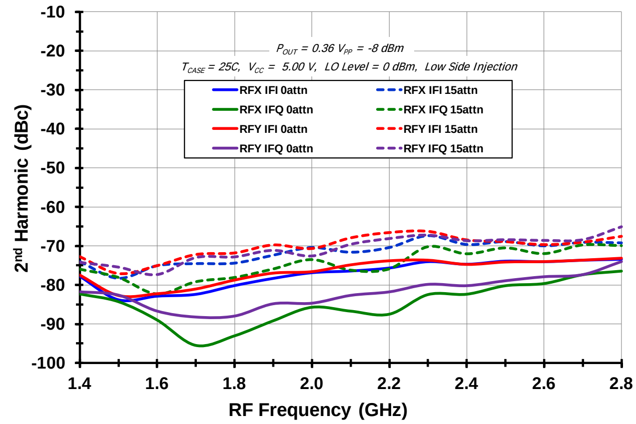
IP3O



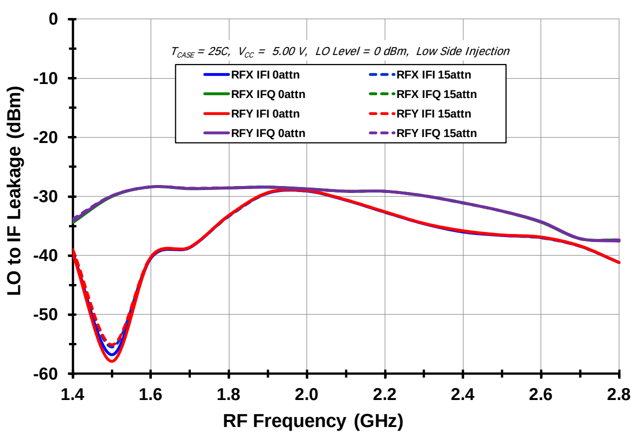
IP2O



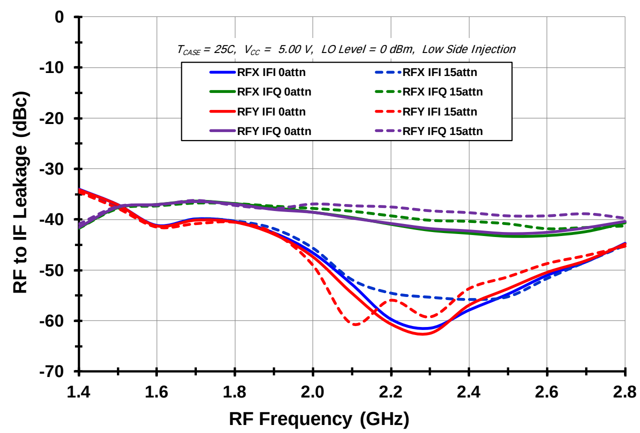
H2



LO – IF

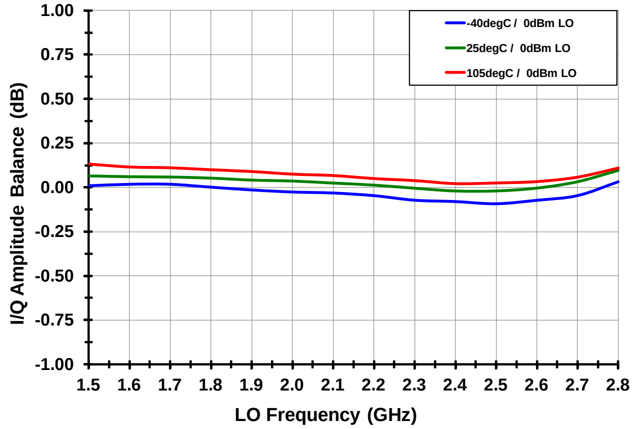


RF - IF

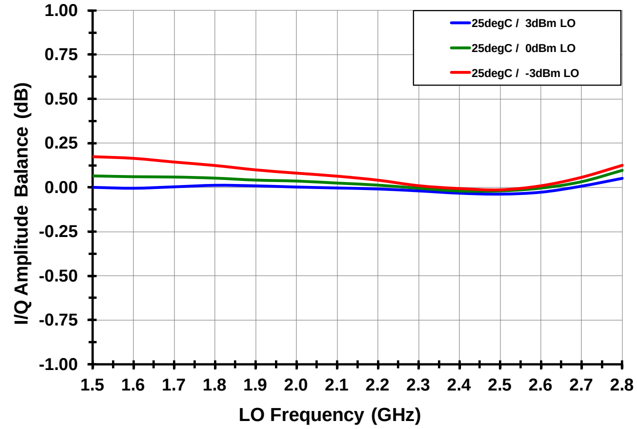


TOCs F1375 [Quadrature, ATTN accuracy, and IF impedance] (-6-)

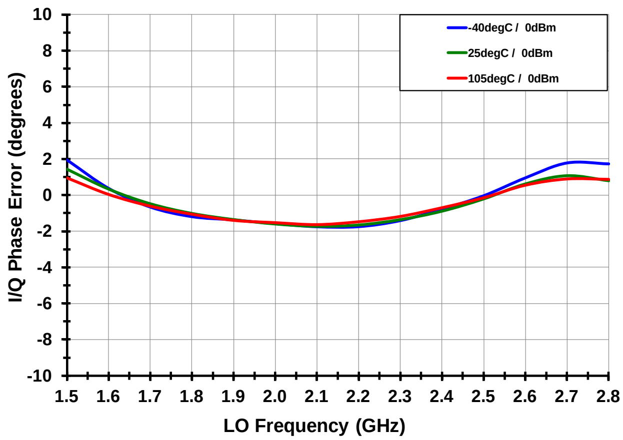
I / Q Amplitude [vs. Tcase]



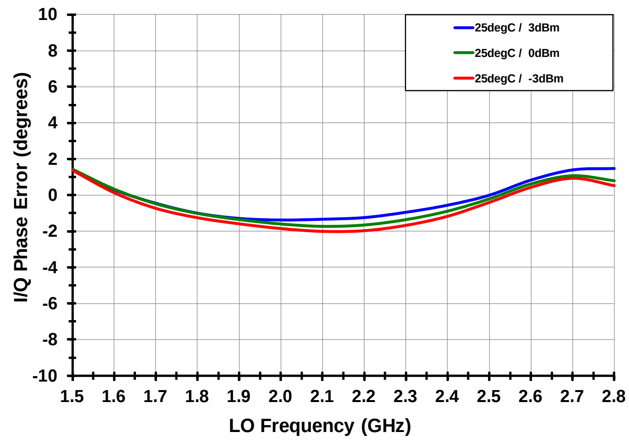
I / Q Amplitude [vs. LO Level]



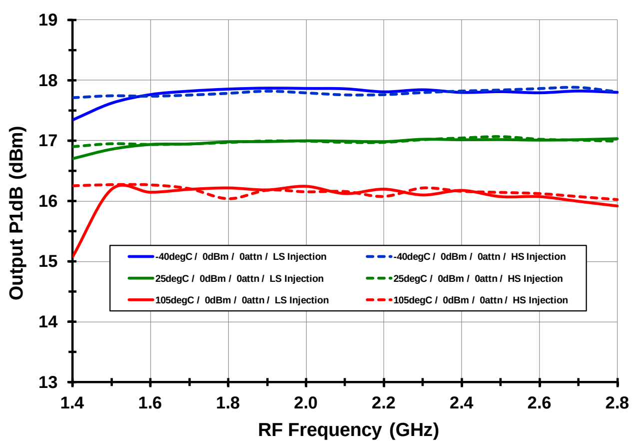
I / Q Phase [vs. Tcase]



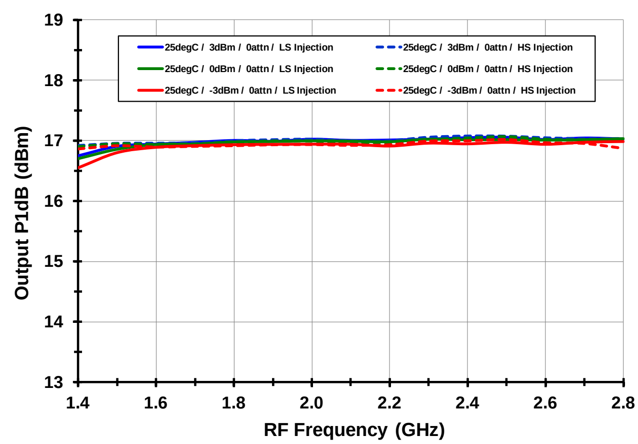
I / Q Phase [vs. LO Level]



Output P1dB [vs. Tcase]

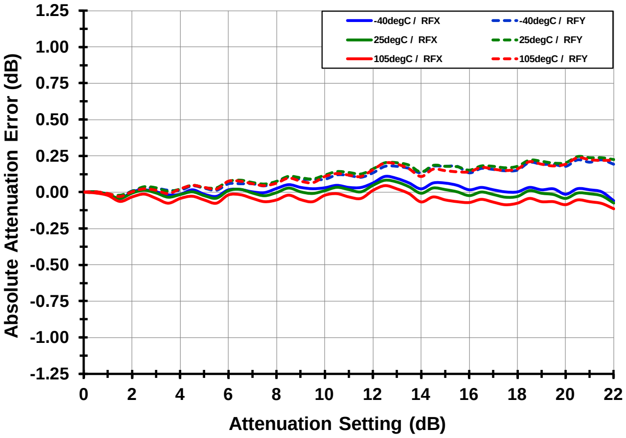


Output P1dB [vs. LO Level]

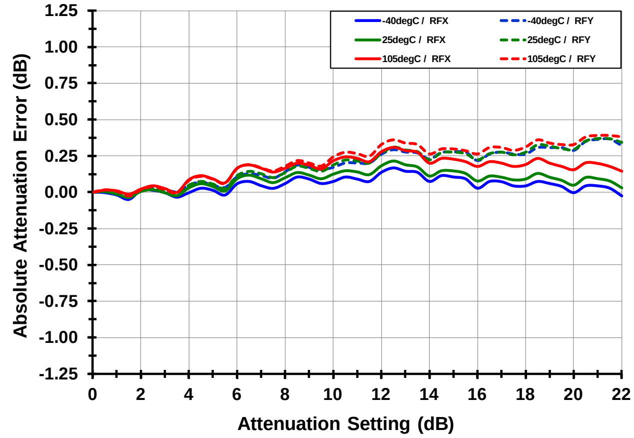


TOCs F1375 [ATTN ACCURACY, NOISE FIGURE] (-7-)

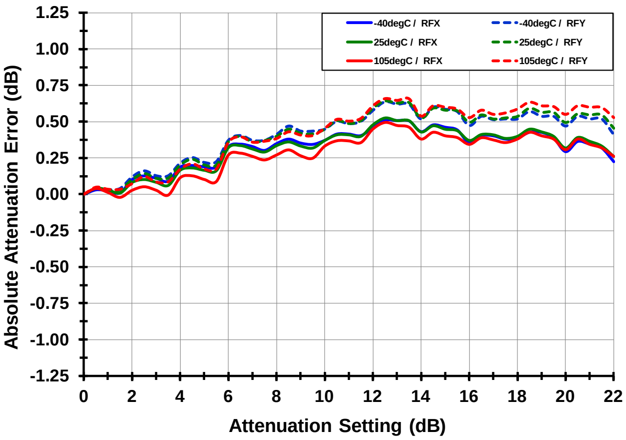
ATTENUATION ACCURACY [1.7 GHZ]



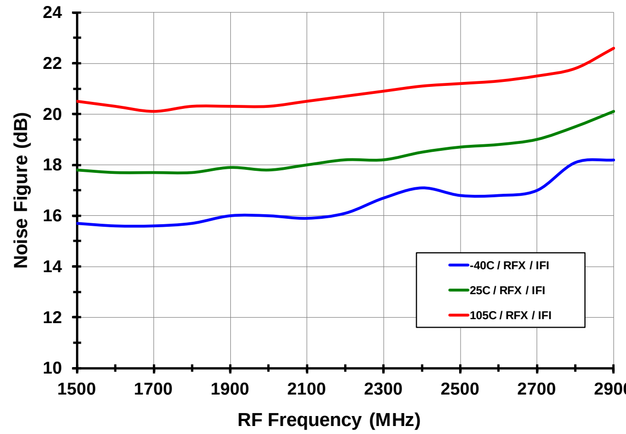
ATTENUATION ACCURACY [2.1 GHZ]



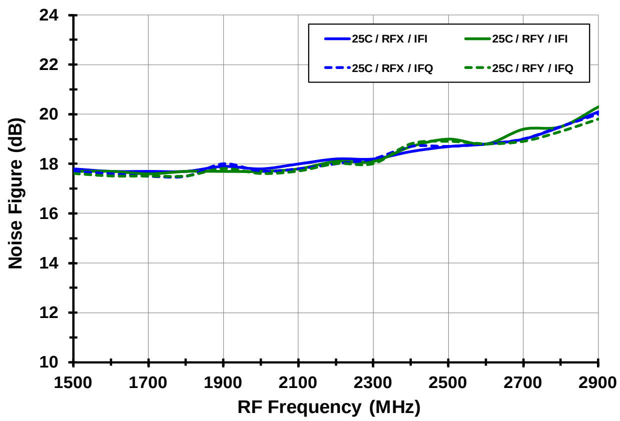
ATTENUATION ACCURACY [2.7 GHZ]



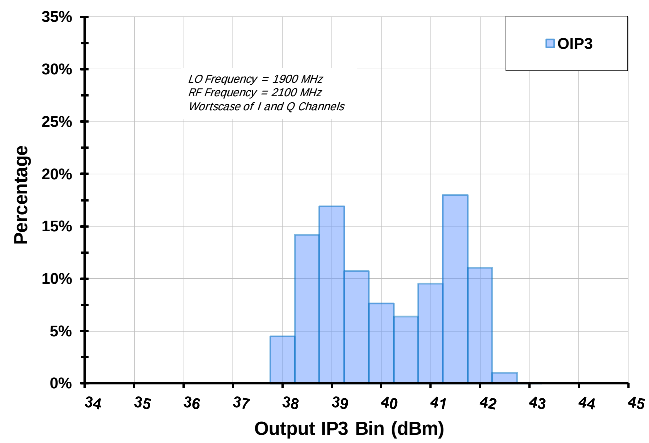
NOISE FIGURE [VS. TCASE, MEASURED RFX TO IFI]



NOISE FIGURE [25C, VS. CONFIGURATION]

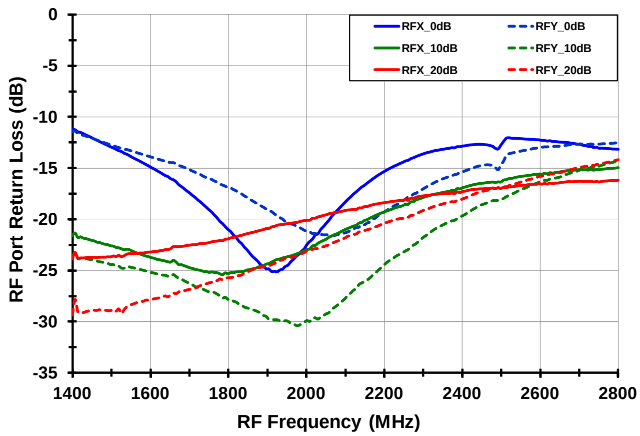


OIP3 HISTOGRAM [N=1440]

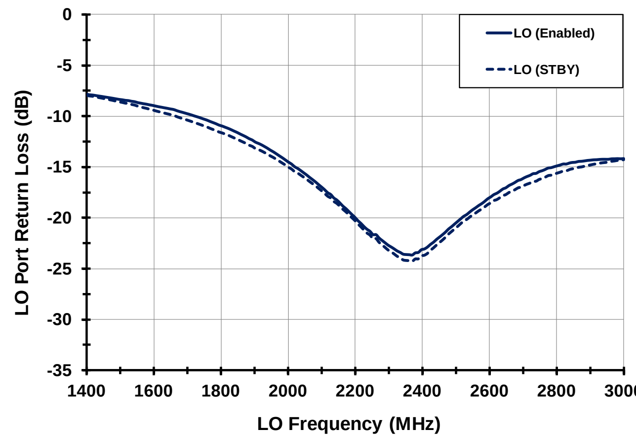


TOCs F1375 [Isolation, Return Loss, Histograms] (-8-)

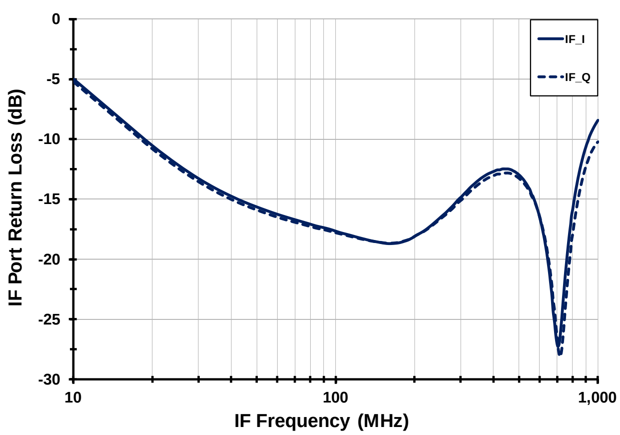
RF Port Return Loss



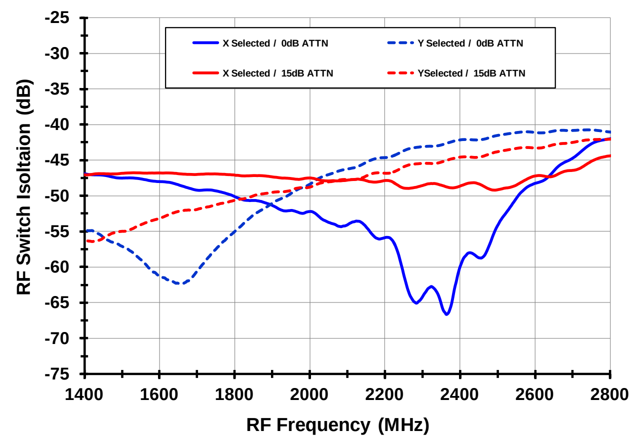
LO Port Return Loss



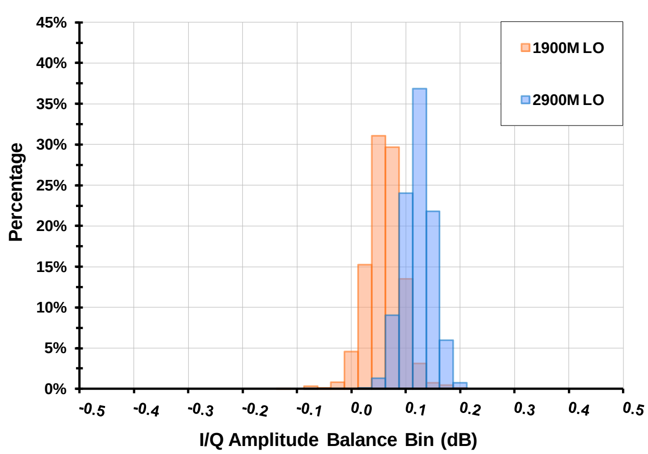
IF Port Return Loss



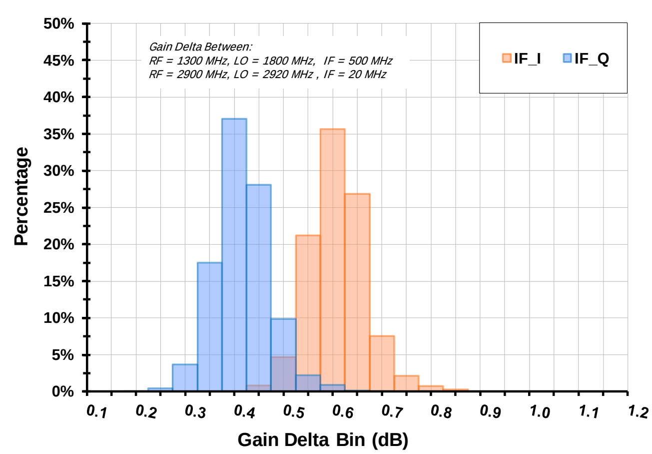
RF SP2T Isolation



I / Q Error Histogram [N = 1440]



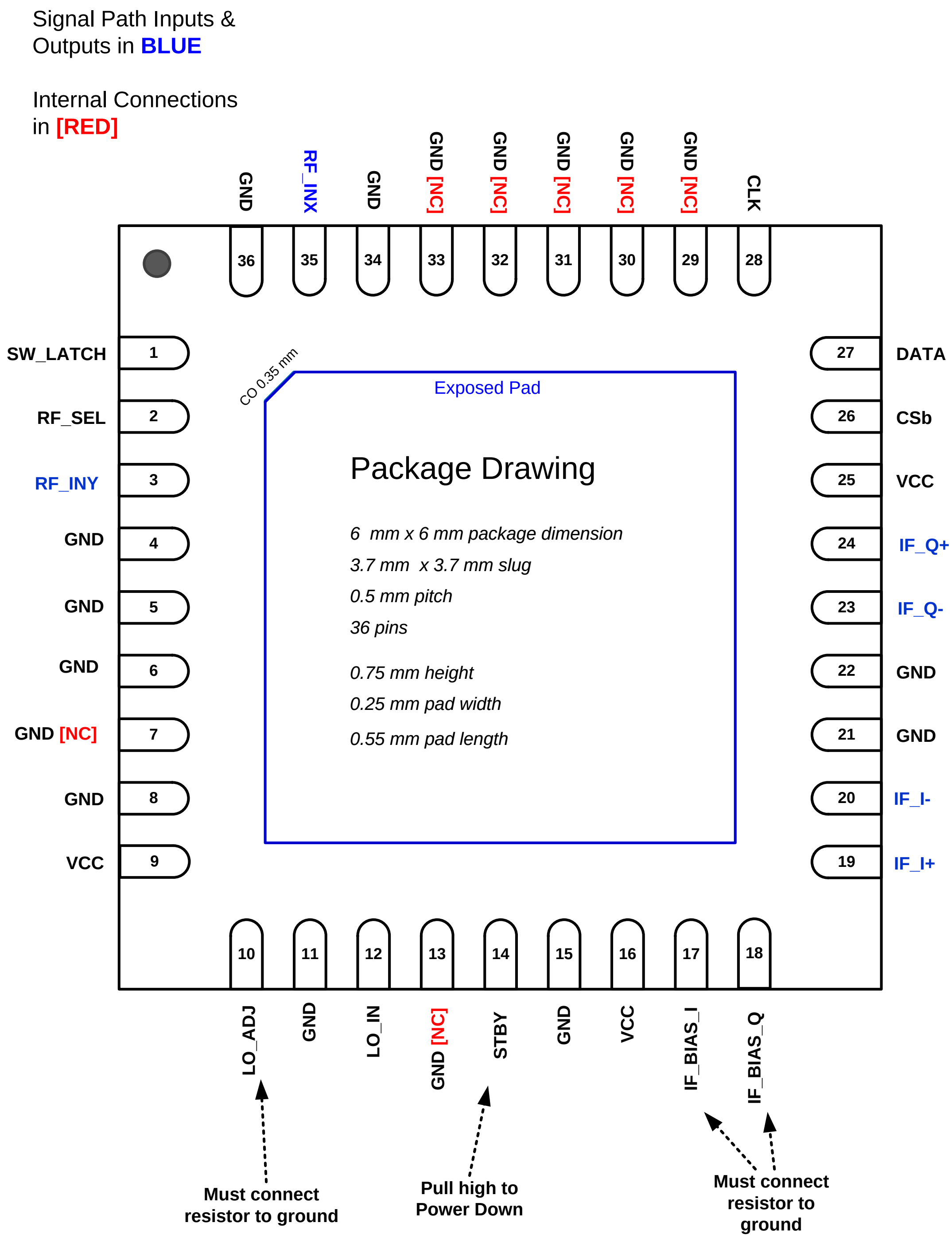
Band Edge Gain Delta [N = 1440]



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website The package information is the most current data available and is subject to change without revision of this document.

Pin Diagram



PIN DESCRIPTIONS

Pins	Name	Function
1	SW_LATCH	Stand-by latch. Pull Low or Ground for Normal Operation. If left floating, this input will be internally pulled high, disabling SPI writes to ENb (Standby) and RF SW bits (A0, A2).
2	RF_SEL	RF input selection. Pull high to select RF_INY. Pull low to select RF_INX.
3	RF_INY	Alternate RF Input. Pull pin 2 high to select RF_INY. AC couple to this pin. Separated from RF_INX by internal SP2T. Internally matched to 50 ohms.
4, 5, 6, 8, 11,15, 21, 22, 34, 36	GND	Ground these Pins.
7, 13, 29, 30, 31, 32, 33	NC	No Connection. Not internally connected. OK to connect to Vcc. Recommended Connection is Ground
9, 16, 25	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
10	LO_ADJ	Connect the specified resistor from this pin to ground to set the LO path I_{CC}. This IS a current setting resistor
12	LO_IN	LO Input. AC couple to this pin. Internally matched to 50 ohms
14	STBY	STBY Mode. Pull this pin high for Standby mode (~26 mA). Pull low or Ground for normal Operation
17, 18	IF_BIAS_I IF_BIAS_Q	Connect the specified resistor from this pin to ground to set the IF amplifier bias reference. This is NOT a current setting resistor
19, 20	IF_I+, IF_I-	*In-Phase* Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the Typical Application Circuit).
23, 24	IF_Q-, IF_Q+	*Quadrature* Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the Typical Application Circuit).
26	CSb	Chip Select Bar. The falling edge initiates a programming cycle and the rising edge latches the programmed shift register data into the active register.
27	DATA	Serial Data Input
28	CLK	Serial Clock Input
35	RF_INX	Main RF Input. Pull pin 2 low to select RF_INX. AC couple to this pin. Separated from RF_INY by internal SP2T. Internally matched to 50 ohms
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

CONTROL PIN VOLTAGE & RESISTANCE VALUES (PINS NOT CONNECTED)

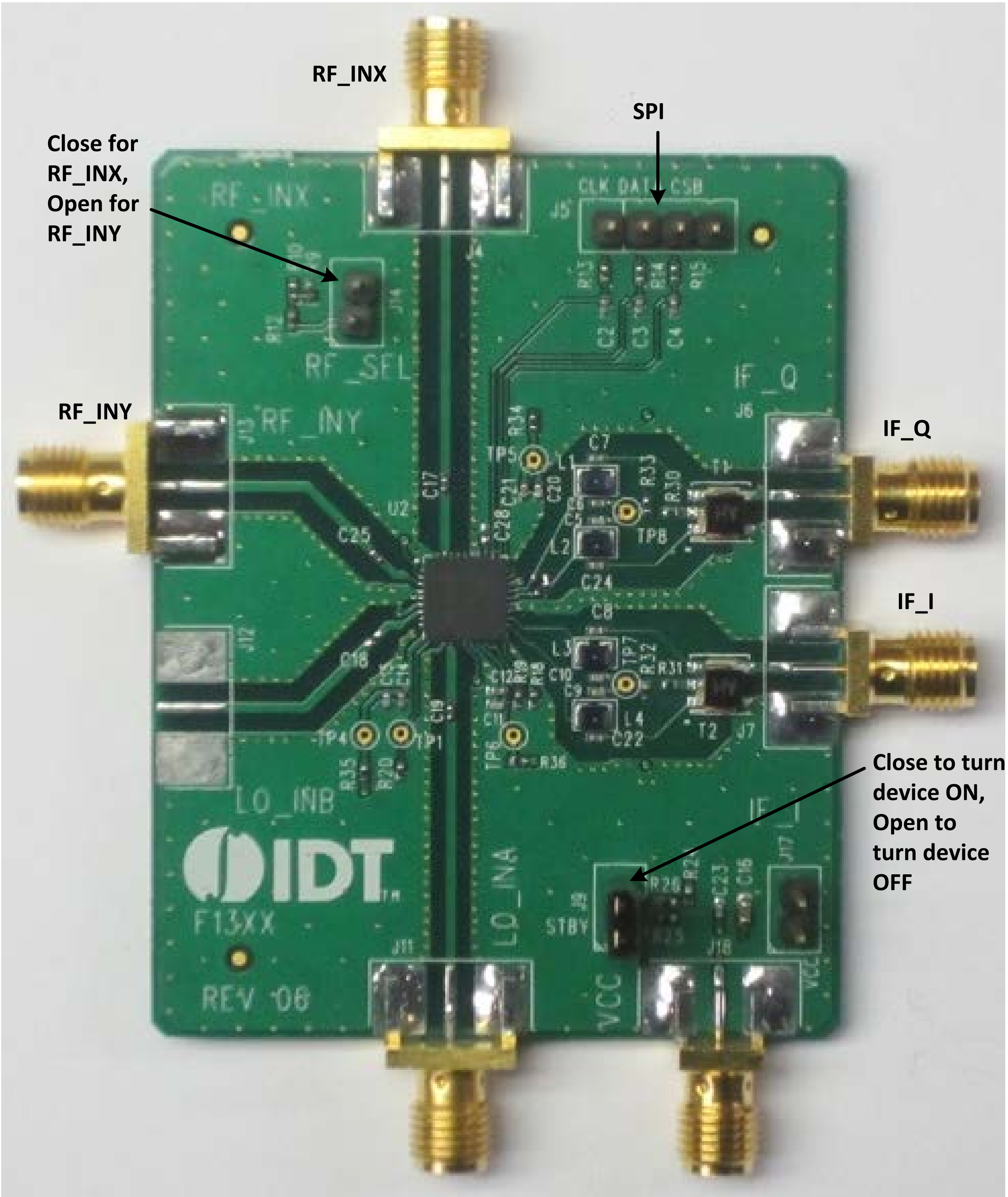
The following table provides open-circuit DC voltage and resistance values referenced to ground for each of the control pins listed.

Pin	Name	DC voltage (volts)	Resistance (ohms)
1	SW_LATCH	1.75	1.6M
2	RF_SEL	1.75	800K
14	STBY	5	50K
26	CSb	1.75	1.6M
27	DATA	1.75	1.6M
28	CLK	1.75	1.6M

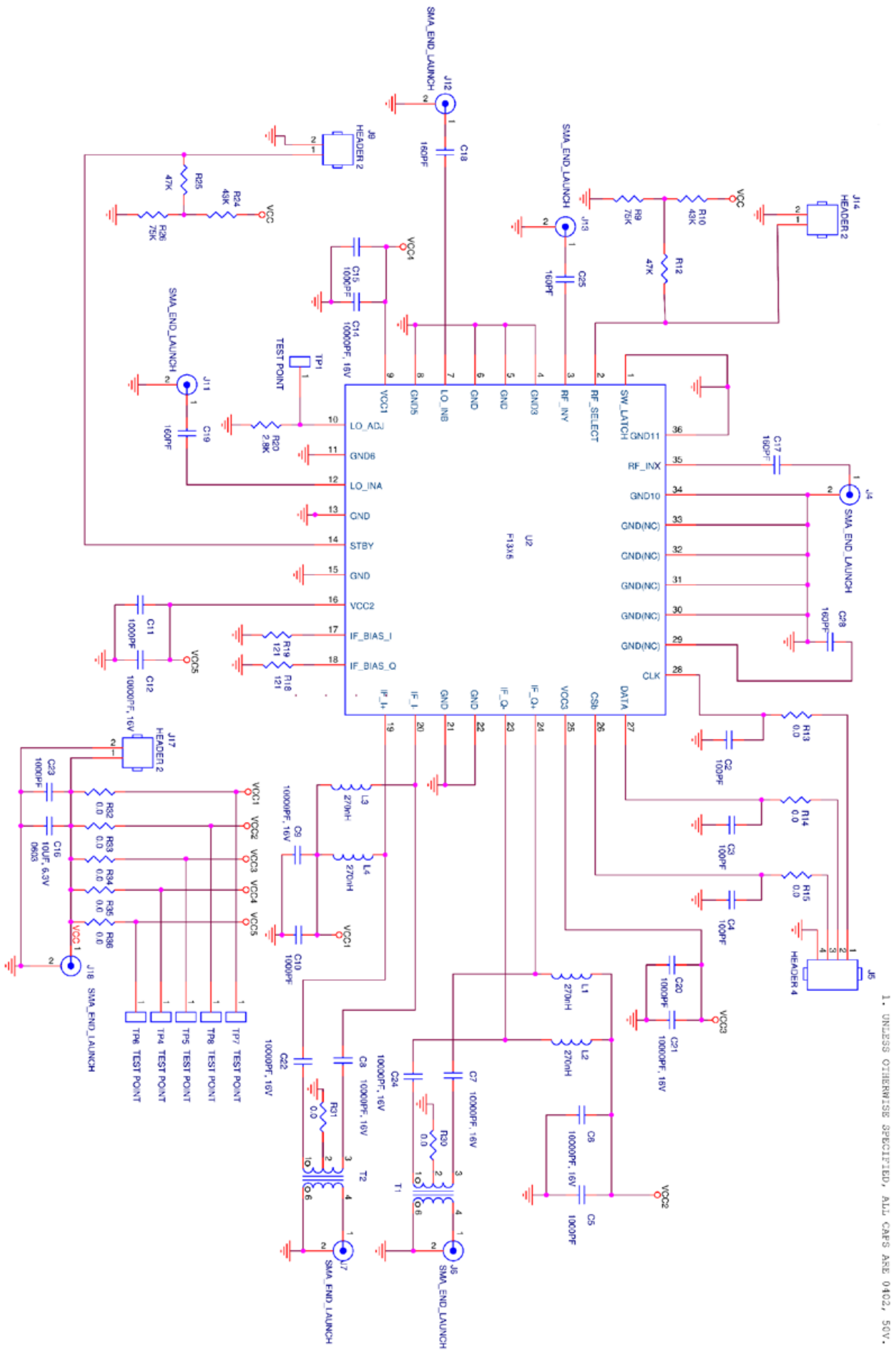
POWER SUPPLIES

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

EVKIT PICTURE / LAYOUT / OPERATION



EVKIT / APPLICATION CIRCUIT

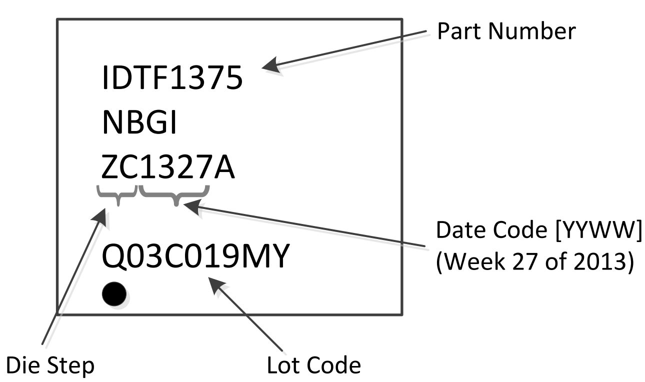


EVKIT BOMS

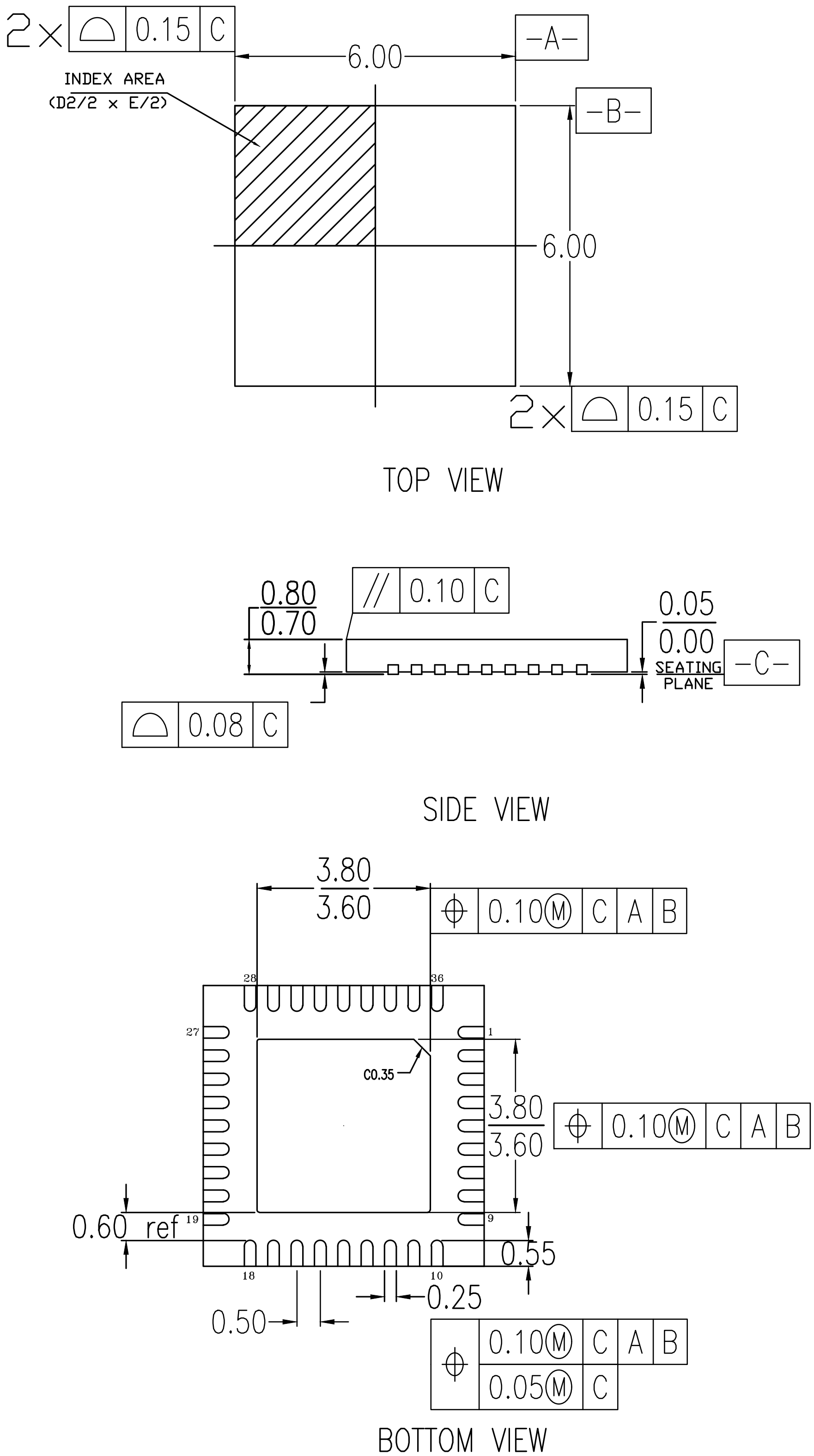
F1375
12/4/2013

Item #	Value	Size/Re	Desc	Mfr. Part #	Mfr.	Supplier Part #	Supplier	Part Reference	Qty
1	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01	MURATA	490-1313-1-ND	Digikey	C6,7,8,9,12,14,21,22	9
2	1000pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01	MURATA	490-3244-1-ND	Digikey	C5,10,11,15,20,23	6
3	39pF	0402	CAP CER 39PF 50V 5% C0G 0402	GRM1555C1H390JZ01	MURATA	490-1286-1-ND	Digikey	C17,19,25	3
4	100pF	0402	CAP CER 100PF 50V 5% NP0 0402	GRM1555C1H101JZ01	MURATA	490-3458-1-ND	Digikey	C2,3,4	3
5	10uF	0603	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47	MURATA	490-3896-1-ND	Digikey	C16	1
6	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	3M9447-ND	Digikey	J9,14,17	3
7	Header 4 Pin	TH 4	CONN HEADER VERT SGL 4POS GOLD	961104-6404-AR	3M	3M9449-ND	Digikey	J5	1
8	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	530-142-0711-821	Mouser	J6,7,18	3
9	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson	530-142-0701-851	Mouser	J4,11,13	3
10	1uH	0805	0805LS (2012) Ceramic Chip Inductor	0805LS-102XJLB	COILCRAFT	0805LS-102XJLB	COILCRAFT	L1,2,3,4	4
11	43K	0402	RES 43K OHM 1/10W 1% 0402 SMD	ERJ-2RKF4302X	Panasonic	P43.0KLCT-ND	Digikey	R9,26	2
12	75K	0402	RES 75K OHM 1/10W 1% 0402 SMD	ERJ-2RKF7502X	Panasonic	P75.0KLCT-ND	Digikey	R10,24	2
13	2.37K	0402	RES 2.37K OHM 1/10W 1% 0402 SMD	ERJ-2RKF2371X	Panasonic	P2.37KLCT-ND	Digikey	R20	1
14	130	0402	RES 130 OHM 1/10W 1% 0402 SMD	ERJ-2RKF1300X	Panasonic	P130LCT-ND	Digikey	R18,19	2
15	47K	0402	RES 47.0K OHM 1/16W 1% 0402 SMD	RC0402FR-0747KL	Yageo	311-47.0KLRCT-ND	Digikey	R12,25	2
16	100	0402	RES 100 OHM 1/10W 1% 0402 SMD	ERJ-2RKF1000X	Panasonic	P100LCT-ND	Digikey	R13-15	3
17	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	P0.0JCT-ND	Digikey	R30-36	7
18	2:1 Balun	SM-22	2:1 Center Tap Balun	TC2-72T+	Mini Circuits	TC2-72T+	Mini Circuits	T1,2	2
19	F1375	QFN-36	DPD Demodulator	F1375	IDT	F1375	IDT	U1	1
20	PCB	06	Printed Circuit Board	F13XX Rev 06			SBC		1
21	BOM	10	Bill Of Material						
22	DNP	0402						C18	
								Total	59

TOP MARKINGS

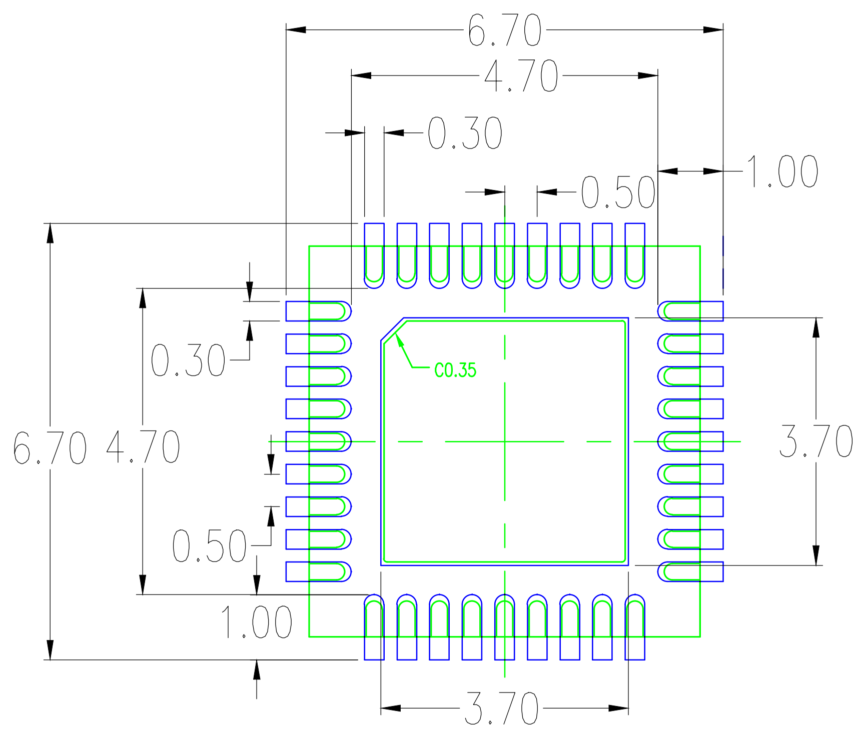


Revision Date	Description
February 7, 2022	Rebranded to Renesas.
January 16, 2014	Initial release.



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 8, 2021	01	Update IDT format to Renesas format
Apr 6, 2016	00	Initial Release