

# F1471

0.5W High Linearity RF Amplifier 400MHz to 4200MHz

The F1471 is a high linearity RF Driver Amplifier designed to operate within the 400MHz to 4200MHz frequency band. Using a single 5V power supply and only 130mA of  $I_{CQ}$ , the F1471 provides 15dB of gain and 3.8dB of noise figure, and 29dBm OP1dB at 3600MHz.

The F1471 is packaged in a 3 × 3 mm, 16-VFQFPN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

## Competitive Advantage

- Excellent linearity maintained over large bandwidths
- OIP3 linearity configurable with bias current adjustments
- Exceptional OP1dB performance maintained at low bias currents
- Robust ESD Performance
  - 1.5kV HBM ESD rating
  - 1kV CDM ESD rating
- Includes on-chip DC overvoltage and RF overdrive protection

## Features

- RF range: 400MHz to 4200MHz
- 15dB typical gain at 3600MHz
- 3.8dB NF at 3600MHz
- +29dBm output P1dB at 3600MHz
- 5V power supply
- Adjustable DC bias
- Bias control compatible for 3.3V and 5V VREF operation allowing power-down mode for power savings
- 50Ω single-ended input and output impedances
- Internal DC overvoltage protection
- Internal RF overdrive protection
- On-chip ESD protection
- Operating temperature ( $T_{EP}$ ) range: -40°C to +115°C
- 3 × 3 mm, 16-VFQFPN package

## Applications

- 4G/5G cellular base stations
- Multi-mode, multi-carrier transmitters
- Active antenna systems
- General purpose wireless

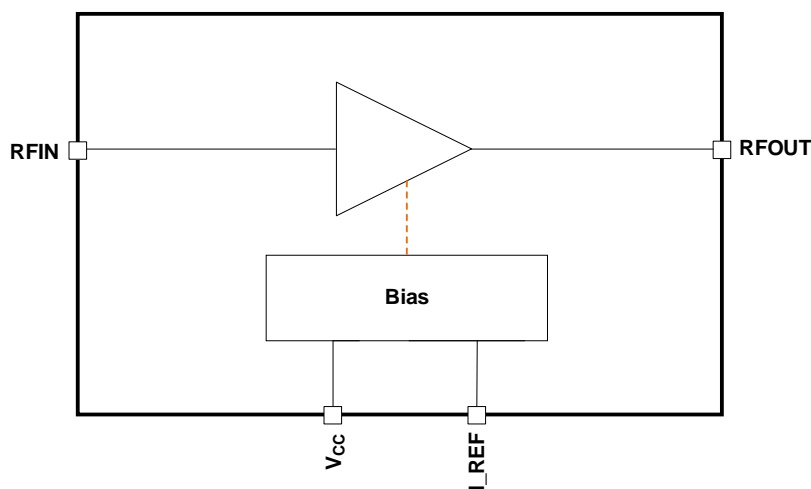


Figure 1. Block Diagram

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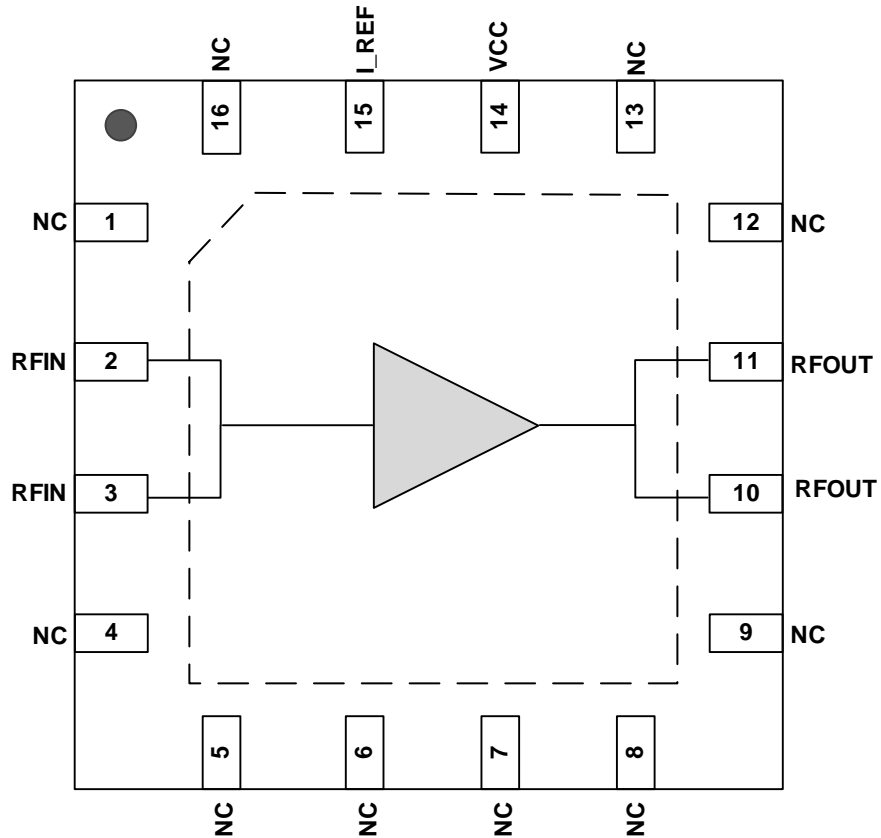
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# 1. Pin Information

## 1.1 Pin Configuration

16 Ld 3 x 3 mm VFQFPN Package  
Top View



## 1.2 Pin Descriptions

| Number                          | Name  | Description   |
|---------------------------------|-------|---|
| 1, 4, 5, 6, 7, 8, 9, 12, 13, 16 | NC    | No internal connection. Renesas highly recommends connecting these pins to a ground via, which is located as close to the pin as possible.  |
| 2, 3                            | RFIN  | RF input internally matched to 50Ω. Must use an external DC block.  |
| 10, 11                          | RFOUT | RF output. Pull up to V <sub>CC</sub> through inductor. Must use an external DC block.  |
| 14                              | VCC   | Connect pin directly to VCC. Renesas recommends placing a 1000pF decoupling capacitor as close to this pin as possible.   |
| 15                              | I_REF | Reference current and STBY pin. Connect an external resistor (reference BOM) to V <sub>REF</sub> to set the quiescent current of the device. Setting V <sub>REF</sub> < 2V disables the amplifier.  |
|                                 | EPAD  | Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

## 2. Specifications

### 2.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1471 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

| Parameter   | Symbol          | Minimum | Maximum | Units              |
|---|-----------------|---------|---------|--------------------|
| $V_{CC}$ to GND   | $V_{CC}$        | 0       | 8.0     | V                  |
| $V_{REF}$ to GND  | $V_{REF}^{[b]}$ | 0       | 5.5     | V                  |
| RFIN Externally Applied DC Voltage  | $V_{RFIN}$      |         | 8.0     | V                  |
| RFOUT Externally Applied DC Voltage   | $V_{RFOUT}$     |         | 8.0     | V                  |
| Maximum CW input power applied for 24 hours<br>$f = 2.6\text{GHz}$ , $T_{EP} = +115^{\circ}\text{C}$ , input/output VSWR < 2:1 based on 50 $\Omega$ system <sup>[a]</sup> | $P_{MAXIN}$     |         | 18      | dBm                |
| Junction Temperature  | $T_{JMAX}$      |         | +175    | $^{\circ}\text{C}$ |
| Storage Temperature Range   | $T_{STOR}$      | -65     | +150    | $^{\circ}\text{C}$ |
| Lead Temperature (soldering, 10s)   | $T_{LEAD}$      |         | +260    | $^{\circ}\text{C}$ |
| Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)  | $V_{ESDHBM}$    |         | 1500    | V                  |
| Electrostatic Discharge – CDM (JEDEC 22-C101F)  | $V_{ESDCDM}$    |         | 1000    | V                  |

[a] Exposure to these maximum RF levels can result in significantly higher  $I_{CC}$  current draw due to overdriving the amplifier stages.

[b]  $V_{REF}$  conditions apply when  $V_{CC}$  is applied

### 2.2 Recommended Operating Conditions

| Parameter                   | Symbol     | Condition      | Minimum | Typical                 | Maximum | Units              |
|-----------------------------|------------|----------------|---------|-------------------------|---------|--------------------|
| Power Supply Voltage        | $V_{CC}$   |                | 4.75    |                         | 5.25    | V                  |
| Reference Voltage           | $V_{REF}$  | Powered On     |         | 3.3 or 5 <sup>[a]</sup> |         | V                  |
|                             |            | Powered Off    | 0       | 1.8                     | 2       |                    |
| Operating Temperature Range | $T_{EPAD}$ | Exposed Paddle | -40     |                         | +115    | $^{\circ}\text{C}$ |
| RF Frequency Range          | $f_{RF}$   |                | 400     |                         | 4200    | MHz                |
| RFIN Port Impedance         | $Z_{RFI}$  | Single-ended   |         | 50                      |         | $\Omega$           |
| RFOUT Port Impedance        | $Z_{RFO}$  | Single-ended   |         | 50                      |         | $\Omega$           |

[a] Refer to R5 value in the BOM.

## 2.3 Electrical Characteristics

See the Electrical Schematic. Specifications apply when operated as a TX amplifier with tuning optimized for desired band of interest,  $V_{CC} = +5.0V$ ,  $V_{REF} = +3.3V$ ,  $T_{EPAD} = +25^{\circ}C$ ,  $R_{BSET} = 174\Omega$ , ( $R_5$  in the electrical schematic),  $Z_S = Z_L = 50\Omega$ , Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

### 2.3.1. General

| Parameter                             | Symbol          | Condition   | Minimum | Typical | Maximum                   | Units   |
|---------------------------------------|-----------------|---|---------|---------|---------------------------|---------|
| Quiescent Current <sup>[b]</sup>      | $I_{CQ}$        |   |         | 130     | <b>160</b> <sup>[a]</sup> | mA      |
| Reference Bias Current <sup>[b]</sup> | $I_{REF}$       |   |         | 2       |                           | mA      |
|                                       | $I_{REF\_STBY}$ | $V_{REF} < 2V$  |         | 500     |                           | $\mu A$ |
| Standby Switching Time                | $T_{ON}$        | 50% STBY control to within 0.5dB of the on-state final gain value |         | 200     |                           | ns      |
|                                       | $T_{OFF}$       | 50% STBY control to $I_{CC} < 10mA$                               |         | 200     |                           | ns      |

### 2.3.2. 2300MHz to 2900MHz

See the Electrical Schematic. Specifications apply when operated as a TX amplifier with tuning optimized for the 2300MHz to 2900MHz band,  $f_{RF} = 2600MHz$ ,  $V_{CC} = +5.0V$ ,  $V_{REF} = +3.3V$ ,  $T_{EPAD} = +25^{\circ}C$ ,  $R_{BSET} = 174\Omega$ , ( $R_5$  in the electrical schematic),  $Z_S = Z_L = 50\Omega$ , Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter                          | Symbol       | Condition   | Minimum | Typical | Maximum | Units |
|------------------------------------|--------------|---|---------|---------|---------|-------|
| Gain                               | G            |   |         | 16      |         | dB    |
| Gain Flatness                      | $G_{FLAT}$   | $f_{RF} = 2300MHz$ to 2900MHz   |         | 1       |         | dB    |
| Gain Variation Over Temp           | $G_{TEMP}$   | $T_{EPAD} = -40^{\circ}C$ to $+115^{\circ}C$ , referenced to $T_{EPAD} = 25^{\circ}C$ |         | +0.5/-1 |         | dB    |
| STBY Mode Gain                     | $G_{STBY}$   | $V_{REF} < 2V$  |         | -16     |         | dB    |
| RF Input Return Loss               | $RL_{RFIN}$  |   |         | 12      |         | dB    |
| RF Output Return Loss              | $RL_{RFOUT}$ |   |         | 12      |         | dB    |
| Reverse Isolation                  | $ISO_{REV}$  |   |         | 27      |         | dB    |
| Noise Figure                       | NF           |   |         | 4       |         | dB    |
| Output Third Order Intercept Point | OIP3         | $P_{OUT} = +18dBm/$ tone<br>1MHz tone separation                                      |         | 38      |         | dBm   |
| Output 1dB Compression Point       | OP1dB        |   |         | 28.5    |         | dBm   |
| ACLR                               | ACLR         | $P_{out} = +18dBm$ ,<br>LTE 20MHz, 9dB PAR  |         | -48     |         | dBc   |

| Parameter | Symbol | Condition   | Minimum | Typical | Maximum | Units |
|-----------|--------|---|---------|---------|---------|-------|
| Stability | K      | K-Factor <sup>[b]</sup><br>T <sub>EPAD</sub> = -40°C to +115°C<br>V <sub>CC</sub> = 4.75V to 5.25V<br>Up to 20GHz | 1       |         |         |       |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] K-Factor calculated taking the matching circuit into consideration, no de-embedding applied.

### 2.3.3. 3300MHz to 3900MHz

See the Electrical Schematic. Specifications apply when operated as a TX amplifier with tuning optimized for the 3300MHz to 3900MHz band, f<sub>RF</sub> = 3600MHz, V<sub>CC</sub> = +5.0V, V<sub>REF</sub> = +3.3V, T<sub>EPAD</sub> = +25°C, R<sub>BSET</sub> = 174Ω, (R5 in the electrical schematic), Z<sub>S</sub> = Z<sub>L</sub> = 50Ω, Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter                          | Symbol              | Condition   | Minimum                 | Typical | Maximum | Units |
|------------------------------------|---------------------|---|-------------------------|---------|---------|-------|
| Gain                               | G                   |   | <b>13<sup>[a]</sup></b> | 15      |         | dB    |
| Gain Flatness                      | G <sub>FLAT</sub>   | f <sub>RF</sub> = 3300MHz to 3900MHz  |                         | 1       |         | dB    |
| Gain Variation Over Temp           | G <sub>TEMP</sub>   | T <sub>EPAD</sub> = -40°C to +115°C,<br>referenced to T <sub>EPAD</sub> = 25°C  |                         | +0.5/-1 |         | dB    |
| STBY Mode Gain                     | G <sub>STBY</sub>   | V <sub>REF</sub> < 2V   |                         | -14     |         | dB    |
| RF Input Return Loss               | RL <sub>RFIN</sub>  |   |                         | 14      |         | dB    |
| RF Output Return Loss              | RL <sub>RFOUT</sub> |   |                         | 12      |         | dB    |
| Reverse Isolation                  | ISO <sub>REV</sub>  |   |                         | 25      |         | dB    |
| Noise Figure                       | NF                  |   |                         | 3.8     |         | dB    |
| Output Third Order Intercept Point | OIP3                | P <sub>OUT</sub> = +18dBm/tone<br>1MHz tone separation  |                         | 38      |         | dBm   |
|                                    |                     | P <sub>OUT</sub> = +18dBm/tone<br>1MHz tone separation<br>V <sub>CC</sub> = 4.75V to 5.25V<br>T <sub>EPAD</sub> = -40°C to +115°C | 32                      |         |         | dBm   |
| Output 1dB Compression Point       | OP1dB               |   |                         | 29      |         | dBm   |
|                                    |                     | V <sub>CC</sub> = 4.75V to 5.25V<br>T <sub>EPAD</sub> = -40°C to +115°C   | 26                      |         |         | dBm   |
| ACLR                               | ACLR                | P <sub>out</sub> = +18dBm,<br>LTE 20MHz, 9dB PAR  |                         | -47     |         | dBc   |
| Stability                          | K                   | K-Factor <sup>[b]</sup><br>T <sub>EPAD</sub> = -40°C to +115°C<br>V <sub>CC</sub> = 4.75V to 5.25V<br>Up to 20GHz                 | 1                       |         |         |       |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] K-Factor calculated taking the matching circuit into consideration, no de-embedding applied.

**2.3.4. 3800MHz to 4200MHz**

See the Electrical Schematic. Specifications apply when operated as a TX amplifier with tuning optimized for the 3800MHz to 4200MHz band,  $f_{RF} = 4000\text{MHz}$ ,  $V_{CC} = +5.0\text{V}$ ,  $V_{REF} = +3.3\text{V}$ ,  $T_{EPAD} = +25^{\circ}\text{C}$ ,  $R_{BSET} = 174\Omega$ , (R5 in the electrical schematic),  $Z_S = Z_L = 50\Omega$ , Evaluation Board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

| Parameter                          | Symbol       | Condition   | Minimum | Typical | Maximum | Units |
|------------------------------------|--------------|---|---------|---------|---------|-------|
| Gain                               | G            |   |         | 14      |         | dB    |
| Gain Flatness                      | $G_{FLAT}$   | $f_{RF} = 3800\text{MHz to } 4200\text{MHz}$  |         | 1.2     |         | dB    |
| Gain Variation Over Temp           | $G_{TEMP}$   | $T_{EPAD} = -40^{\circ}\text{C to } +115^{\circ}\text{C}$ ,<br>referenced to $T_{EPAD} = 25^{\circ}\text{C}$                                    |         | +0.5/-1 |         | dB    |
| STBY Mode Gain                     | $G_{STBY}$   | $V_{REF} < 2\text{V}$   |         | -13     |         | dB    |
| RF Input Return Loss               | $RL_{RFIN}$  |   |         | 15      |         | dB    |
| RF Output Return Loss              | $RL_{RFOUT}$ |   |         | 9       |         | dB    |
| Reverse Isolation                  | $ISO_{REV}$  |   |         | 25      |         | dB    |
| Noise Figure                       | NF           |   |         | 3.8     |         | dB    |
| Output Third Order Intercept Point | OIP3         | $P_{OUT} = +18\text{dBm/tone}$<br>1MHz tone separation  |         | 37      |         | dBm   |
| Output 1dB Compression Point       | OP1dB        |   |         | 28.5    |         | dBm   |
| ACLR                               | ACLR         | $P_{out} = +18\text{dBm}$ ,<br>LTE 20MHz, 9dB PAR   |         | -44     |         | dBc   |
| Stability                          | K            | K-Factor <sup>[b]</sup><br>$T_{EPAD} = -40^{\circ}\text{C to } +115^{\circ}\text{C}$<br>$V_{CC} = 4.75\text{V to } 5.25\text{V}$<br>Up to 20GHz | 1       |         |         |       |

- [a] Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
- [b] K-Factor calculated taking the matching circuit into consideration, no de-embedding applied.

**2.4 Thermal Characteristics**

| Parameter  | Symbol            | Value | Units                |
|--|-------------------|-------|----------------------|
| Junction to Ambient Thermal Resistance.                                      | $\theta_{JA}$     | 48.6  | $^{\circ}\text{C/W}$ |
| Junction to Case Thermal Resistance. (Case is defined as the exposed paddle) | $\theta_{JC-BOT}$ | 4.3   | $^{\circ}\text{C/W}$ |
| Moisture Sensitivity Rating (Per J-STD-020)                                  |                   | MSL 1 |                      |



### 3. Typical Operating Conditions (TOC)

Unless otherwise noted, the following conditions apply for the TOC graphs on the following pages:

- $V_{CC} = 5.0V$
- $Z_L = Z_S = 50\Omega$  Single-ended
- $f_{RF} = 2600MHz$  (set 1)
- $f_{RF} = 3600MHz$  (set 2)
- $f_{RF} = 4000MHz$  (set 3)
- $T_{EP} = +25^{\circ}C$
- $V_{REF} = 3.3V$
- 1MHz Tone Spacing
- All temperatures are referenced to the exposed paddle.
- ACLR measurements used with LTE signal, 20MHz, PAR = 9dB at 0.01% probability.
- Evaluation Kit traces and connector losses are de-embedded

## 4. Typical Performance Characteristics

### 4.1 2300MHz to 2900MHz

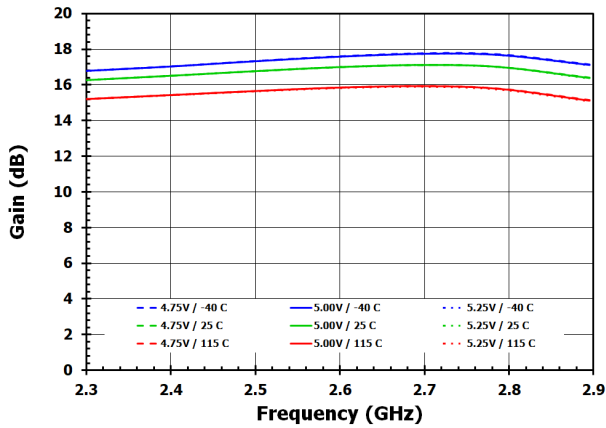


Figure 2. Gain

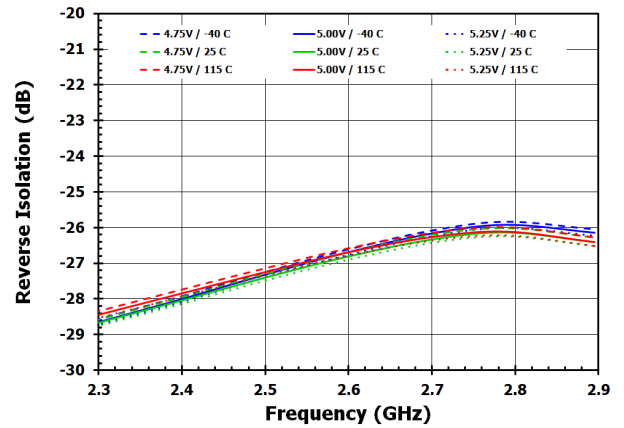


Figure 3. Reverse Isolation

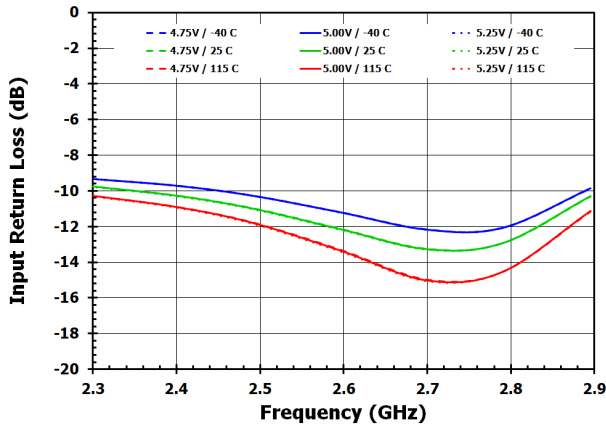


Figure 4. Input Return Loss

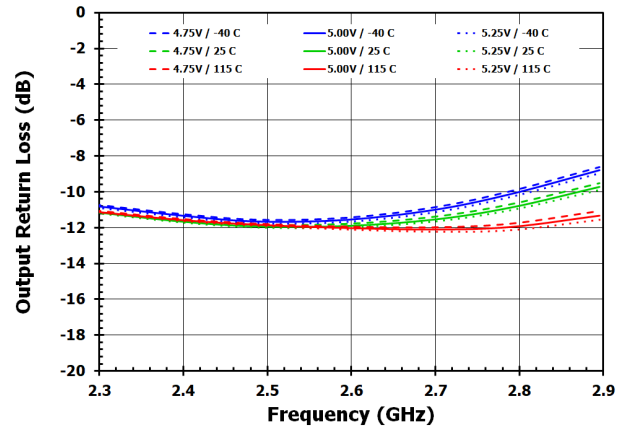


Figure 5. Output Return Loss

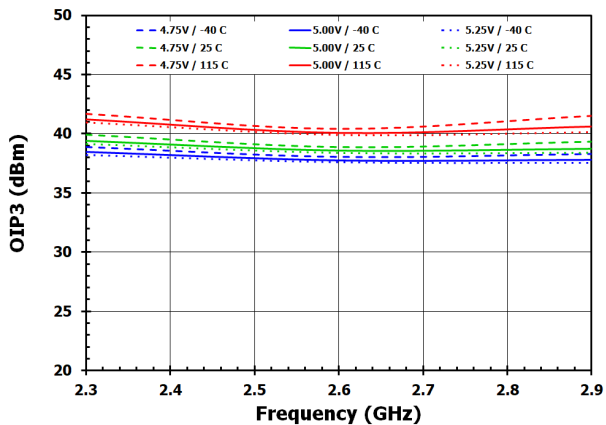


Figure 6. OIP3

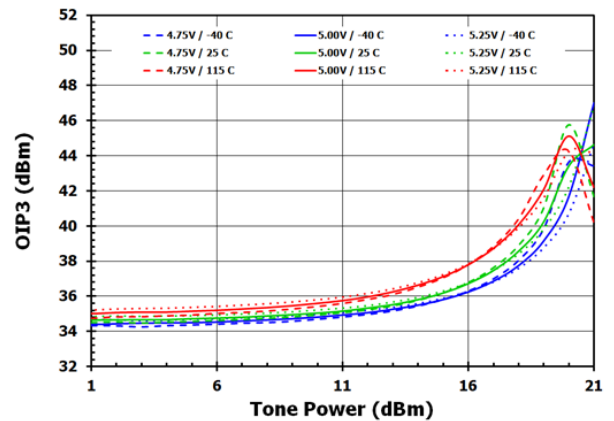


Figure 7. OIP3 vs Tone Power (2.6GHz)

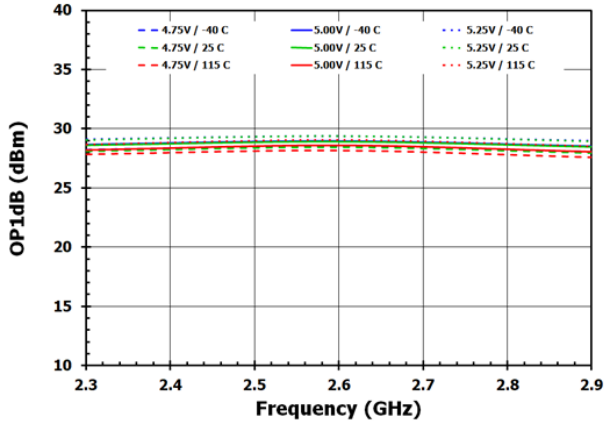


Figure 8. OP1dB (2.6GHz)

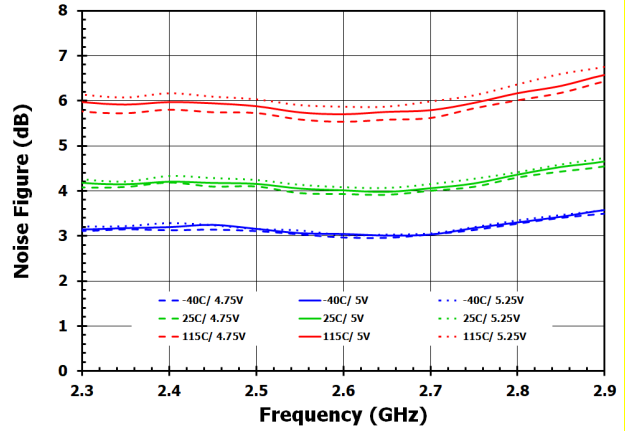


Figure 9. Noise Figure

### 4.2 3300MHz to 3900MHz

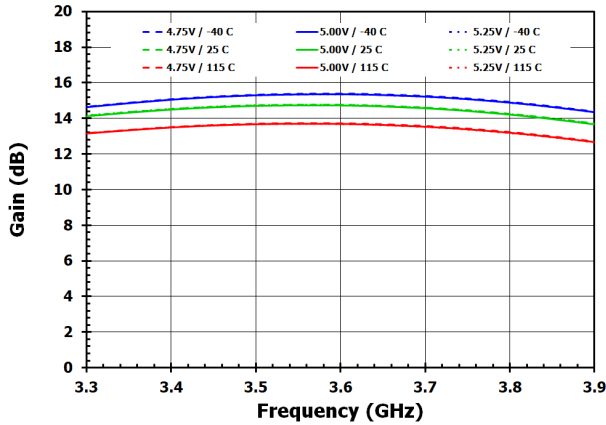


Figure 10. Gain

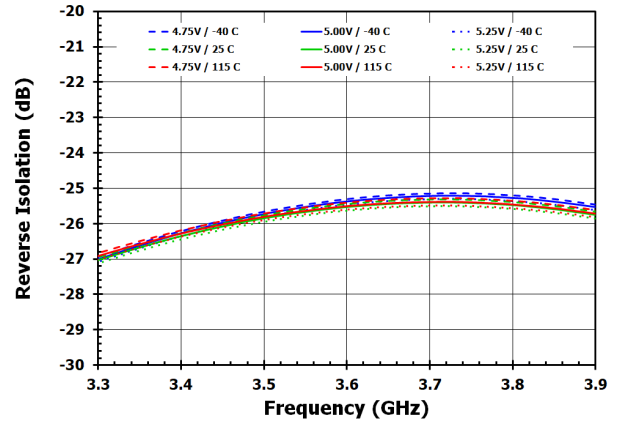


Figure 11. Reverse Isolation

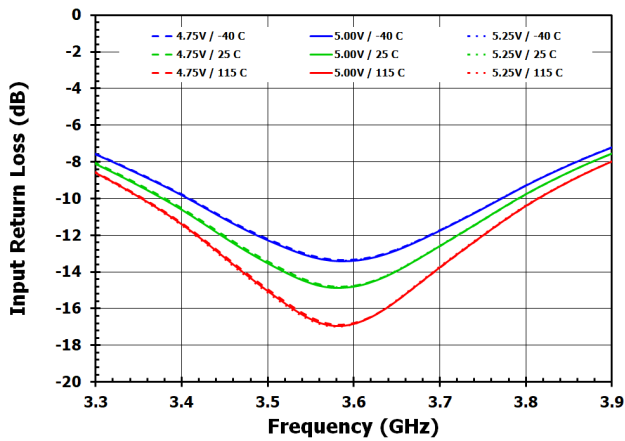


Figure 12. Input Return Loss

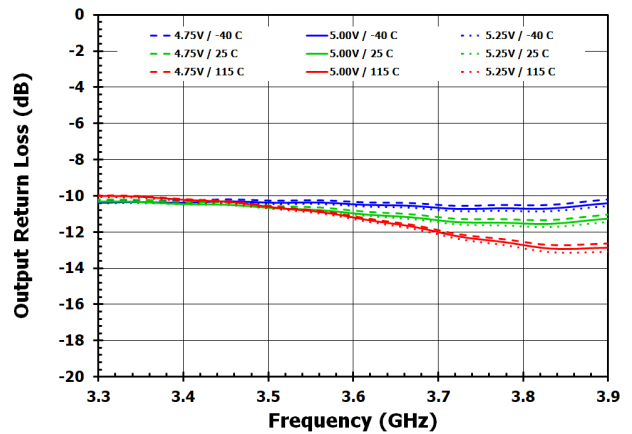


Figure 13. Output Return Loss

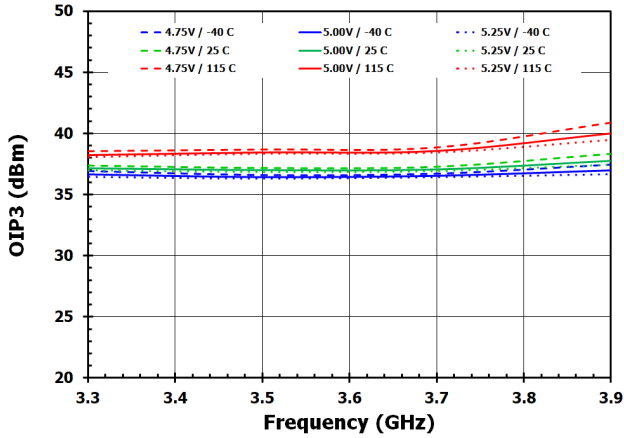


Figure 14. OIP3

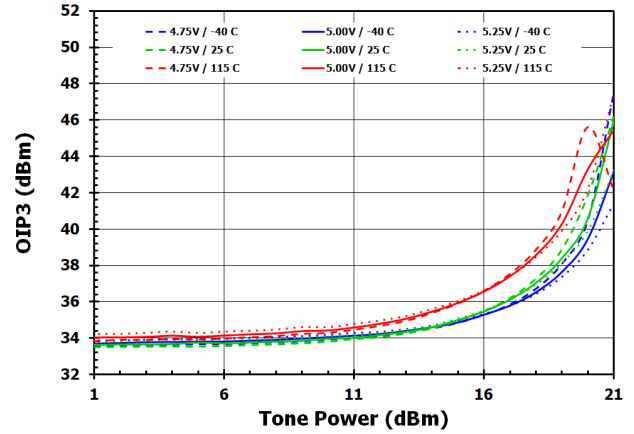


Figure 15. OIP3 vs Tone Power (3.6GHz)

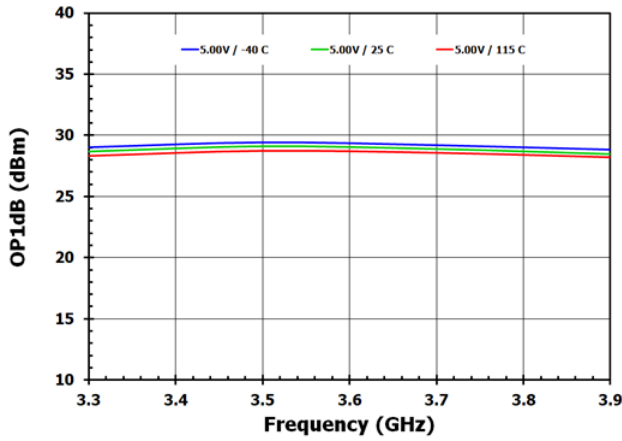


Figure 16. OP1dB (3.6GHz)

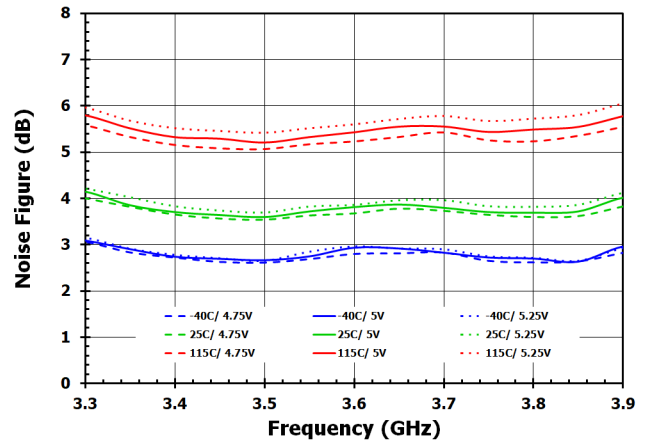


Figure 17. Noise Figure

### 4.3 3800MHz to 4200MHz

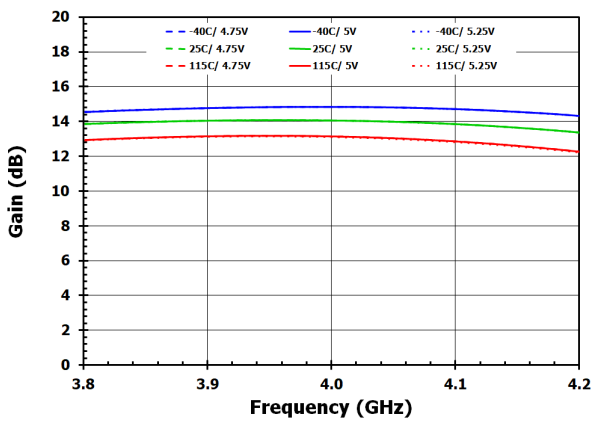


Figure 18. Gain

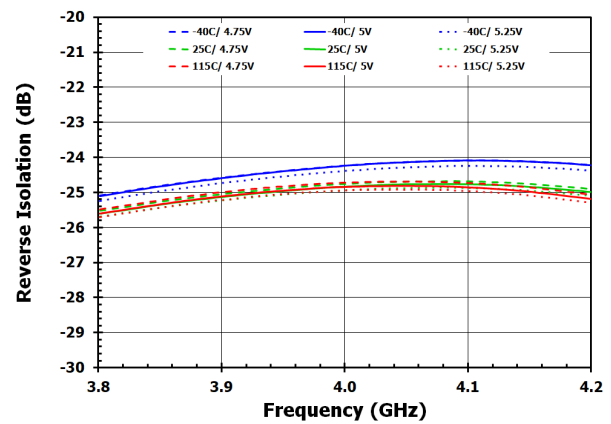


Figure 19. Reverse Isolation

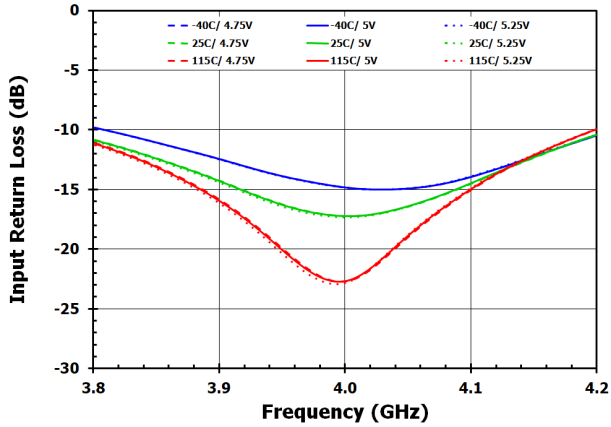


Figure 20. Input Return Loss

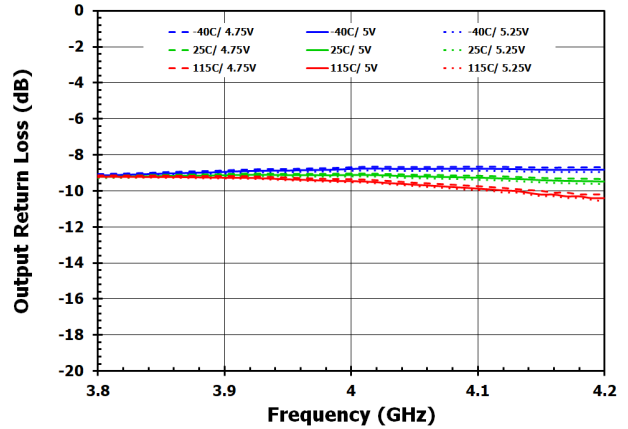


Figure 21. Output Return Loss

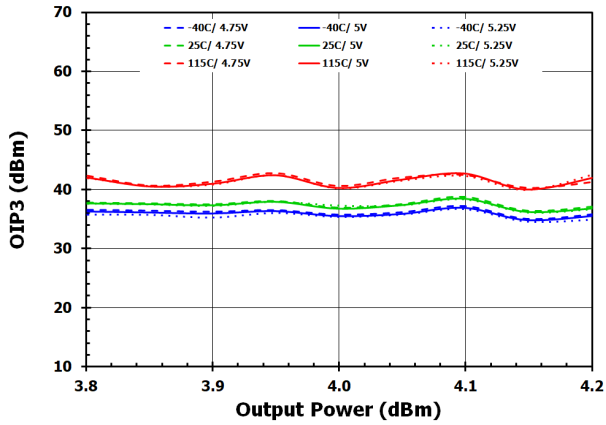


Figure 22. OIP3

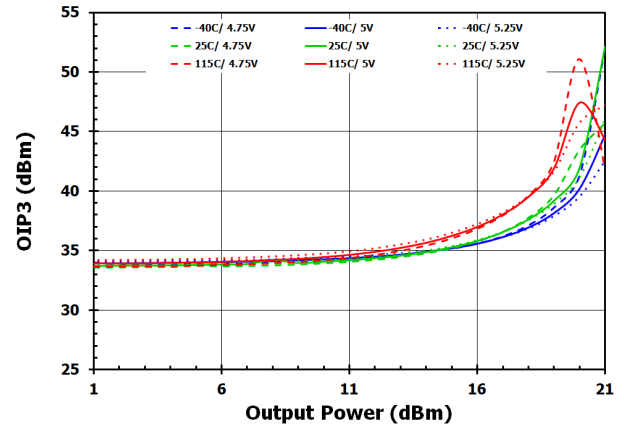


Figure 23. OIP3 vs Tone Power (4GHz)

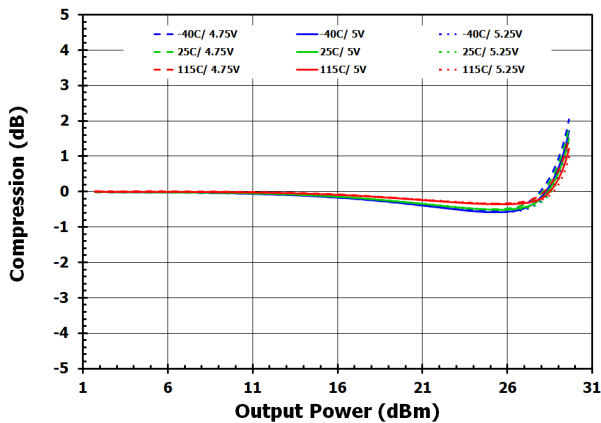


Figure 24. OP1dB (4GHz)

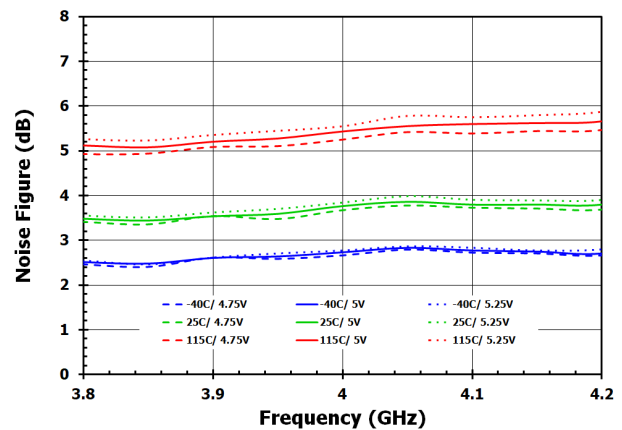


Figure 25. Noise Figure

## 5. Programming

The F1471 includes a STBY feature as defined in the following table.

**Table 1. STBY Truth Table**

| $V_{REF}$ Voltage | State          | Condition                                |
|-------------------|----------------|--|
| $V_{REF} = 5V$    | Full operation | $R_{BSET} =$ See R5 in band specific BOM |
| $V_{REF} = 3.3V$  | Full operation | $R_{BSET} =$ See R5 in band specific BOM |
| $V_{REF} < 2V$    | Amplifier OFF  | $R_{BSET} =$ See R5 in band specific BOM |

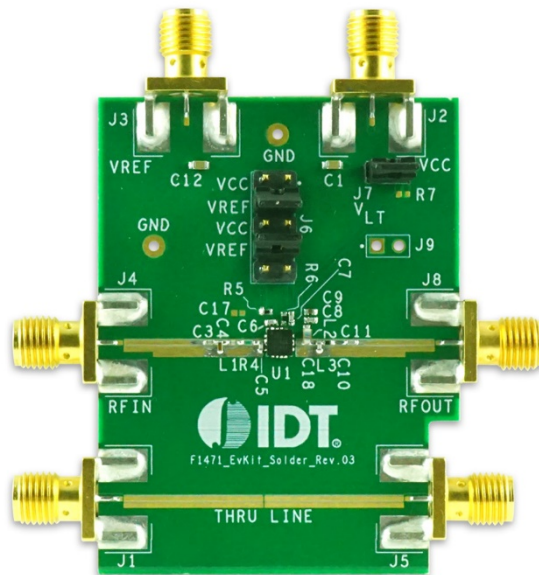
## 6. Applications Information

The F1471 has been optimized for use in high performance RF applications from 400MHz to 4200MHz.

### 6.1 Power Supplies

Use a common  $V_{CC}$  power supply for all power supply pins. To minimize noise and fast transients, de-coupling capacitors to all supply pins. Supply noise can degrade noise figure and fast transients can trigger ESD clamps causing them to fail. Supply voltage changes or transients should have a slew rate smaller than  $1V/20\mu s$ . In addition, keep all control pins at  $0V (\pm 0.3V)$  while the supply voltage ramps or while it returns to zero.

## 7. Evaluation Kit Information



**Figure 26. Evaluation Kit Photo**

**Note:** See the Evaluation Kit Operation section for proper setup and configuration

### 7.1 Evaluation Kit Circuit

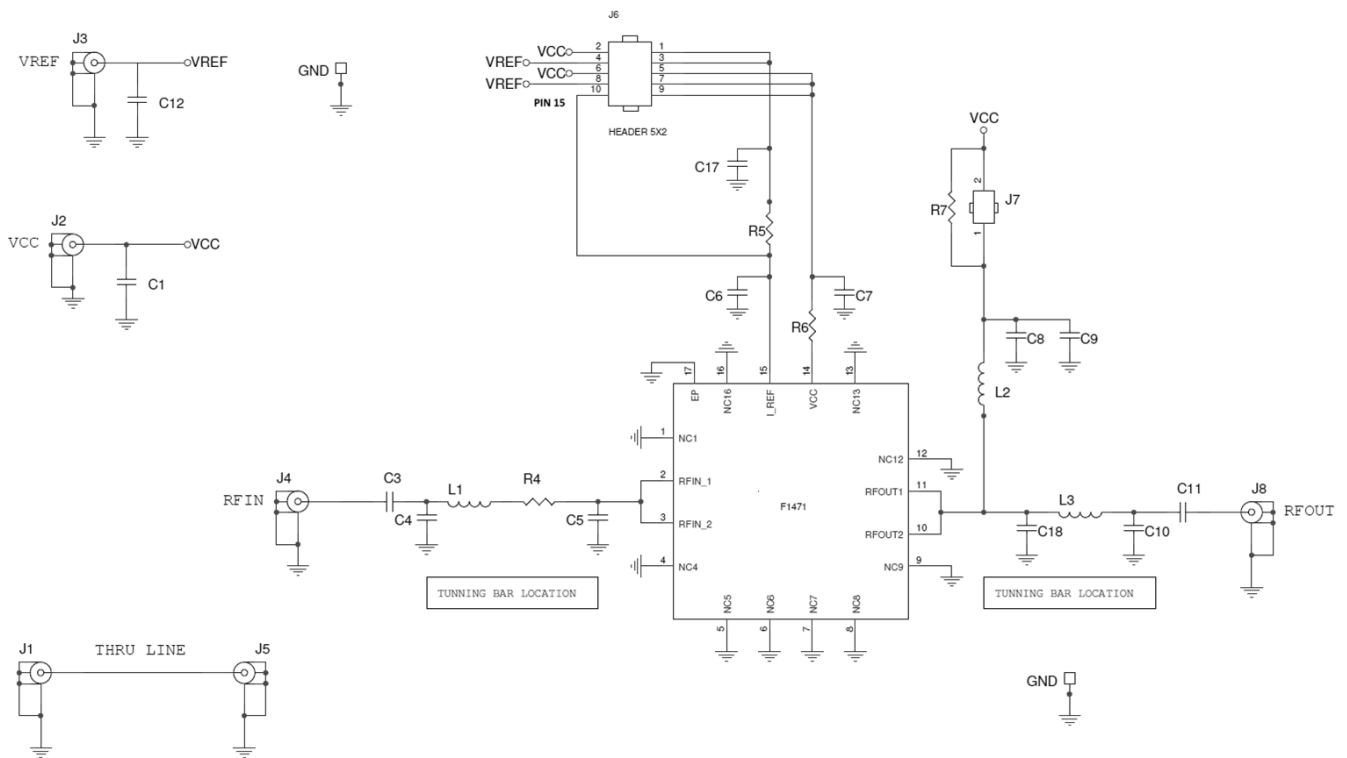


Figure 27. Electrical Schematic for the Evaluation Kit

## 7.2 Bill of Materials

Table 2. Evaluation Kit Bill of Material (BOM) – 2300MHz to 2900MHz Tune

| Part Reference      | Qty | Description   | Manufacturer Part # | Manufacturer    |
|---------------------|-----|---|---------------------|-----------------|
| C4                  | 1   | 4.7nH $\pm$ 0.1nH, 160mA, film Inductor (0402)                              | LQP15MN4N7B02       | Murata          |
| C5                  | 1   | 3.1pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H3R1WB01   | Murata          |
| C3, C6, C7, C8, C11 | 5   | 1000pF $\pm$ 5%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C1H102JA01   | Murata          |
| C1, C12             | 2   | 47uF $\pm$ 20%, 10V, C0G Ceramic Capacitor (0805)                           | GRM21BR61A476ME15   | Murata          |
| C9                  | 1   | 100nF $\pm$ 10%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C81H104KE14  | Murata          |
| C10                 | 1   | 0.9pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GRM1555C1HR90W      | Murata          |
| C18                 | 1   | 1.3pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H1R3WB01   | Murata          |
| L1                  | 1   | 1.2pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GRM1555C1H1R20WA01  | Murata          |
| L2                  | 1   | 3.9nH $\pm$ 2%, 250MHz, Ceramic Chip Inductor (0603)                        | 0603CS-3N9XGE       | Coilcraft       |
| L3                  | 1   | 1.2nH $\pm$ 0.05nH, Inductor (0402)   | LQP15MN1N2W         | Murata          |
| R4                  | 1   | 5.1 $\Omega$ $\pm$ 1% 0.063W, 1/16W Resistor (0402)                         | CRCW04025R10FKED    | Vishay Dale     |
| R5                  | 1   | <b>Vref at 3.3V:</b> 174 $\Omega$ $\pm$ 0.5%, 0.063W, 1/16W Resistor (0402) | TNPW0402174RDEED    | Vishay Dale     |
|                     |     | <b>Vref at 5V:</b> 2.5k $\Omega$ $\pm$ 0.1%, 0.063W, 1/16W Resistor (0402)  | TNPW04022K52BEED    | Vishay Dale     |
| R6                  | 1   | 0 $\Omega$ Jumper 0.063W, 1/16W Chip Resistor (0402)                        | CRCW04020000Z0ED    | Vishay Dale     |
| R7                  |     | DNP   |                     |                 |
| J2, J3, J4, J8      | 4   | Edge Launch SMA (0.375-inch pitch ground, tab, 50 $\Omega$ )                | 142-0701-851        | Emerson Johnson |
| J6                  | 1   | CONN HEADER VERT DBL 5x2 POS GOLD   | 961210-6404-AR      | 3M              |
| J7                  | 1   | CONN HEADER VERT SGL 2x1 POS GOLD   | 961102-6404-AR      | 3M              |
| EVB                 | 1   | F1471_Evkit_Solder_Rev.03   |                     | Renesas         |
| Module              | 1   | F1471YAA  |                     | Renesas         |



Table 3. Evaluation Kit Bill of Material (BOM) – 3300MHz to 3900MHz Tune

| Part Reference      | Qty | Description   | Manufacturer Part # | Manufacturer    |
|---------------------|-----|---|---------------------|-----------------|
| C4                  | 1   | 5.6nH $\pm$ 0.1nH, 160mA, film Inductor (0402)                              | LQP15MN5N6B02       | Murata          |
| C5                  | 1   | 1.3pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H1R3WB01   | Murata          |
| C3, C6, C7, C8, C11 | 5   | 1000pF $\pm$ 5%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C1H102JA01   | Murata          |
| C1, C12             | 2   | 47 $\mu$ F $\pm$ 20%, 10V, C0G Ceramic Capacitor (0805)                     | GRM21BR61A476ME15   | Murata          |
| C9                  | 1   | 100nF $\pm$ 10%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C81H104KE14  | Murata          |
| C10                 | 1   | DNI   |                     |                 |
| C18                 | 1   | 1.2pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H1R2WB01   | Murata          |
| L1                  | 1   | 0.5pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GRM1555C1HR50WA01   | Murata          |
| L2                  | 1   | 3.3nH $\pm$ 2%, 250 MHz, Ceramic Chip Inductor (0603)                       | 0603CS-3N3XGE       | Coilcraft       |
| L3, R6              | 2   | 0 $\Omega$ Jumper 0.063W, 1/16W Chip Resistor (0402)                        | CRCW04020000Z0ED    | Vishay Dale     |
| R4                  | 1   | 1 $\Omega$ $\pm$ 1% 0.063W, 1/16W Resistor (0402)                           | CRCW04021R00FKED    | Vishay Dale     |
| R5                  | 1   | <b>Vref at 3.3V:</b> 174 $\Omega$ $\pm$ 0.5%, 0.063W, 1/16W Resistor (0402) | TNPW0402174RDEED    | Vishay Dale     |
|                     |     | <b>Vref at 5V:</b> 2.5k $\Omega$ $\pm$ 0.1%, 0.063W, 1/16W Resistor (0402)  | TNPW04022K52BEED    | Vishay Dale     |
| R7                  |     | DNP   |                     |                 |
| J2, J3, J4, J8      | 4   | Edge Launch SMA (0.375 inch pitch ground, tab, 50 $\Omega$ )                | 142-0701-851        | Emerson Johnson |
| J6                  | 1   | CONN HEADER VERT DBL 5x2 POS GOLD   | 961210-6404-AR      | 3M              |
| J7                  | 1   | CONN HEADER VERT SGL 2x1 POS GOLD   | 961102-6404-AR      | 3M              |
| EVB                 | 1   | F1471_Evkit_Solder_Rev.03   |                     | Renesas         |
| Module              | 1   | F1471YAA  |                     | Renesas         |

Table 4. Evaluation Kit Bill of Material (BOM) – 3800MHz to 4200MHz Tune

| Part Reference      | Qty | Description   | Manufacturer Part # | Manufacturer    |
|---------------------|-----|---|---------------------|-----------------|
| C4                  | 1   | 5.1nH $\pm$ 0.1nH, 160mA, film Inductor (0402)                              | LQP15MN5N1B02       | Murata          |
| C5                  | 1   | 1.2pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H1R2WB01   | Murata          |
| C3, C6, C7, C8, C11 | 5   | 1000pF $\pm$ 5%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C1H102JA01   | Murata          |
| C1, C12             | 2   | 47uF $\pm$ 20%, 10V, C0G Ceramic Capacitor (0805)                           | GRM21BR61A476ME15   | Murata          |
| C9                  | 1   | 100nF $\pm$ 10%, 50V, C0G Ceramic Capacitor (0402)                          | GRM1555C81H104KE14  | Murata          |
| C10                 | 1   | DNI   |                     |                 |
| C18                 | 1   | 1.0pF $\pm$ 0.05pF, 50V, C0G Ceramic Capacitor (0402)                       | GJM1555C1H1R0WB01   | Murata          |
| L1, L3, R6          | 3   | 0 $\Omega$ Jumper 0.063W, 1/16W Chip Resistor (0402)                        | CRCW04020000Z0ED    | Vishay Dale     |
| L2                  | 1   | 3.3nH $\pm$ 2%, 250MHz, Ceramic Chip Inductor (0603)                        | 0603CS-3N3XGE       | Coilcraft       |
| R4                  | 1   | 0.5pF $\pm$ 0.05, 50V, COG Ceramic Capacitor (0402)                         | GRMC1HR50WA01       | Murata          |
| R5                  | 1   | <b>Vref at 3.3V:</b> 174 $\Omega$ $\pm$ 0.5%, 0.063W, 1/16W Resistor (0402) | TNPW0402174RDEED    | Vishay Dale     |
|                     |     | <b>Vref at 5V:</b> 2.5k $\Omega$ $\pm$ 0.1%, 0.063W, 1/16W Resistor (0402)  | TNPW04022K52BEED    | Vishay Dale     |
| R7                  |     | DNP   |                     |                 |
| J2, J3, J4, J8      | 4   | Edge Launch SMA (0.375-inch pitch ground, tab, 50 $\Omega$ )                | 142-0701-851        | Emerson Johnson |
| J6                  | 1   | CONN HEADER VERT DBL 5x2 POS GOLD   | 961210-6404-AR      | 3M              |
| J7                  | 1   | CONN HEADER VERT SGL 2x1 POS GOLD   | 961102-6404-AR      | 3M              |
| EVB                 | 1   | F1471_Evkit_Solder_Rev.03   |                     | Renesas         |
| Module              | 1   | F1471YAA  |                     | Renesas         |

## 7.3 Evaluation Kit Operation

### 7.3.1. Power Supply Setup

Set up a power supply in the voltage range of 4.75V to 5.25V with the power supply output disabled. The voltage is applied using the following connection (see Figure 26):

- Directly to the J2 SMA connector

Set up a control supply of either 3.3V or 5V (Use the correct value of resistance (R5) based on the applied control voltage as indicated per the BOM). The voltage is applied using the following connection (see Figure 26):

- Directly to the J3 SMA connector

### 7.3.2. Shunt Jumper Setup

- J7 Header Pins
  - Always place the Shunt Jumper to bias the amplifier output (see Evaluation Schematic in Figure 27).
- J6 Header Pins
  - J6 Header pins provide the  $V_{CC}$  and  $V_{REF}$  voltages to the DUT.
  - Always place a shunt jumper on pins 5 and 6 to provide the supplied  $V_{CC}$  to the DUT.
  - Place a shunt jumper on pins 3 and 4. In this configuration,  $V_{REF}$  is set independent to the supply voltage,  $V_{CC}$ .
  - Place a shunt jumper on pins 1 and 2. In this configuration,  $V_{REF}$  is set to the same level as the supply voltage,  $V_{CC}$ .
- Only place jumpers on Pins 3 and 4 or Pins 1 and 2 at any given time.  
**Important:** Do not place jumpers on all four pins (1, 2, 3, and 4) simultaneously.

### 7.3.3. Power-On Procedure

1. Set up the voltage supplies, and Evaluation Board as described in the Power Supply Setup section.
2. Enable the  $V_{CC}$  supply.
3. Enable the  $V_{REF}$  supply.

### 7.3.4. Power-Off Procedure

Disable the  $V_{REF}$  supply and then disable the  $V_{CC}$  power supply.

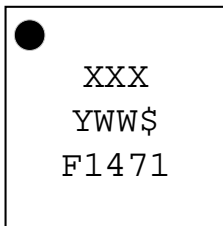
## 8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

## 9. Ordering Information

| Part Number  | Package                                   | MSL Rating | Carrier Type | Temperature Range |
|--------------|---|------------|--------------|-------------------|
| F1471NTGI    | 3 × 3 × 0.75 mm <a href="#">16-VFQFPN</a> | 1          | Tray         | -40° to +115°C    |
| F1471NTGI8   | 3 × 3 × 0.75 mm <a href="#">16-VFQFPN</a> | 1          | Reel         | -40° to +115°C    |
| F1471EVB-0P9 | Evaluation Board 700MHz – 1100MHz Tune    |            |              |                   |
| F1471EVB-2P1 | Evaluation Board 1700MHz – 2300MHz Tune   |            |              |                   |
| F1471EVB-2P6 | Evaluation Board 2300MHz – 2900MHz Tune   |            |              |                   |
| F1471EVB-3P6 | Evaluation Board 3300MHz – 3900MHz Tune   |            |              |                   |
| F1471EVB-4P0 | Evaluation Board 3800MHz – 4200MHz Tune   |            |              |                   |

## 10. Marking Diagram

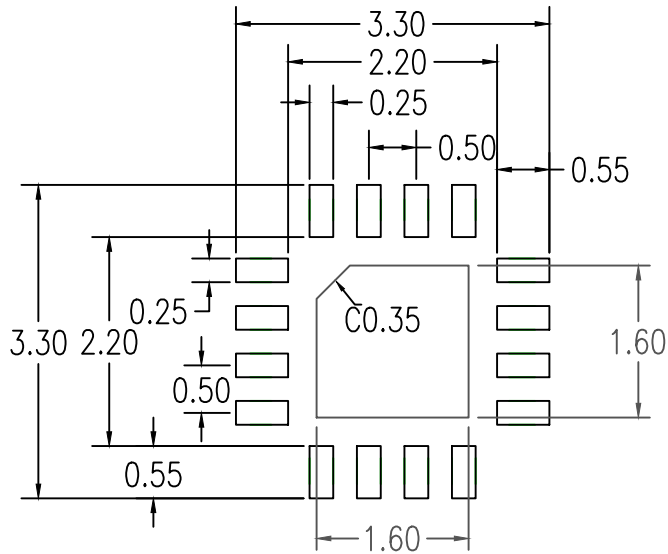


- “XXX” denotes the last 3 digits of the assembly lot number
- “Y” denotes the last digit of the year
- “WW” denotes the work week
- “\$” denotes the mark location code
- F1471 is the product name

## 11. Revision History

| Revision | Revision Date | Description of Change  |
|----------|---------------|--|
| 1.1      | Jun.24.21     | <ul style="list-style-type: none"> <li>• Added Ordering Information for 0.9GHz and 2.1GHz Tune evaluation boards</li> <li>• Completed other minor changes</li> </ul> |
| 1.0      | Oct.16.20     | Initial release.   |





RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History |         |                            |
|--------------------------|---------|----------------------------|
| Date Created             | Rev No. | Description                |
| July 8, 2019             | Rev 03  | Correct Typo Error Minimum |
| Sept 5, 2018             | Rev 02  | Add "K" Value 0.20 Minimum |