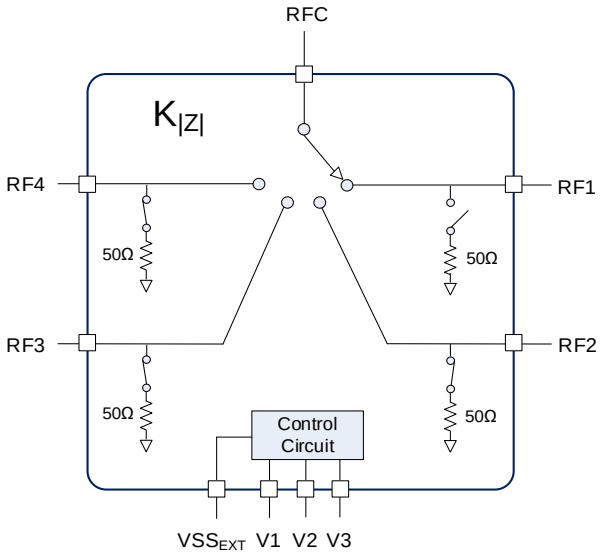
F2914

High Reliability SP4T RF Switch, 50MHz to 8000MHz

The F2914 is a high reliability, low insertion loss, 50Ω SP4T absorptive RF switch designed for a multitude of RF applications including wireless communications. This device covers a broad frequency range from 50MHz to 8000MHz. In addition to providing low insertion loss, the F2914 also delivers excellent linearity and isolation performance while providing a 50Ω termination to the unused RF input ports. The F2914 also includes a patent pending constant impedance (K_Z) feature. K_Z improves system hot switching ruggedness, minimizes LO pulling in VCOs, and reduces phase and amplitude variations in distribution networks. It is also ideal for dynamic switching / selection between two or more amplifiers while avoiding damage to upstream /downstream sensitive devices such as PAs and ADCs.

The F2914 uses a single positive supply voltage supporting three logic control pins using either 3.3V or 1.8V control logic. Connecting a negative voltage to pin 20 disables the internal negative voltage generator and becomes the negative supply.

Functional Block Diagram



Features

- Four symmetric, absorptive RF ports
- High Isolation: 50dB at 4000MHz
- Low Insertion Loss: 1.1 dB at 4000MHz
- High Linearity:
  - IIP2 of 114 dBm at 2000MHz
  - IIP3 of 60 dBm at 4000MHz
- High Operating Power Handling:
  - 33 dBm CW on selected RF port
  - 27 dBm on terminated ports
- Single 2.7V to 5.5V supply voltage
- External Negative Supply Option
- 3.3V and 1.8V compatible control logic
- Operating temperature -40°C to +105°C
- 4 × 4 mm 24-pin QFN package
- Pin compatible with competitors

Competitive Advantage

The F2914 provides constant impedance in all RF ports during transitions improving a system's hot-switching ruggedness. The device also supports high power handling, and high isolation; particularly important for DPD receiver use.

- Constant impedance K|Z| during switching transition
- RFX to RFC Isolation = 50dB at 4GHz
- Insertion Loss = 1.1 dB at 4GHz
- IIP3: +60 dBm at 4GHz
- Extended temperature: -40°C to +105°C

Applications

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- Military Systems, JTRS radios
- Cable Infrastructure
- Test / ATE Equipment

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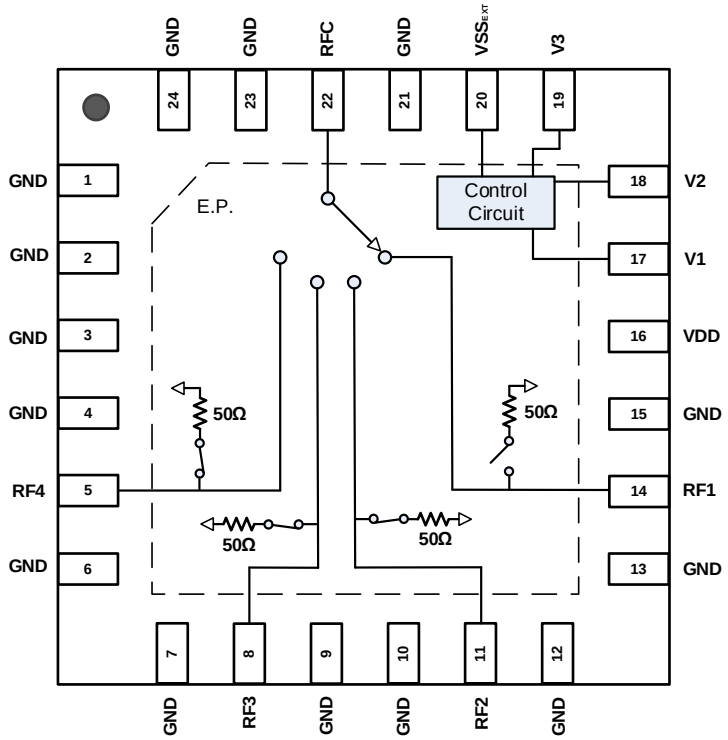
1. Pin Information

1.1 Pin Assignments



1.2 Pin Descriptions

Pin	Name	Function
1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	Ground these pins as close to the device as possible.
2	GND	This pin is internally connected to the exposed paddle. This pin can be left open or grounded. Note: The EVKIT layout has a floating RF trace connected to this pin to make the board compatible with the F2915.
5	RF4	RF4 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
8	RF3	RF3 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
11	RF2	RF2 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
14	RF1	RF1 Port. Matched to 50 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	VDD	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
17	V1	Control pin to set switch state. See Table 6 or Table 7.
18	V2	Control pin to set switch state. See Table 6 or Table 7.
19	V3	Control pin to set switch state. See Table 6 or Table 7.
20	VSS_{EXT}	External VSS negative voltage control. Connect to ground to enable on chip negative voltage generator. To bypass and disable on chip generator connect this pin to an external VSS.
22	RFC	RF Common Port. Matched to 50 ohms when one of the 4 RF ports is selected. If this pin is not 0V DC, then an external coupling capacitor must be used.
25	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
V_{DD} to GND	V_{DD}	-0.3	+6.0	V
V1, V2, V3 to GND	V_{CNTL}	-0.3	Minimum (3.6, V_{DD} + 0.3)	V
RF1, RF2, RF3, RF4, RFC to GND	V_{RF}	-0.3	+0.3	V
VSS_{EXT} to GND	V_{EXT}	-4.0	+0.3	V
Input Power for any one selected RF through port. (V_{DD} applied at 2GHz and T_C = +85°C)	$P_{MAXTHRU}$		37	dBm
Input Power for any one selected RF terminated port .(V_{DD} applied at 2GHz and T_C = +85°C)	$P_{MAXTERM}$		30	dBm
Input Power for RFC when in the all off state. (V_{DD} applied at 2GHz and T_C = +85°C)	P_{MAXCOM}		33	dBm
Continuous Power Dissipation (T_C = 95 °C Max)			3	W
Maximum Junction Temperature	T_{Jmax}		+140	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
ESD Voltage– HBM (Per JESD22-A114)	V_{ESDHBM}		Class 1C (1000 V)	
ESD Voltage – CDM (Per JESD22-C101)	V_{ESDCDM}		Class III (1000 V)	

T_C = Temperature of the exposed paddle

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Package Thermal and Moisture Characteristics

Table 2. Package Thermal and Moisture Characteristics

Characteristic	Value
θ_{JA} (Junction – Ambient)	41 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	6.4 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

2.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Voltage (s)	V_{DD}	Pin 20 grounded		2.7		5.5	V
		Pin 20 Driven with VSS_{EXT}		2.7		5.5	
	VSS_{EXT}	Negative Supply[1]		-3.6	-3.4	-3.2	
Operating Temp Range	T_{CASE}	Exposed Paddle Temperature		-40		+105	°C
RF Frequency Range	F_{RF}			50		8000	MHz
RF Continuous Input CW Power [2]	P_{RF}	Selected Port				33	dBm
		Terminated Ports[3]				27	
RF Continuous Input CW Power for Hot RF Switching[2]	P_{RFSW}	RFC as the input	Switch to RF1 thru RF4.			27	dBm
			Switched into or out of all off state.			24	
		RF1 thru RF5 as the inputs	Switched to RFC or into Term[3].			27	
			Switch into or out of all off condition.			27	
RF1 - 4 Port Impedance	Z_{RFx}				50		Ω
RFC Port Impedance	Z_{RFC}				50		

1. For normal operation, connect VSS_{EXT} = 0 V (pin 20) to GND to enable the internal negative voltage generator. By applying VSS_{EXT} to pin 20, the negative voltage generator is disabled thereby completely eliminating any generator spurious responses.
2. Levels based on $T_C \leq 85$ °C. See Figure 1 power derating curve for higher case temperatures.
3. In any of the insertion loss modes or switching into any insertion loss mode, the 3 remaining terminated port paths can be each exposed to the maximum stated power level during continuous or hot switching operation.

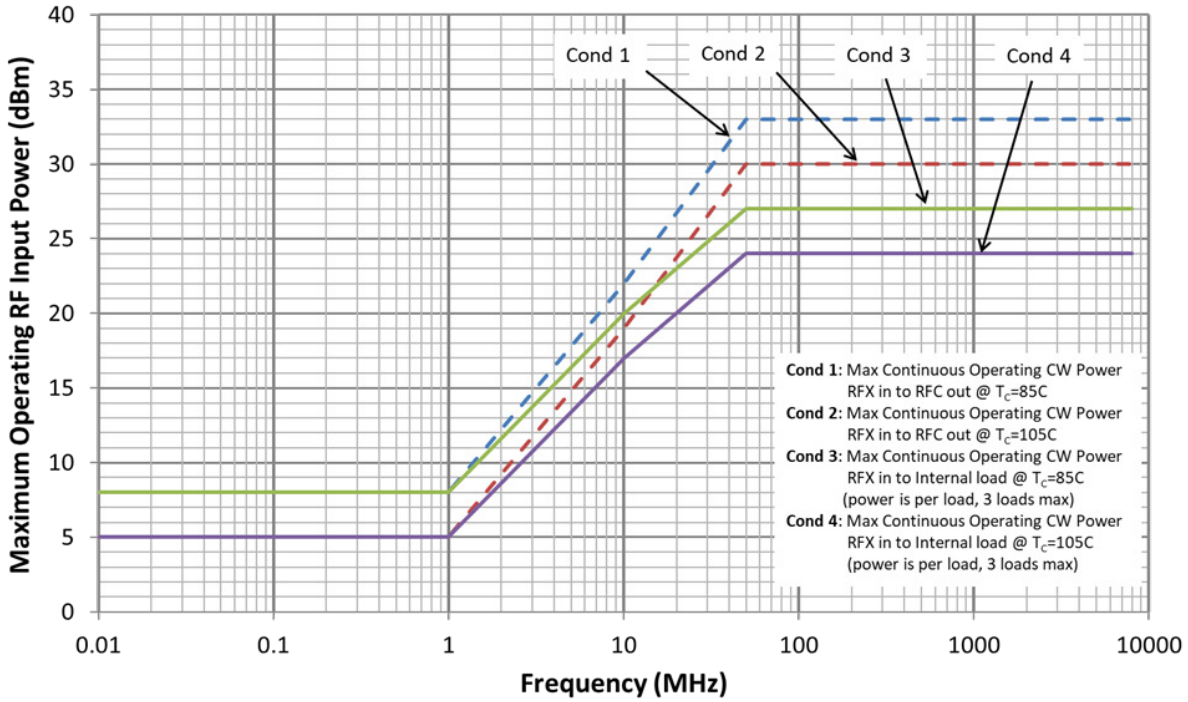


Figure 1. Maximum RF Input Power vs. RF Frequency

2.4 Electrical Specifications

Typical Application Circuit, Normal mode (V_{DD} = 3.3V, VSS_{EXT} = 0V) or Bypass mode (V_{DD} = 3.3V, VSS_{EXT} = -3.3V), T_C = +25°C, F_{RF} = 2000MHz, Input power = 0dBm, Z_S = Z_L = 50Ω, RFX = one of the four input ports, PCB board trace and connector losses are de-embedded unless otherwise noted.

Table 4. Electrical Specifications (T_C = +25°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Logic Input High Threshold	V_{IH}			***1.1***		Minimum (3.6, V_{DD})	V
Logic Input Low Threshold	V_{IL}			***-0.3***		***0.6***	V
Logic Current	I_{IH}, I_{IL}	For each control pin		***-2***		***+2***	µA
DC Current (V_{DD})	I_{DD}	Normal Mode	3.3V or 1.8V Logic		290	***360***	µA
		Bypass Mode	3.3V or 1.8V Logic		270	***340***	
DC Current (VSS_{EXT})	I_{VSS}	VSSEXT = -3.3V			-44	***-60***	µA
Insertion Loss RFX to RFC	IL	900 MHz			0.90	***1.4*** [1]	dB
		2100 MHz			1.1	***1.5***	
		2700 MHz			1.15	***1.6***	
		2700 MHz - 4000 MHz			1.2	1.65[2]	
		4000 MHz - 8000 MHz			1.8		
Minimum Isolation RFX to RFC	ISOC	400 MHz - 900 MHz		56	62.2		dB
		900 MHz - 2100 MHz		48.5	55.4		
		2100 MHz - 2700 MHz		48	53.5		
		2700 MHz - 4000 MHz		46	50		
		4000 MHz - 5000 MHz		46	50		
		5000 MHz - 8000 MHz		29.5	35.7		
Minimum Isolation RFX to RFX	ISOX	400 MHz - 900 MHz		55	60.3		dB
		900 MHz - 2100 MHz		49.5	53.6		
		2100 MHz - 2700 MHz		47	52		
		2700 MHz - 4000 MHz		43	47.6		
		4000 MHz - 5000 MHz		40	45		
		5000 MHz - 8000 MHz		29	36		
Total Coupling RFC to RFX	CPL_{RF}	Difference between active RFX input signal and 3 terminated RFX input signals at the RFC port. 50 MHz - 5000 MHz.		42			dB
Maximum RFX Port VSWR During Switching	$VSWR_T$	From RFX Active to RFX Term			1.7:1		-
		From RFX Term to RFX Active			2:1		
Minimum Return Loss (RFC Port)	RFC_{RL}	400 MHz - 4000 MHz			15		dB

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Minimum Return Loss (RFX Port)	RFX_{RL}	400 MHz –4000 MHz	Active		13		dB
			Terminated		17		
Input 0.1dB Compression[3]	$ICP_{0.1dB}$				35		dBm
Input IP2	IIP2	FRF1 = 2000 MHz, FRF2 = 2010 MHz RF Input = RFX, PIN = +20 dBm / tone FRF1 + FRF2 Term			114		dBm
Input IP3	IIP3	Δ F = 1MHz RF Input = RFX PIN = +20 dBm / tone	FRF = 2000MHz		59.5		dBm
			FRF = 4000MHz		60		
Switching Time[4]	T_{SW}	Bypass Mode	50% CTRL to 90% RF		256	345	ns
			50% CTRL to 10% RF		256	345	
			50% CTRL to RF settled within ±0.1 dB of I.L. value.		285		
Maximum Switching Rate[5]	SW_{RATE}	Pin 20 = GND			25		kHz
		Pin 20 = VSSEXT applied			290		
Maximum spurious level on any RF port[6]	$Spur_{MAX}$	RF ports terminated into 50Ω RFX connected to RFC			-120		dBm

1. Items in min/max columns in *bold italics* are confirmed by Test.
2. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
3. The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power and Figure 1 for maximum operating RF input power.
4. F_{RF} = 1GHz.
5. Minimum time required between switching of states =1/ (Maximum Switching Rate).
6. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

Typical Application Circuit, Normal mode (V_{DD} = 3.3V, VSS_{EXT} = 0V), T_C = +105°C, Input power = 0dBm, Z_S = Z_L = 50Ω, RFX = one of the four input ports, PCB board trace and connector losses are de-embedded unless otherwise noted.

Table 5. Electrical Specifications (T_C = +105°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Insertion Loss RFX to RFC	IL	50 MHz - 900 MHz			1.1	1.6	dB
		900 MHz - 2100 MHz			1.3	1.7	
		2100 MHz - 2700 MHz			1.4	1.9	
		2700 MHz - 4000 MHz			1.4	1.9	
		4000 MHz - 8000 MHz			2		
Minimum Isolation RFX to RFC	ISOC	50 MHz - 900 MHz		55.5	61.7		dB
		900 MHz - 2100 MHz		48.1	55.0		
		2100 MHz - 2700 MHz		47.6	53.1		
		2700 MHz - 4000 MHz		45.4	49.4		
		4000 MHz - 5000 MHz		45.5	49.5		
		5000 MHz - 8000 MHz		28.8	35.0		
Minimum Isolation RFX to RFX	ISOX	50 MHz - 900 MHz		54.5	59.8		dB
		900 MHz - 2100 MHz		49.1	53.2		
		2100 MHz - 2700 MHz		46.5	51.5		
		2700 MHz - 4000 MHz		42.5	47.1		
		4000 MHz - 5000 MHz		39.2	44.2		
		5000 MHz - 8000 MHz		28.3	35.3		
Minimum Return Loss (RFC Port)	RFC_{RL}	50 MHz - 4000 MHz		8	14		dB
Minimum Return Loss (RFX Port)	RFX_{RL}	50 MHz - 4000 MHz	Active	8	12		dB
			Terminated	11	15		

1. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.

Table 6. 3-Pin Switch Control Truth Table

Mode	V3	V2	V1
RF4 on*	0	0	0
RF1 on	0	0	1
RF2 on	0	1	0
RF3 on	0	1	1
RF4 on	1	0	0
All off	1	0	1
All off	1	1	0
All off	1	1	1

1. * Redundant state with state “100”

Table 7. 2-Pin Switch Control Truth Table[1,2]

Mode	V2	V1
RF4 on	0	0
RF1 on	0	1
RF2 on	1	0
RF3 on	1	1

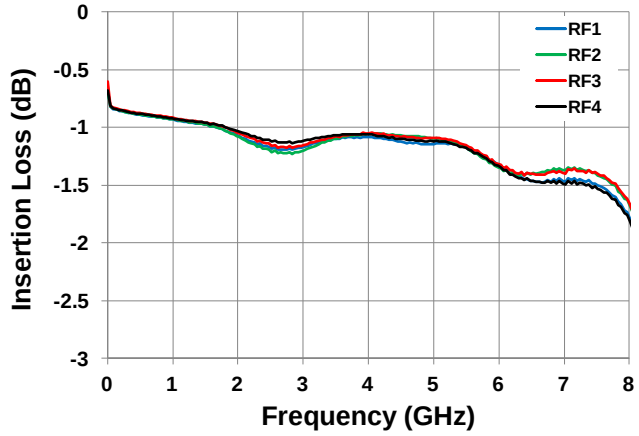
1. Note 1 - Pin 19 (V3) must be grounded for 2-pin control.
2. Note 2 – 2-pin control can be used if All Off mode is not required.

3. Typical Operating Conditions (TOC)

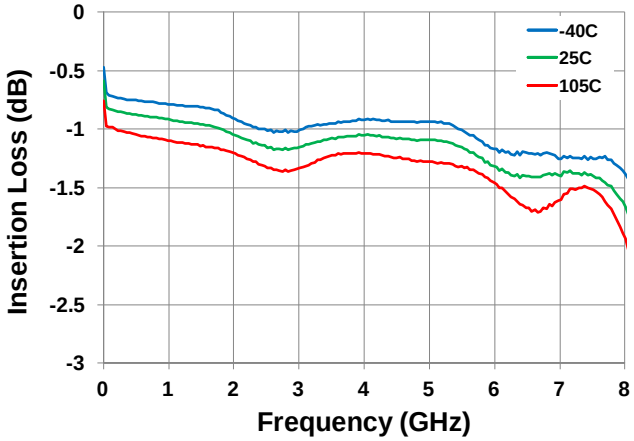
Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- V_{DD} = 3.3 V.
- T_{CASE} = +25 ºC (T_{CASE} = Temperature of exposed paddle).
- F_{RF} = 2000 MHz.
- RFX is the driven RF port and RFC is the output port.
- Pin = 10 dBm for all small signal tests.
- Pin = +15 dBm/tone applied to selected RFX port for two tone linearity tests.
- Two tone frequency spacing = 5 MHz.
- $Z_S = Z_L$ = 50 ohms.
- All unused RF ports terminated into 50 ohms.
- For Insertion Loss and Isolation plots, RF trace and connector losses are de-embedded (see EVKIT Board and Connector loss plot).
- Plots for Isolation and Insertion Loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.

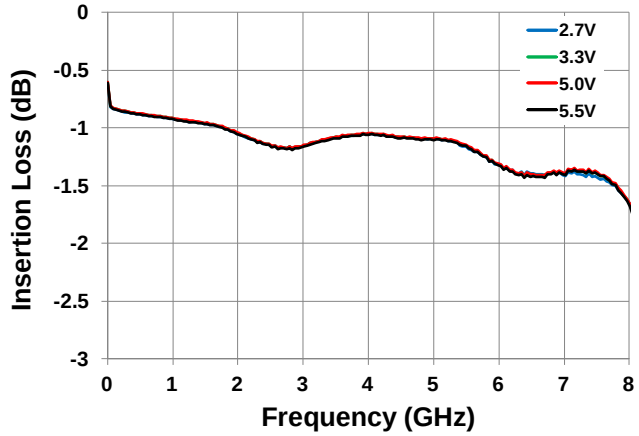
Insertion Loss vs. Selected Switch Path



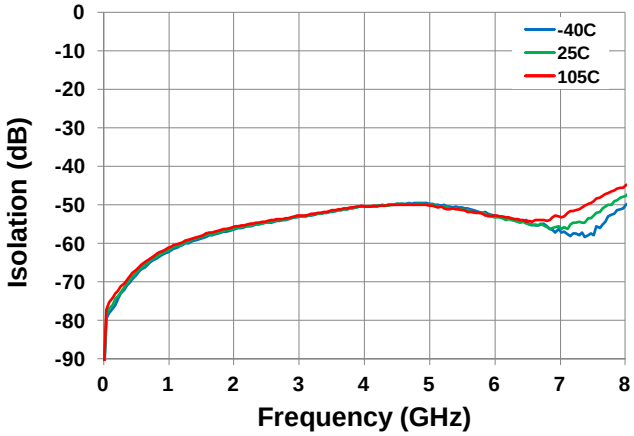
Insertion Loss vs. Temperature



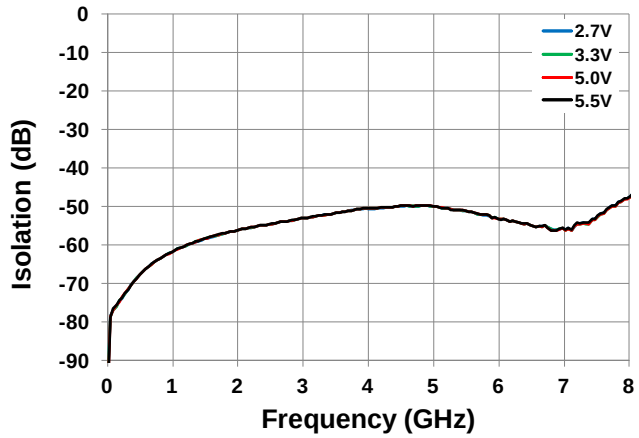
Insertion Loss vs. Voltage



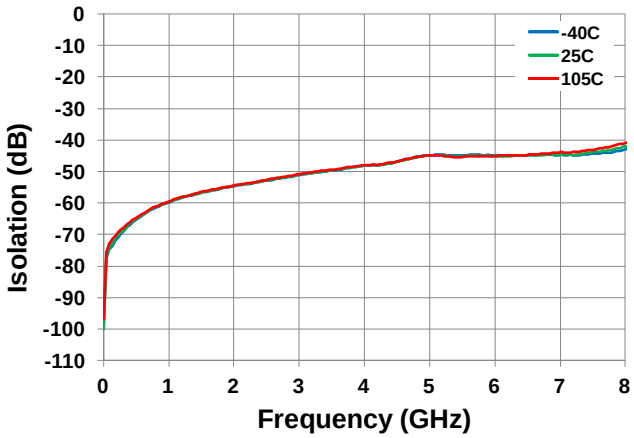
RFX → RFC Isolation vs. Temperature



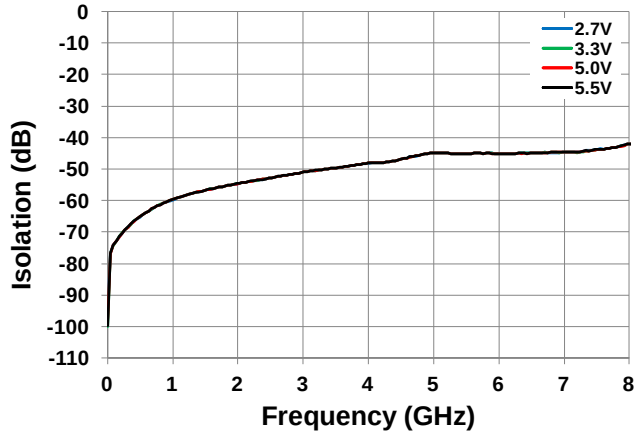
RFX → RFC Isolation vs. Voltage



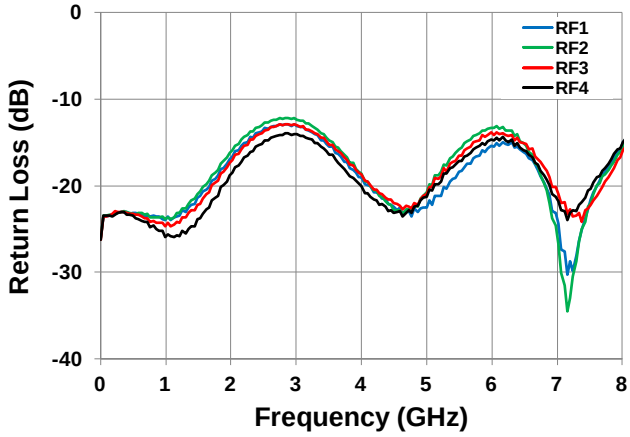
RFX → RFX Isolation vs. Temperature



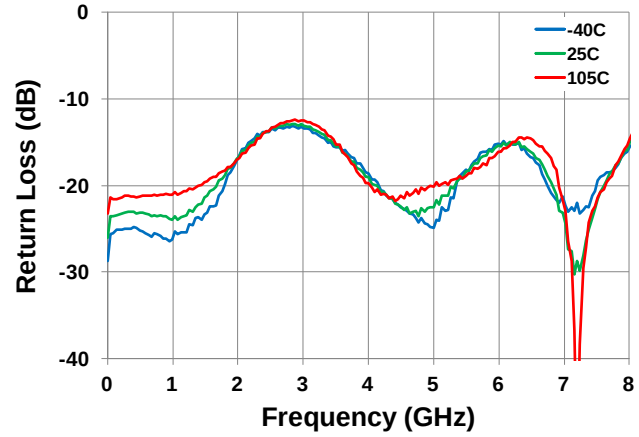
RFX → RFX Isolation vs. Voltage



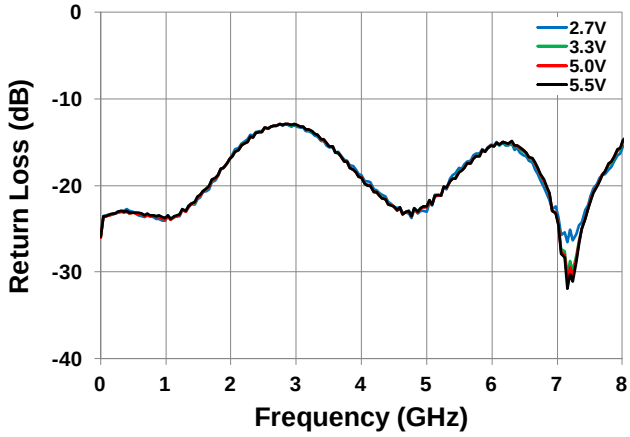
RFX Return Loss vs. Selected RFX Port



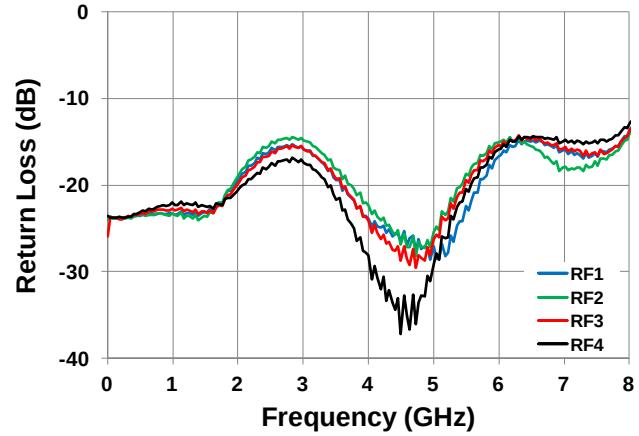
RFX Selected Return Loss vs. Temperature



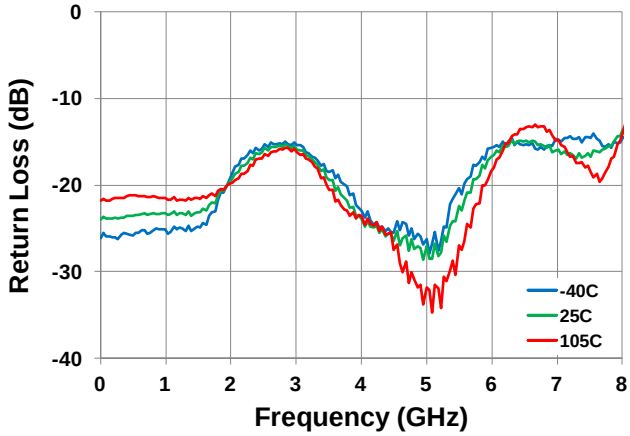
RFX Selected Return Loss vs. Voltage



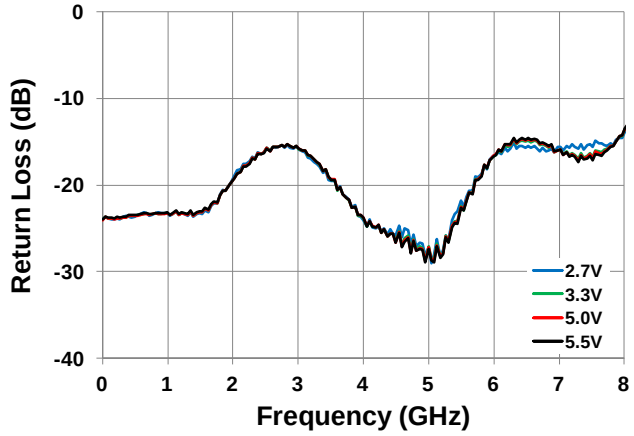
RFC Return Loss vs. Selected RFX Port



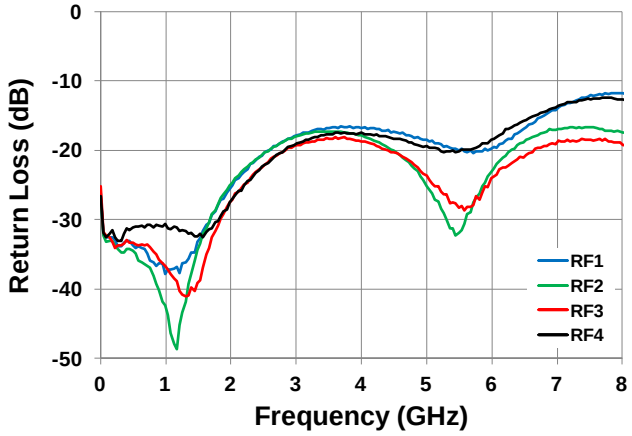
RFC Return Loss with RFX Selected vs. Temperature



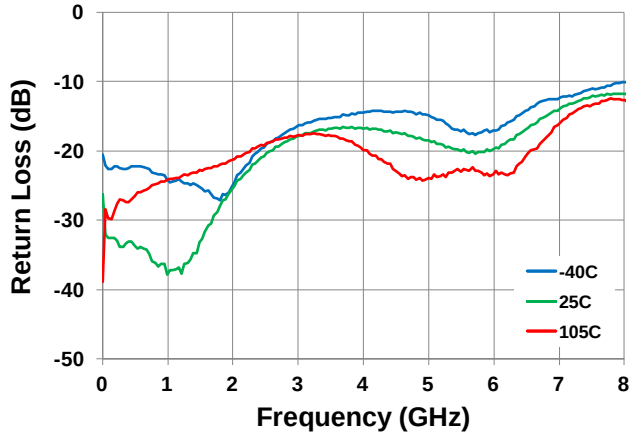
RFC Return Loss with RFX Selected vs. Voltage



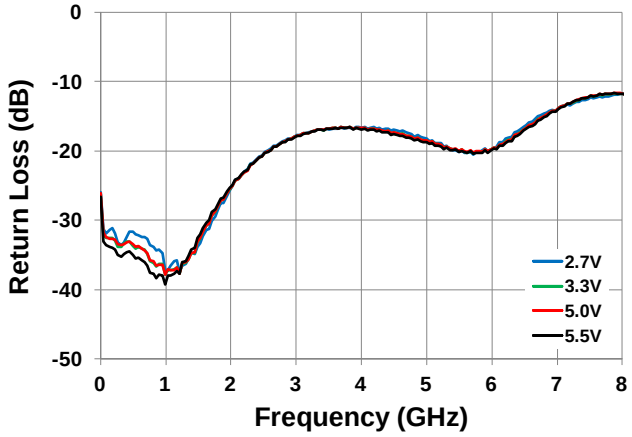
RFX Terminated Return Loss vs. RFX Port



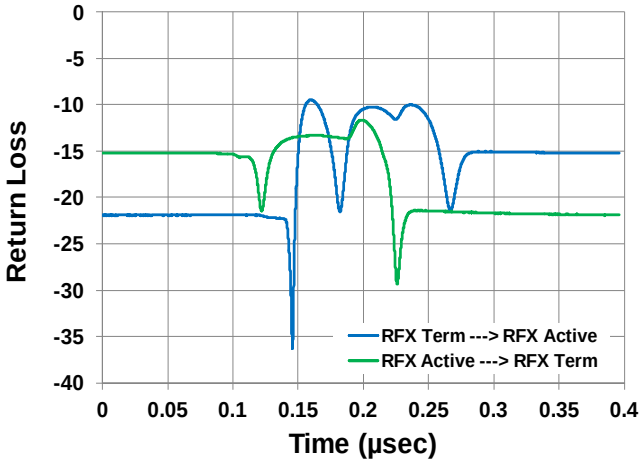
RFX Terminated Return Loss vs. Temperature



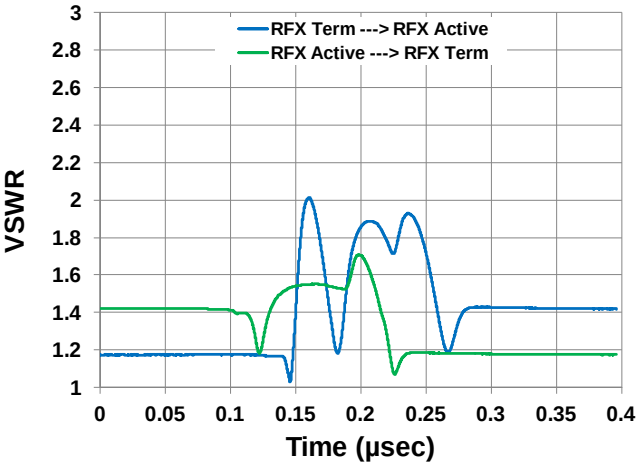
RFX Terminated Return Loss vs. Voltage



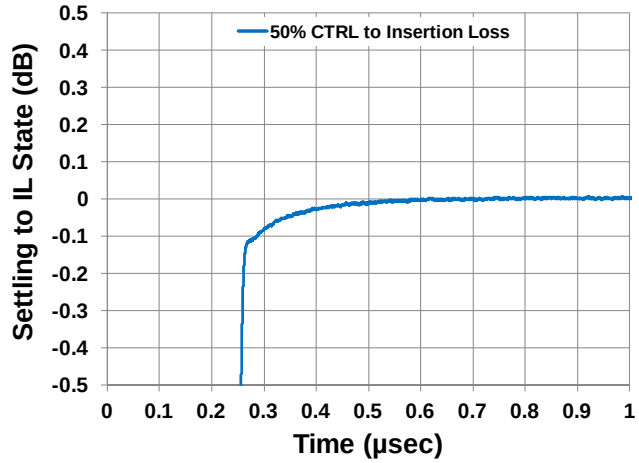
Return Loss (During Switching) vs. Time



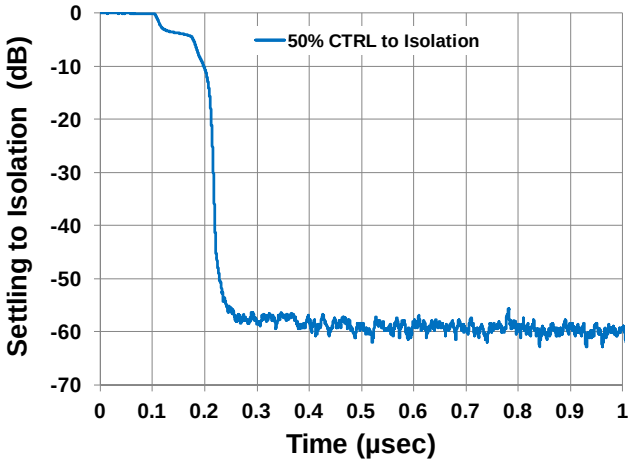
VSWR (During Switching) vs. Time



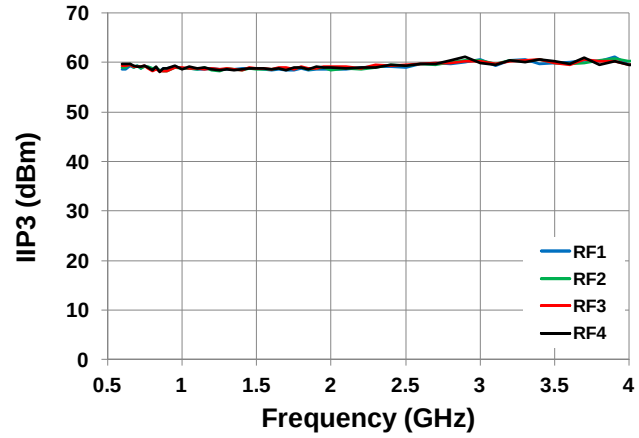
RFX Switching Time [RFX Terminated to RFX Active]



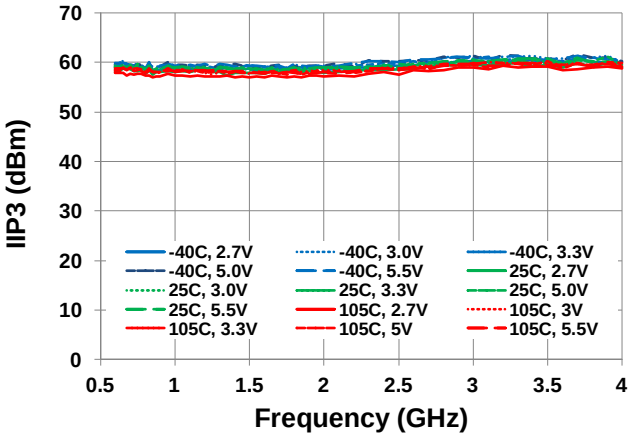
RFX Switching Time [RFX Active to RFX Terminated]



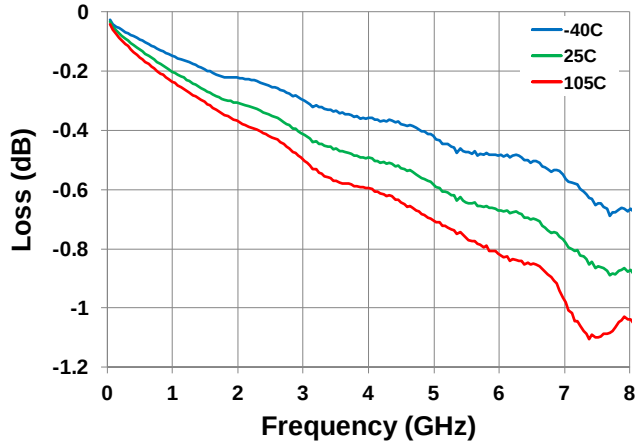
RFX IIP3 vs. Selected RFX Port



RFX IIP3 vs. Temperature and Voltage



EVKIT Trace and Connector Loss vs. Temperature



4. Applications Information

4.1 Default Start-up

Control pins include no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

4.2 Logic Control

Three control pins V1, V2, and V3 are used to set the state of the SP4T switch (see Table 6 or Table 7).

4.3 External Vss

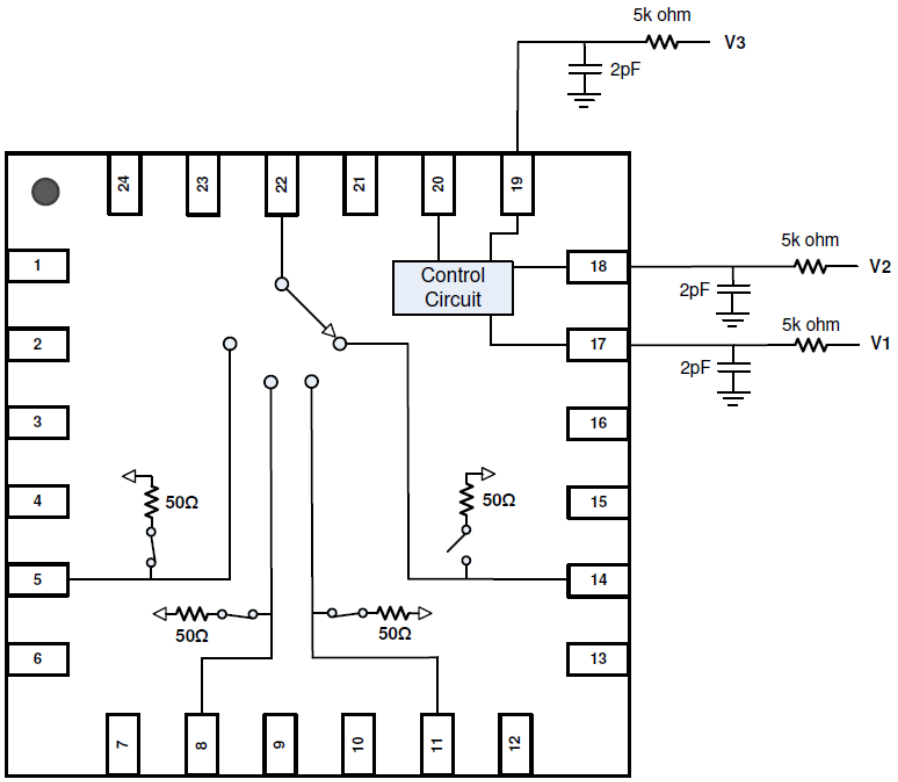
The F2914 is designed with an on-chip negative voltage generator. This on-chip generator is enabled by connecting pin 20 of the device to ground. To disable the on-chip generator apply a negative voltage to pin 20 (VSSEXT) of the device within the range stated in the Recommended Operating Conditions Table.

4.4 Power Supplies

A common VDD power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

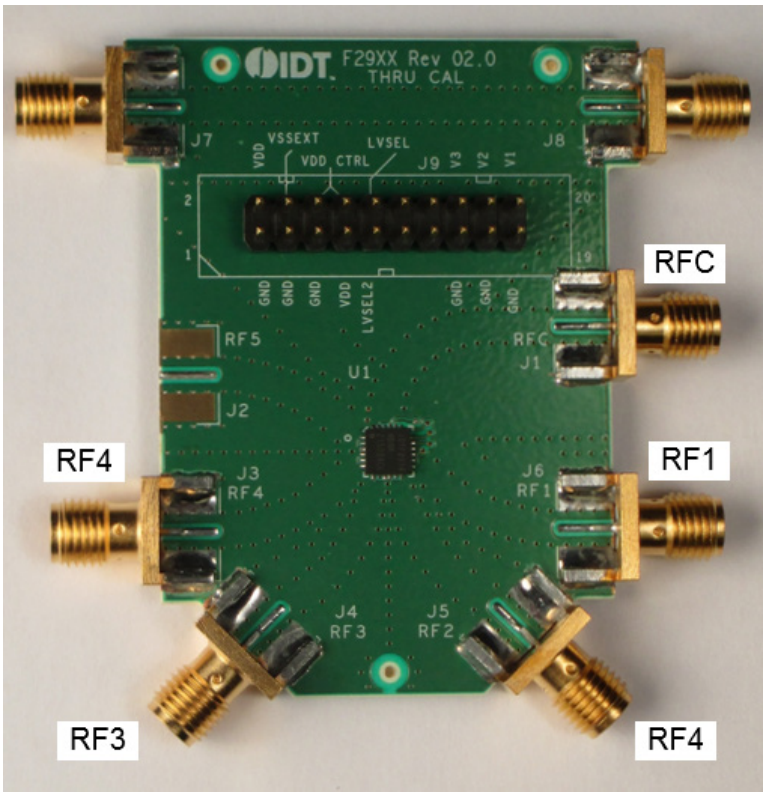
4.5 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 17, 18, and 19 as shown below.

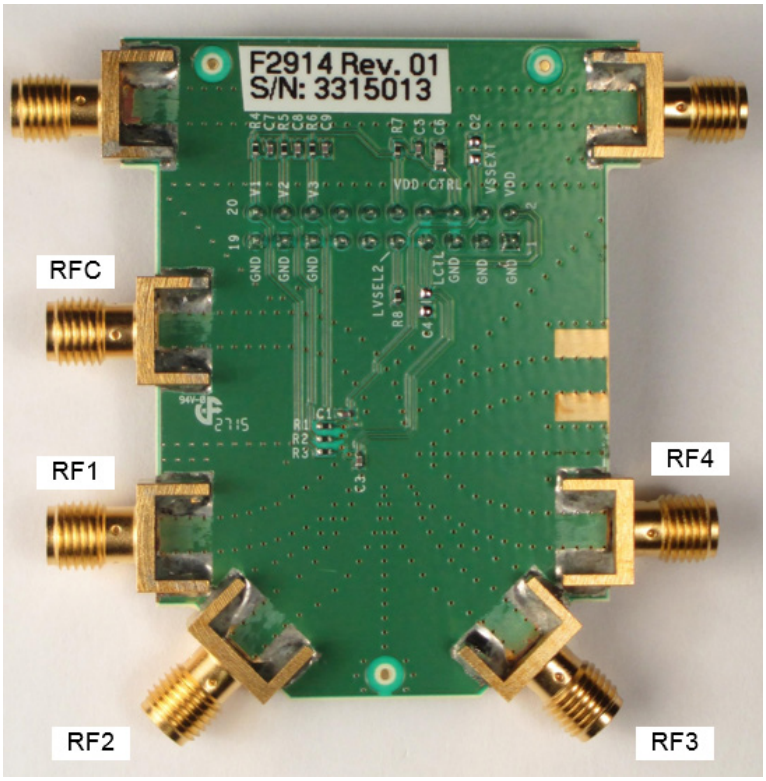


5. EvKit Picture

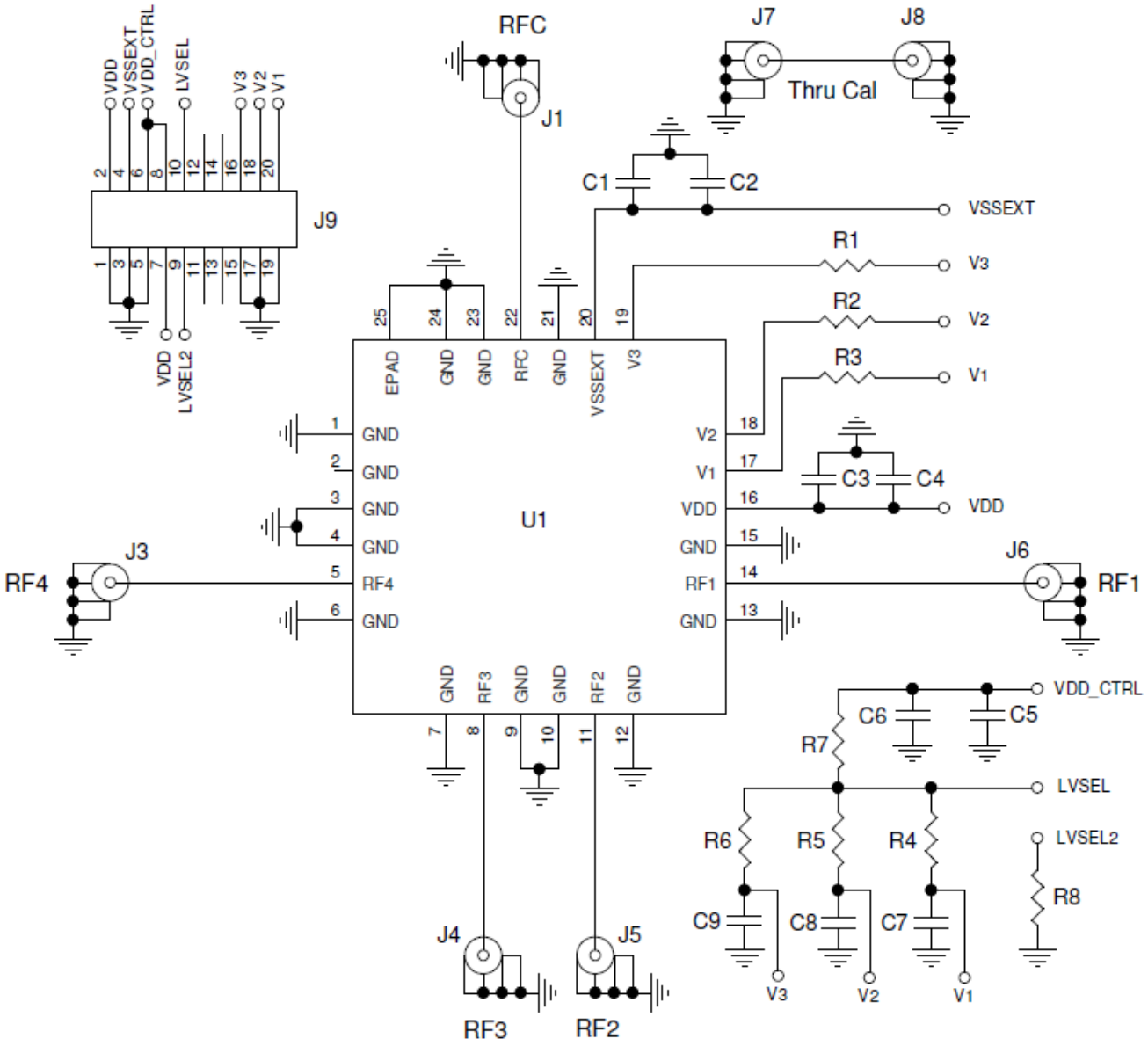
Top View



Bottom View



6. EVkit / Applications Circuit



7. EVKit BOM

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C1, C3, C5, C7, C8, C9	6	100 pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C2	0	Not Installed (0603)		
C4	0	Not Installed (0603)		
C6	1	1000 pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H102J	Murata
R1, R2, R3	3	0 Ω ±1%, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
R4, R5, R6	3	100 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
R7	1	15 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R8	1	22 kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2202X	Panasonic
J1, J3-J8	7	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J9	1	CONN HEADER VERT DBL 10 X 2 POS GOLD	67997-120HLF	FCI
U1	1	SP4T Switch 4 mm x 4 mm QFN24-EP	F2914NBGK	IDT
	1	Printed Circuit Board	F29XX EVKIT Rev 02.0	IDT

8. EVkit Operation

8.1 External Supply Setup

Set up a VDD power supply in the voltage range of 2.7 V to 5.5 V and disable the power supply output.

If using the on-chip negative voltage generator install a 2-pin shunt to short out pins 3 and 4 of J9.

If an external negative voltage supply is to be used set the supply voltage within the range of -3.6 V to

-3.2 V and disable the negative voltage power supply output. Also, be sure there are no jumper connections on pins 3 and 4 of J9.

8.2 Logic Control Setup

Using the EVKIT to manually set the control logic:

On connector J9 connect a 2-pin shunt from pin 7 (VDD) to pin 8 (VDD_CTRL). This connection provides the VDD voltage supply to the Eval Board logic control pull up network.

On connector J9 connect a 2-pin shunt from pin 9 (LVSEL2) to pin 10 (LVSEL). This connection enables R7 (15 kΩ) and R8 (22 kΩ) to form a voltage divider to set the proper logic control levels to support the full voltage range of VDD. Note that when using the on-board R7 / R8 voltage divider the current draw from the VDD supply will be higher by approximately VDD / 37 kΩ.

Connector J9 has 3 logic input pins: V1 (pin 20), V2 (pin 18), and V3 (pin 16). See Table 6 or Table 7 for Logic Truth Table. With the pullup network enabled (as noted above), these pins open will provide a logic high through pull up resistors R4, R5, and R6. To set a logic low to V1, V2, and V3 connect 2-pin shunts from pin 16 to pin 15, pin 18 to pin 17 and pin 20 to pin 19 respectively.

8.3 Using External Control Logic

Pins 6, 7, 8, 9, and 10 of J9 should have no connection. External logic controls would be applied to J9 pins 16 (V3), 18 (V2) and 20 (V1). See Table 6 or Table 7 for Logic Truth Table.

8.4 Turn-on Procedure

1. Setup the supplies and Eval Board as noted in the “External Supply Setup” and “Logic Control Setup” sections.
2. Connect the preset disabled VDD power supply to pin 2 (VDD) and pin 1 (GND) of J9.
3. If the external negative voltage source is to be used, connect the disabled supply to pin 4 (VSSEXT) and pin 3 (GND) of J9. If using on-chip negative supply be sure the 2-pin shunt is installed connecting pin 3 to pin 4.
4. Enable the VDD supply then enable the VSSEXT supply (if used).
5. Set the desired logic setting using V1, V2, and V3 to achieve the desired Table 6 or Table 7 setting. Note that external control logic should not be applied without VDD being applied first.

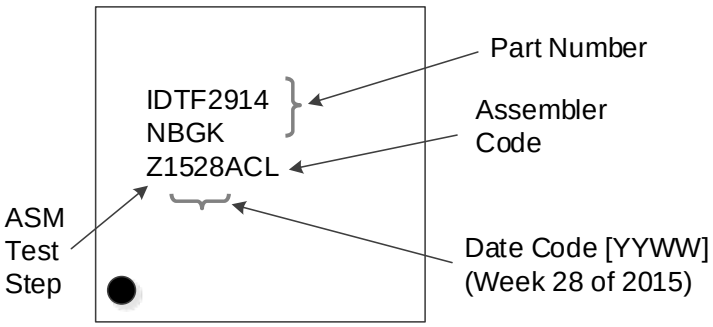
8.5 Turn-off Procedure

1. If using external control logic for V1, V2, V3 then set to a logic low.
2. Disable any external VSSEXT supply.
3. Disable the VDD supply.

9. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

10. Marking Diagram



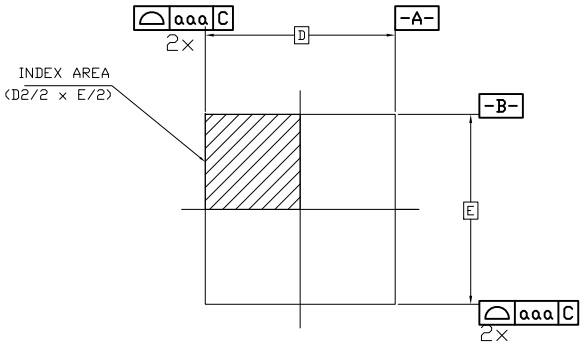
11. Ordering Information

Part Number	Package Description	Temperature Range (°C)	Carrier Type
F2914NBGK8	4.0 x 4.0 x 0.80 mm 0.50mm Pitch 24-VFQFPN	-40 to +85	Reel

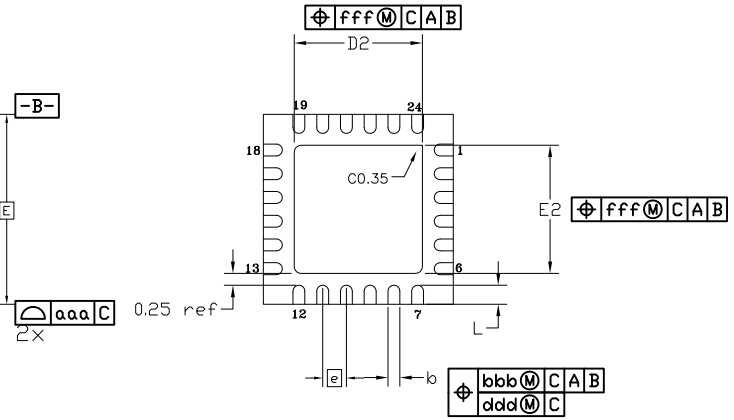
12. Revision History

Revision	Date	Description
1.01	Oct.29.2021	• Added RF performance data at 105°C (see Table 5) • Completed other minor changes.
1.00	Dec.1.20	• Updated RFX to RFC and RFX to RFX isolation specifications. • Added Total Coupling RFC to RFX specification.
N/A	Jun.19.20	Completed minor changes throughout.
N/A	Mar.1.16	Initial release.

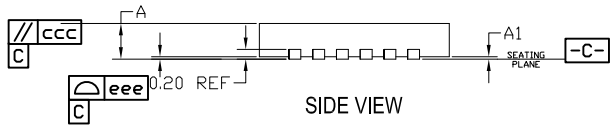
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION

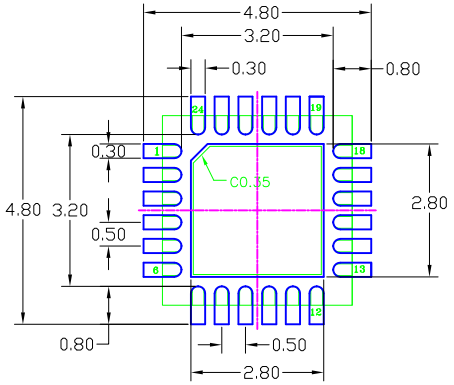
SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED DECIMAL X± .1 XX± .05 XXX± .030 ANGULAR ±1°		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE NB/NBG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY,EPAD 2.70mm SQ 0.50 mm PITCH QFN	
DRAWN RAC	5/11/16		
CHECKED			
		SIZE C / DRAWING No. PSC-4313-03	REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± .1 ±1° XX± .05 XXX± .030		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE NB/NBG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY,EPAD 2.70mm SQ 0.50 mm PITCH QFN	
DRAWN RAC	5/11/16		
CHECKED			
		SIZE C / DRAWING No. PSC-4313-03	REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2